TransistorTester with AVR microcontroller and a little more
Version 1.10k

Karl-Heinz Kübbeler
kh_kuebbeler@web.de

March 2, 2014

Contents

Preface

Basically Motive

Every hobbyist knows the following problem: You disassemle a Transistor out of a printed board or you get one out of a collection box. If you find out the identification number and you already have a data sheet or you can get the documents about this part, everything is well. But if you don't find any documents, you have no idea, what kind of part this can be. With conventional approach of measurement it is difficult and time-consuming to find out the type of the part and parameters. It could be a NPN, PNP, N- or P-Channel-Mosfet etc. It was the idea of Markus F. to hand over the work to a AVR microcontroller.

As my work has started

My work with the software of the TransistorTester of Markus F. [1] has started, because I had problems with my programmer. I had bought a printed board and components, but I could not program the EEprom of the ATmega8 with the Windows driver without error messages. Therefore I took the software of Markus F. and changed all the accesses from the EEprom memory to flash memory accesses. By analysing the software in order to save memory at other places of program, I had the idea, to change the result of the ReadADC function from ADC units to millivolt (mV) units. The mV resolution is needed for any output of voltage values. If ReadADC returns directly the mV resolution, I can save the conversion for each output value. This mV resolution can be get, if you first accumulate the results of 22 ADC readings. The sum must be multiplied with two and divided by nine. Then we have a maximum value of $\frac{1023 \cdot 22 \cdot 2}{9} = 5001$, which matches perfect to the wanted mV resolution of measured voltage values. So I additionally had the hope, that the enhancement of ADC resolution by oversampling could help to improve the voltage reading of the ADC, as described in AVR121 [5]. The original version ReadADC has accumulated the result of 20 ADC measurements and divides afterwards by 20, so the result is equal to original ADC resolution. By this way never a enhancement of ADC resolution can take place. So I had to do little work to change the ReadADC, but this forced analysing the whole program and change of all "if-statements" in the program, where voltage values are queried. But this was only the beginning of my work!

More and more ideas to make measurement faster and more accurate has been implemented. Additionally the range of resistor and capacity measurements are extended. The output format for LCD-Display was changed, so symbols are taken for diodes, resistors and capacitors instead of text. For further details take a look to the actual feature list chapter 1. Planned work and new ideas are accumulated in the To Do List in chapter 8. By the way, now I can program the EEprom of the ATmega with Linux operating system without errors.

At this place I would like to thank the originator and software author Markus Frejek, who has enabled the continuation with his initial work. In addition I would like to say thanks to the authors of numerous input to the discussion forum, which have assist me, to find new tasks, weak points and errors. Next I would like to thank Markus Reschke, who give me the permission, to publish his cheerful software versions at the SVN server. Furthermore some ideas and software part of Markus R. was integrated in my own software version, again thank you very much. I have to thank also Asco B., who has developed a new printed board, to enable the reproductions for other hobbyists. Another thank I would like to send to Dirk W. , who has handled the omnibus order for this printed board. Never I had time anough to handle these things concurrently with my software developement, at no time the state of further developement of software would have the same level. Thanks for the many suggestions to improve the tester to the members of the local chapter of the "Deutscher Amateur Radio Club (DARC)" in Lennestadt.

Chapter 1

Features

1. Operates with ATmega8, ATmega168 or ATmega328 microcontrollers. Additionally ATmega1280 or ATmega2560 microcontrollers can be used.
2. Displaying the results to a 2x16 character LCD-Display.
3. One key operation with automatic power shutdown.
4. Battery operation is possible since shutdown current is only about 20nA.
5. Low cost version is feasible without crystal and auto power off. With software version 1.05k the sleep modus of the Atmega168 or ATmega328 is used to reduce current if no measurement is required.
6. Automatic detection of NPN and PNP bipolar transistors, N- and P-Channel MOSFETs, JFETs, diodes, double diodes, Thyristors and Triacs.
7. Automatic detection of pin layout of the detected part.
8. Measuring of current amplification factor and Base-Emitter threshold voltage of bipolar transistors.
9. Darlington transistors can be identified by the threshold voltage and high current amplification factor.
10. Detection of the protection diode of bipolar transistors and MOSFETs.
11. Measuring of the Gate threshold voltage and Gate capacity value of MOSFETs.
12. Up to two Resistors are measured and shown with symbols  and values with up to four decimal digits in the right dimension. All symbols are surrounded by the probe numbers of the Tester (1-3). So Potentiometer can also be measured. If the Potentiometer is adjusted to one of its ends, the Tester cannot differ the middle pin and the end pin.
13. Resolution of resistor measurement is now up to 0.01Ω, values up to $50M\Omega$ are detected.
14. One capacitor can be detected and measured. It is shown with symbol  and value with up to four decimal digits in the right dimension. The value can be from $25pF$ (8MHz clock, $50pF$ @1MHz clock) to $100mF$. The resolution can be up to $1pF$ (@8MHz clock].
15. For capacitors with a capacity value above $0.18\mu F$ the Equivalent Serial Resistance (ESR) is measured with a resolution of 0.01Ω and shown with two significant decimal digits. This feature is only avaiable for ATmega with at least 16K flash memory (ATmega168 or ATmega328).

16. For capacitors with a capacity value above $5000pF$ the voltage loss after a load pulse can be determined. The voltage loss give a hint for the quality factor of the capacitor.

17. Up to two diodes are shown with symbol  or symbol  in correct order. Additionally the flux voltages are shown.

18. LED is detected as diode, the flux voltage is much higher than normal. Two-in-one LEDs are also detected as two diodes.

19. Zener-Diodes can be detected, if reverse break down Voltage is below 4.5V. These are shown as two diodes, you can identify this part only by the voltages. The outer probe numbers, which surround the diode symbols, are identical in this case. You can identify the real Anode of the diode only by the one with break down (threshold) Voltage nearby 700mV!

20. If more than 3 diode type parts are detected, the number of founded diodes is shown additionally to the fail message. This can only happen, if Diodes are attached to all three probes and at least one is a Z-Diode. In this case you should only connect two probes and start measurement again, one after the other.

21. Measurement of the capacity value of a single diode in reverse direction. Bipolar Transistors can also be analysed, if you connect the Base and only one of Collector or Emitter.

22. Only one measurement is needed to find out the connections of a bridge rectifier.

23. Capacitors with value below 25pF are usually not detectet, but can be measured together with a parallel diode or a parallel capacitor with at least 25pF. In this case you must subtract the capacity value of the parallel connected part.

24. For resistors below 2100Ω also the measurement of inductance will be done, if your ATmega has at least 16K flash memory. The range will be from about $0.01mH$ to more than $20H$, but the accuracy is not good. The measurement result is only shown with a single component connected.

25. Testing time is about two seconds, only capacity or inductance measurement can cause longer period.

26. Software can be configured to enable series of measurements before power will be shut down.

27. Build in selftest function with optional 50Hz Frequency generator to check the accuracy of clock frequency and wait calls (ATmega168 and ATmega328 only).

28. Selectable facility to calibrate the internal port resistance of port output and the zero offset of capacity measurement with the selftest (ATmega168 and ATmega328 only). A external capacitor with a value between $100nF$ and $20\mu F$ connected to pin 1 and pin 3 is necessary to compensate the offset voltage of the analog comparator. This can reduce measurement errors of capacitors of up to $40\mu F$. With the same capacitor a correction voltage to the internal reference voltage is found to adjust the gain for ADC measuring with the internal reference.

29. Display the Collector cutoff current I_{CE0} with currentless base ($10\mu A$ units) and Collector residual current I_{CES} with base hold to emitter level (ATmega328 only). This values are only shown, if they are not zero (especially for Germanium transistors).

30. For the ATmega328 a dialog function can be selected, which enable additional functions. Of course you can return from dialog to the normal Transistor Tester function.

31. With dialog function you can use a frequency measurement at port PD4 of the ATmega. The resolution is 1 Hz for input frequencies above 10 kHz. For lower frequencies the resolution can be up to 0.0001 Hz with measurement of the period.

32. With dialog function and without serial output a external voltage of up to 50V can be measured with the 10:1 voltage divider at the PC3 port.

33. With dialog function a frequency output can be selected at the TP2 pin (PB2 Port of the ATmega). Currently a preselection of frequencies from 10 Hz up to 2 MHz can be selected.

Thyristors and Triacs can only be detected, if the test current is above the holding current. Some Thyristors and Triacs need as higher gate trigger current, than this Tester can deliver. The available testing current is only about 6mA! Notice that all features can only be used with microcontroller with more program memory such as ATmega168.

Attention: Allways be shure to **discharge capacitors** before connecting them to the Tester! The Tester may be damaged before you have switched it on. There is only a little protection at the ATmega ports.

Extra causion is required if you try to test components mounted in a circuit. In either case the equipment should be disconnected from power source and you should be shure, that **no residual voltage** remains in the equipment.

Chapter 2

Hardware

2.1 Circuit of the TransistorTester

The circuit of the TransistorTester in figure 2.1 is based on the circuit of Markus F. released in Abb. 1 of AVR-Transistortester report [1]. Changed or moved parts are marked with green color, optional parts are marked with red color.

Some changes are made because the electronical power switch make problems in some implementations. Therefore the resistor R7 is reduced to $3.3k\Omega$. The capacitor C2 is reduced to 10nF and R8 is moved so that the PD6 output does not try to switch the C2 capacitor directly. Additional blocking capacitors are added and should be placed near the power connection of the Atmega and near the Voltage regulator.

Because the PD7 input and PC6 (RESET) are the only pins, where pull up resistors where needed, one extra $27k\Omega$ resistor is added to the PD7 (pin 13) input. With this modification the software can disable all internal pull up resistors of the ATmega.

The additional crystal with its 22pF capacitors are optional added. The accuracy of a crystal has the benefit of more stable time measurement for getting the capacitor values.

New software version can use a voltage scale switch of the ADC. The speed of switching is reduced by the external capacitor C1 at the AREF (21) pin of the ATmega. To avoid slowing down the measurement speed more than necessary, the value of this capacitor should be reduced to 1nF. Removing of the capacitor C1 is also possible. For adapting the software to the actual circuit take a look to the Makefile options in the configuring chapter 4.

Some different versions of R11 / R12 resistor combinations circulates in the internet. I have adapted my software to the original of Markus F. [1] with $10k\Omega$ and $3.3k\Omega$.

The additional 2.5V precision voltage reference connected at pin PC4 (ADC4) can be used to check and calibrate the VCC voltage, but is not required. You can use a LM4040-AIZ2.5 (0.1%), a LT1004CZ-2.5 (0.8%) or a LM336-Z2.5 (0.8%) as voltage reference. A optional ISP connector has been added to easier load new software versions to the tester.

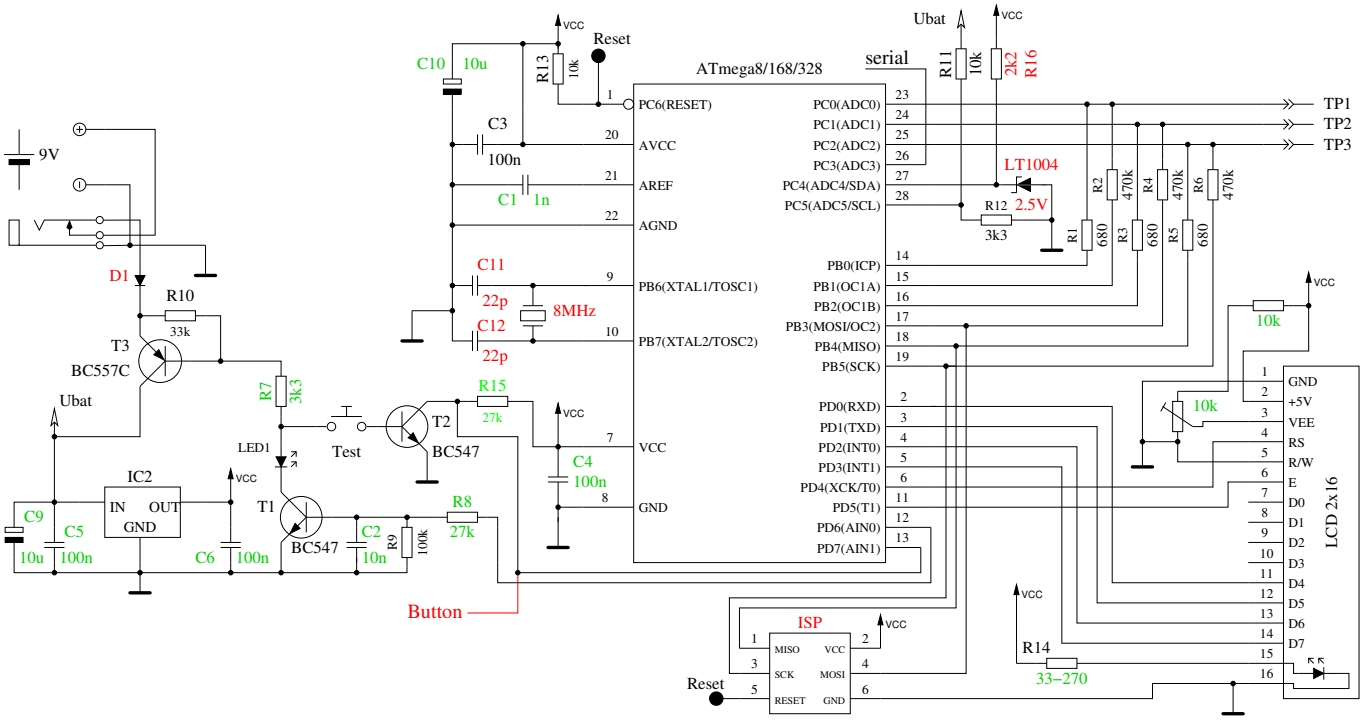


Figure 2.1. New circuit of TransistorTester

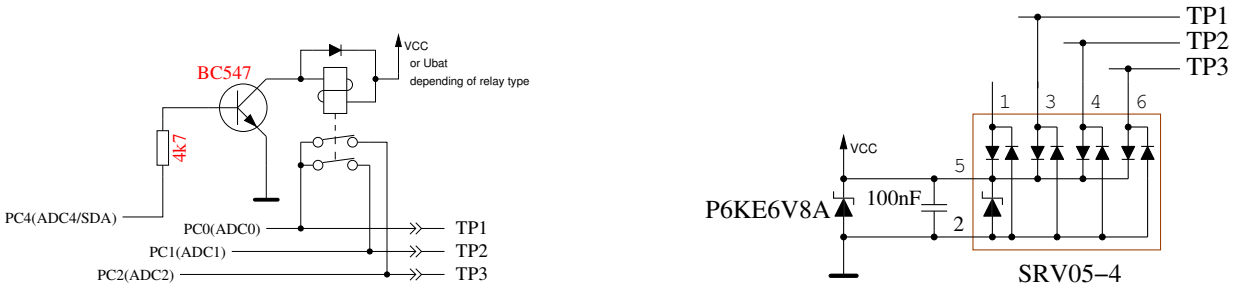
The software can follow to another pin assignment of port D for a simpler connection of the LCD display. The following table 2.1 shows the modified assignments.

Signal	circuit diagram	strip grid board version
pushbutton input	PD7	PD0
LCD-RS	PD4	PD7
LCD-E	PD5	PD5
LCD-D4	PD0	PD4
LCD-D5	PD1	PD3
LCD-D6	PD2	PD2
LCD-D7	PD3	PD1

Table 2.1. Changes for strip grid board

2.2 Extensions for the Transistor Tester

For better protection of the ATmega inputs one of the additional circuits 2.2 can be integrated. The de-energized contacts of the relay protect the ATmega without power. The contacts will be opened by software only for measurement. Also with the additional diode protection the chance of the ATmega will be better to survive the connection of a capacitor with higher residual voltage. A complete protection is not possible. Therefore capacitors should always be discharged before measuring.



(a) with Relay (b) with Diodes

Figure 2.2. Additional protection of the ATmega inputs

If the serial output of text is not required, the Pin PC3 of the ATmega can be used as analog input for measuring a external voltage. The voltage can be up to 50V with the optional 10:1 resistor divider and can be used for measuring the breakdown voltage of a zener diode. A current limiting power supply with up to 50V can be switched on with low signal at PD7 pin of the ATmega to deliver current for testing the break down voltage of a zener diode. Figure 2.3 shows a suggestion for this expansion. The tester shows the external voltage as long as you hold the key pressed. About 40mA more battery current is used by this expansion during key pressing.

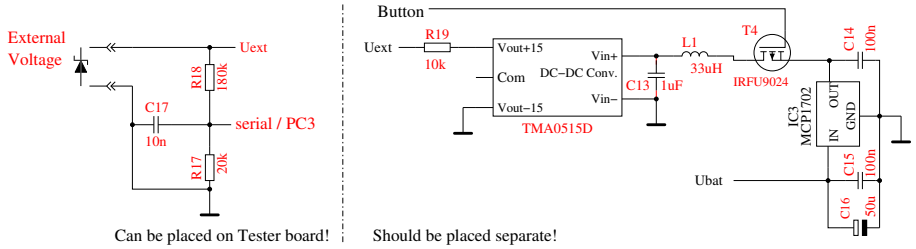


Figure 2.3. Expansion for measuring of break down voltage of Zener diodes

The 10:1 voltage divider can be used with the optional dialog part for the ATmega328 without the activated DC-DC converter for the zener diode measurement. Without the pressed key the voltage converter is not powered. For that the external voltage (for example battery voltage) can be measured at the zener diode port. You can only measure positiv DC voltages up to 50V. You have also to respect the correct polarity.

With the dialog part of the ATmega328 you can also select a frequency generator, which supports currently a selection of frequencies from $10Hz$ up to $2MHz$. The output of the 5V signal is done with a 680Ω resistor to test port TP2. You can use the GND signal from the minus pin of the zener diode extension or the test port TP1. The test port TP3 is connected to GND with a 680Ω resistor.

For using the with the dialog selectable frequency measurement is a little hardware extension necessary. The input pin PD4 (T0/PCINT20) of the ATmega is used for the frequency measurement. The same pin is also used for the connection of the LCD. With normal layout, the PD4 pin is connected to the LCD-RS signal, with the strip grid design it is connected to LCD-D4. For both signals the PD4 pin can be switched to input as long as no output to the LCD is required. The LCD respect the input value only, if the LCD-E signal is switched to GND. For driving the input pin from external clock source at least one serial resistor of 270Ω should be used. Better you should use the circuit of figure 2.4 . The voltage at the PD4 pin (LCD-RS or LCD-D4) should be adjusted to $2.4V$ without the assembled ATmega or during frequency measurement of the ATmega, to get the best sensivity for the input frequency signal. The LCD should always be installed for adjusting, because the pull up resistor of the LCD change the voltage.

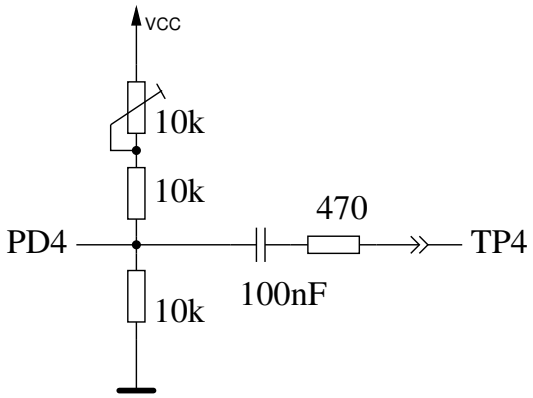


Figure 2.4. Extension for measurement of frequency

2.3 Hints for building the TransistorTester

Every LCD-display with at least 2x16 character and a HD44780 compatible controller can be used with the TransistorTester. You should respect the current needed for illumination, some LCD need lower current than others. I had tried OLED type displays, but this type cause interference with measurements of the ATmega and are **not** recommended. Also loading of special characters for displaying the resistor symbol has caused problems with the OLED.

The resistors R1 to R6 are critical for measurements and this 680Ω and 470$k\Omega$ resistors should be measurement type resistors (tolerance of 0.1%) to get the full accuracy. You should use a precision socket for the ATmega microcontroller to enable the replacement of the microcontroller. The microcontroller ATmega8, ATmega168 and ATmega328 can be used. Recommended is a ATmega168 or ATmega328, if you wish to use all features.

Anyway you should assemble all parts to printed board without the microcontroller. A up-to-date low voltage drop regulator like MCP1702-5002 is recommended as IC2, because it need only 2μA of standby current and can still deliver 5V, if your input voltage is only 5.4V. But this part is not pin compatible to well known 78L05 with TO92 body!

After checking, that all needed parts are at the correct place, you should first connect the battery or power supply to the printed board without LCD-display and microcontroller. You should check the voltage at the power pins of the microcontroller and LCD-display terminal during the Test key is pressed. The voltage should disappear, if you release the Test key. If the voltage had correct polarity and value, you should disconnect the power and assemble the microcontroller with correct alignment. Be careful and make shure, that all pins of the microcontroller are in the socket holes. Now you can also connect the LCD. Check if power pins of the LCD has the right connection to GND and VCC of your board.

If you are shure that everything is all right, reconnect the power. If you have already programmed the ATmega, you can press the Test button. By pressing the Test key, the background light of the LCD should switch on. If you release the Test button, the LED should illuminate weak. Notice, that the software for the microcontroller must be compiled for the correct processor type. A program for the ATmega8 does not run on a ATmega168!

2.4 Changeover for tester versions designed by Markus F.

Voltage control If the problem exist, the tester will shut down immediately with every switch on. With imy suggested setting of the fuses (Makefile) the voltage control of the different ATmega versions is switched to 4V (brown out level). This may be the reason why the tester makes trouble with the power on sequence. The Pin PD6 tries to switch the 100nF capacitor C2

to VCC level causing a voltage breakdown of the VCC voltage (5V). The capacitor C2 can be reduced to <10nF without problems. If possible, the direct connection of PD6 should be replaced by a resistor >220Ω.

Improvement of power on circuit Often this problem is the reason, if the tester starts with the button hold pressed, but switch off directly by releasing. The problem is enforced by a high current background light for the LCD. The resistor R7 to the base of the PNP transistor T3 was optimized with the value $27k\Omega$ too much to save power consuming. To improve the switching with lower battery voltage or lower current amplification factor of the PNP transistor T3, you should reduce the resistance to $3.3k\Omega$.

Additional pull-up resistor at PD7 The missing pull-up resistor results to a switch off of the tester with the message "Timeout" after a short display time. The software is configured with the option PULLUP_DISABLE, that all internal pull-up resistors are switched off. For that reason the voltage of pin PD7 is not definded, if the level is not switched by the push button or transistor T2 to GND. One external pull-up resistor of $27k\Omega$ to VCC avoid this error.

Capacitor C1 at the AREF pin Many designs use a 100nF capacitor at the AREF pin, like the design of Markus F. too. As long as the reference voltage of the ADC is never changed, this is a good solution. The software of the TransistorTester for the ATmega168/328 uses a automatic selection of the internal 1.1 V reference voltage of the ADC, if the input voltage is below 1V. With this solution a better resolution of the ADC can be reached for little input voltages. Unfortunately the switching from 5V to 1.1V reference is very slowly. A additional wait time of 10ms must be respected for this reason. With changing the capacity value to 1nF this wait time can be reduced significant. I have not noticed any degration of measurement quality with this change. Even a removing of the capacitor has no significant change of measurement results. If you prefer to leve the capacitor unchanged, you can remove the option NO_AREF_CAP in the Makefile to activate longer wait times in the program.

Expanding of a 8MHz crystal With some skill you can expand a 8MHz crystal to the backside of the printed board directly to the pins PB6 and PB7 (pin 9 and pin 10). My own expansion was done without the both 22pF capacitors. This solution has operated well with all tested ATmega. But it is not required to use a crystal. You can still use the 8MHz RC oszillator by setting the fuses to get the better resolution of time constant measuring (capacity value).

Smoothing of the operating voltage The original circuit of Markus F. shows only one 100nF capacitor to block the VCC voltage. This is clearly too little smoothing. You should at least use one 100nF near the ATmega power pins and one near the voltage regulator. The input of the voltage regulator should be blocked with a 100nF too. Additional $10\mu F$ capacitors (electrolytic or ceramic) at the input and output of the voltage regulator can stable the voltage level. Ceramic $10\mu F$ capacitos with SMD mounting form are easier to use for backfitting and have usually a lower ESR value.

Selection of the ATmega processor The using of the base function of the tester is still possible with a ATmega8. The flash memory of that device is used near 100% . Because the ATmega168 or ATmeg328 processors are pin-compatible to the ATmega8, I can recommend the replacement. Actually the price for ATmega328 is so cheap, that there is no reason to take a ATmega168 type. With a ATmega168/328 you get the following advantages: Self test with automatic calibration.
Improvement of measurement quality by automatic switching of ADC scale.
Measurement of inductors with resistance below 2100Ω.
Measurement of ESR value of capacitors with value of above $0.18\mu F$.

The resolution of resistor measurement below 10Ω is 0.01Ω.
Using of pin PC4 as serial output.

Missing precision voltage reference Usually the software should detect the missing voltage reference with the unconnected pin PC4. In this case no VCC=x.xV message should appear in row 2 of the LCD on power on. If this message appear without the reference, you should connect a $2.2k\Omega$ resistor to the PC4 input and VCC.

2.5 Chinese clones

As I know, the tester is rebuild in China in two versions. The first model is rebuild from the first design of Markus F. without the ISP port. The assembled ATmega8 is placed in a socket, so you can replace it with a ATmega168 or ATmega328. For this version you should consider all the hints of section 2.4. Additional $100nF$ ceramic cpacitors should be connected near by the VCC-GND and AVCC-GND pins of the ATmega for better stabilization of the power voltage. In addition you should notice, that if you expand the board with the additional 8 MHz crystal, your external ISP programmer must have a external clock for programming.

The second version of rebuilded tester is build with SMD components. Also the fix installed ATmega168 is a SMD type with 32TQFP body. Fortunately on the board is a 10-pole ISP connector provided for the programming. I have analysed the board version "2.1 2012/11/06". One error is the assembly of the part "D1", which should be a precision 2.5V voltage reference. Assembled is only a zener diode. This part should be removed. You can mount a LM4040AIZ2.5 or LT1004CZ-2.5 precision voltage reference at this place. A missing voltage reference is noticed by the software, so that you must not install the voltage reference. My exemplar was delivered with software version 1.02k. The 10-pole ISP plug was not assembled and I must install a jumper from ISP pin 6 to ISP pin 10. My programmer expect a GND connection at pin 10, but the board has GND level only on pin 4 and pin 6 of the ISP. The label of the ATmega168 was rub away and there was no documentation delivered with the part. The lock fuses of the ATmega were set, so no readout was possible. But I could install the software version 1.05k without any problems. Another user has problems with the same software version 1.05k. This user has the chinese board "2.2 2012/11/26". The software runs only without problems, if a additional $100nF$ keramic capacitor was placed between the pin 18-AVCC and 21-GND near by the ATmega. The software 1.05k uses the sleep state of the ATmega for waiting time. For this reason the current alternates often and the voltage regulator is stressed more. Further I have noticed, that the VCC voltage is blocked with a $100nF$ ceramic capacitor and with a $220\mu F$ electrolytic capacitor nearby the 78L05 voltage regulator. The 9V supply voltage is blocked with the same capacitors, but not at the input of the regulator but at the emitter of the PNP transistor (parallel with the battery). The printed circuit board track from the ATmega168 to the test port is very thin, so that a resistance of $100m\Omega$ could be measured for one path. This will be the reason for measuring a resistance of 0.3Ω for two direct connected pins. The ESR measuring can usually consider this by zero compensation. Beginning with version 1.07k the software does respect this offset for measuring resistors below 10Ω too.

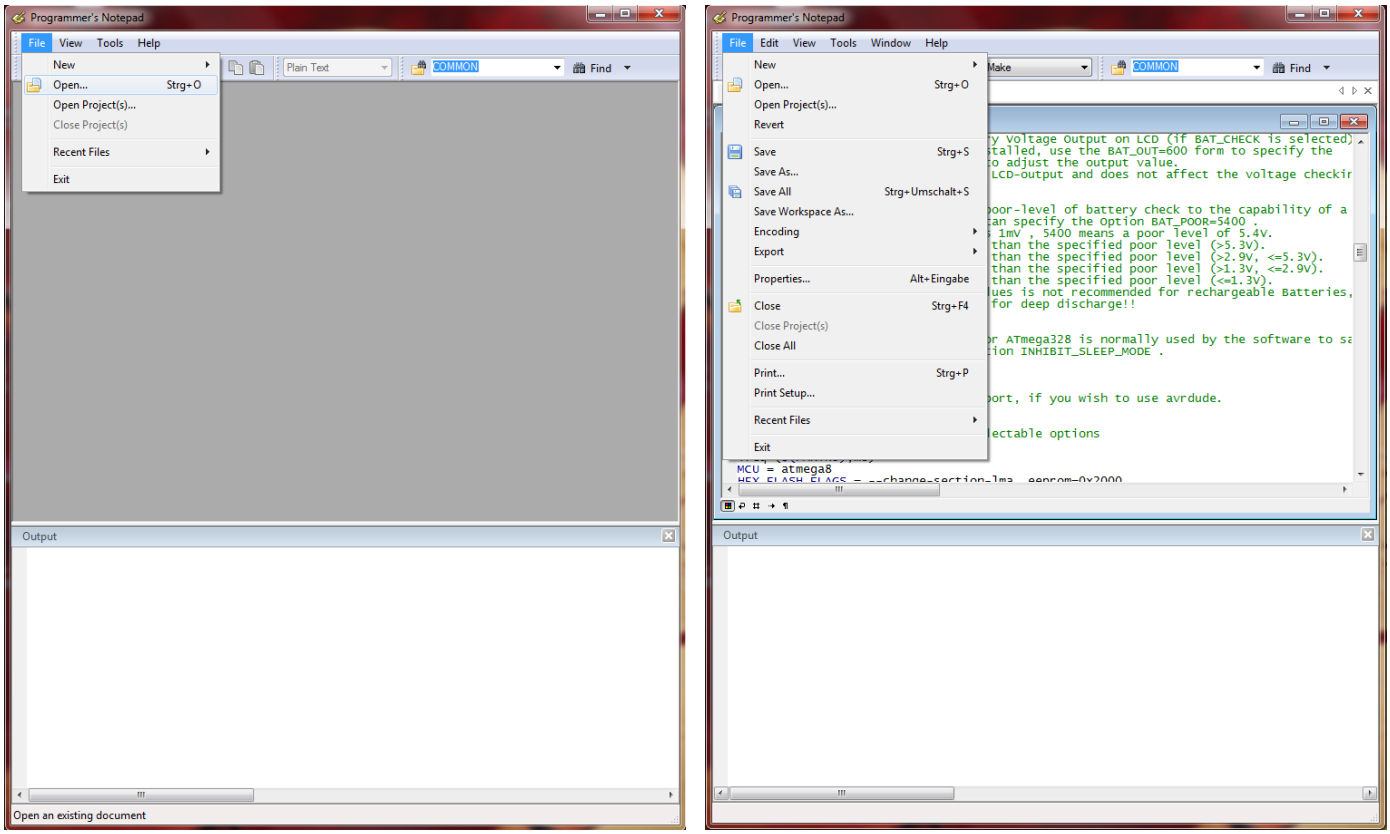
2.6 Programming of the microcontroller

I release the software for the microcontroller with source code. The developement is done with Linux operationg system (Ubuntu) and is controlled with a Makefile. The Makefile makes shure, that your software will be compiled with the prior selected Makefile options. Some constellations are precom-

piled with the source. Please take a look to the ReadMe.txt file in the directory Software/default and to the chapter 4. The result of compilation have the extensions .hex and .eep . Usually the names will be TransistorTester.hex and TransistorTester.eep . The .hex file contains the data for the program memory (flash) of the ATmega processor. The .eep file contains the data for the EEprom memory of the ATmega. Both data files must be loaded to the correct memory.

Additionally the operating state of the ATmega processor must be programmed with the "fuses". If you can use my Makefile and additionally the program avrdude [12], you need no exact knowledge of the details about the fuses. You have only to type "make fuses" if you have no crystal or "make fuses-crystal" if you have installed the 8MHz crystal to your printed board. With the ATmega168 series of the microcontroller you can also use "make fuses-crystal-lp" to use a crytal with the low power mode. Never choose the crystal mode of clock generation, if you don't have installed the 8MHz crystal. If you are not shure with the fuses, leave them as default set by manufactor and first bring the the tester to operation in this mode. Maybe your program runs too slow, if you use program data compiled for 8MHz operation, but you can correct this later! But a wrong set of fuses may inhibit later ISP-programming. If you use the Windows operating system, the easiest way to get a correct programmed ATmega is to use the WinAVR package [16],[17]. With my patch [18] you can also set the fuses by using the Makefile. Of course the avrdude program must support your programmer and the configuration in the Makefile must match to your environment.

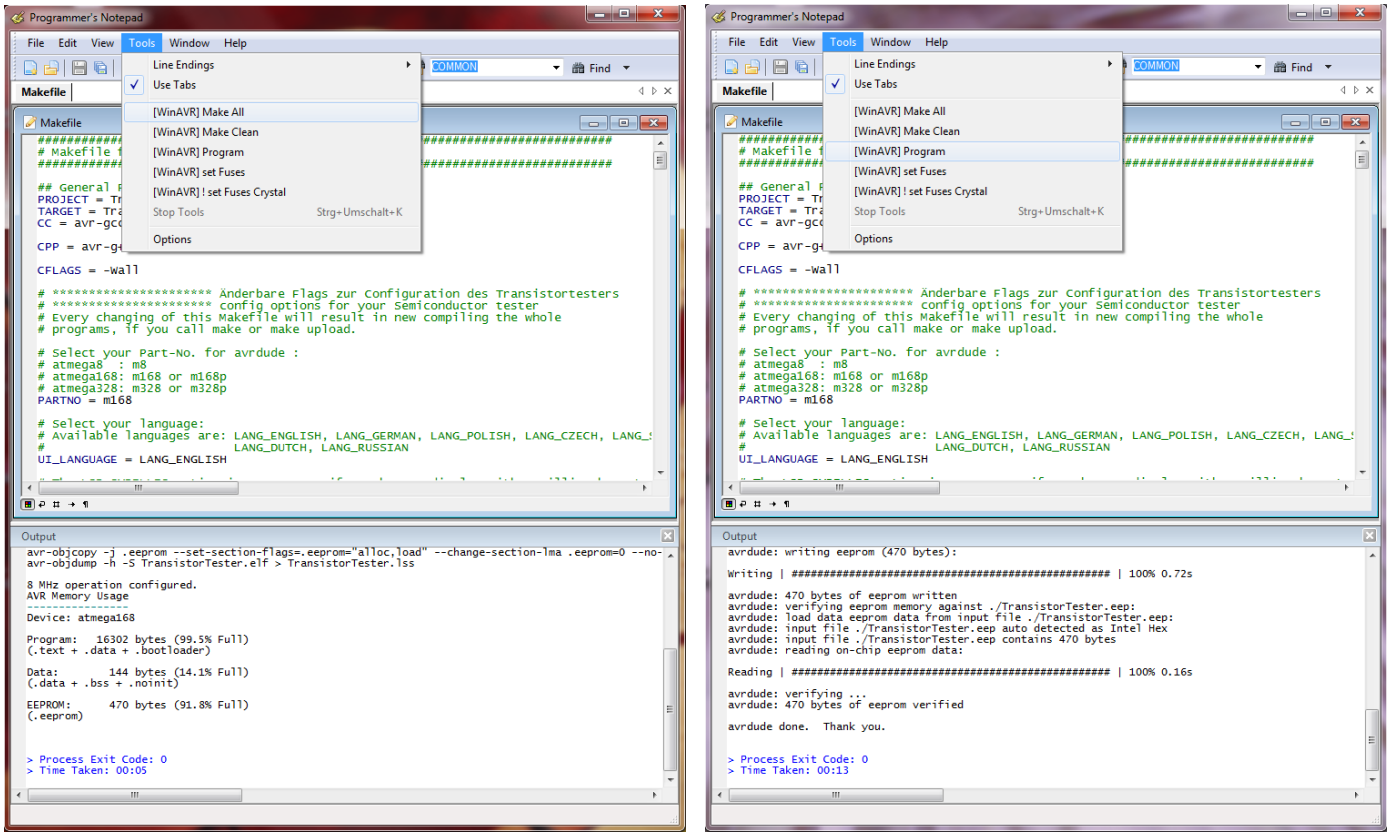
The figures 2.5 show the File menu of the graphical user interface of WinAVR for open the file Makefile and for saving the changed Makefile (Save).



(a) open Makefile (b) save Makefile

Figure 2.5. Using of the WinAVR user interface Programmer's Notepad

The next figures 2.6 show the Tools menu of the Programmer's Notepad for compiling the program (Make All) and for programming the ATmega (Program) with avrdude.



(a) Build programming data (.hex/.eep) (b) Programming the ATmega

Figure 2.6. Using of the WinAVR user interface Programmer's Notepad

2.7 Troubleshooting

In most cases of problems you will miss the text output to the LCD-display. At first you should check, if the LED was illuminated weak, if you release the Test button.

Power does not switch on. If the LED is without light and the VCC power has correct 5V voltage during holding the Test button, the microcontroller does not switch the power correctly. The microcontroller should hold the power by switching the PD6 output to 5V, which is usually done as one of the first actions. If you hold the Test key pressed, the power is switched on anyway. So you can check the value of VCC power and additionally the voltage value of the PD6 output, if you hold the key pressed. If VCC voltage has correct value (5V), but PD6 voltage is below 4V, your microcontroller does not start the program. In this case you should check if the microcontroller flash has been loaded with proper data for your installed type and if ATmega is correctly configured with the fuses. If your ATmega put the PD6 output to 5V and the power does not stay if you release the Test key, it is more difficult to find the reason. First you can shorten the LED and try again. If your Tester now starts, your LED may be faulty or mounted with wrong polarity. If this is not the reason, the current amplification factor of your T3 transistor (BC557C) is insufficient. The current to the base of T3 is lower in the microcontroller state as in the "key pressed" state.

Nothing is readable on the LCD display Check the voltage at the contrast pin at the LCD display (pin 3). Adjust to correct value specified in the data sheet of your display and optimize by viewing. If you have a high temperature display type, you must provide a negative contrast voltage for operation. In this case you can use the ICL 7660 device for generating a negative voltage from positive 5V.

If there is no output readable on the LCD and the background light is on, you should disconnect the power and check all four data plus the two control signal connections. If all connection are well, the only reason I see is a uncorrect timing of control signals. This can be caused by a slower LCD controller than expected by the software or the ATmega software runs at wrong clock speed. Please check for which clock speed your programming data was compiled and if the fuses of the ATmega are correct set to that speed. You find the clock parameter in the corresponding Makefile. If the tester is build without the switch off electronic, you can test with a LED connected to the test pins, if the program operates normally. If the LED flickers, the program operates well. The missing text on the LCD must be caused by wrong connection or timing.

Something but not all is readable on the LCD display Check if the .eep data are loaded to the EEprom memory of ATmega. If all data are loaded correctly, you should check the clock speed of your programming data (Makefile) and ATmega processor settings (fuses).

Measurement is slow and Capacitors are measured about 8 times too small You run software compiled for 8MHz clock at real clock speed of 1MHz. Please set the fuses of the ATmega correctly.

Measurement has strangely values Check if your programmer is still connected to the ISP-plug. The ISP interface should be disconnected for measuring. Very often the reason of wrong measurements is the use of software compiled with the AUTOSCALE_ADC option and with the option NO_REF_CAP, but the capacitor at the AREF pin has still a value of 100nF. Wrong assembly of components or remaining soft solder flux can disturb the measurements too. Please check with the selftest function of your TransistorTester software if possible. For the details see Chapter 5.5.

Otherwise inspect your board visually and check the resistor values with a ohmmeter. You can use the pins of the ATmega for this check, for example to check the R1 you can measure between pin 23 and pin 14. Take a look at the circuit diagram 2.1 for details. There is no need to remove the microcontroller, only battery or power supply should be removed before.

The Tester switch off the power after 2 seconds display time This condition exists, if the external Pull-Up resistor at the PD7 input is missing or the key button is keep pressed. The software switch off the internal Pull-Up resistors to prevent a influence to the measurement results. Therefore a external Pull-Up resistor (27k) is required.

Der Tester shows only Vext=xx.xV in row 2 This problem exists, if the Pull-Up resistor at the PD7 input is missing or the key button is keep pressed. Additionally the software is configured without the serial output (without option WITH_UART) and without the internal Pull-Up resistors (with option PULLUP_DISABLE). You should install the Pull-Up resistor at pin PD7.

Chapter 3

Instructions for use

3.1 The measurement operation

Using of the Transistor-Tester is simple. Anyway some hints are required. In most cases are wires with alligator clips connected to the test ports with plugs. Also sockets for transistors can be connected. In either case you can connect parts with three pins to the three test ports in any order. If your part has only two pins, you can connect this pins to any two of the tree test ports. Normally the polarity of part is irrelevant, you can also connect pins of electrolytical capacitors in any order. The measurement of capacity is normally done in a way, that the minus pole is at the test port with the lower number. But, because the measurment voltage is only between 0.3 V and at most 1.3 V, the polarity doesn't matter. When the part is connected, you should not touch it during the measurement. You should put it down to a nonconducting pad if it is not placed in a socket. You should also not touch to the isolation of wires connected with the test ports. Otherwise the measurement results can be affected. Then you should press the start button. After displaying a start message, the measurement result should appear after two seconds. If capacitors are measured, the time to result can be longer corresponding to the capacity.

How the transistor-tester continues, depends on the configuration of the software.

Single measurement mode If the tester is configured for single measurement mode, the tester shut off automatical after displaying the result for 28 seconds for a longer lifetime of battery. During the display time a next measurement can be started by pressing the start button. After the shut off a next measurement can be started too of course. The next measurement can be done with the same or another part. If you have not installed the electronic for automatic shut down, your last measurement result will be displayed until you start the next measurement.

Endless measurement mode A special case is the configuration without automatical shut off. This configuration is normally only used without the transistors for the shut off function. A external off switch is necessary for this case. The tester will repeat measurements until power is switched off.

Multi measurement mode In this mode the tester will shut down not after the first measurement but after a configurable series of measurements. In the standard case the tester will shut down after five measurements without found part. If any part is identified by test, the tester is shut down after double of five (ten) measurements. A single measurement with unknown part after a series of measurement of known parts will reset the counter of known measuerements to zero. Also a single measurement of known part will reset the counter of unknown measurements to zero. This behavior can result in a nearly endless series of measurements without pressing the start button, if parts are disconnected and connected in periodical manner.

In this mode there is a special feature for the display period. If the start button is pressed only short for switching on the tester, the result of measurement ist only shown for 5 seconds. Buf if you press and hold the start button until the first message is shown, the further measurement results are shown for 28 seconds. The next measurement can started earlier by pressing the start button during the displaying of result.

3.2 Optional menu functions for the ATmega328

If the menu function is selected, the tester start a selection menu after a long key press (¿ 300ms) for additional functions. The selectable functions are shown in row two of the display. After 5 seconds the selectable function changes automatically. After showing the last function, the first will be shown next. With a short key press the next selection can also be shown quicker. With a long key press you will start the shown function.

With the additional function f-generator (frequency generator) the selectable frequencies can be switched with short key presses. With a long key press you will stop the frequency generator and return to the function menu.

The additional function frequency (frequency measurement) uses the ATmega Pin PD4, which is also connected to the LCD. First is always the frequency measured. If the measured frequency is below 10 kHz, additionally the period of the input signal is measured and with this value the frequency is computed with a resolution of up to 0.001 Hz. The frequency measurement will be finished with a key press and the selectable functions are shown again.

The additional function Vext (Voltage measurement) is only possible, if the serial output is deselected. Because a 10:1 voltage divides is connected to PC3, the maximum external voltage can be 50V. This measurement can also be finished with a key press.

With the additional function "Switch off" the tester can be switched off immediately.

Of course you can also select the function Transistor (Transistor tester) to return to a normal Transistor tester measurement. Currently all additional functions are limited in time to prevent a discharged battery.

3.3 Selftest and Calibration

If the software is configured with the selftest function, the selftest can be prepared by connecting all three test ports together and pushing of the start button. To begin the self test, the start butten must be pressed again within 2 seconds, or else the tester will continue with a normal measurement.

If the self test is started, all of the documented tests in the Selftest chapter 5.5 will be done. The repetition of the tests can be avoided, if the start button is hold pressed. So you can skip uninteresting tests fast and you can watch interresting tests by releasing the start button. The test 4 will finish only automatically if you separate the test ports (release connection).

If the function AUTO_CAL is selected in the Makefile, the zero offset for the capacity measurement will be calibrated with the selftest. It is important for the calibration task, that the connection between the three test ports is relased during test number 4. You should not touch to any of the test ports or connected cables when calibration (after test 6) is done. But the equipment should be the same, which is used for further measurements. Otherwise the zero offset for capacity measurement

is not detected correctly. The resistance values of port outputs are determined at the beginning of every measurement with this option.

A capacitor with any capacity between $100nF$ and $20\mu F$ connected to pin 1 and pin 3 is required for the last task of calibration. To indicate that, a capacitor symbol is shown between the pin number 1 and 3, followed by the text " >100nF". You should connect the capacitor not before this text is shown. With this capacitor the offset voltage of the analog comparator will be compensated for better measurement of capacity values. Additionally the gain for ADC measurements using the internal reference voltage will be adjusted too with the same capacitor for better resistor measurement results with the AUTOSCALE_ADC option.

The zero offset for the ESR measurement will be preset with the option ESR_ZERO in the Makefile. With every self test the ESR zero values for all three pin combinations are determined. The solution for the ESR measurement is also used to get the values of resistors below 10Ω with a resolution of 0.01Ω.

3.4 special using hints

Normally the Tester shows the battery voltage with every start. If the voltage fall below a limit, a warning is shown behind the battery voltage. If you use a rechargeable 9V battery, you should replace the battery as soon as possible or you should recharge. If you use a tester with attached 2.5V precision reference, the measured supply voltage will be shown in display row two for 1 second with "VCC=x.xxV".

It can not repeat often enough, that capacitors should be discharged before measuring. Otherwise the Tester can be damaged before the start button is pressed. If you try to measure components in assembled condition, the equipment should be allways disconnected from power source. Furthermore you should be shure, that no residual voltage reside in the equipment. Every electronical equipment has capacitors inside!

If you try to measure little resistor values, you should keep the resistance of plug connectors and cables in mind. The quality and condition of plug connectors are important, also the resistance of cables used for measurement. The same is in force for the ESR measurement of capacitors. With poor connection cable a ESR value of 0.02Ω can grow to 0.61Ω.

You should not expect very good accuracy of measurement results, especially the ESR measurement and the results of inductance measurement are not very exact. You can find the results of my test series in chapter 5.

3.5 Compoments with problems

You should keep in mind by interpreting the measurement results, that the circuit of the TransistorTester is designed for small signal semiconductors. In normal measurement condition the measurement current can only reach about 6 mA. Power semiconductors often make trouble by reason of residual current with the identification an the measurement of junction capacity value. The Tester often can not deliver enough ignition current or holding current for power Thyristors or Triacs. So a Thyristor can be detected as NPN transistor or diode. Also it is possible, that a Thyristor or Triac is detected as unknown.

Another problem is the identification of semiconductors with integrated resistors. So the base - emitter diode of a BU508D transistor can not be detected by reason of the parallel connected internal 42Ω resistor. Therefore the transistor function can not be tested also. Problem with detection is also given with power Darlington transistors. We can find often internal base - emitter resistors, which make it difficult to identify the component with the undersized measurement current.

3.6 Measurement of PNP and NPN transistors

For normal measurement the three pins of the transistor will be connectet in any order to the measurement inputs of the TransistorTester. After pushing the start button, the Tester shows in row 1 the type (NPN or PNP), a possible integrated protecting diode of the Collector - Emitter path and the sequence of pins. The diode symbol is shown with correct polarity. Row 2 shows the current amplification factor (B=...) and the Base - Emitter threshold voltage. You should know, that the Tester can measure the amplification factor with two different circuits, the common Emitter and the common Collector circuit (Emitter follower). Only the higher result is shown on the LCD.

With the common Emitter circuit the tester has only two alternative to select the base current:

1. The 680Ω resistor results to a base current of about 6.1mA. This is too high for low level transistors with high amplification factor, because the base is saturated. Because the collector current is also measured with a 680Ω resistor, the collector current can not reach the with the amplification factor higher value. The software version of Markus F. has measured the Base - Emitter threshold voltage in this ciruit (Uf=...).

2. The $470k\Omega$ resistor results to a base current of only $9.2\mu A$. This is very low for a power transistor with low current amplification factor. The software version of Markus F. has identified the current amplification factor with this circuit (hFE=...).

The software of the Tester figure out the current amplification factor additionally with the common Collector circuit. The higher value of both measurement methodes is reported. The common collector circuit has the advantage, that the base current is reduced by negative current feedback corresponding to the amplification factor. In most cases a better measurement current can be reached with this methode for power transistors with the 680Ω resistor and for Darlington Transistors with $470k\Omega$ resistor. The reported Base - Emitter threshold voltage Uf is now measured with the same current used for determination of the current amplification factor. However, if you want to know the Base - Emitter threshold voltage with a measurement current of about 6mA, you have to disconnect the Collector and to start a new measurement. With this connection, the Base - Emitter threshold voltage at 6 mA is reported. The capacity value in reverse direction of the diode is also reported. Of course you can also analyse the base - collector diode.

With Germanium transistors often a Collector cutoff current I_{CE0} with currentless base or a Collector residual current I_{CES} with base hold to the emitter level is measured. Only for ATmega328 processors the Collector cutoff current is shown in this case at the row 2 of the LCD for 5 seconds or until the next keypress before showing the current amplification factor. With cooling the cutoff current can be reduced significant for Germanium transistors.

3.7 Measurement of JFET and D-MOS transistors

Because the structure of JFET type is symmetrical, the Source and Drain of this transistores can not be differed. Normally one of the parameter of this transistor is the current of the transistor with the Gate at the same level as Source. This current is often higher than the current, which can be reached with the measurement circuit of the TransistorTester with the 680Ω resistor. For this reason the 680Ω resistor is connected to the Source. Thus the Gate get with the growing of current a negative bias voltage. The Tester reports the Source current of this circuit and additionally the bias voltage of the Gate. So various models can be differed. The D-MOS transistors (depletion type) are measured with the same methode.

You should know for enhancement MOS transistors (P-E-MOS or N-E-MOS), that the measurement of the gate threshold voltage (Vth) is more difficult with little gate capacity values. You can get a better voltage value, if you connect a capacitor with a value of some nF parallel to the gate /source. The gate threshold voltage will be find out with a drain current of about 3.5mA for a P-E-MOS and about 4mA for a N-E-MOS.

Chapter 4

Configuring the TransistorTester

The complete software for the TransistorTester is available in source code. The compilation of modules is controlled with a Makefile. The developement was done at the Ubuntu Linux operating system with the GNU toolchain (gcc version 4.5.3). It should be possible to use other Linux operating systems without problems. To load the compiled data to the flash memory or the EEprom memory, the tool avrdude (version 5.11svn) was taken by the Makefile, if you call "make upload". The program avrdude [12] is available for Linux and Windows operating system. The gnu C-compiler gcc is also taken by the AVR studio software and by the WinAVR [16],[17] software at the Windows operating system. You can load the program data (.hex and .eep) also with other tools to the ATmega, but only my Makefile version takes care to load the correct data to the choosed processor. Avrdude loads only data to the ATmega if the Signature Bytes of the connected ATmega is identical to the choosed one. If you alter the Makefile, all the software will be compiled new, if you call a "make" or "make upload" command. The software compiled for a ATmega8 does not run on a ATmega168. The software compiled for a ATmega328 does not run on the ATmega168! A exeption fron this rule is the software compiled for ATmega168, this data can also be used for a ATmega328 without changes. Be careful, if you don't use my Makefile.

With the correct options set, my software runs on the unchanged hardware of Markus F. (PARTNO=M8, NO option NO_AREF_CAP and NO PULLUP_DISABLE option). The clock rate can also be set to 8 MHz with fuses, no crystal is required!

The following options in the Makefile are avaiable to configure the software for your Tester.

PARTNO describes the target processor:
m8 = ATmega8
m168 or m168p = ATmega168
m328 or m328p = ATmega328
example: PARTNO = m168

UI_LANGUAGE specifies the favored Language
LANG_ENGLISH, LANG_GERMAN, LANG_POLISH, LANG_CZECH, LANG_SLOVAK, LANG_SLO
LANG_DUTCH, LANG_BRASIL, LANG_RUSSIAN, LANG_UKRAINIAN and LANG_LITHUANIAN
is currently avaiable. The russian or ukrainian language requires a LCD with cyrillic character set.
example: UI_LANGUAGE = LANG_ENGLISH

LCD_CYRILLIC is only needed for a LCD-display with cyrillic character set. The μ and Ω character is not avaiable with the cyrillic character set. If you specify this option, both characters are loaded to the LCD with software.
example: CFLAGS += -DLCD_CYRILLIC

LCD_DOGM must be set, if a LCD with ST7036 controller (Type DOG-M) is used for displaying. The LCD-contrast is then set with software commands.
example: CFLAGS += -DLCD_DOGM

STRIP_GRID_BOARD This option adapts the software to a changed port D connection for strip grid printed boards. You can find the details in the chapter hardware 2.1.

WITH_MENU activated a menu function for a ATmega328. You can select some additional functions with a selection menu, which you can call with a long key press (¿300ms).
example: CFLAGS += -DWITH_MENU

WITH_SELFTEST If you specify this Option, software will include a selftest function. Selftest will be started, if you connect all three probes together and start measurement.
example: CFLAGS += -DWITH_SELFTEST

NO_COMMON_COLLECTOR_HFE disables the hFE measurement of transistors with the common collector circuit. You can save memory to enable the extended selftests T1 to T7 for a ATmega168 processor. By default both measurement circuits for the hFE measurement are enabled, but there is no place in the program memory of the ATmega168 for the extended selftests.
example: CFLAGS += -DNO_COMMON_COLLECTOR_HFE

NO_COMMON_EMITTER_HFE disables the hFE measurement of transistors with the common emitter circuit. You can save memory to enable the extended selftests T1 to T7 for a ATmega168 processor. By default both measurement circuits for the hFE measurement are enabled, but there is no place in the program memory of the ATmega168 for the extended selftests.
example: CFLAGS += -DNO_COMMON_EMITTER_HFE

NO_TEST_T1_T7 This option disable the execution of the selftest parts T1 to T7. This tests are usefull to find errors in the hardware like incorrect measurement resistors or isolation problems. If your hardware is well, you can omitt this selftest parts T1 to T7 by setting this option to get a faster calibration. The ATmega168 processor does not use the selftest parts T1 to T7, if both measurement types for hFE determination are used.
example: CFLAGS += -DNO_TEST_T1_T7

AUTO_CAL The zero offset for capacity measurement will be written additionally to the EEprom with the selftest routine. Additionally the offset voltage of the analog comparator (REF_C_KORR) and the voltage offset of the internal reference voltage (REF_R_KORR) will be measured automatically, if you connect a capacitor with a capacity value between $100nF$ and $20\mu F$ to pin 1 and pin 3 after measurement of capacity zero offset. All found values will be written to EEprom and will be used for further measurements automatically. The port output resistance values will be determined at the beginning of each measurement.
example: CFLAGS += -DAUTO_CAL

FREQUENCY_50HZ At the end of selftest a 50 Hz Signal will be generated on Port 2 and Port 3 for up to one minute.
example: CFLAGS += -DFREQUENCY_50HZ

CAP_EMPTY_LEVEL This option defines the voltage level for discharged capacitor (mV units). You can set the level to higher value as 3mV, if the tester does not finish discharging of capacitors. In this case the tester ends after longer time with the message “Cell!”.
example: CFLAGS += -DCAP_EMPTY_LEVEL=3

WITH_AUTO_REF specifies, that reference voltage is read to get the actual factor for capacity measuring of low capacity values (below $40\mu F$).
example: CFLAGS += -DWITH_AUTO_REF

REF_C_KORR specifies a offset for readed reference voltage in mV units. This can be used to adjust the capacity measurement of little capacitors. A correction value of 10 results to about 1 percent lower measurement results. If the option AUTO_CAL is selected together with the WITH_SELFTEST option, the REF_C_KORR will be a offset to the measured voltage difference of the test capacitor and the internal reference voltage.
example: CFLAGS += -DREF_C_KORR=14

REF_L_KORR specifies a additional offset in mV units to the reference voltage for the measurement of inductance values. The REF_C_KORR offset and respectively the offset value from the calibration is additionally used with the inductance measurement. The REF_L_KORR value will be subtracted for measurements without a 680Ω resistor, for measurements with a 680Ω resistor the value will be added.
example: CFLAGS += -DREF_L_KORR=40

C_H_KORR specifies a correction value for the measurement of big capacitor values. A value of 10 results to 1 percent lower measurement results.
example: CFLAGS += -DC_H_KORR=10

WITH_UART uses the pin PC3 as output for the serial text (V24). If the option is not set, the pin PC3 can be used for reading a external voltage with a 10:1 resistor divider. With this equipment you can check the breakdown voltage of zener diodes, which have more than 4.5V breakdown voltage. This measurement will repeat with 3 measurements per second until you release the Start button.
example: CFLAGS += -DWITH_UART

AUTOSCALE_ADC enables the automatic scale switchover of the ADC to either VCC or internal reference. Internal reference gives a 2.56V scale for ATmega8 and a 1.1V scale for other processors.
example: CFLAGS += -DAUTOSCALE_ADC

ESR_ZERO defines a zero offset for ESR measurements. The zero offsets for all three pin combinations will be determined with the selftest and replaces the preset zero offset. This zero offsets will be subtracted from all ESR measurements. Example: CFLAGS += -DESR_ZERO=29

NO_AREF_CAP tells your Software, that you have no capacitor ($100nF$) installed at pin AREF (pin 21). This enables a shorter wait-time for the AUTOSCALE_ADC scale switching of the ADC. A $1nF$ capacitor was tested in this mode without detected errors. Figure 4.1a and 4.1b show the switching time with a $1nF$ capacitor. As you can see the switching from 5V to 1.1V is much slower than switching back to 5V. If you have still installed the $100nF$, switching time will be about factor 100 longer!
example: CFLAGS += -DNO_AREF_CAP

REF_R_KORR specifies a offset for the internal ADC-reference voltage in mV units. With this offset a difference by switching from VCC based ADC reference to internal ADC reference for resistor measurement can be adjusted. If you select the AUTO_CAL option of the selftest section, this value is only a additionally offset to the found voltage difference in the AUTO_CAL function.
example: CFLAGS += -DREF_R_KORR=10

OP_MHZ tells your software at which Clock Frequency in MHz your Tester will operate. The software is tested only for 1 MHz, 8MHz and additionally 16MHz. The 8MHz operation is recommended for better resolution of capacity and inductance measurement.
example: OP_MHZ = 8

RESTART_DELAY_TICS must be set to 6, if the ATmega168 or ATmega328 is used with the internal RC-oszillator instead of the crystal oszillator. If this value is not preset, the software respects the 16384 clock tics delay for restart from sleep mode with the crystal operation.
example: CFLAGS += -DRESTART_DELAY_TICS=6

USE_EEPROM specifies if you wish to locate fix text and tables in EEprom Memory. Otherwise the flash memory is used. Recommended is to use the EEprom (option set).
example: CFLAGS += -DUSE_EEPROM

EBC_STYLE specifies, that the output of transistor pin layout is done with format "EBC=..." or "GDS=...". This way of output save program memory for the ATmega. Without this option the layout is shown with the format "123=...", where every point represent a E (Emitter), B (Base) or C (Collector). For FET transistors every point can be a G (Gate), D (Drain) or S (Source). If the sequence of the test pins is not 1, 2 and 3 in the reading direction, you can invert the sequence with the option EBC_STYLE=321 . The pin assignment is then shown with style "321=...", which will better match the usual reading direction.
Example: CFLAGS += EBC_STYLE

NO_NANO specifies that the decimal prefix nano will not be used to display the measurement results. So capacity values will be shown in μF instead of nF.
Example: CFLAGS += NO_NANO

PULLUP_DISABLE specifies, that you don't need the internal pull-up resistors. You must have installed a external pull-up resistor at pin 13 (PD7) to VCC, if you use this option. This option prevents a possible influence of pull-up resistors at the measuring ports (Port B and Port C).
example: CFLAGS += -DPULLUP_DISABLE

ANZ_MESS this option specifies, how often an ADC value is read and accumulated. You can select any value between 5 and 200 for building mean value of one ADC measurement. Higher values result to better accuracy, but longer measurement time. One ADC measurement with 44 values takes about 5ms.
example: CFLAGS += -DANZ_MESS=25

POWER_OFF This option enables the automatic power off function. If you don't specify this option, measurements are done in a loop infinitely until power is disconnected with a ON/OFF switch. If you have the tester without the power off transistors, you can deselect the option POWER_OFF.

If you have NOT selected the POWER_OFF option with the transistors installed, you can also shut down the tester. During displaying the measurement result you should hold the start key pressed for several seconds until the "Timeout" message is displayed. If you then release the key, the tester will be shut off.

You can also specify, after how many measurements without a founded part the tester will shut down. The tester will also shut down the power after twice as much measurements are done in sequence without a single failed part search. If you have forgotten to unconnect a test part, total discharging of battery is avoided. Specify the option with a form like CFLAGS += -DPOWER_OFF=5 for a shut off after 5 consecutive measurements without part found. Also 10 measurements with any founded part one after another will shut down. Only if any

sequence is interrupted by the other type, measurement continues. The result of measurement stay on the display for 28 seconds for the single measurement, for the multiple measurement version display time is reduced to 5 seconds (set in config.h). If the start key is pressed a longer time on power on time, the display time is also 28 seconds for the multiple measurement. The maximum value is 255 (CFLAGS += -DPOWER_OFF=255).
example 1: CFLAGS += -DPOWER_OFF=5
example 2: CFLAGS += -DPOWER_OFF

BAT_CHECK enables the Battery Voltage Check. If you don't select this option, the version number of software is output to the LCD instead. This option is usefull for battery powered tester version to remember for the battery change.
example: CFLAGS += -DBAT_CHECK

BAT_OUT enables Battery Voltage Output on LCD (if BAT_CHECK is selected). If your 9V supply has a diode installed, use the BAT_OUT=600 form to specify the threshold voltage (mV) of your diode to adjust the output value. Also the voltage loss of transistor T3 can be respected with this option. threshold level does not affect the voltage checking levels (BAT_POOR).
example 1: CFLAGS += -DBAT_OUT=300
example 2: CFLAGS += -DBAT_OUT

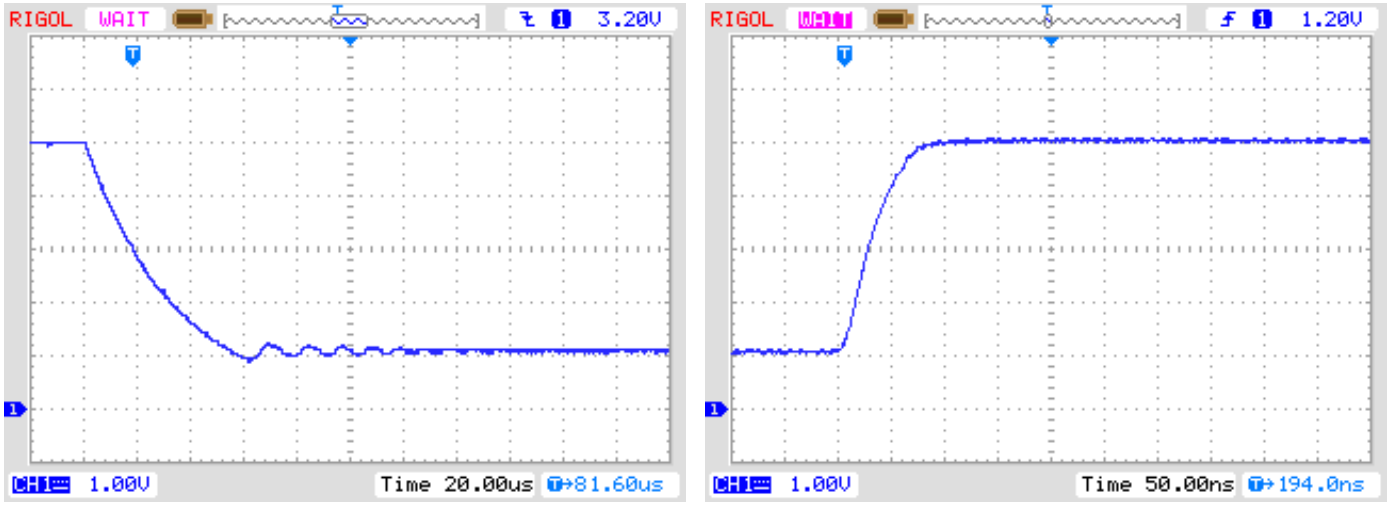
BAT_POOR sets the poor level of battery voltage to the specified 1mV value. The warning level of battery voltage is 0.8V higher than the specified poor level, if the poor level is more than 5.3V. If the poor level is 5.3V or less, the warning level is 0.4V higher. If the poor level is below 3.25V, the warning level is only 0.2V higher than the selected poor level and if the poor level is below 1.3V, the warning level is only 0.1V higher than the specified poor level. Setting the poor level to low values such as 5.4V is not recommended for rechargeable 9V batteries, because this increase the risk of battery damage by the reason of the deep discharge! If you use a rechargeable 9V Battery, it is recommended to use a Ready To Use type, because of the lower self-discharge.
example for low drop regulator (5.4V): CFLAGS += -DBAT_POOR=5400
example for 7805 type regulator (6.4V): CFLAGS += -DBAT_POOR=6400

INHIBIT_SLEEP_MODE disable the use of the sleep mode of the processor. Normaly the software uses for longer work breaks the sleep mode to avoid unneeded current consumption. The usage of this sleep mode indeed spare battery capacity, but produce additional stress for the voltage regulator.
example: CFLAGS += -DINHIBIT_SLEEP_MODE

PROGRAMMER select your programmer type for avrdude interface program. The correct selection of this option is needed, if you use the "make upload" or "make fuses" call of this Makefile. For further information please look to the manual pages of avrdude and online documentation [12].
example: PROGRAMMER=avrisp2

BitClock selects the Bit clock period for the Programmer. See the description of the -B parameter of avrdude.
example: BitClock=5.0

PORT select the port where avrdude can reach your microcontroller (atmega). For further information please look to the manual pages of avrdude.
example: PORT=usb



(a) from 5V to 1.1V

(b) from 1.1V to 5V

Figure 4.1. AREF switching with a $1nF$ Capacitor

Additional parameters can be set in the files transistortester.h and config.h . The file config.h contains global settings, defines the port / pin constellation, the clock frequency of the ADC and the resistor values used for measurement. The file Transistortester.h contains the global variables and tables and also the text used for LCD output. Normally there is no reason to change these values.

Chapter 5

Description of the measurement procedures

The simplified schematic of a Input/Output-Port pin of the ATmega is shown in figure 5.1. The PUD switch isolates all “pull up” resistors of the ATmega. The output of a pin can be switched off with the DD switch. The Input can operate regardless to the state of the switch DD. The PORT switch usually defined the output level, but also switches the pull up resistor. Because the Switches PORT and DD can not be changed at the same time but only one after another, the pull up resistors can disturb the measurement. Therefore I prefere to disable the pull up resistors with the PUD switch. Of course all the switches are electronic type and the resistors 19Ω and 22Ω are approximated values.

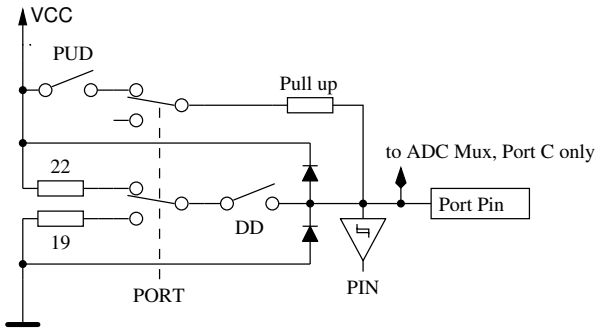


Figure 5.1. simplified diagram of each ATmega port pin

Every of the three terminal probes of your Transistor Tester is build with three ATmega port pins, which is shown as simplified diagram for the terminal probe TP2 (middle of three pins) in figure 5.2.

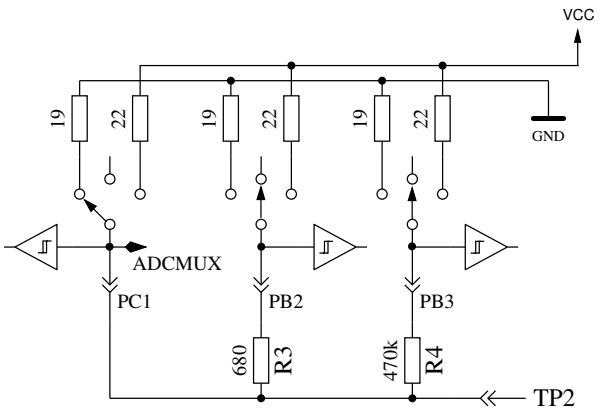


Figure 5.2. simplified circuit of each measurement terminal probe TP

Every test pin (measurement port) can be used as digital or analog input. This measurement capability is independent of using the port as output. Every test pin can be switched to output and in this mode it can be directly connected to GND (0V) or VCC (5V), or it can be connected via a 680Ω resistor or a $470k\Omega$ resistor to either GND or VCC. Table 5.1 shows all possible combination of measurements. Notice, that the positive state can be switched directly to VCC (Port C) or it can be connected with the 680Ω resistor to VCC (Port B). The same possibility has the negative state of terminal probe to the GND side. The test state means, that probe can be open (Input), connected with the $470k\Omega$ resistor to VCC or GND, or that the probe can be connected with the 680Ω resistor to VCC or GND.

	state pin 1	state pin 2	state pin 3
1.	positive	negative	test
2.	positive	test	negative
3.	test	negative	positive
4.	test	positive	negative
5.	negative	test	positive
6.	negative	positive	test

Table 5.1. all combinations of measurement

If the capacitor measuring is configured for the tester, the tester will try to discharge the capacitors connected at all test pins. If discharge will fail, that means the remaining voltage is to high, the discharging will be aborted after about 12 seconds with the meassage "Cell!". This can also be happen, if no capacitor is connected to any test pin. The cause for this can be, that the cut-off voltage is choosed to low for this ATmega. You can choose a higher voltage with the Makefile option CAP_EMPTY_LEVEL.

5.1 Measurement of Semiconductors

The currentflow of the device with currentless control gate (third pin, also called Tristate pin) is to be examined first. The Tristate pin of the device under test is the base or gate for example. One probe pin is selected as the positive side of the device and connected directly to VCC. The other probe pin selectes as negative side of the device. The negative side is connected with the 680Ω resistor to GND. With fieldeffect transistors the state of the device depends on the voltage of the gate. The Tristate pin is first connected with the 680Ω resistor for 5ms to the GND side and the voltage at the negative side is measured. After that the voltage of the negative side is measured again during the Tristate pin switched as input (High Impedance). Then the assumed gate is connected with the 680Ω resistor for 5ms to the VCC side and the voltage on the negative side is measured again. If the measured voltage is lower than the first measurement result, this circuit will be assumed as the right one. Then the voltage is measured again with currentless Tristate pin.

If the voltage of the negative pin with fixed Tristate pin is higher than $115mV$ and this level is not $100mV$ lower than the voltage measured with currentless Tristatepin, a depletion transistor type is assumed. With bipolar transistors, which have a high collector residual current, the residual current with currentless base is usually significant higher. With the checking of both voltages we can avoid the wrong detection of some Germanium transistors with a higher collector cutoff current as depletion transistors (JFET).

Then additional tests are done to differ N-channel JFET or N-D-MOSFET and P-channel JFET or P-D-MOSFET. Die MOSFET-Versionen knnen erkannt werden durch das Fehlen von Steuerstrom in jedem TriStatePins Zustand. The MOSFET versions can be differed by the missing of gate current in any state of the TriStatePin.

To get parameters of the depletion types, they will be measured with a 680Ω resistor at the source pin, as shown in figure 5.3 . This measurement will be done instead of the usually measurement of current with the gate hold at source level, because the I_{DSS} current of the FET transistor can often not be reached with the relative high resistance of the 680Ω resistor.

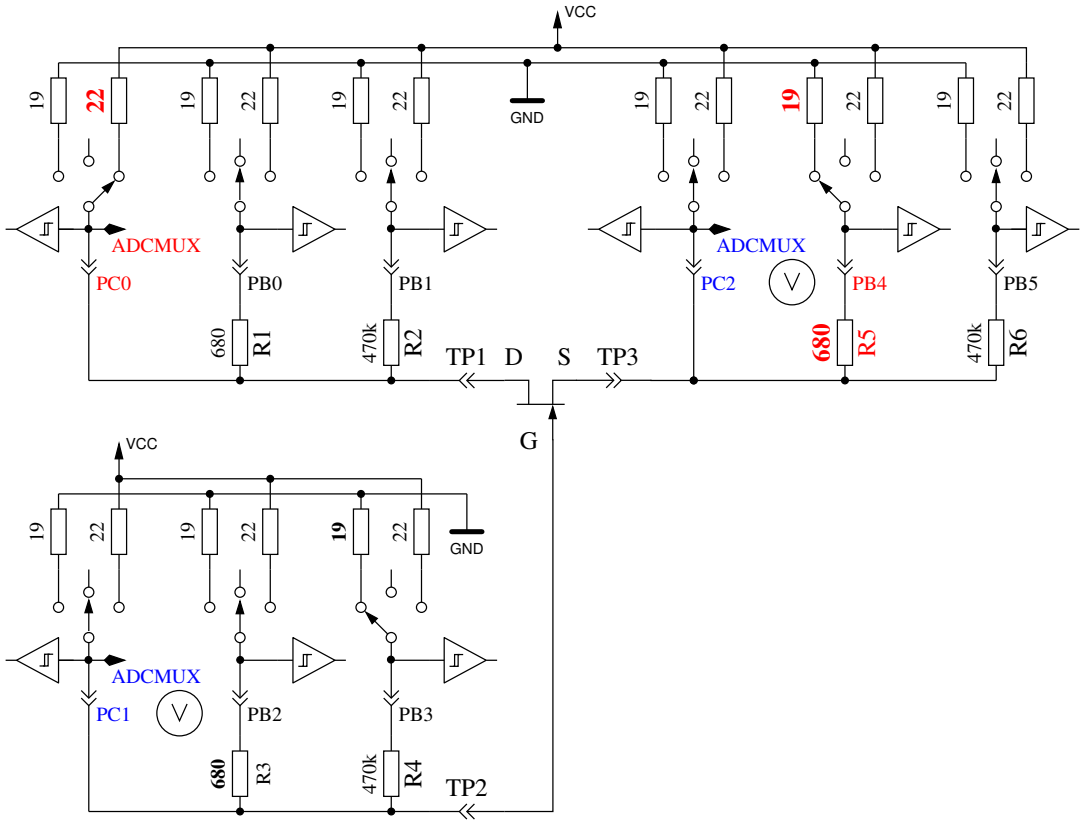


Figure 5.3. Measurement of the Gate-Source voltage and Source current of a N-JFET transistor

If the component has no current between positive probe and negative probe without signal at the TristatePin, the next tests are specified in the next section 5.1.1. If current was detected, the next test is described in the diode section 5.1.4.

5.1.1 Measurement of PNP Transistor or P-Channel-MOSFET

First the current amplification factor is measured with common collector (emitter follower) for the assumed PNP transistor. The measuring situation is shown in figure 5.4. If the measured voltage at the Base (UB) is above 9mV with the 680Ω resistor, the hFE is build as $hFE = \frac{UE-UB}{UB}$. The voltage UE is the difference of the Emitter-voltage to VCC. The difference between the 22Ω and 19Ω resistors are not respected. If the UB voltage is below 10mV, the measurement is done with the $470k\Omega$ resistor at the base. In this case the current amplification factor is build as $hFE = \frac{UE \cdot 470000}{UB \cdot (680+22)}$.

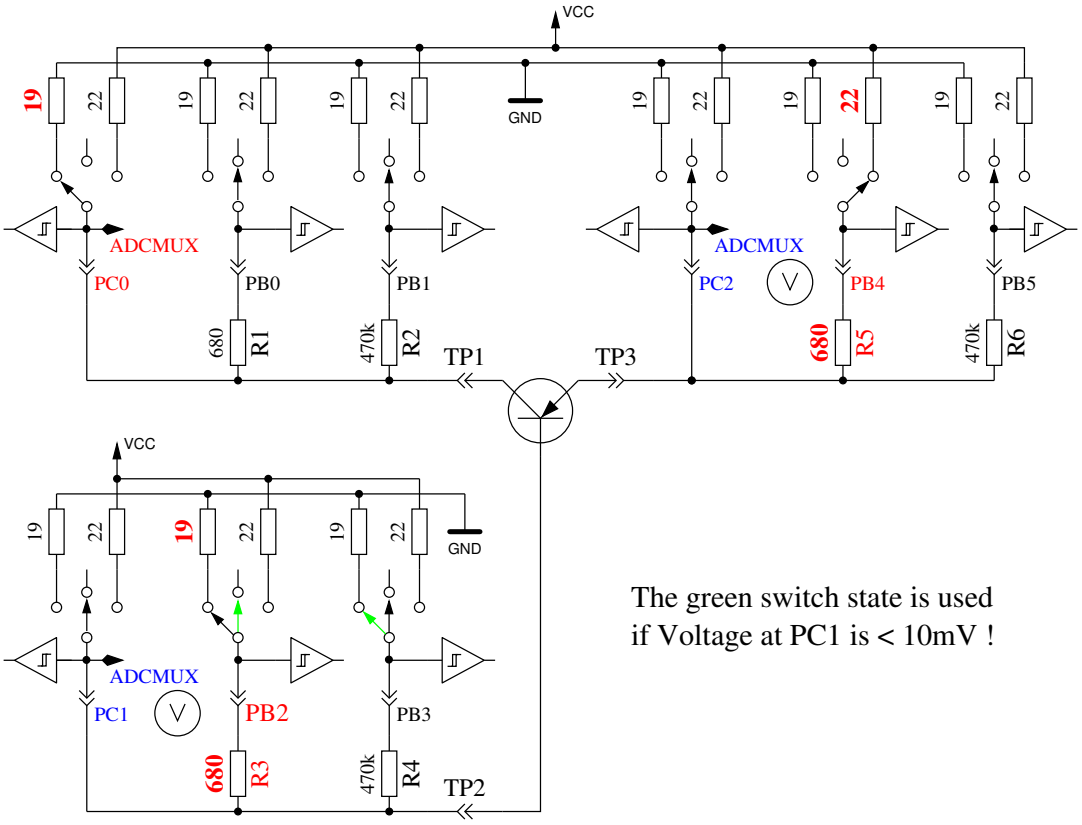


Figure 5.4. hFE measurement of PNP transistor with common collector circuit

Next the tests with common emitter are done for the assumed PNP transistor. The positive side of component is now direct connected to VCC, the negative side 680Ω resistor is connected to GND as shown in Figure 5.5. If the negative side of component has a voltage of above 3.4V, when the base side 680Ω resistor was connected to GND, it must be a PNP transistor or a P-Channel FET. This can be easy find out by analysing the base voltage. If the base voltage is greater 0.97V, it must be a PNP. For measuring the current amplification factor, the $470k\Omega$ resistor is taken as Base resistor instead of the 680Ω. The current amplification factor is build by $hFE = \frac{(UC-UC0)\cdot 470000}{UB\cdot(680+19)}$. The voltage UC0 is the voltage at the colletor resistor without base current. The higher current amplification factor is assumed to be the right one, this one or the one found with the common collector circuit.

The values found for the PNP are only valid, if a second set of measurements is done. In order to prevent detecting the PNP in the inverse mode (collector and emitter are swapped), the measurement with the higher current amplification is taken as the right one. If base voltage is lower than 0.97V, it must be a P-E-MOS. In this case the gate threshold voltage is measured by switching the gate slowly with the $470k\Omega$ resistor up and down, waiting for a digital input signal change of the Drain side and then read the voltage of the gate pin.

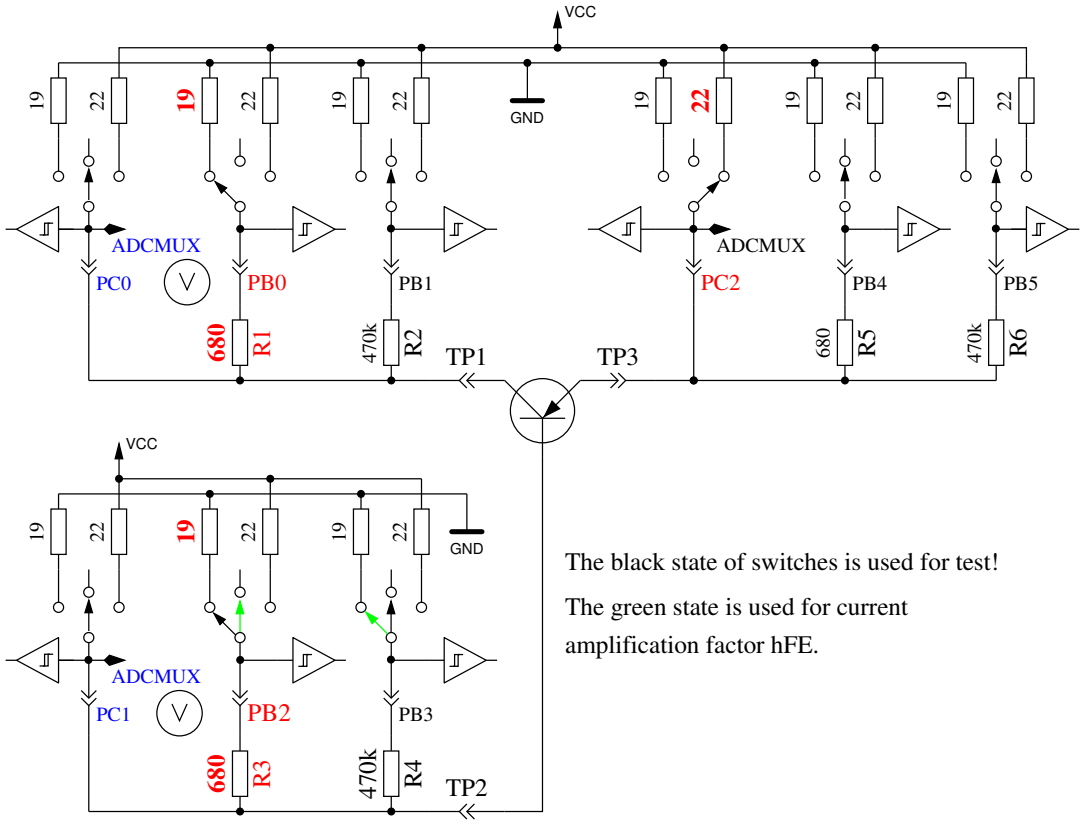


Figure 5.5. test and hFE measurement of PNP transistor with common emitter circuit

5.1.2 Measurement of NPN Transistor or N-Channel-MOSFET

The measuring of NPN-Transistors begin in the same way as PNP-Transistors with measuring the current amplification factor in the common collector circuit. First measurement is done with a 680Ω base resistor switched to VCC. If the voltage at the base resistor ist too low, the $470k\Omega$ resistor is taken instead. Measurement then continues with the common emitter circuit as shown in figure 5.6.

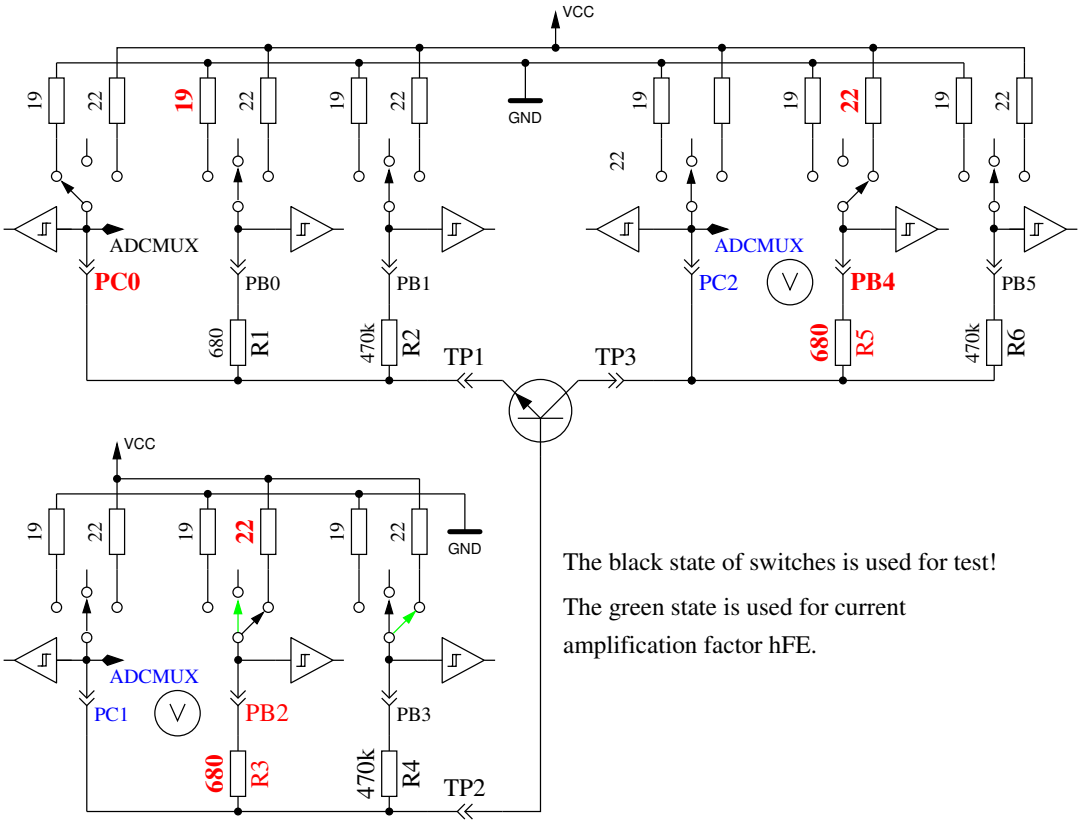


Figure 5.6. test and hFE measurement of NPN transistor with common emitter circuit

If the voltage of collector sinks below 1.6V, when the 680Ω base resistor is connected to VCC, ist must be a NPN, N-Channel MOSFET or Thyristor/Triac. With two simple tests a Thyristor or Triac can be identified. If the gate pin resistor is connected for 10ms to GND and than made currentless, the current at the anode should stay. If then the anode resistor is short connected to GND and reconnected to VCC, the Thyristor should not trigger again (no current). Please keep in mind, that only low power Thyristors can be tested, because the holding current of the tester can reach only 6mA. If both tests attest a Thyristor, further tests with reverse polarity are done to exclude or confirm a Triac.

If neither Thyristor nor Triac could be confirmed, it can be a NPN or N-Channel E-MOSFET. The Base voltage of a NPN Transistor will be near the Emitter voltage, so this type can be identified definitely. The current amplification factor in the common emitter circuit is build by $hFE = \frac{(VCC-UC-UC0)\cdot 470000}{(VCC-UB)\cdot(680+22)}$. If the voltage of the Base or better Gate shows, that there is no or little current, part will be a N-Channel E-MOS (Enhancement MOSFET). In this case the threshold voltage is measured by switching the Gate slowly with the $470k\Omega$ resistor to VCC and GND, waiting for a digital input signal change of the Drain side and then read the voltage of the Gate pin. This measurement is done eleven times with ADC results accumulated as shown in Figure 5.7. The result is multiplied by four and divided by 9 to get the voltage in mV resolution.

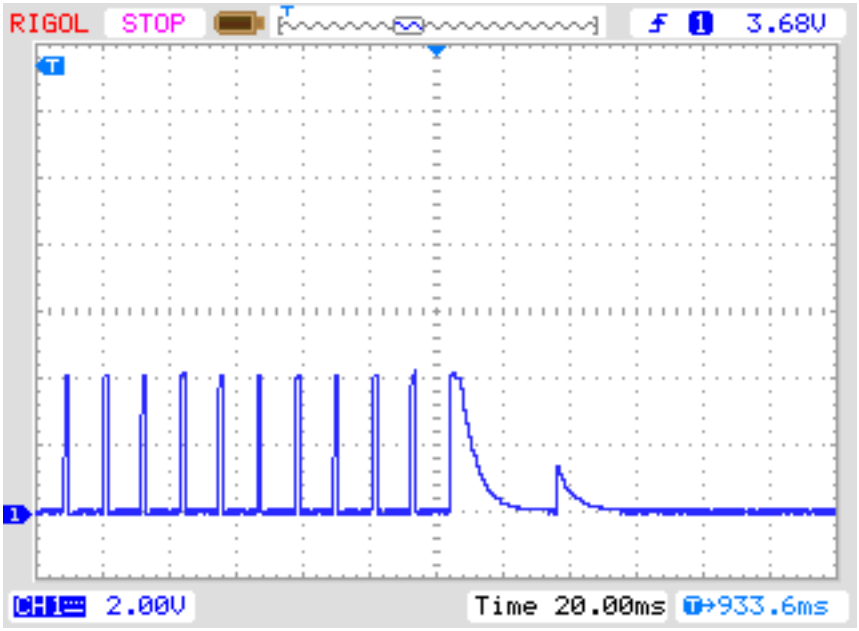


Figure 5.7. measuring of threshold voltage of N-Channel-MOSFET

5.1.3 Simplified flowchart of the transistors tests

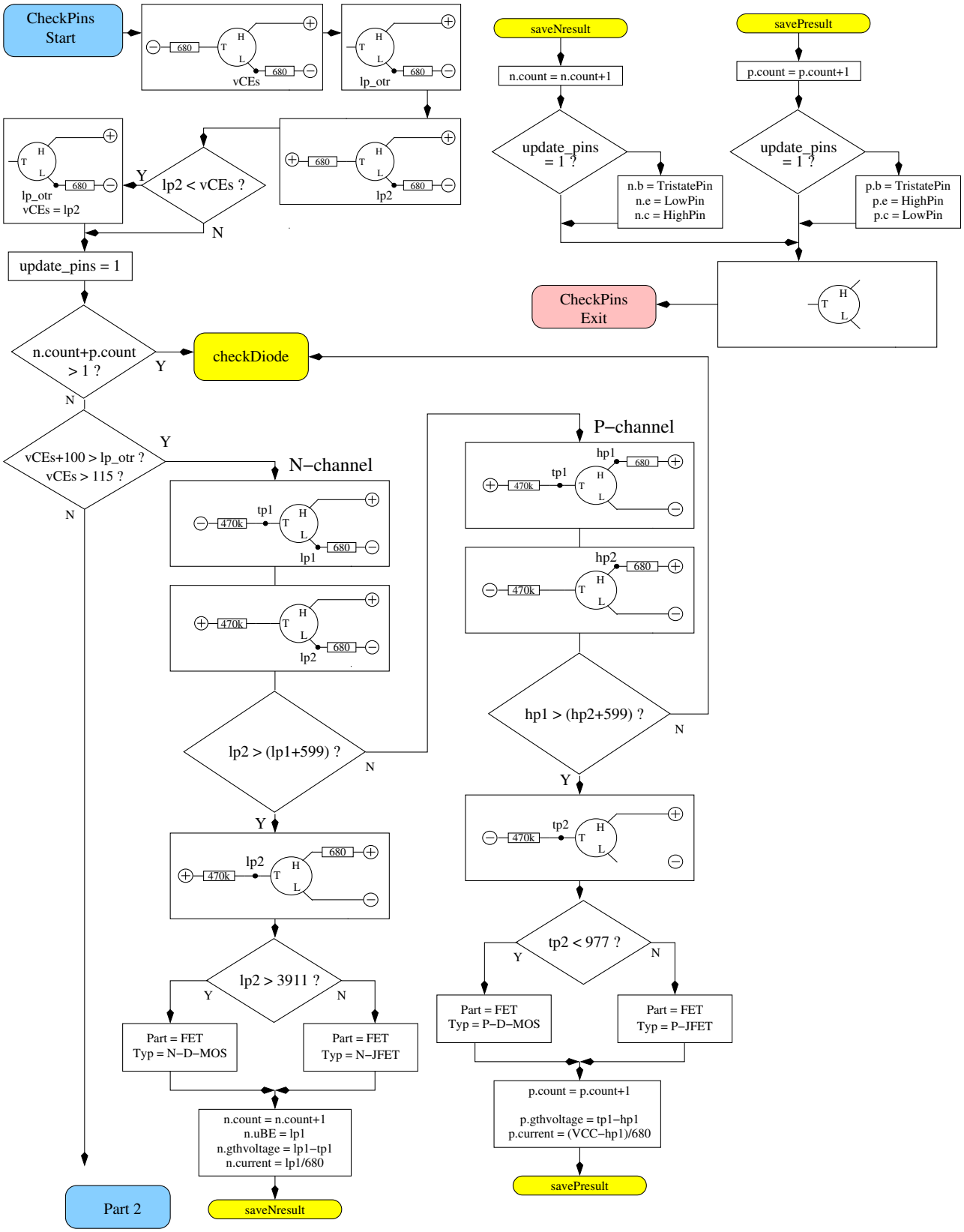


Figure 5.8. Flowchart transistor test Part 1, JFET and D-MOS

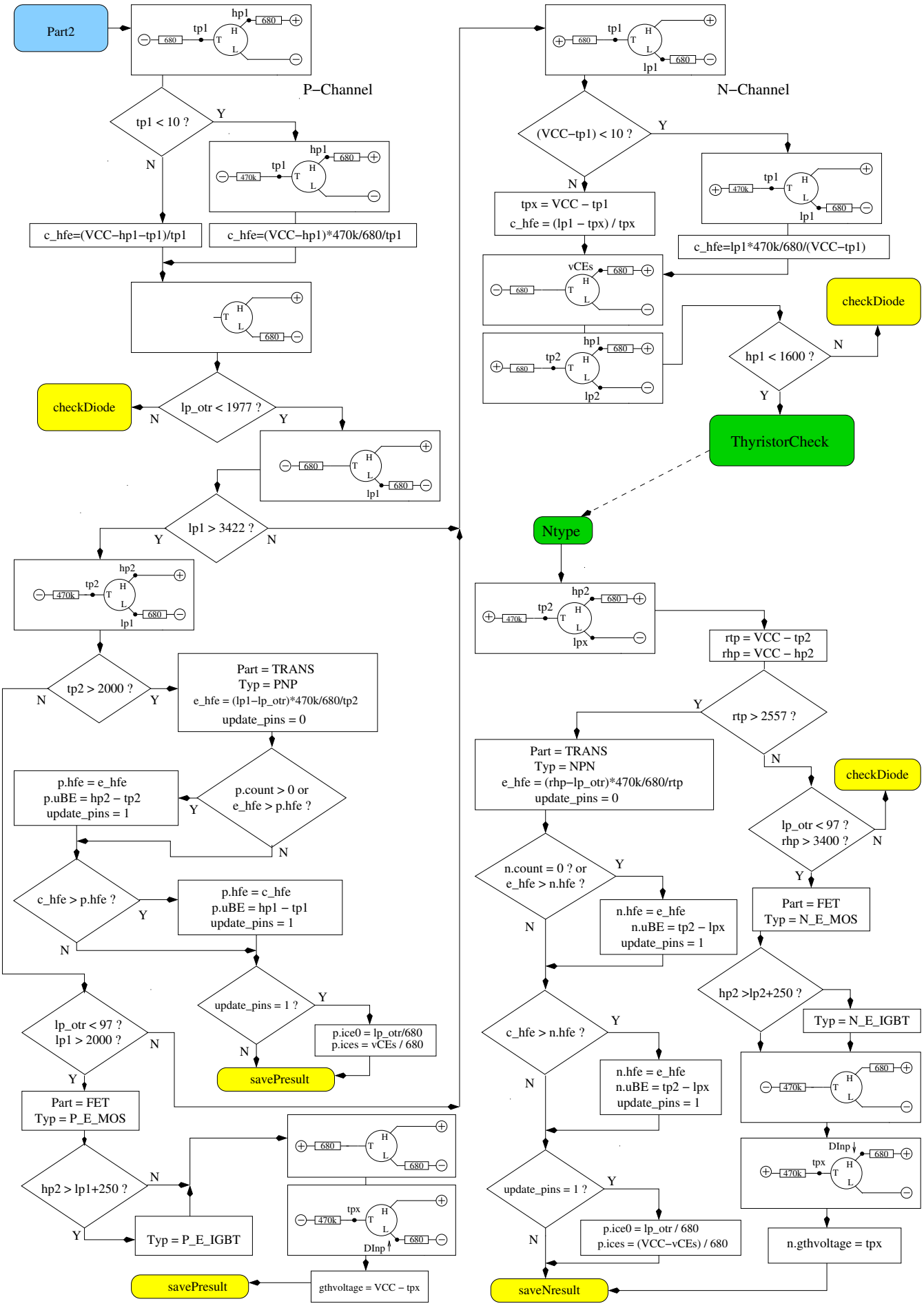


Figure 5.9. Flowchart transistor test Part 2, BJT and E-MOS

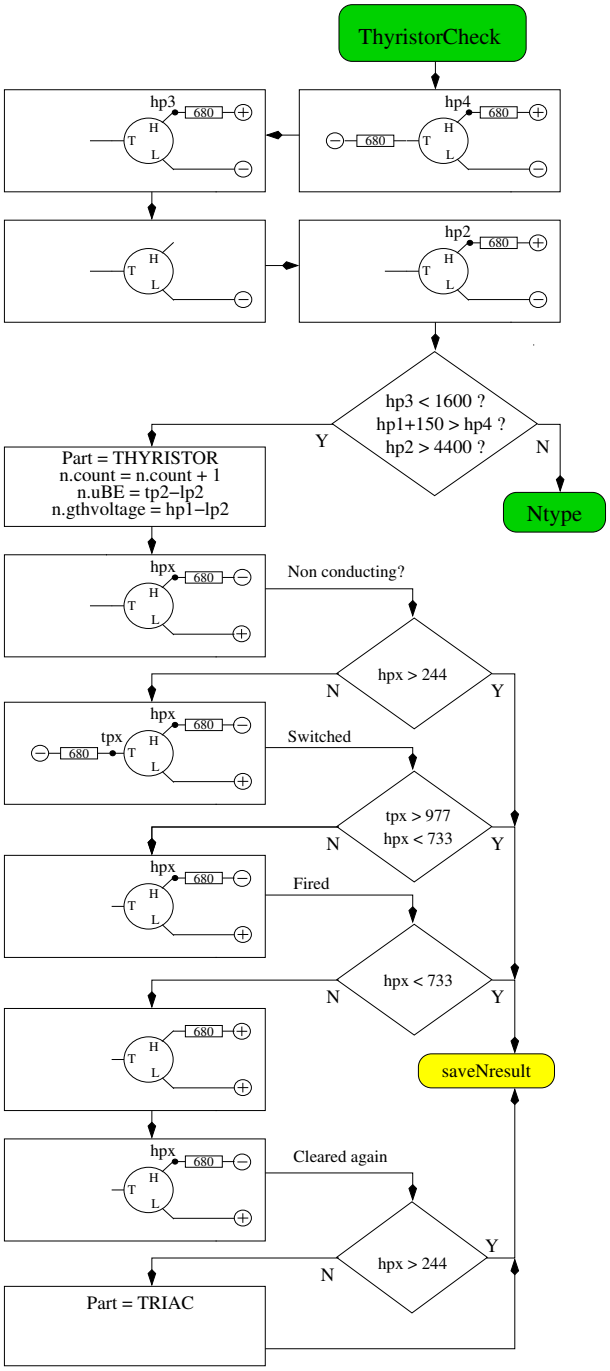


Figure 5.10. Flowchart transistor test Part 3, Thyristor and Triac

5.1.4 Measurement of Diodes

If current is detected with the pre-tests, the behavior of the part will be checked to be a diode. The flow voltage with the 680Ω resistor must be between 0.15V and 4.64V. The flux voltage with the 680Ω must be greater than 1.125 times the flux voltage with the $470k\Omega$ resistor and sixteen times the flux voltage with the $470k\Omega$ must be greater than the flux voltage with the 680Ω resistor. Additionally the afterward renewed measurement with the $470k\Omega$ resistor should not have a higher voltage than the previous measurement with the 680Ω resistor. I hope, that this behavior identifies always a diode. The identification of a diode by no current flow in the opposite direction is not possible with a inverse parallel diode. If only a single diode is detected, the residual current in reverse direction is measured with the $470k\Omega$ resistor at 5V. The resolution is about $2nA$. If the residual current is greater as $5.3\mu A$ (voltage at the $470k\Omega$ is more than 2.5V), the measurement is done with the 680Ω

instead. Then the resolution is only about $1\mu A$. Furthermore the capacity in reverse direction is also measured for single diodes.

5.1.5 Results of different measurements

The following three tables shows results of different test probes with one ATmega8, a ATmega168 and a ATmega328 processor. The measurement of the inverse capacity value for the double diode MBR4045PT is only possible with cooling. This will be caused by high residual current of this 40A diode. Also the capacity value of the inverse base emitter diode of the germanium transistor AC128 can only be measured with cooling.

Diode Type	Mega8@8MHz	Mega168 @8MHz	Mega328 @8MHz
1N4148	Diode, 715mV, 1pF	Diode, 718mV, 0pF, 2nA	Diode, 715mV, 1pF, 4nA
1N4150	Diode, 665mV, 1pF	Diode, 672mV, 1pF, 4nA	Diode, 666V, 2pF, 6nA
BA157	Diode, 619mV, 19pF	Diode, 621V, 17pF, 12nA	Diode, 615mV, 18pF, 12nA
BY398	Diode, 538mV, 16pF	Diode, 541mV, 14pF, 63nA	Diode, 537mV, 15pF, 63nA
1N4007	Diode, 650mV, 13pF	Diode, 655mV, 10pF, 6nA	Diode, 650mV, 13pF, 6nA
LED green	Diode, 1.96V, 5pF	Diode, 1.95V, 4pF	Diode, 1.95V, 4pF
ZPD2,7	2xDi, 743mV, 2.53V	2xDi, 737mV, 2.52V	2xDi, 733mV, 2.51V
BU508A B+E	Diode, 609mV, 5.15nF	Diode, 611mV, 5.20nF, 0.39uA	Diode, 606mV, 5.25nF, 0.4uA
BU508A B+C	Diode, 582mV, 256pF	Diode, 586mV, 255pF, 21nA	Diode, 587mV, 259pF, 19nA
AC128 B+E	Diode, 272mV, 0pF	Diode, 277mV, 0pF, 2.2uA	Diode, 273mV, 0pF, 2.3uA
AC128 B+E cooled			Diode, 349mV, 140pF, 0.57uA
MBR20100CT	2xDi, 337mV, 337mV	2xDi, 338mV, 338mV	2xDi, 336mV, 335mV
MBR20100CT	Diode, 337mV, 345pF	Diode, 339mV, 351pF, 29nA	Diode, 337mV, 350pF, 25nA
MBR4045PT cooled	Diode, 243mV, 1.80nF	Diode, 233mV, 1.94nF, 1.7uA	Diode, 235mV, 1.95nF, 1.8uA
SK14	Diode, mV, 0pF	Diode, mV, pF, nA	Diode, 263mV, 0pF, 0.57uA
SK14 cooled	Diode, mV, nF	Diode, mV, pF, nA	Diode, 334mV, 88pF, 4nA
SF38G	Diode, 519mV, 107pF	Diode, 521mV, 105pF, 2nA	Diode, 516mV, 106pF, 2nA

Table 5.2. measurement results of diode testing

Transistor Type	Typ	Mega8 common-collector	Mega328	Mega328 common-collector	Mega328 common-emitter
BU508A	NPN	B=9, 601mV	B=9, 597mV	B=9, 598mV	B=4, 484mV
2N3055	NPN	B=20, 557mV	B=21, 550mV	B=21, 550mV	B=6, 442mV
BC639	NPN	B=148, 636mV	B=172, 629mV	B=172, 629mV	B=158, 605mV
BC640	PNP	B=226, 650mV	B=176, 609mV	B=171, 655mV	B=177, 608mV
BC517	NPN	B=23.9k, 1.23V	B=24.8k, 1.22V	B=25.1k, 1.22V	B=764, 1.23V
BC516	PNP	B=75.9k, 1.21V	B=76.2k, 1.20V	B=76.2k, 1.20V	B=760, 1.23V
BC546B	NPN	B=285, 694mV	B=427, 687mV	B=427, 687mV	B=369, 683mV
BC556B	PNP	B=304, 704mV	B=254, 668mV	B=235, 709mV	B=255, 668mV
AC128 (Ge.)	PNP	B=63, 191mV	B=59, 191mV	B=57, 193mV	B=43, 117mV
BUL38D parasitic	NPNp PNPn	B=37, 627mV B=11, 654mV	B=41, 617mV B=81, 543mV	B=40, 624mV B=10, 656mV	B=36, 562mV B=83, 541mV
BRY55/200	Thyrist.	0.84V	0.81V	0.81V	0.82V
MAC97A6	Triac	0.92V	0.90V	0.90V	0.90V

Table 5.3. measurement results of bipolar transistor testing

Some results are very different to the earlier results of the software of Markus Frejek. For example a darlington transistor BC517 has been measured by the older software with a hFE of 797 instead of 77200 and a base emitter voltage of 1438mV. This will be caused by the additional measurement of current amplification with the common collector circuit. Also the new version shows the same low hFE result with the common emitter circiut, as you can see in the last column of table 5.3. The base emitter voltage is measured by the older Version as separate diode test with 1438mV. Now the base emitter voltage is measured with the state of current amplification testing (1.20V). The BUL38D Transistor has a build in protection diode over the anode and cathode of the NPN transistor, by what a parasitical PNP transistor with swapped Base - Collector connection is build. With software revision 1.10k both transistors are detected and marked with a appended p. The right transistor will be found with comparation of the gate - emitter junction capacitance. It is assumed, that the right transistor has the higher junction capacitance. If you hold down the start key during the output of the measurement result, the parameter of the parasitical transistor are shown. With the label PNPn the existance of another transistor will be marked. The parasitical transistor structure is build only by integration of the protection diode nearby the transistor within the same material, not with a external diode.

The following table 5.4 shows the measurement results for germanium transistors, which are extra problematic to measure because of the temperatur dependent and high residual collector current. The results of the original version of Markus F. and the results of the actual 1.10k version are compared together. The 1.10k version for a ATmega328 measures the current amplification factor with common collector and common emitter circuit with respect to the collector residual current, the higher result will be shown. The collector residual current is not respected by earlier versions.

Transistor Type	Mega8@1MHz Original Version Markus F.	Mega168 @8MHz Version 1.10k	Mega328 @8MHz Version 1.10k
AC128	PNP, B=52, 279mV	PNP, B=59, 184mV	PNP, B=59, 191mV
AC116-65	PNP, B=505, 378mV	PNP, B=72, 146mV	PNP, B=72, 149mV
AC116-145	PNP, B=485, 294mV	PNP, B=146, 161mV	PNP, B=146, 163mV
AC176-65	NPN, B=98, 235mV	NPN, B=58, 94mV	NPN, B=56, 96mV
GC122	PNP, B=84, 368mV	PNP, B=55, 117mV	PNP, B=56, 117mV
GC301	PNP, B=48, 289mV	PNP, B=39, 184mV	PNP, B=39, 188mV
AD161	NPN, B=360, 230mV	NPN, B=296, 126mV	NPN, B=298, 128mV
AD162	PNP, B=2127, 280mV	PNP, B=89, 107mV	PNP, B=89, 107mV

Table 5.4. Measurement results of bipolar junction germanium transistors

In the table 5.5 the results of some field-effect transistor measurements are shown. One measured parameters of the E-type MOS types is the gate-source voltage, by which the digital input of the ATmega connected to the 680Ω drain resitor changes the state. The other parameter is the gate capacity value. For very fast change of the gate voltage due to a small gate capacity, the detected voltage is slightly inaccurate. With the BS250 the Voltage changes from 2.6V to 2.5V, if you connect a additional $10nF$ capacitor to the gate-source. For JFET transistors often the characteristic current Idss is specified, the current in the drain when the gate-source voltage is 0V. Here, however, the current is given by a 680Ω load resistance at the source side of the JFET. The load resistor generates a reverse voltage Vgs, which is also shown. Due to the symmetrical design of the JFET transistors, the drain and source can not be distinguished.

Transistor	Type	Mega8@8MHz	Mega168 @8MHz	Mega328 @8MHz
ZVNL120A	N-E-MOS	D, 1.6V, 147pF	D, 1.5V,141pF	D, 1.5V, 140pF
IRF530N	N-E-MOS	D, 3.6V, 1.55nF	D, 3.6V, 1.54nF	D, 3.6V, 1.54nF
BS170	N-E-MOS	D, 2.6V, 78pF	D, 2.6V, 68pF	D, 2.6V, 68pF
IRL3803	N-E-MOS	D, 2.3V, 9.81nF	D, 2.3V, 9.71nF	D, 2.3V, 9.74nF
IRFU120N	N-E-MOS	D, 4.2V, 909pF	D, 4.2V, 913pF	D, 4.2V, 911pF
BUZ71A	N-E-MOS	D, 3.2V, 714pF	D, 3.2V, 708pF	D, 3.2V, 705pF
ZVP2106A	P-E-MOS	D, 3.2V, 122pF	D, 3.2V,115pF	D, 3.2V, 116pF
IRF5305	P-E-MOS	D, 3.6V, 2.22nF	D, 3.6V, 2.22nF	D, 3.6V, 2.22nF
BS250	P-E-MOS	D, 2.6V, 53pF	D, 2.6V, 43pF	D, 2.6V, 44pF
IRFU9024	P-E-MOS	D, 3.5V, 937pF	D, 3.6V, 945pF	D, 3.5V, 933pF
J310 Idss=24-60mA	N-JFET	3.1mA Vgs=2.2V	3.1mA Vgs=2.2V	3.1mA Vgs=2.2V
2N5459 Idss=4-16mA	N-JFET	2.1mA Vgs=1.5V	2.1mA Vgs=1.5V	2.1mA Vgs=1.5V
BF256C Idss=11-18mA	N-JFET	3.4mA Vgs=2.4V	3.4mA Vgs=2.4V	3.4mA Vgs=2.4V
BF245A Idss=2-6mA	N-JFET	1.1mA Vgs=.75V	1.1mA Vgs=0.75V	1.1mA Vgs=0.75V
BF245B Idss=6-15mA	N-JFET	2.5mA Vgs=1.7V	2.5mA Vgs=1.7V	2.5mA Vgs=1.7V
BF245C Idss=12-25mA	N-JFET	3.9mA Vgs=2.7V	3.9mA Vgs=2.7V	3.9mA Vgs=2.7V
J175 Idss=7-60mA	P-JFET	3.2mA Vgs=2.2V	3.2mA Vgs=2.2V	3.2mA Vgs=2.2V
2N5460 Idss=1-5mA	P-JFET	0.78mA Vgs=0.54V	0.77mA Vgs=0.54V	0.78mA Vgs=0.54V
BSS139	N-D-MOS	1.7mA Vgs=1.2V	D, 1.7mA Vgs=1.2V	D, 1.7mA Vgs=1.2V
BSS169	N-D-MOS	2.6mA Vgs=1.8V	D, 2.6mA Vgs=1.8V	D, 2.6mA Vgs=1.8V
GP07N120	N-E-IGBT	C=3.81nF Vt=4.2V	C=3.76nF Vt=4.2V	C=3.74nF Vt=4.2V

Table 5.5. measurement results of MOS transistor testing

5.2 Resistor Measurement

Each resistor is measured with four different types of measurement in one current direction. The same resistor ist also tested with the same four measurement types in the other current direction. The measurement in the opposite direction is only used to identify a resistor. If mismatch between both measurements is too big, it's not a resistor.

5.2.1 Resistor Measurement with 680 Ohm Resistors

The measurement of a unknown resistor Rx is done in two ways with the build in precision 680Ω resistors. The diagram of this measurements for test pin 1 (TP1) and test pin 3 (TP3) are simplified shown in figure 5.11 and figure 5.12 as a example of the six choises of probe combinations.

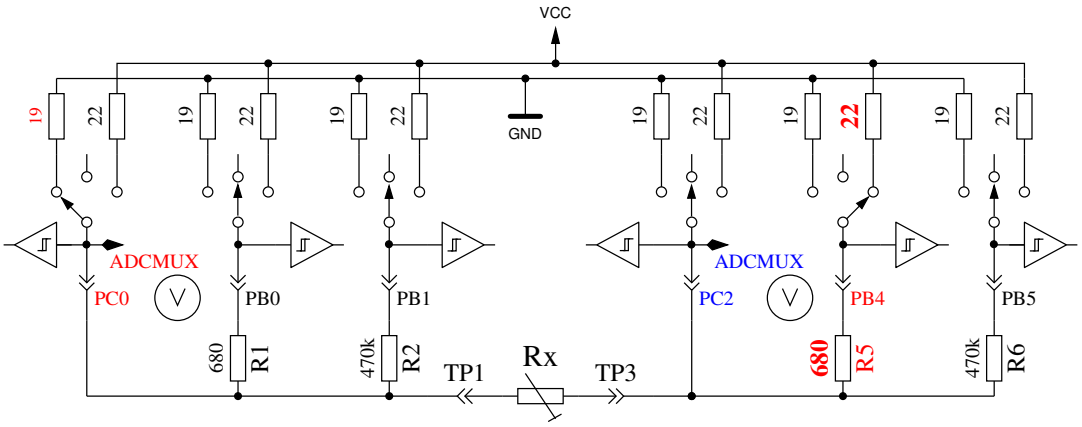


Figure 5.11. Measurement type 1 with 680Ω

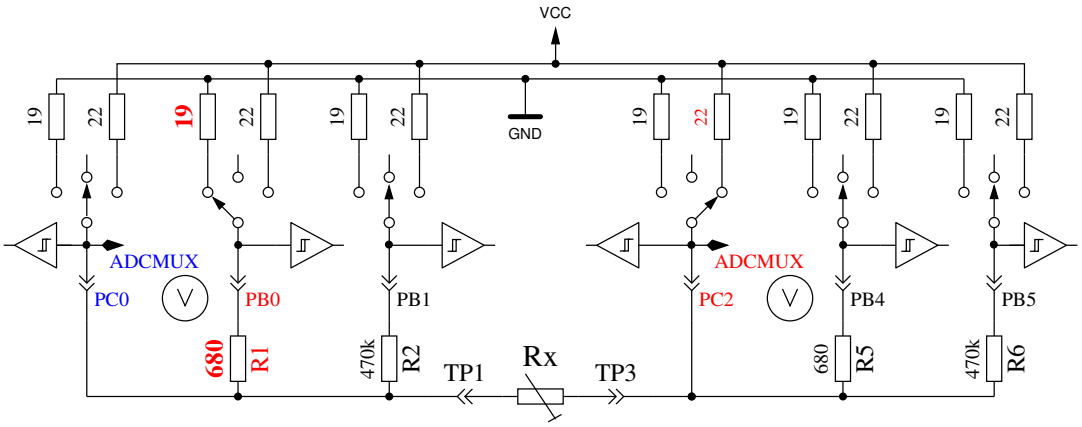


Figure 5.12. Measurement type 2 with 680Ω

On the left side test pin 1 is shown and on the right side you can see test pin 3. In both diagrams you see, that the terminal 3 (right side) is connected to VCC, the left side is connected to GND. The direction of current flow through the resistor Rx is allways the same. The values of ports switched to output are shown with red color, the values of ports used as Input are shown in blue color, the inactive ports are black. In both shown measurement types the current should have the same value, because the sum of resistor values between VCC and GND is identical (if the build in resistors are identical). Usually the measured voltage is not the same, because the sequence of resistors has changed.

The V symbol within the circle marks the ports used for voltage measurement. In both configurations the value of resistor Rx can be computed with the known resistor values and the measured voltages, if the relation of resistor Rx and the 680Ω is not too high. The theoretical voltage gradient is shown in figure 5.13, where resistor values are shown in logarithmic scale.

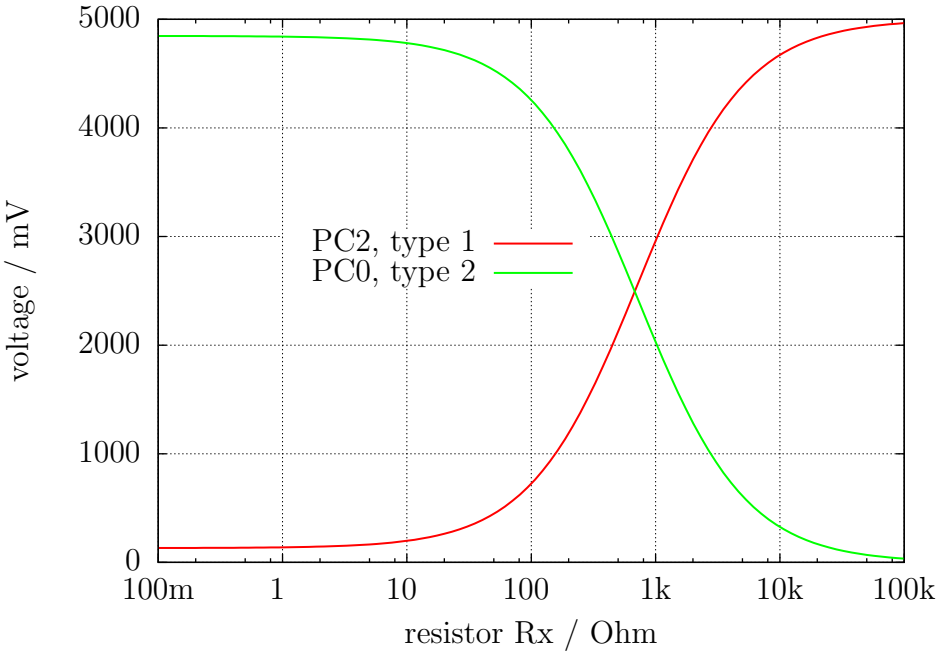
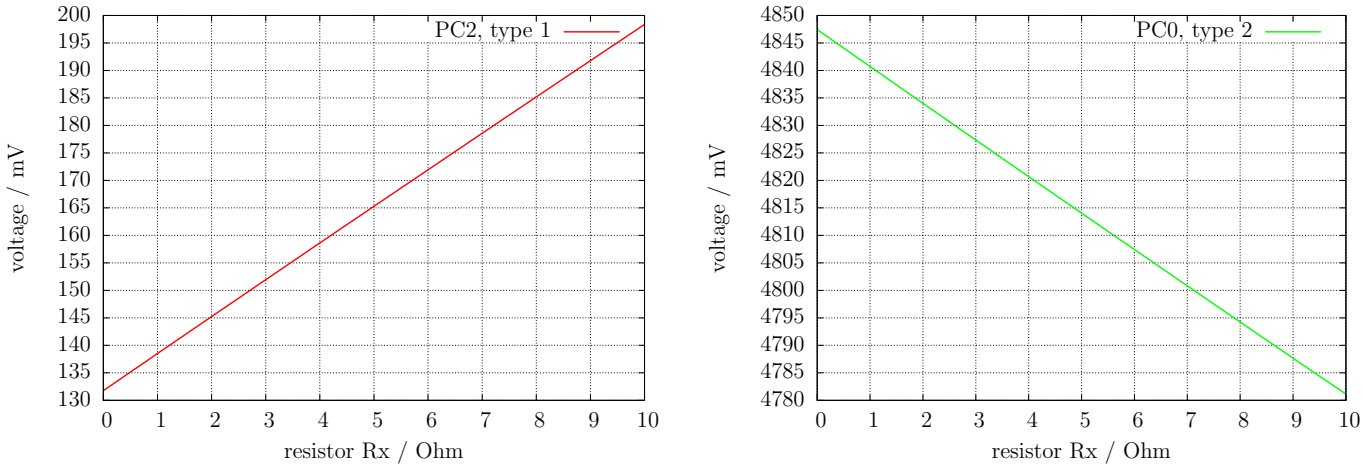


Figure 5.13. Voltages of type 1 and type 2 measurements with 680Ω

The graph of measurement type 1 is shown in figure 5.14a with zoomed scale for the lower resistor range. You can see, that you need a better ADC resolution than the standard 4.9mV resolution at the 5V ADC reference, to get the right resistor value from measured voltage below 2Ω. There are only three ADC steps from 0Ω to 2Ω. The range switching with the AUTOSCALE_ADC option can help in this case. The same zoomed range of measurement type 2 shows the figure 5.14b. Unfortunately we can not use the higher ADC resolution for measurement type 2 in this range, because the voltage is too high and our ATmega have no differential ADC input. Measurements with the 680Ω resistors are taken for building the result of measurements up to 20$k\Omega$ (Voltage of measurement type 2 will be below 169mV).

For higher resistor values the measurements with the 470$k\Omega$ resistors are used. The mean value of both measurements is taken as displayed resistor value, if all tests attests, that it is no other type of part. If the AUTOSCALE_ADC function is selected and one of the voltages of the both measurement types is below 0.98V, a weighted average is build with factor four for this value. The other value is weighted with factor one. This is done to respect the factor four better resolution of this measurement. Factor four is only taken for ATmega168 and ATmega328 processors, for the ATmega8 two is taken as weighting factor if voltage is below 0.98V, because the reference voltage for the ADC is here 2.54V instead of 1.1V . If the ATmega has more than 8KByte flash memory, the voltage measurement at the resistors will be delayed until no more changes are detected or the time limit is reached. With this method big capacitors are no more detected as resistors by mistake and the DC resistance of big inductors will be measured correctly.



(a) Type 1 measurement

(b) Type 2 measurement

Figure 5.14. Cut-out of theoretical Voltage from 0Ω to 10Ω

5.2.2 Resistor Measurement with 470 kOhm resistors

The next figures 5.15 and 5.16 shows the same measurement procedure for the measurement with the precision $470k\Omega$ resistors. Because the $470k\Omega$ is very big in relation to the port resistor values 22Ω and 19Ω, the port resistor values are ignored for the computing of the resistor value Rx.

For both measurement types with the $470k\Omega$ resistors only one Voltage is measured, because the current is so low, that no voltage difference at the internal port resistors of the ATmega can be measured (as expected). The theoretical voltage gradient is shown in figure 5.17 where the resistor values are again shown in logarithmic scale. The theoretical gradient in this diagram ends at $100M\Omega$, but the resulting value of the Tester is limited to $60M\Omega$, otherwise the Tester assumes that no resistor is connected. The weighted average of both measurement types is taken as result with the same rules described for the measurements with the 680Ω resistors. For all ATmega processors I had found, that the measured results with the $470k\Omega$ resistors are more exactly, if a constant offset of 350Ω will be added. This offset can be adjusted with the RH_OFFSET define in the config.h file.

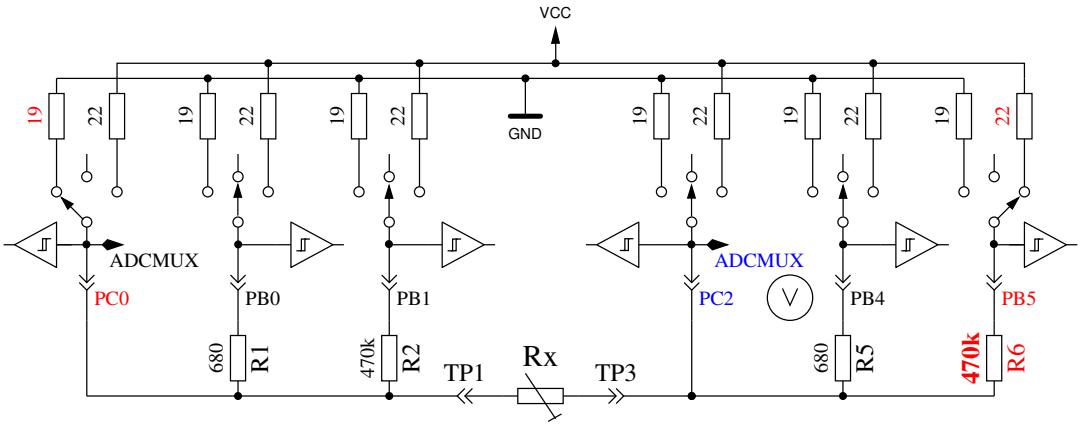


Figure 5.15. Measurement type 3 with $470k\Omega$

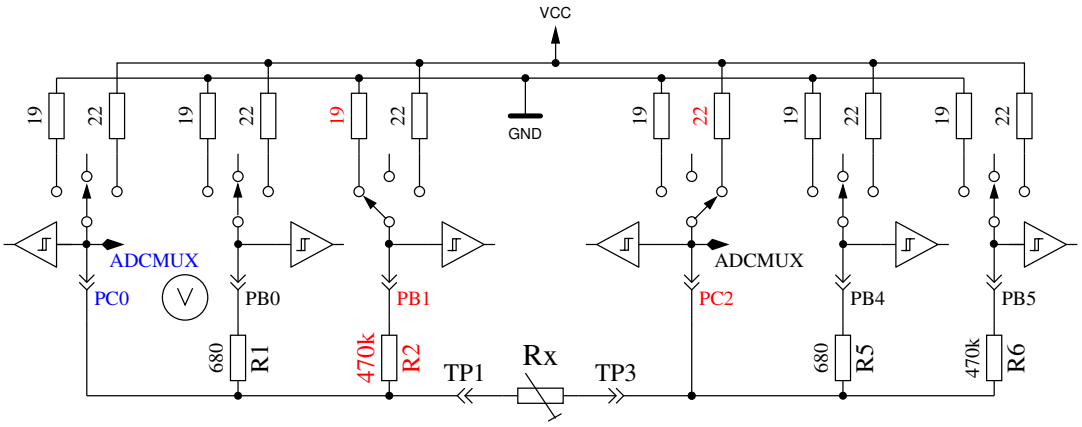


Figure 5.16. Measurement type 4 with $470k\Omega$

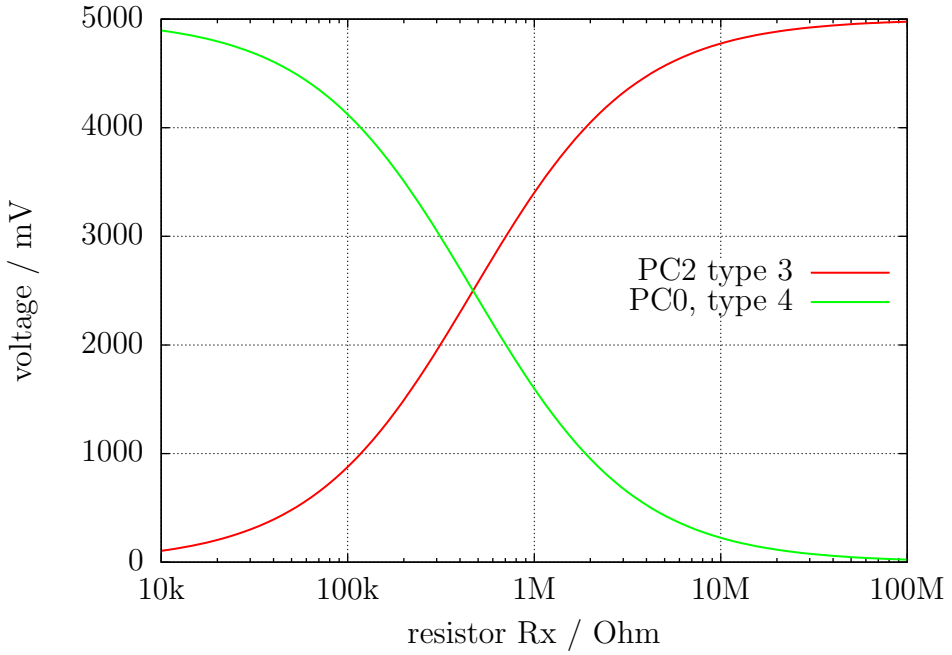


Figure 5.17. Voltages of type 3 and type 4 measurements with $470k\Omega$

5.2.3 Results of the resistor measurements

Figure 5.18 shows the relative errors of the resistor measurements with three ATmega8 microcontrollers. Additionally some results with the original software of Markus F. with one ATmega8 are shown as "Mega8orig" in this figure. More measurements results with ATmega8A and ATmega8L are shown in figure 5.19a and 5.19b. Figure 5.20 shows the same measurements with a ATmega168 microcontroller. Mega168 are the results without the AUTOSCALE_ADC option, Mega168as are the same measurements with the AUTOSCALE_ADC option. With the ATmega168 microcontroller it seems to be possible, that measurements of resistors in the range from 20Ω to $20M\Omega$ can be measured with a tolerance of $\pm 1\%$. For Measurements below 100Ω you should keep in mind, that any measurement probe with wire have a resistance too. It is better to connect the resistor directly to the terminal pins. If this is not possible, subtract the resistance value of the shortened probe. For example, if your Resistor have a printed value of 30Ω, your tester shows a value of 30.6Ω and the two probes shortened have a value of 0.5Ω, then your resistor has been measured with 30.1Ω. Below a resistance value of 10Ω one resolution step results to a error of more than 1%!

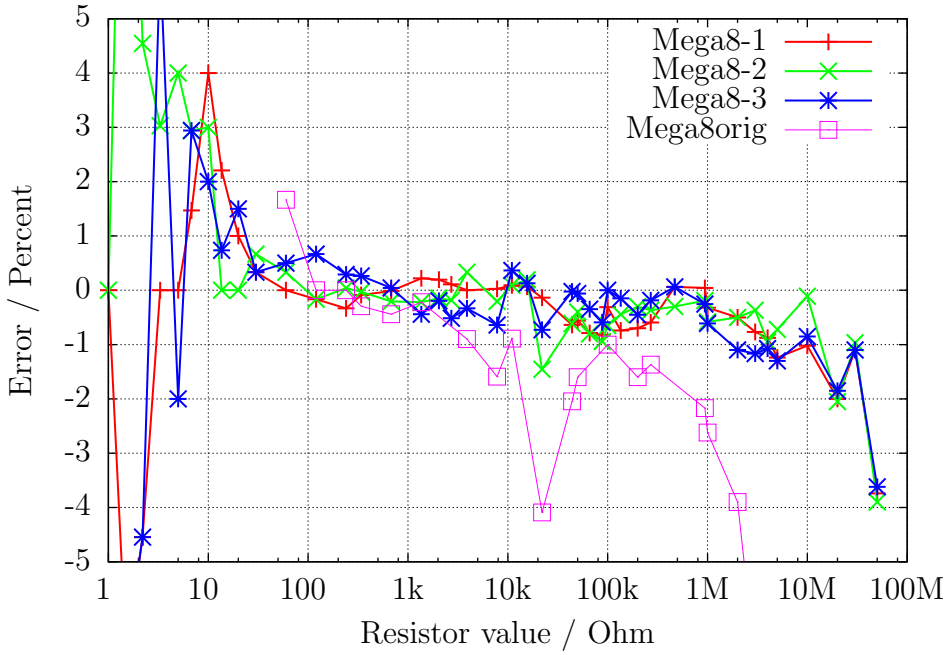
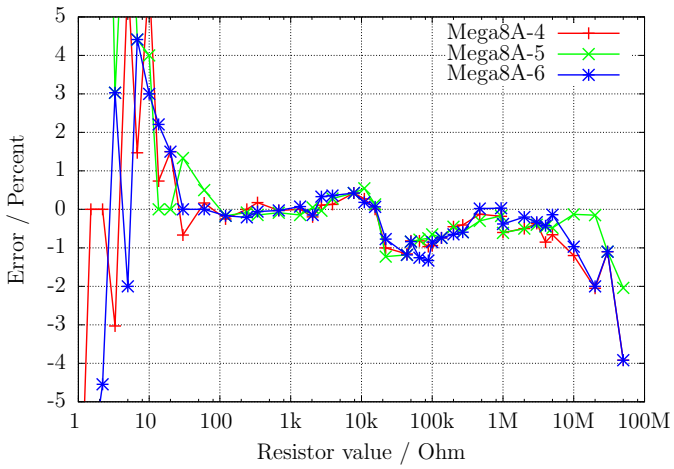
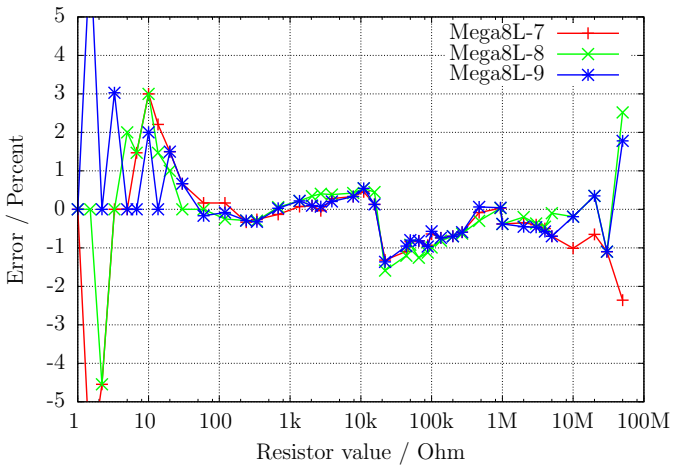


Figure 5.18. Relative error for resistor measurements with ATmega8



(a) with three ATmega8A



(b) with three ATmega8L

Figure 5.19. Relative error for resistor measurements

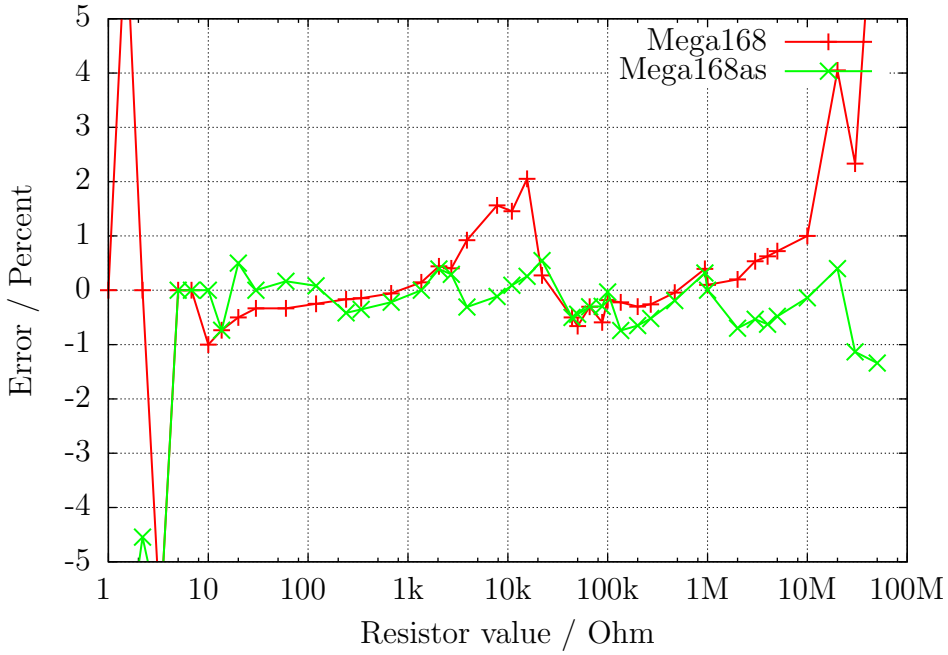
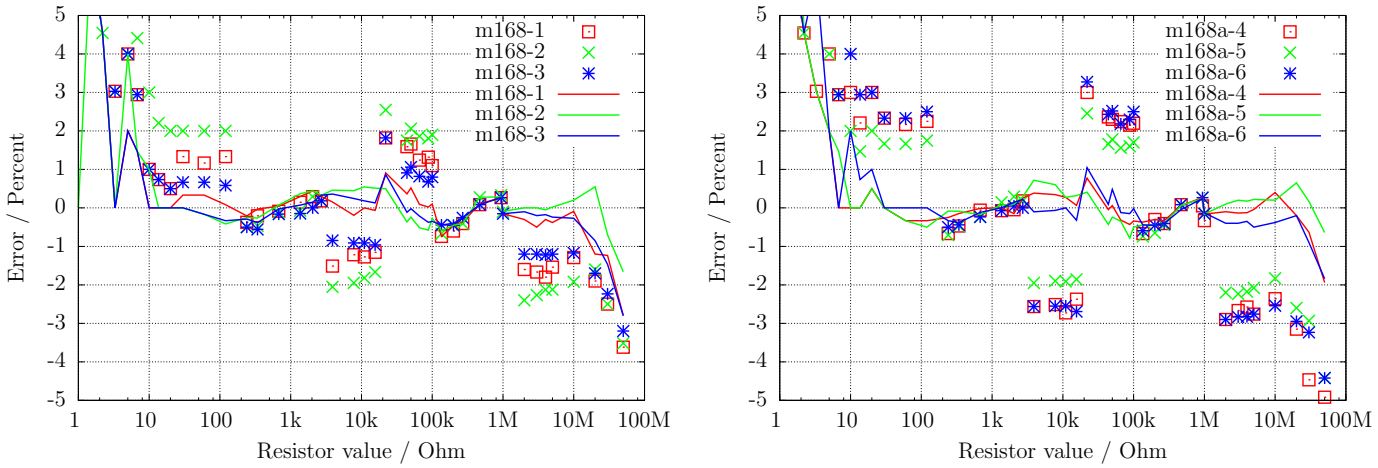


Figure 5.20. Relative error for resistor measurements with ATmega168

The figure 5.21a shows the measurement errors of three ATmega168 processors before calibration as points, after the calibration as line. The equivalent measurement errors of three ATmega168A prozessors are shown in figure 5.21b and the measurement errors of three ATmega168P prozessors are shown in figure 5.22 . The measurement errors of three ATmega328 prozessors are shown in figure 5.23a and 5.23b. After the automatic calibration the relative measurement errors of resistors between 10 Ω − 20$M\Omega$ usually are in the limit ± 1 %. Only one measurement of a 22$k\Omega$ resistor with the ATmega328P-13 shows a higher error. Before the calibration errors of some processors are found with ± 3%. This will be caused by the AUTOSCALE_ADC switching of the ADC reference. The direct compare of a capacitor voltage below 1 V, once measured with the VCC reference and another once measured with the internal reference, can adjust this error. With this measurement condition the voltage is measured with the same multiplexor channel and the internal bandgap reference is connected to the AREF pin of the ATmega. Unfortunately the direct measurement of the bandgap reference with the special multiplexor channel results to this offset, which can be manually adjusted with the REF_R_KORR option or automatically with the AUTO_CAL option of the selftest. With the AUTO_CAL option the REF_R_KORR value is a additional offset to the automatic find out value!



(a) with three ATmega168 (b) with three ATmega168A

Figure 5.21. Relativ error for resistor measurements

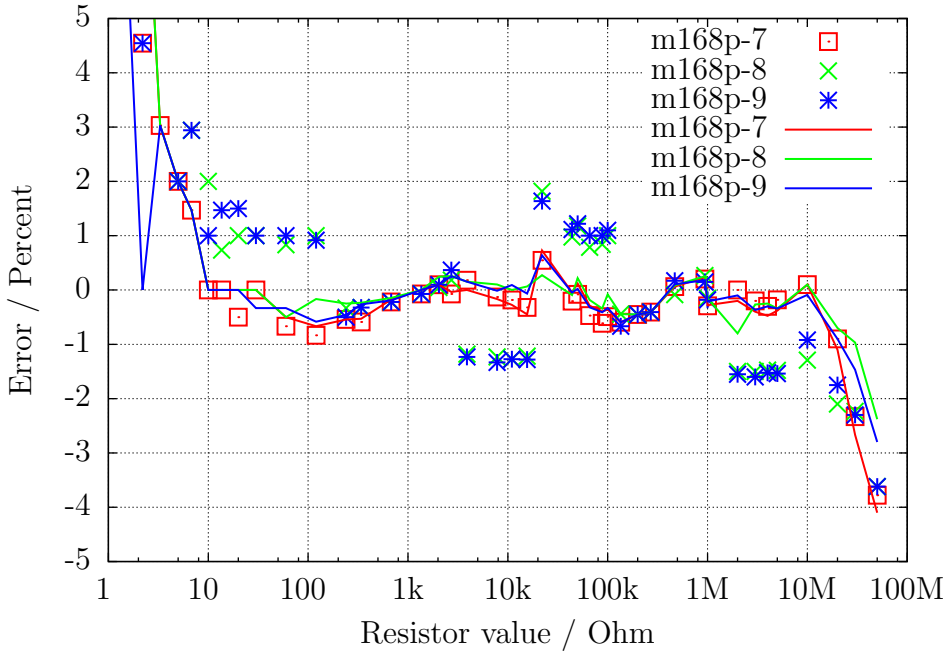
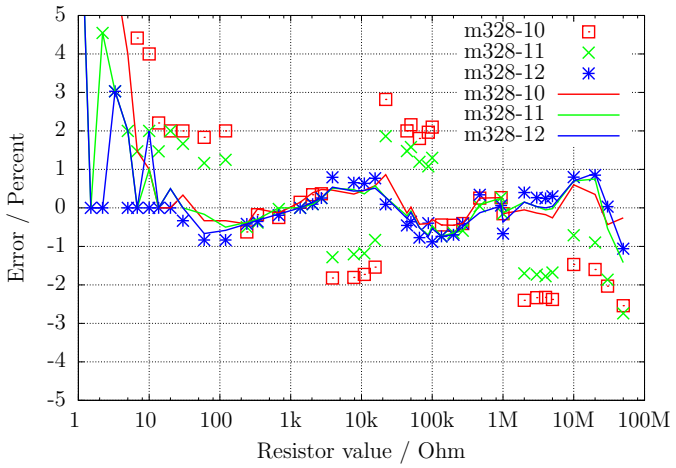
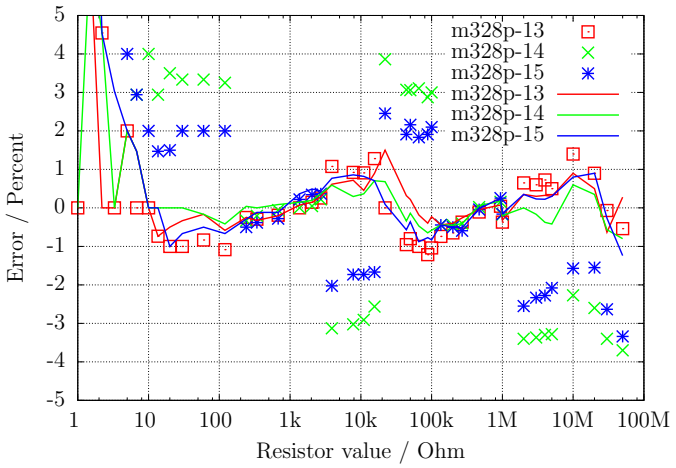


Figure 5.22. Relativ error for resistor measurements with three ATmega168P



(a) with three ATmega328



(b) with three ATmega328P

Figure 5.23. Relativ error for resistor measurements

5.3 Measurement of Capacitors

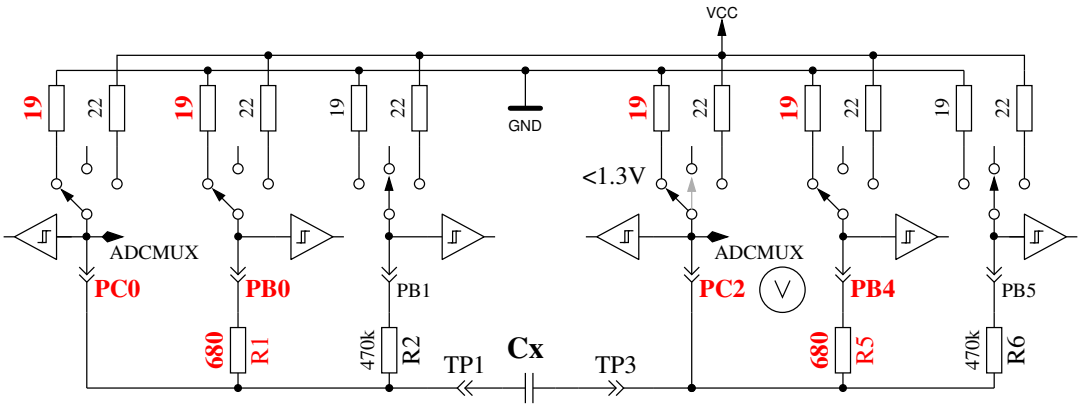
The measurement of capacitor values are done as separate task by measurement of load time after all other measurements. The original software of Markus F. did this with a program loop, which reads the corresponding digital input pin until a switch occured and count the loop cycles. This has the handicap, that the resolution of time measurement is limited by the time consumption of one loop cycle. This usually was done in all six combinations for all three probe pins. The actual software uses two different ways to get the load time in only three combinations for the three probe pins. The positive side is now always the higher probe number. Only if capacity is measured parallel with a diode, the polarity can be in the other order.

5.3.1 Discharging of Capacitors

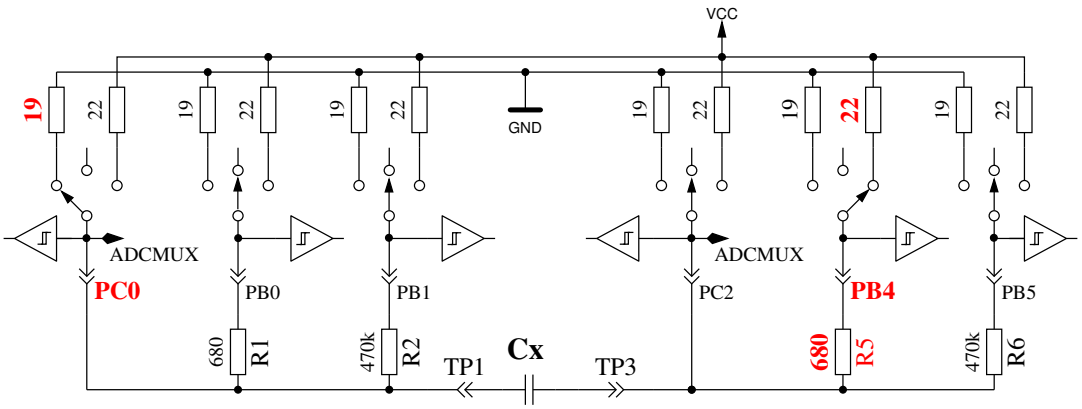
You should always discharge the capacitor before connecting it to the tester. The tester additionally discharge the capacitor before any measurement. If the voltage is below 1300mV, the capacitor is shortened by the output pins of the connected ADC port (Port C). I believe that this is legal because every output port has a built in resistance of about 20Ω. The data sheet Figure 149 (page 258) [2] shows voltage drop of output pins up to 2V. Of course I can not guaranty, that no damage can occur. I have tested the function with big capacitors of more than $15mF$ many times and I have never noticed any problem. The current should be below the specified limit of 40mA and is reduced fast by discharging. Off course damage can occur if you do not discharge a (high voltage) capacitor before connecting it to your tester.

5.3.2 Measurement of big Capacitors

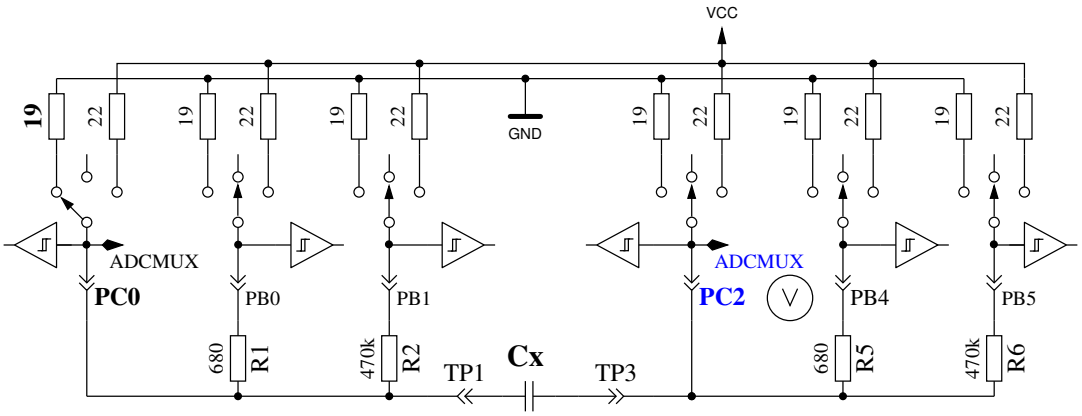
One side of the capacitor is connected to GND. The other side of the capacitor is connected with the 680Ω resistor to VCC for a period of 10ms. Afterwards this probe pin is switched to Input (High Impedance). After this 10 ms current pulse the voltage of the capacitor is measured without any current. If the voltage has not reached a minimal value of 300mV, the load pulse is repeated up to 499 times. If after 127 pulses a minimum voltage of 75mV is not reached (about 2s), further load is stopped, because never the 300mV can be reached with the remaining load pulses. Figure 5.24 shows the three phases of measuring the capacity value of a capacitor. The value of the capacity is then computed with the count of load pulses and the reached load voltage from a table. The table contains the factors to get the capacity in nF units from load time and the reached voltage with a spacing of 25mV. Interim value of voltage will be interpolated.



Quick Discharge of capacitor



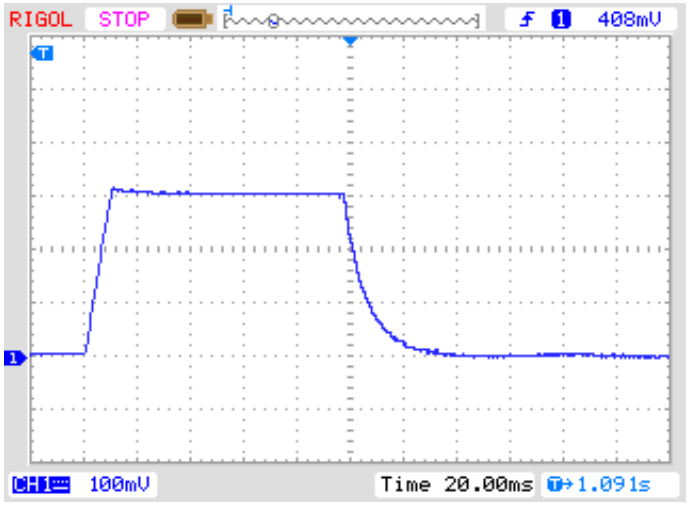
10ms Charge Phase of capacitor



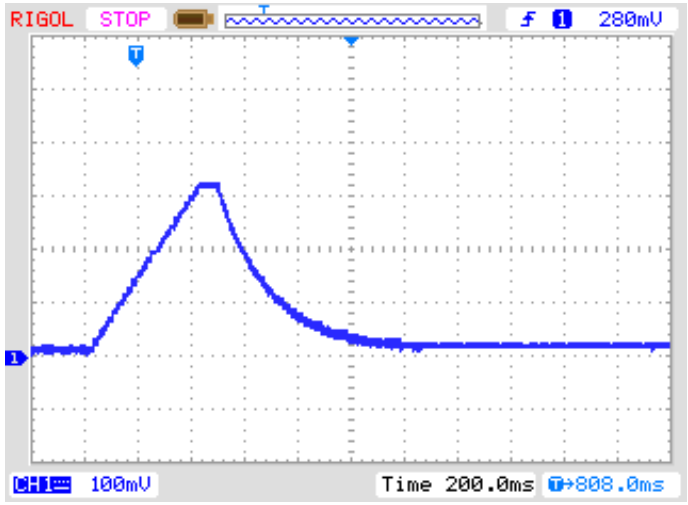
Voltage Measurement Phase of capacitor

Figure 5.24. discharge a capacitor and load with 10ms load pulses until voltage reach a value of 300mV

As a result of the low load voltage, the measurement is much faster than the initial software version, because this advantage works also on discharging. So bigger capacitors can be measured. Furthermore a diode, which is parallel connected to the capacitor dont disturb the measurement in most cases, because the flux voltage of most diodes is not reached. Figure 5.25a shows the charge and discharge for a $229\mu F$ capacitor. The flat top of diagram from load end to discharge begin is caused by the measuring and computing time of the ATmega. Figure 5.25b shows the same measurement for a $5mF$ capacitor, notice how the time for measurement is grown to about 1.5 seconds inclusive the discharge. The last example shows the capacity measuring of a $15mF$ capacitor in Figure 5.26



(a) 229μF Capacitor



(b) 5mF Capacitor

Figure 5.25. Charge and discharge of big Capacitors for measuring

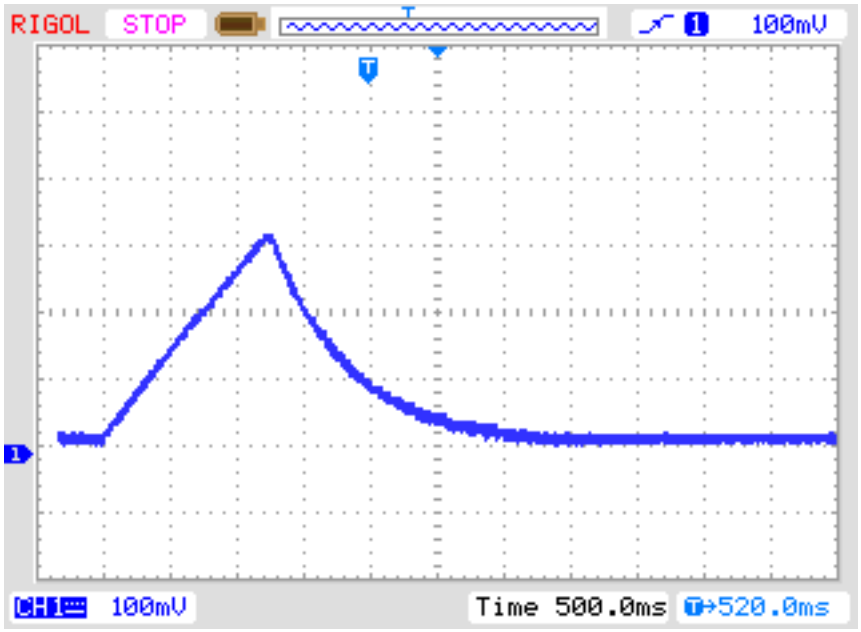


Figure 5.26. Charge and discharge of a 15mF Capacitor for measuring

After this capacity measurement the self-discharge of the capacitor will be checked by waiting a proportional period the loading has taken and reading the load voltage again. The measured capacity value is corrected due to this voltage drop. A test with a parallel connection of a 68μF capacitor and a 2.2$k\Omega$ resistor shows the effectivity of this method. The measured capacity value without the resistor is 66.5μF, with the parallel 2.2$k\Omega$ resistor results to a capacity value of 66.3μF. For comparison here are the results measured with a Peaktech 3315 multimeter: Without the resistor a capacity value of 68.2μF is measured, with the parallel 2.2$k\Omega$ resistor a value of 192μF is measured with the multimeter.

5.3.3 Measurement of small Capacitors

If the first 10 ms load pulse has overloaded the capacitor, another technique of measurement is used. The ATmega processor has a build in 16-Bit counter, which can operate at the full clock rate (1MHz

or 8MHz). This counter has also the feature to save his counter value by a external event. This event can be built by the output of the comparator. The comparator can operate with any ADC input pin and the band gap reference. Figure 5.27 shows a simplified diagram of the measurement situation. So I discharge the capacitor, prepare the comparator to the proper pin input, start the counter at 0 and start immediately the charging of the capacitor with one side connected to GND and the other side connected with the $470k\Omega$ resistor to VCC. Now I check within a program loop, if the counter flags signals a overflow event or a input capture (external) event. I count the overflow events until I detect the input capture event. In this case I stop the counter and check if I must count a additional overflow, because the counter can't be stopped by the input capture event.

The input capture counter and the overflow counter built together the total time, from which we can get the capacity with a factor. The actual software can use a table with the theoretical dependency of the load time in respect to the comparator voltage. The table is spaced in 50mV steps and will be interpolated according to the actual reference voltage. This table will only be acticated with the Makefile option WITH_AUTO_REF. From the build capacity value I subtract a predefined experimental find out constant or a value found by the last selftest with AUTO_CAL option to eliminate the zero offset. The zero offset may vary with printed board type, the used test equipment or processor. The selftest with AUTO_CAL option will find out your zero offset automatically.

I noticed that the reference voltage is permanently somewhat to low, so that you can choose an offset with the Makefile option REF_C_KORR. After calibration with the AUTO_CAL option , the REF_C_KORR will only be a offset to the measured difference voltage between loaded capacitor and internal reference. The measured reference voltage will then be corrected (added) by your value (mV units). If option WITH_AUTO_REF is not used, the reference voltages of ATmega8, ATmega168 and ATmega328 are applied as noted in the data sheets [2] [3]. A sample measurement of this type is shown in figure 5.28. The measurement time for the $22\mu F$ capacitor is above 2.6s because the $470k\Omega$ is used for charging. But discharging is in this case much faster than charging.

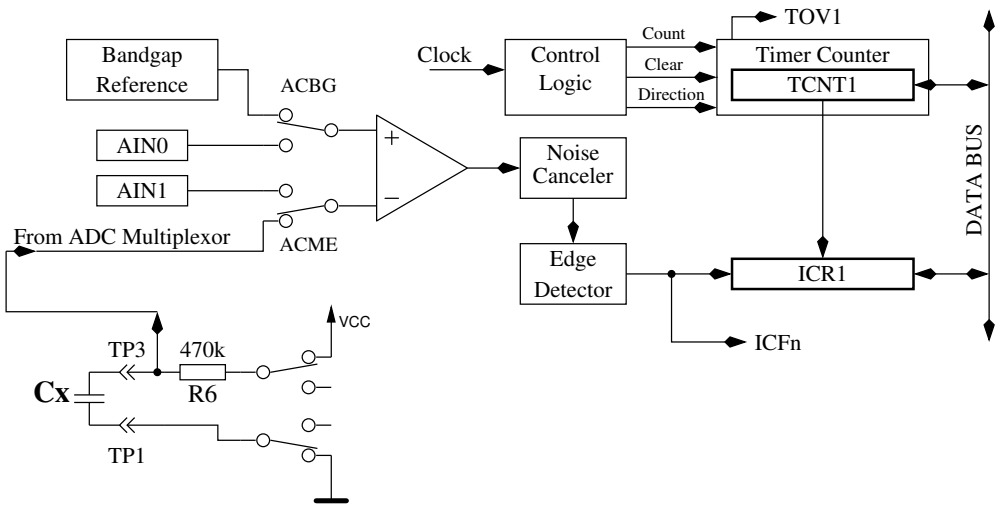


Figure 5.27. measurement little capacity values with comparator

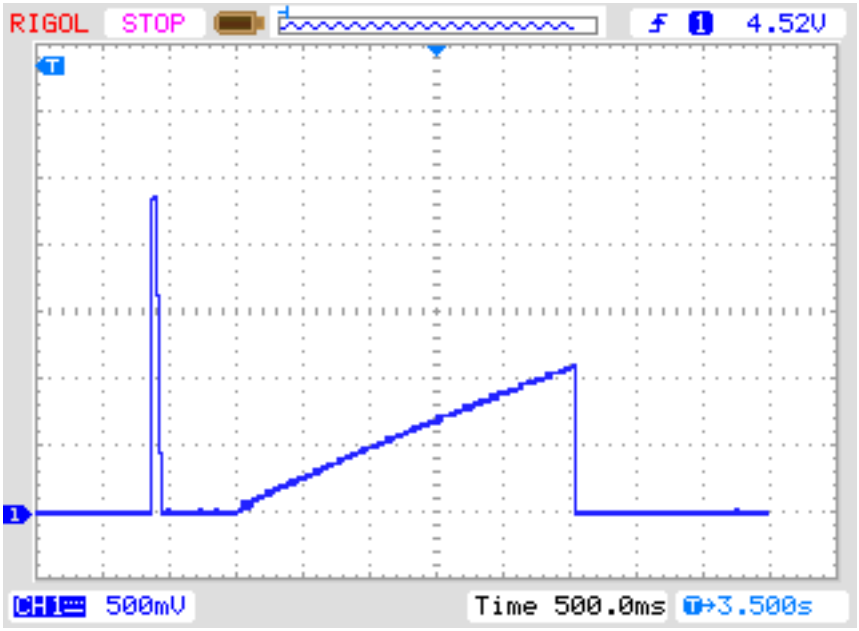


Figure 5.28. Charge and discharge of a $22\mu F$ Capacitor for measuring

In principle this technique of measurement can also be done with the 680Ω resistor, but because the ADC can't be used if the comparator is working, I have no chance to monitor the load voltage until the comparator is stopped. If a undetected diode is parallel connected with the capacitor, the load current of the capacitor can be absorbed by the diode (threshold voltage) and the band-gap voltage will never be reached. The method taken in actual software for big capacitors in section 5.3.2 avoids this conceptual bug.

5.3.4 Measurement of the Equivalent Series Resistance ESR, first way

The series resistance ESR [8] is a good indicator for the aging of electrolytical capacitors for example. The figure 5.29 shows a equivalent circuit of a capacitor. The resistor Rp represents the leakage resistance of the capacitor, ESL the equivalent series inductivity and the resistance ESR represents the equivalent series resistance. If the measured capacitor has a capacity of more than $0.45\mu F$, the tester will try to measure the series resistance too. For a capacity of more than $3.6\mu F$ the normal clock rate of $125kHz$ for the Analog-Digital converter is used. For lower capacities the higher clock rate of $500kHz$ is used to accelerate the measurement. The accuracy of the ADC results will be more worth by the higher clock rate, but this could be accepted by the higher ESR values of capacitors with lower capacity. Otherwise the measurement of ESR with this method is not possible for a capacity of less than $1.8\mu F$ at the normal clock rate of $125kHz$.

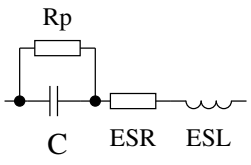


Figure 5.29. Equivalent circuit of a capacitor

Strictly speaking the ESR of a capacitor depends on the operating frequency and temperature. Usually the value measured with sine wave-form signal of $100kHz$ is denoted in the data sheets. This measurement can not be done with the ATmega without external equipment. With the subsequent written method the measurement frequency with the standard ADC clock rate will be below 640 Hz with nearly rectangular signal. With $500kHz$ ADC clock rate the measurement frequency will be

2400 Hz. To get the value of the equivalent series resistance, the voltage of both connections will be measured during loading in one direction with the ADC internal reference voltage (1.1 V). After the measurement the load current will be switched off and the voltage of the capacitor is measured again without the current. If this voltage is below 3 mV, the sequence of measurement is repeated. The figure 5.30 shows the corresponding circuits.

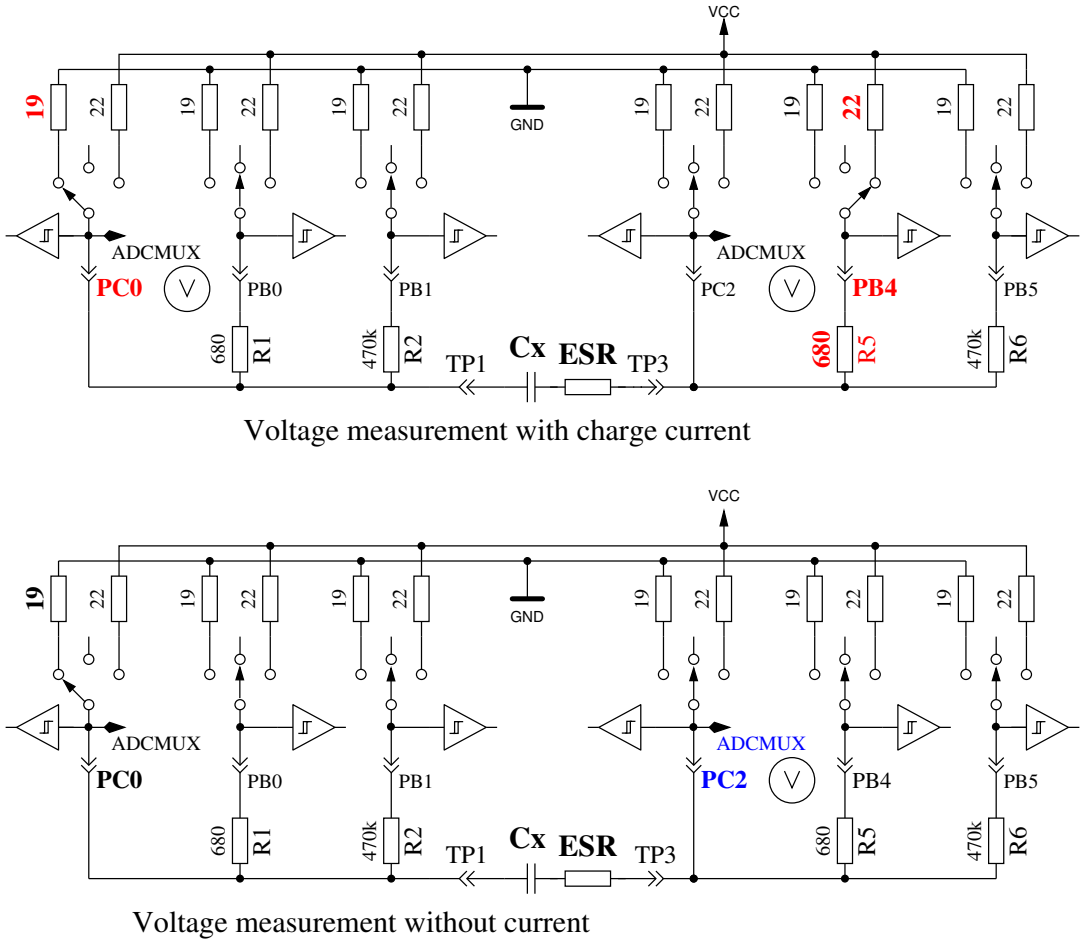
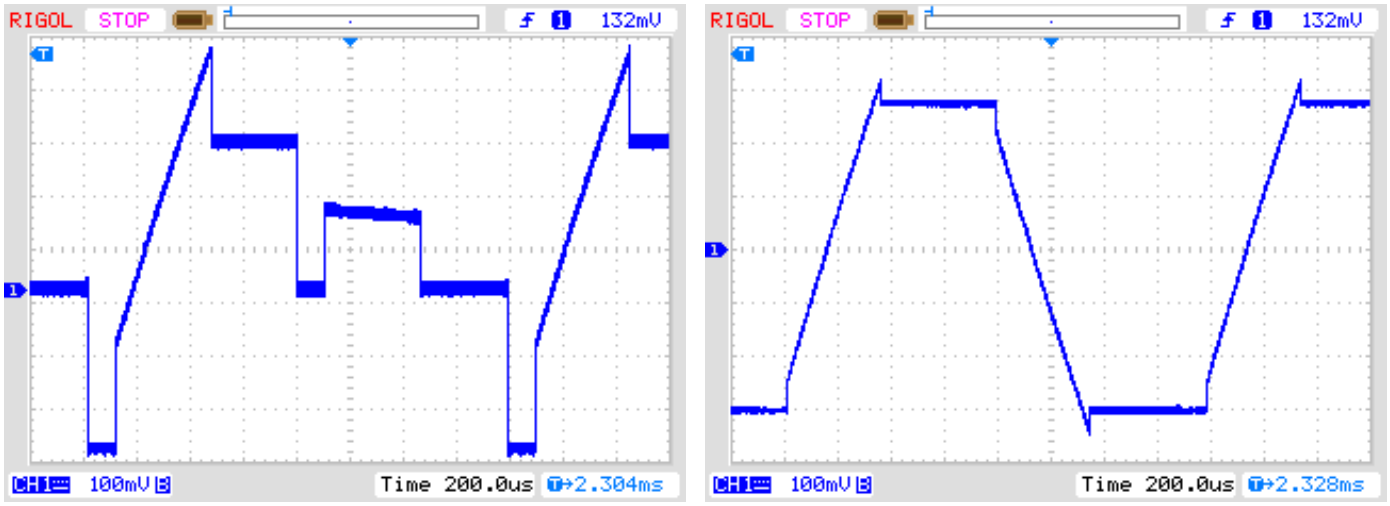


Figure 5.30. Circuit of the ESR measurements of a capacitor

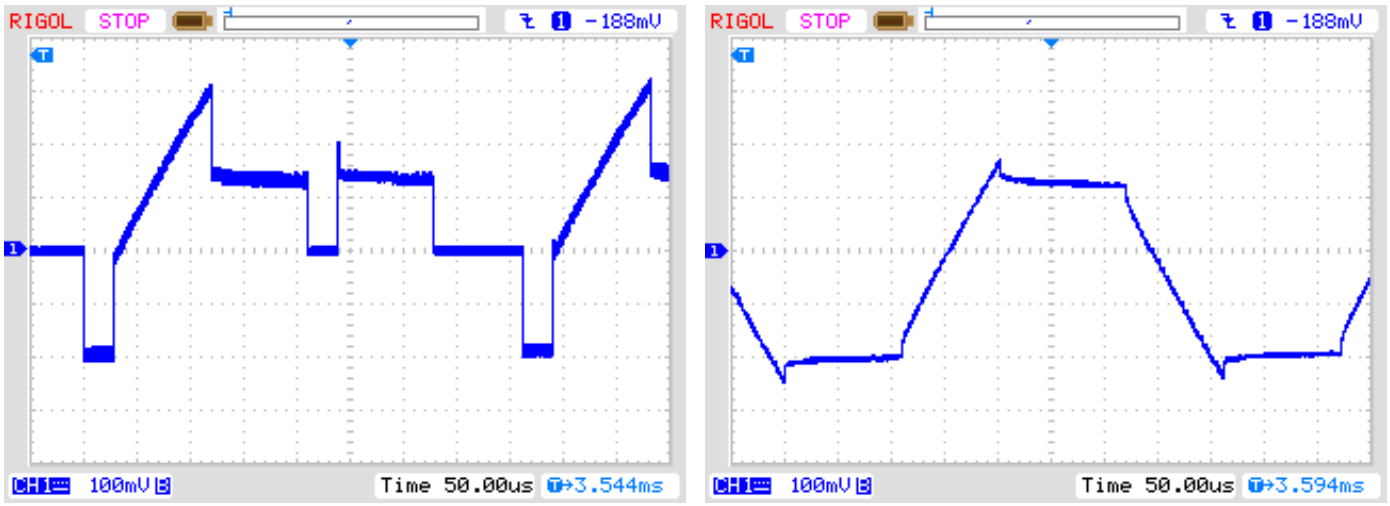
The difference of capacitor voltages with and without current is proportional to the internal resistance of the capacitor. The expected voltage of this difference is so low, that one measurement can not result to a feasible result. Therefore after this the current will be switched to the opposite direction and the same measurement will be repeated. The whole measurement sequence will be done 128 times and the results of the voltage measurements will be added. So we have three sums of voltages, the voltage Ulp at the low side of the capacitor with current, the voltage Uhp at the high side of the capacitor with current and the voltage Uc of the high side of the capacitor without current. The sum of voltages at the low side of the capacitor represents the potential drop with the mean load current at the port output resistance $Rport$. The voltage difference of the high side and the low side of the capacitor represents the voltage of the capacitor with load current $Udiff = Uhp - Ulp$. The difference $Uesr = Udiff - Uc$ should represent the voltage drop at the internal resistance of the capacitor with mean load current. We will get the resistance value with the relation of this voltage $Uesr$ to the voltage Ulp, scaled with the known resistance value of the port output $Rport$. The scale factor is selected to get a resistance resolution of 0.01Ω: $Resr = \frac{Uesr \cdot 10 \cdot Rport}{Ulp}$ The figure 5.31 shows a part of the voltage curve of a $4.2\mu F$ capacitor during the ESR measurement. To explain the influence of the ESR, a series 6.8Ω resistor is added to the capacitor. The little voltage break after loading the capacitor is interpreted by software to get the ESR. The greater voltage drop of

the measurement to GND potential is caused by the port output resistance of about 20Ω. For this measurement a total ESR of 7.5Ω is reported by the tester, without the series 6.8Ω resistor a ESR of 0.56Ω is found. The figure 5.32 shows the same measurement with higher measurement frequency of a 2.2μF electrolytical capacitor with a ESR of 6.5Ω.



(a) measured one pin to GND (b) measured pin to pin

Figure 5.31. Voltage curve of a 4.2μF capacitor during the ESR measurement



(a) measured one pin to GND (b) measured pin to pin

Figure 5.32. Voltage curve of a 2.2μF capacitor during the ESR measurement

The accuracy of the ESR measurement is not very high by different reasons:

1. The voltage measurement at both pins of the capacitor can not be done at the same time, the only way is to do it in sequence. In the interim time between both measurements the load current has changed due to the charge of capacitor. The program tries to compensate this fact with a capacity dependent correction of the low side voltage.

2. The ADC takes the measurement voltage after 1.5 clock ticks after the start of conversion. The conversion beginns with the rising edge of the ADC-clock, if the start bit is set. If the charge current will be switched off to early, the ADC takes the wrong voltage for the measurement with current. If the charge current will be switched off to late, the capacitor will take more

electric charge, than that of the corresponding measurement with load current. This will cause a too high voltage of the measurement without current. But it is difficult to switch off the current at the right time by software.

3. The port output resistance is used as a reference value by this measurement method, but this resistance value is not exacly known too.

4. The resolution of the ADC is not sufficient to get a resolution of resistance of 0.01Ω. To get the best avaiable resolution of ADC, the internal reference (1.1 V) is used for all measurements. The resolution deficit will be attenuated by accumulating a big number of single measurements too.

5. The switching of ports can not be exactly synchronized to the ADC clock with polling of conversion done.

Anyway the results seems to be practical, as shown with the following figure 5.33. The ESR values of the same part measured with the Transistortester vary more than the values measured with the LCR meter. The ESR values from the LCR meter are measured with a frequency of 1 kHz or are interpolated for little capacities to 2.4 kHz. You must respect the quality of all connection parts. The used cable connections can cause a higher measured resistance value. The plug connectors can also result a higher resistance value. The LCR meter has the advantage of the used Kelvin terminals. Only one capacitor with a capacity below $1\mu F$ was a $500nF$ ceramic type, all others were plastic film capacitors. The only electrolytical capacitor of the test series below $9\mu F$ was a $2.2\mu F$ capacitor.

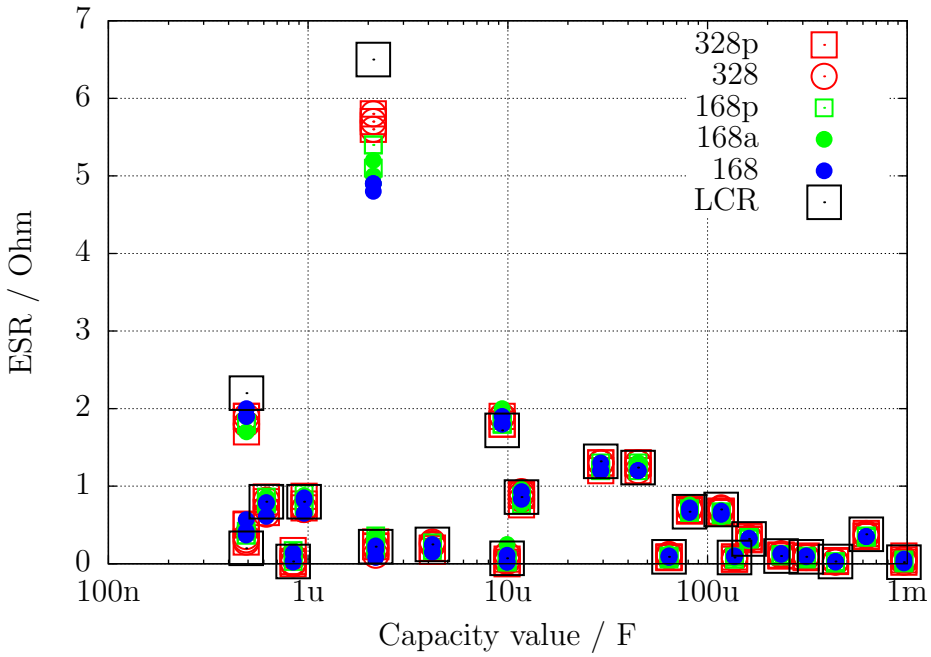


Figure 5.33. ESR measurement results of 15 different ATmega

5.3.5 Measurement of the Equivalent Series Resistance ESR, second way

From beginning with software version 1.07k the ESR measurement way is changed to a new measurement method. The different measurement steps are shown in figure 5.35. The difference to the previous way is that the period of current flow through the capacitor is essential shorter. The capacitor is preloaded with a half pulse to the negative direction and is than loaded in a cyclic way in both direction. The timing of the load pulse is so selected, that the middle of the load puls at

sample 4 and 8 is pointed to the sample and hold time of the ADC (2.5 clock tics after start of ADC). A complete measurement cycle is shown in figure 5.34. The sums of 255 measurement cycle results is used for getting a result with adequate resolution. A continuing charge of the capacitor in any direction is avoided by the same charge and discharge pulse length and the same circuit. By measuring the reference voltage the capacitoe remains currentless. By that this measurement are not time critital. It is only assumed, that the capacitor hold the voltage until the next charge or discharge pulse begins.

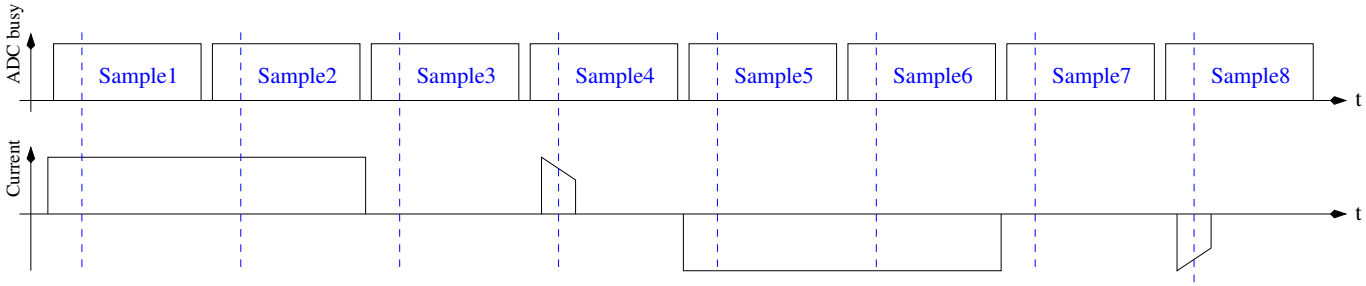
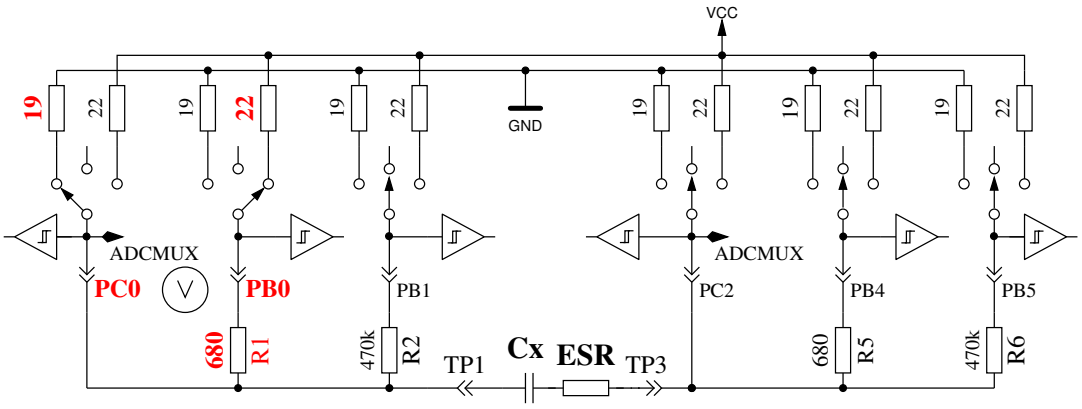
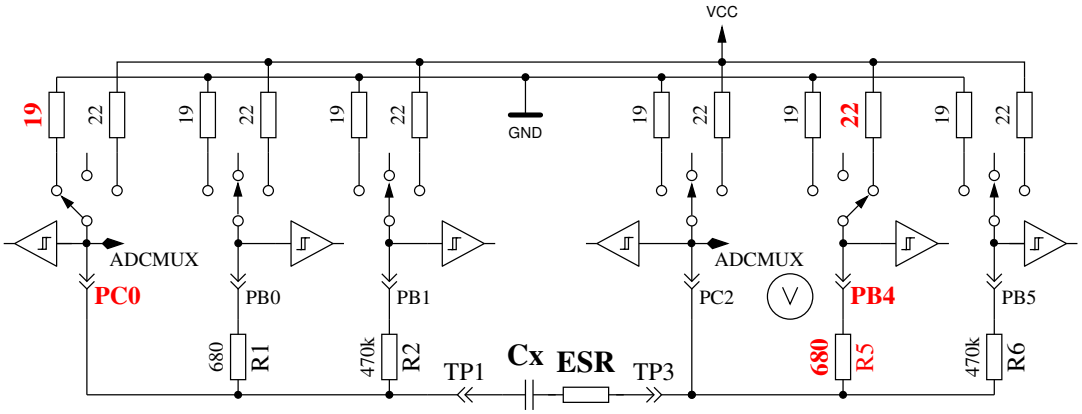


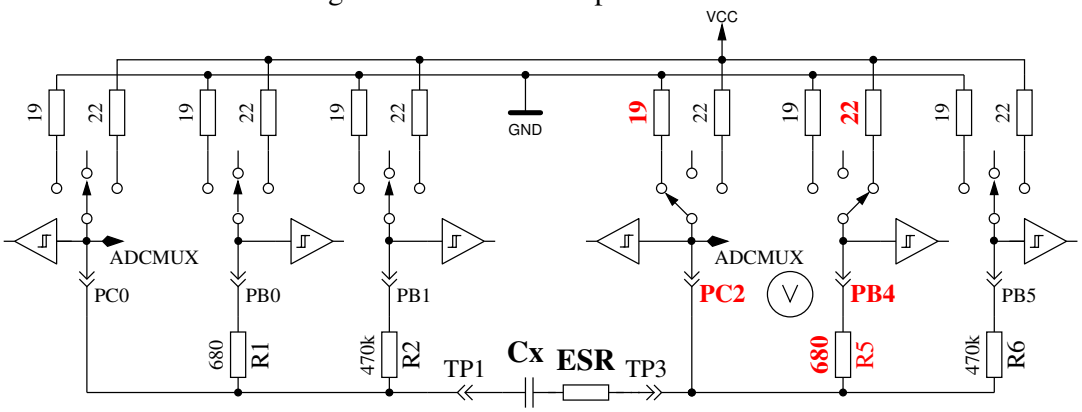
Figure 5.34. Timing of a measurement cycle for the new ESR-measurement way



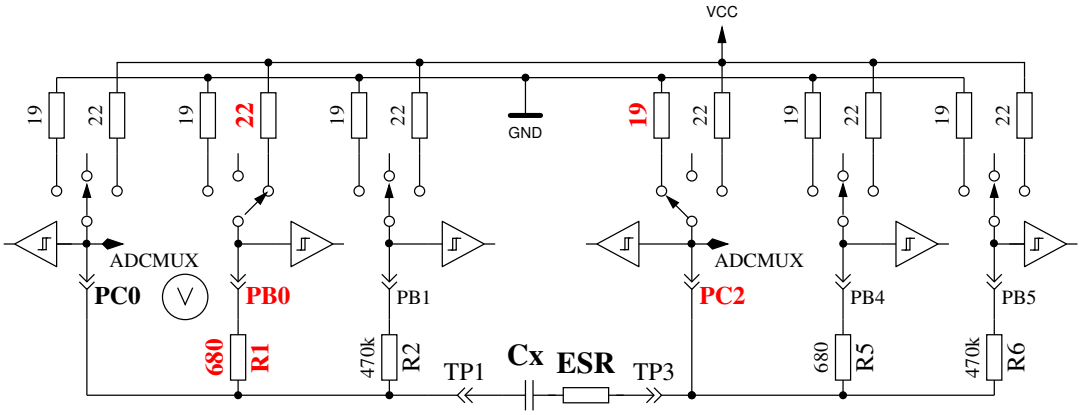
Forward reference measurement



Forward voltage measurement with probe current



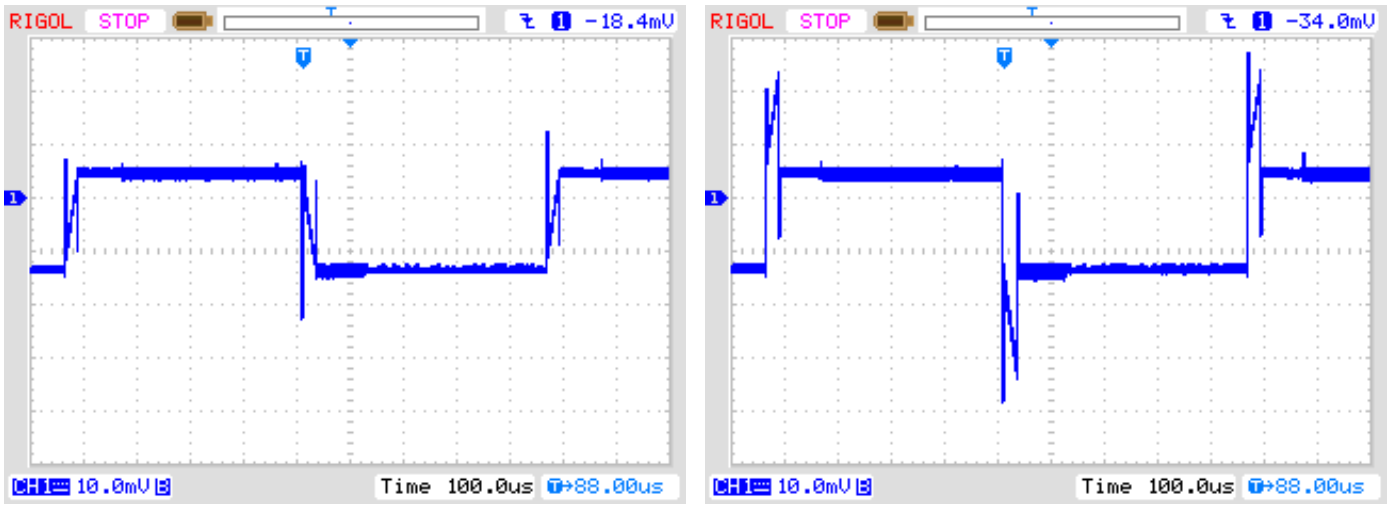
Reverse reference measurement



Reverse voltage measurement with probe current

Figure 5.35. More simple ESR measurement of a capacitor

Due to the shorter load puls not only the ESR of capacitors with lower capacity can be measured, but this way of measurement can also be used for the measurement of resistors with little resistance, if they don't have a detectable inductance. By doing that, a resolution of 0.01Ω for this resistors can be achieved. Also the zero resistance can be detected by the calibration part of the selftest for all three test pin combination. You should keep in mind, that stable plug sockets or clamping connectors are essential for stable results. The measurement periode is about $900\mu s$, which results to a frequency of about $1.1kHz$. Because the load pulse is very short, the measurement result is comparable to measurements with $10kHz$. A measurement example with a $10\mu F$ foil capacitor, once measured alone and once measures with a 2.7Ω series resistor is shown in figure 5.36. You can see the effect of the additional resistance by comparing both diagrams. You can see also, why the ADC measurement (SH) should point to the middle of the load pulse. With big capacity values the load current is nearly stable during the total pulse length, so you will get the middle voltage at the middle time of the load pulse. With lower capacity values you will get a significant difference, which can be compensated by the known capacity value.



(a) without series resistance (b) with 2.7Ω series resistance

Figure 5.36. Voltage curve of a $10\mu F$ capacitor during new ESR measurement

The measurement results of the new ESR measurement method is shown in figure 5.37. The ESR values are different from the results shown for the previous mesurement procedure in figure 5.33 because the ESR is frequency dependence of the ESR. The reference values are determined with a LCR meter at a measurement frequency of $10kHz$.

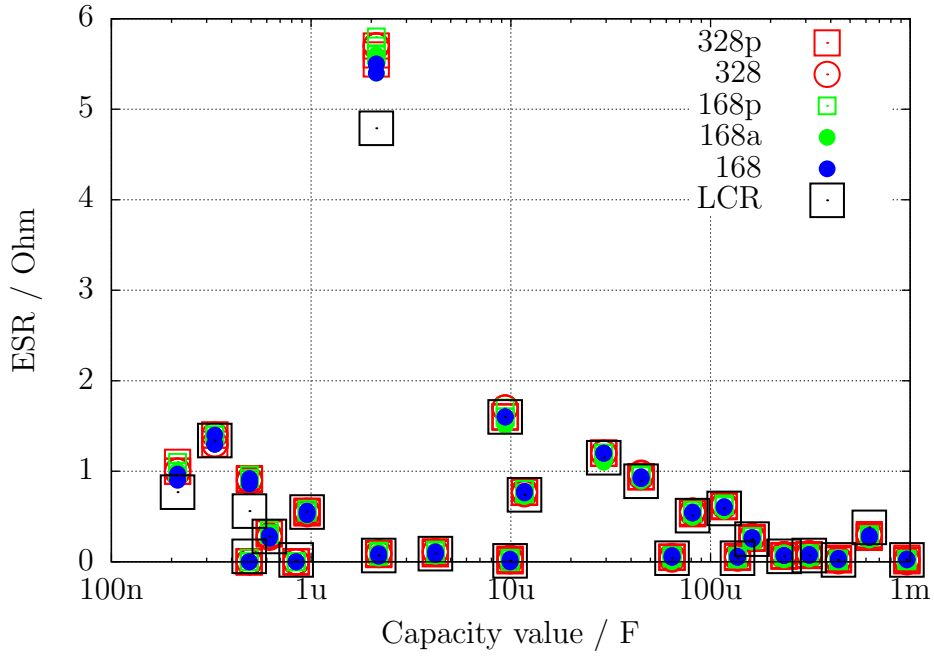


Figure 5.37. ESR results with 15 different ATmega, method 2

A measurement series with different sized electrolytic capacitors are shown in figure 5.38. The results of a PeakTech 3315 LCR meter of measurements with different frequencies and the results of the TransistorTester are shown together. The resistance is illustrated with logarithmic scale in this diagram. In all cases the results of the TransistorTester is near by the results of the $10kHz$ measurements of the LCR meter. Only the $500\mu F/3V$ capacitor is a older exemplar, all others capacitors are as good as new.

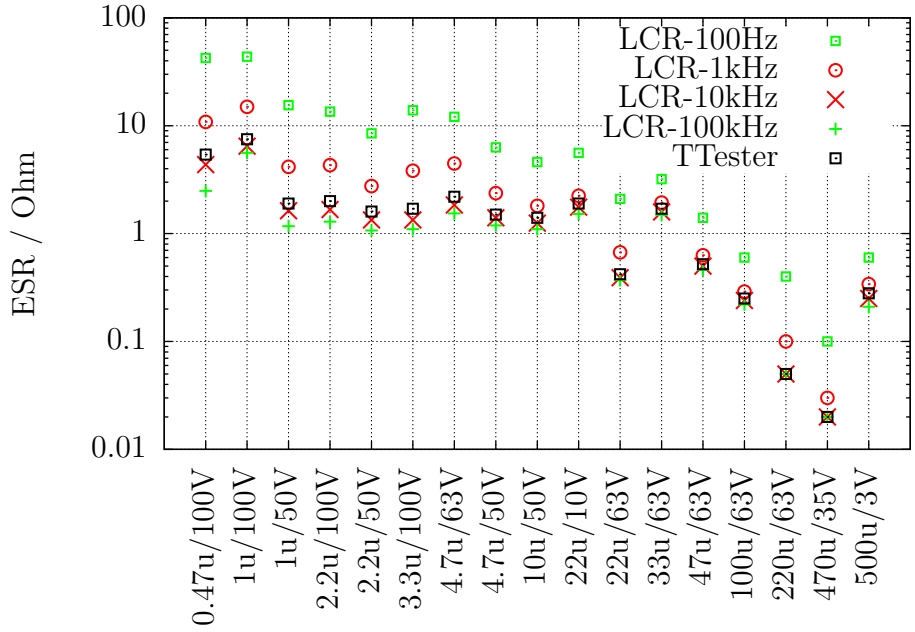


Figure 5.38. Results of the ESR measurements of different electrolytic capacitors

Because the new measurement method can be taken for measuring of resistors with low values, the measurement errors of some resistors below 10Ω with three example of each ATmega type will be shown in figure 5.39.

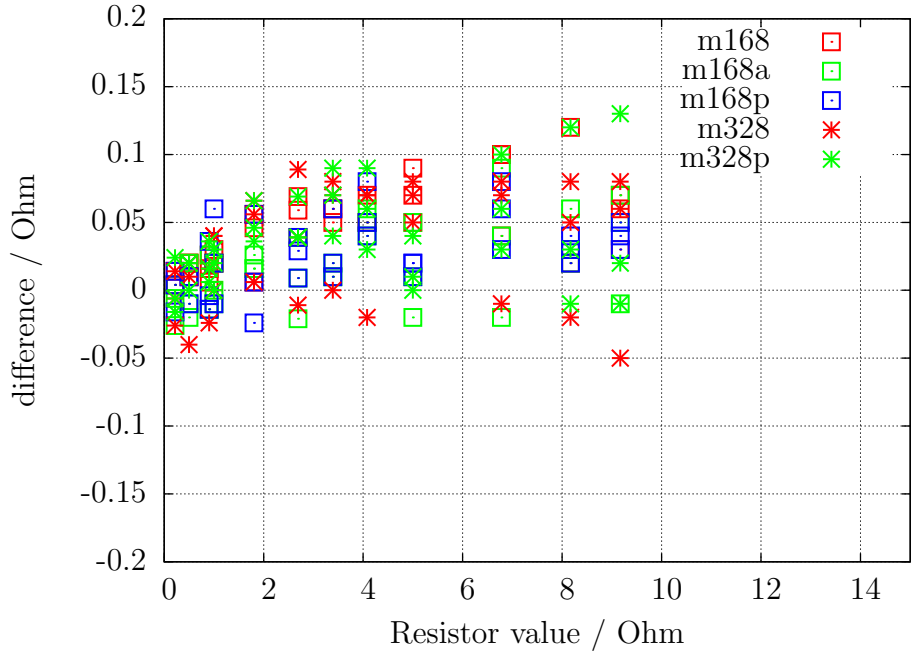


Figure 5.39. Measurement errors of resistors with the ESR method

5.3.6 Voltage loss after a load pulse, Vloss

With the measurement of capacitors with big capacity values the voltage loss after the loading is analysed. The reached load voltage is lost with electrolytic capacitors after a short periode. This voltage loss can be caused by a parallel connected resistor. But I assume, that this voltage loss of electrolytic capacitors is caused by a internal load dispersion directly after the load pulse. By loading the capacitors with the $470k\Omega$ resistor, as it is done for little capacity values, this dispersion is already done after switching off the current. No voltage loss is detectable for this case. But if you load the same capacitor with a short current pulse, you can also detect the voltage loss for capacitors with lower capacity. The same effect with lower loss can also be noticed for ceramic type capacitors. I have noticed, that capacitors with more than some % voltage loss are suspect. Especially noticable with respect to the voltage loss are older paper type capacitors, which are for other measurement a problem too. Some measurement examples will be shown in the following table.

capacitor type	Nenn-capacity	PeakTech LCR 2170	Voltcraft M2650-B	PeakTech 3315	Transistor-Tester
paper	4700pF	6.75-10.36nF Q=2.5-32	8.00nF	25.40nF	10.71nF Vloss=11%
paper	6800pF	9.40-11.40nF Q=5-25	10.41nF	23.30nF	11.65nF Vloss=5.0%
unknown	4700pF	5.85-6.33nF Q=16-87	6.12nF	6.90nF	6225pF Vloss=1.7%
foil	7870pF	7.86-7.87nF Q= ¿1540	7.95nF	7.95nF	7872pF Vloss=0%
paper	22000pF	37.4-57.5nF Q=2.5-32	52.8nF	112nF	118.5nF Vloss=12%
foil	22600pF	22.4-22.5nF Q= ¿1540	22.57nF	22.69nF	22.54nF Vloss=0%
paper	100nF	144-256nF Q=2.6-28	177nF	318nF	529.7nF Vloss=12%
ceramic	100nF	97.7-102nF Q=90-134	103.7nF	103.3nF	103.1nF Vloss=0.1%
foil	100nF	98.0-101nF Q=58-700	101.4nF	102.2nF	101.6nF Vloss=0%

In this table you will find, that the capacity of all foil type capacitors can be measured by all intruments with good precision. The capacity values and the quality factor Q of the PeakTech LCR meter are minimum and maximum values of the measurements in the frequency range $100Hz$ to $100kHz$. At all examples in the table the voltage loss Vloss of the TransistorTester is big, if the capacitors have a low quality factor. Only in this case the differences of the capacity measurement results are also big. The TransistorTester can only determine the voltage loss, if the measured capacity is more than $5000pF$.

5.3.7 Results of Capacitor measurement

The results of my capacity measurements are shown in figure 5.40 for three ATmega8 processors. Additionally some values of original software are shown with a correction factor of 0.88 (-12%). Other measurement results of different ATmega8 versions are shown in figure 5.41a and 5.41b. The results of the measurement of the same capacitors for a ATmega168 is shown in figure 5.42. The base for the error computing are the measurement results of a PeakTech 2170 RCL-meter, not the printed value of the parts. A part of the relative high measurement difference is caused by the too high measurement frequency of the RCL-meter for big electrolytical capacitors. On the other side the bad quality factor of the electrolytical capacitors may cause another percentage.

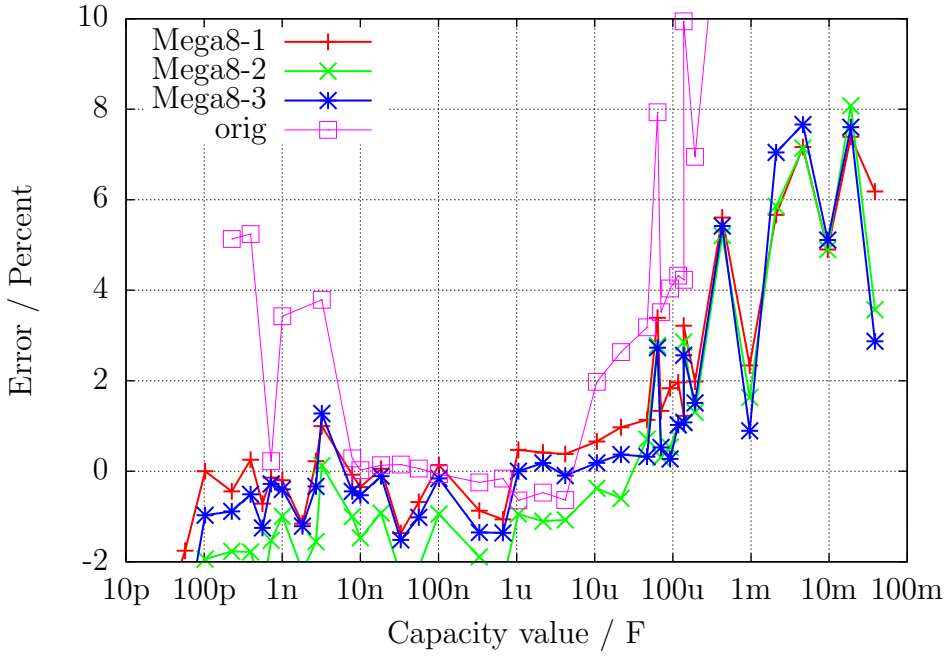
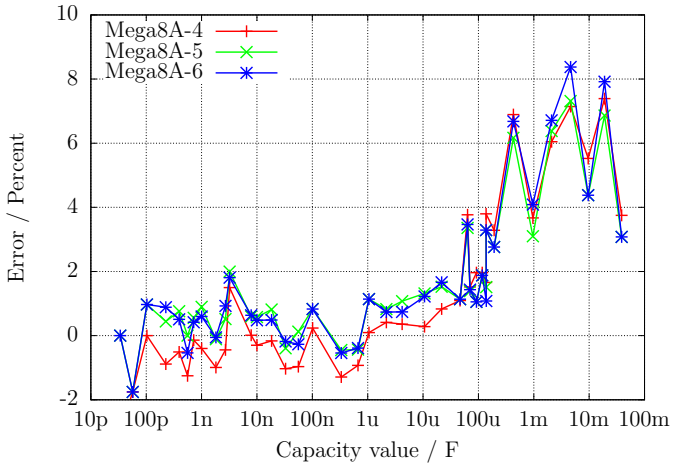
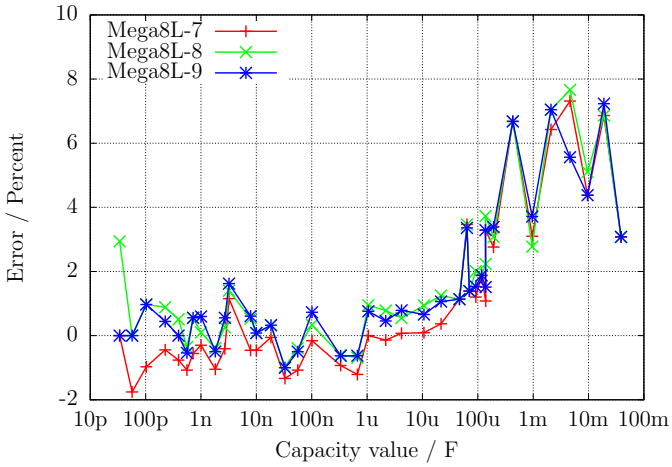


Figure 5.40. Error in % for capacitor measurements with ATmega8



(a) with three ATmega8A



(b) with three ATmega8L

Figure 5.41. Relative error of capacitor measurement

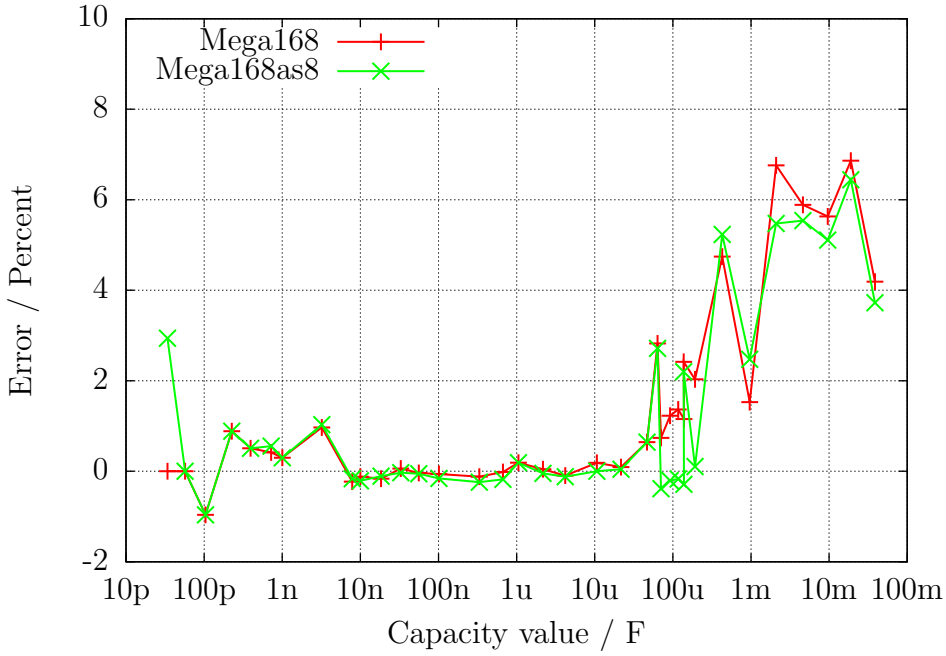


Figure 5.42. Error in % for capacitor measurements with ATmega168

Figure 5.43 illustrates, how difficult is it to choose the right base for the capacity measurement. All measurement results are compared with the best estimated value of the capacitors. The gradient ,,Multimeter" shows the differences of the Peaktech 3315 Multimeter results. The next gradient ,,LCR" shows the differences of the Peaktech 2170 LCR-Meter results, which is taken from best frequency approach. To compare this results to the results of a ATmega168 equipped Transistor-Tester the gradient ,,ATmega168as" is also shown. I beleave, that this errors are not real measurement errors of the particular equipment, because my best estimated value are also not the real capacity value of the capacitors.

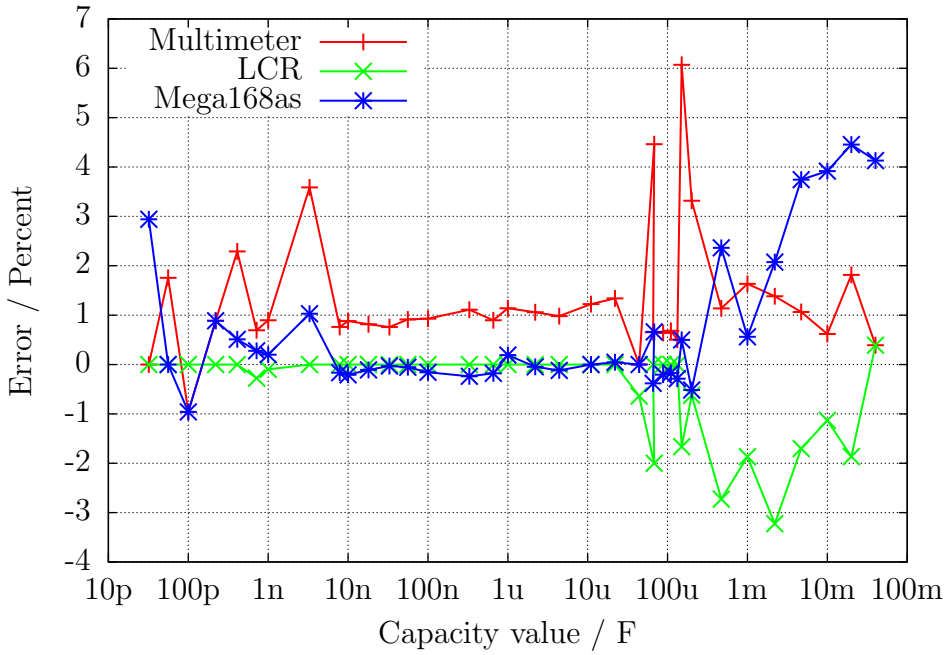
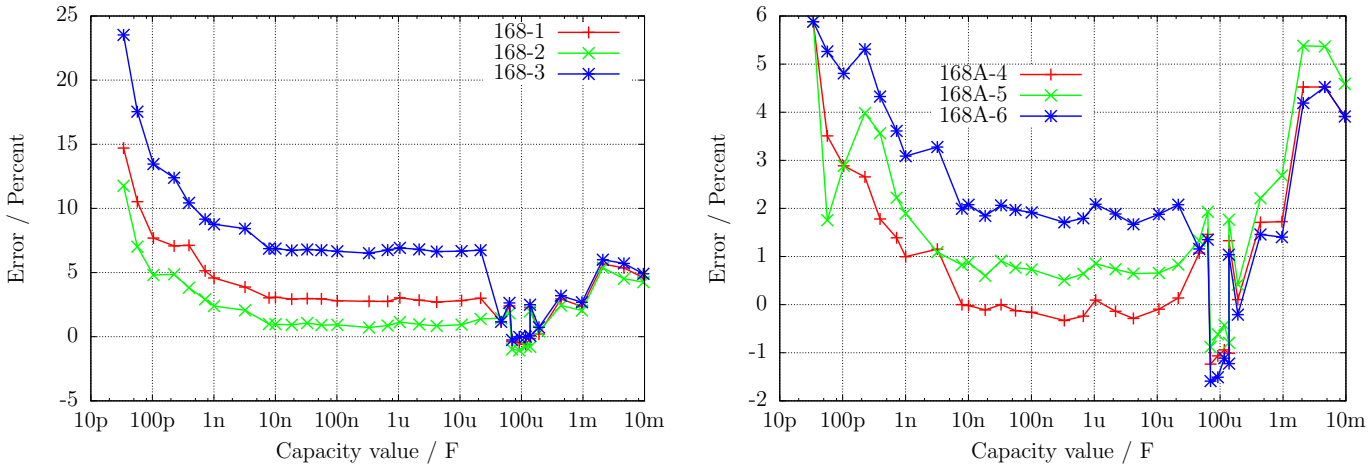


Figure 5.43. Comparison of capacity measurement results of Multimeter, LCR-meter and ATmega168

The differences of measurements of three different ATmega168 processors are shown in figure 5.44a

. In this case the results of the LCR meter is taken as base of comparison. The same results of three different ATmega168A processors are shown in figure 5.44b and three different ATmega168PA processors are shown in figure 5.45. The results of three ATmega328 are additianally shown in figure 5.46a and the results from three ATmega328P are shown in figure 5.46b. At this only the zero value of the capacity measurement of 39pF is respected, all other facility to correct the results are not used. This zero value includes the 2-3pF, which are caused by the 12 cm long cable with the clips. The board layout can cause a different zero value, I have fixed this zero value with the board "DG2BRS V 5.2.1".



(a) three ATmega168 (b) three ATmega168A

Figure 5.44. capacity measurement error, not calibrated

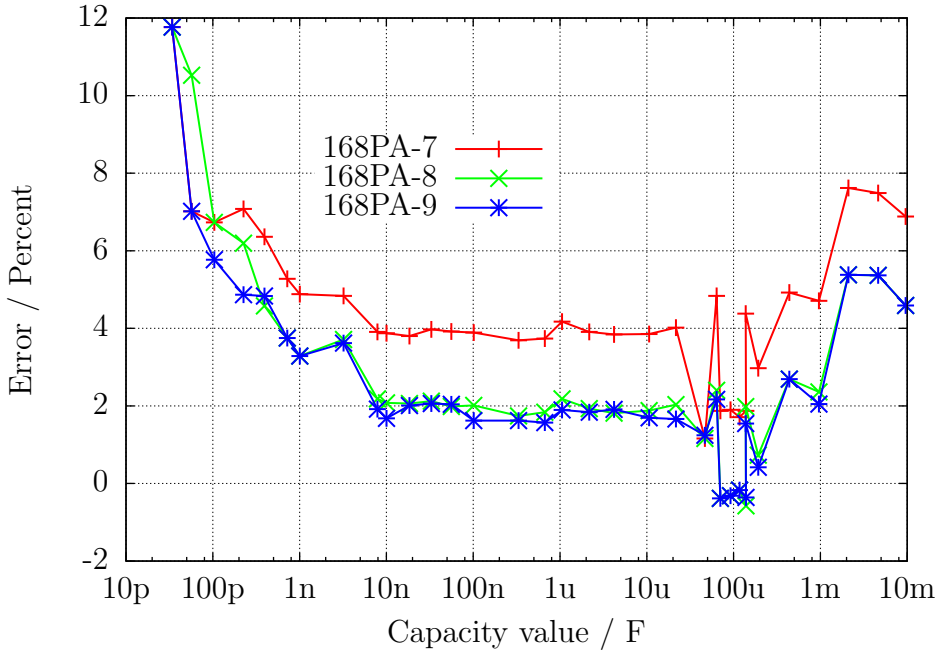
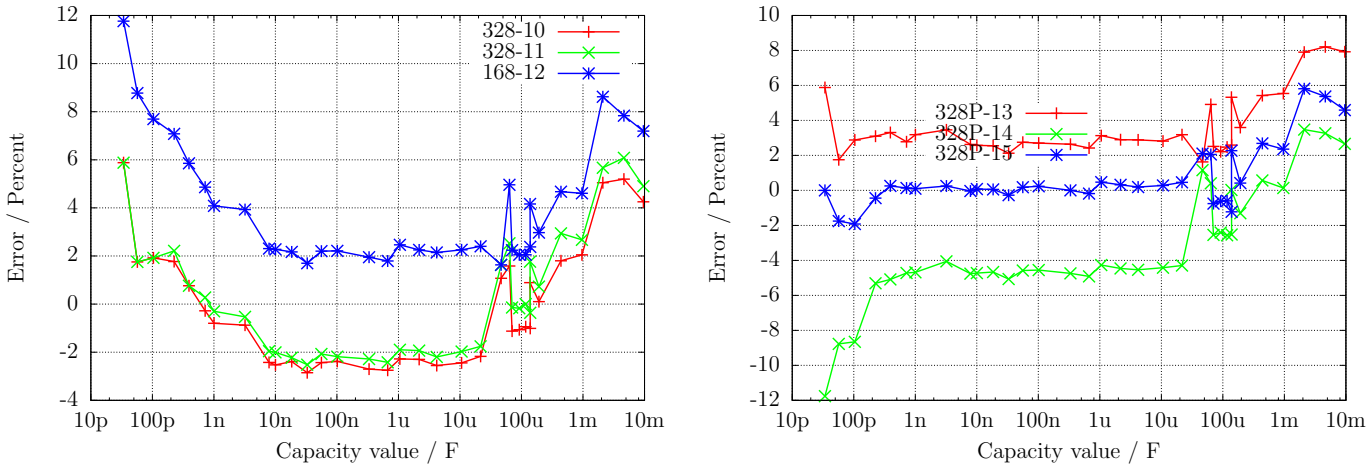


Figure 5.45. capacity measurement error of three ATmega168PA, not calibrated



(a) three ATmega328

(b) three ATmega328P

Figure 5.46. capacity measurement error, not calibrated

To get the best accuracy you must adapt the software to the individual characteristic of your ATmega exemplar. For this you can set a correction voltage REF_C_KORR for the comparator, which will be used for measurement of little capacity values. A correction of 1 mV will reduce the measurement results to 0.11 % . For big capacity values you can specify with the per mill value C_H_KORR, how much your capacity values are measured too big. Because the capacitors with big values are most electrolytic capacitors with worse quality factor, the measurement of the capacity value is difficult. So it is also extra difficult to get the difference to the real value of a capacitor.

Especially with the ATmega168 processors I have noticed a anomaly of measurement results of little capacity values, which depend on the slew rate of the voltage during loading of the capacitor. Figure 5.47 shows the error of the capacity measurement when only the zero value is respected (168-3-A), with correction factor for little capacitors REF_C_KORR=66 as well as the correction factor for big capacitors C_H_KORR=5 (168-3-B), plus additional as gradient 168-3-C with a model of the slew rate dependency of little capacitor measurements (COMP_SLEW1=4000 und COMP_SLEW2=220). Also the self-discharge of big capacitors is respected with gradient 168-3-C. The component with the slew rate dependent value is computed with $\frac{COMP\_SLEW1}{cval+COMP\_SLEW2} - \frac{COMP\_SLEW1}{COMP\_SLEW2}$, where cval is the measured capacity value with pF units.

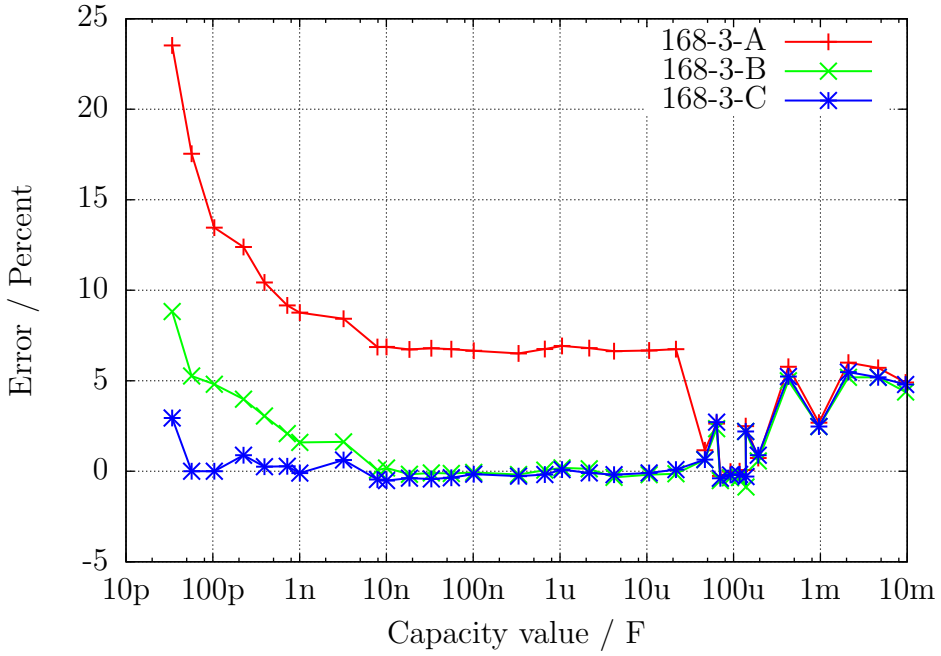


Figure 5.47. Improvement of the capacitor measurement of one ATmega168

5.3.8 Automatic calibration of the capacitor measurement

The automatic calibration is build in two parts. The first part find out the zero offset of the capacity measurement. For that the mean value of the capacity measured without connected capacitor is build. A mean value for all 6 measurement combinations is build with 8 repetitions. After successfull determination the zero offsets are written to the EEprom and will be used for further measurements. More difficult was the clearance of the variance of the different ATmega processors for little capacitors ($<40\mu F$), which is shown in Figure 5.44a, 5.44b and 5.45. As a significant reason for this is found the different characteristic (Offset voltage) of the analog comparator.

The date of measurement of nine different processors is shown in figure 5.48 . The "diff2ref" points show the difference of the voltage of a loaded capacitor of $660nF$ to the individual internal reference voltages (band gap). Ideally this difference Voltage should be zero, if the analog comparator has stopped the loading by the signal to the processor. The short handling time of the processor should not result to a measurably rising of the capacitor voltage of this relative big capacitor. The "CapErr" points show the estimated measurement errors of each processor out of figure 5.44a, 5.44b and 5.45 with per mill units. It is noticeable, how the "CapErr" points will follow the "diff2ref" points. Therefore the "diff" points show the difference between the particular "CapErr" and "diff2ref" points. With a mean value of the "diff" points we can get a good estimation for the correction of the capacitor measurements together with the difference voltage of the loaded capacitor and the internal reference.

For the second part of adjustment you must connect a capacitor to pin 1 and pin 3. This capacitor should have a good quality factor and should have a capacity between $100nF$ and $20\mu F$. It should be a film capacitor, as far as possible not a ceramic capacitor und in no case a electrolytic capacitor. You don't need to know the exact value of this capacitor.

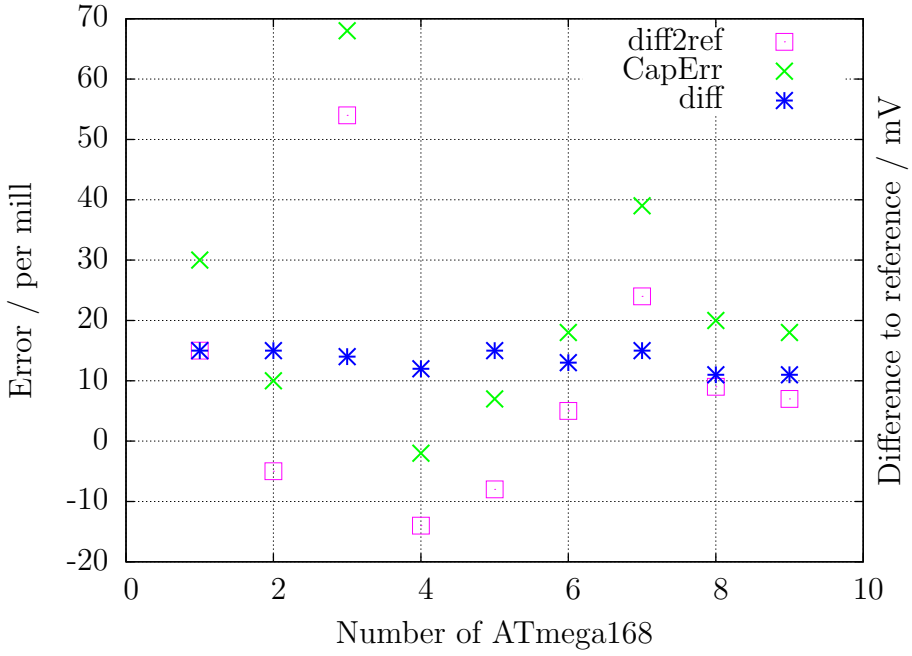
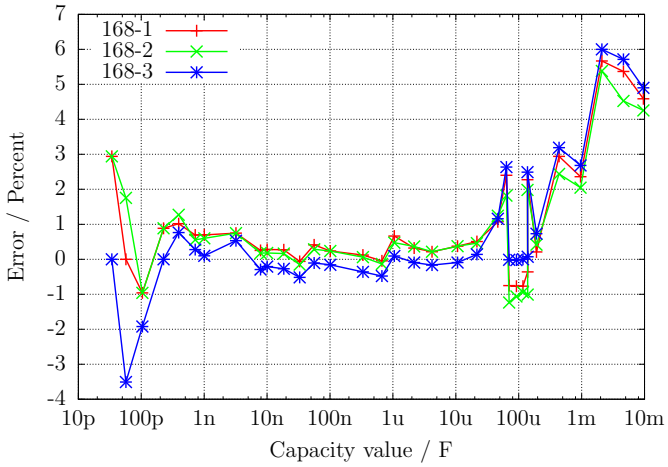
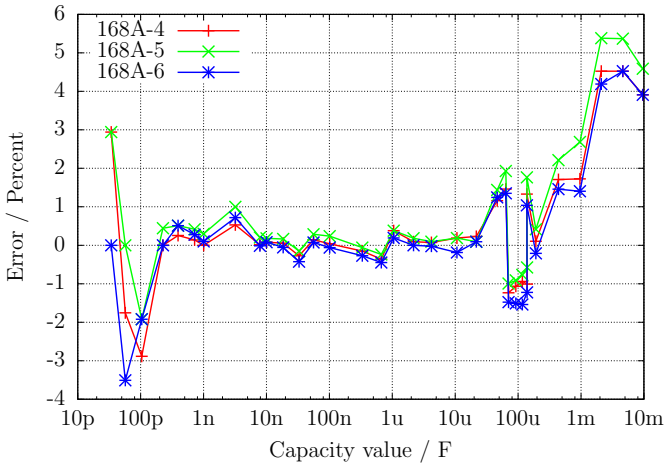


Figure 5.48. Date of nine ATmega168 processors

The figures 5.49a, 5.49b, 5.50, 5.51a and 5.51b shows the measurement results of the different processors with a standard software after the auto calibration. The flash of the processors was loaded with the same software, only the Makefile option "PARTNO = " must be adapted to the different processor type ("m168", "m168p", "m328" or "m328p") for the avrdude program. After loading the data the selftest was started for each ATmega and a capacitor with $330nF$ was connected during test No. 10 to pin 1 and pin 3.



(a) three ATmega168



(b) three ATmega168A

Figure 5.49. capacity measurement error, calibrated

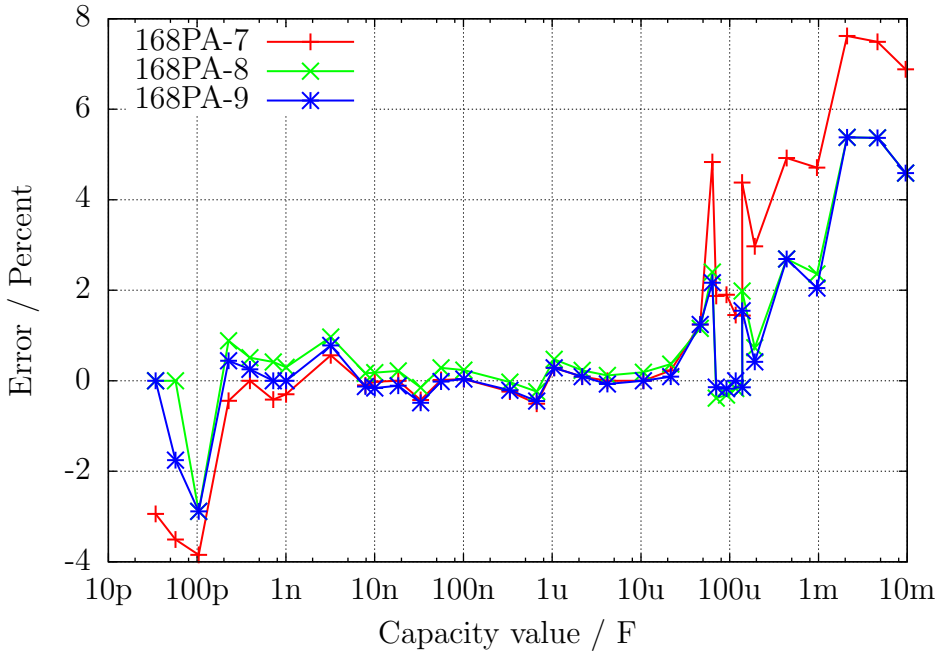
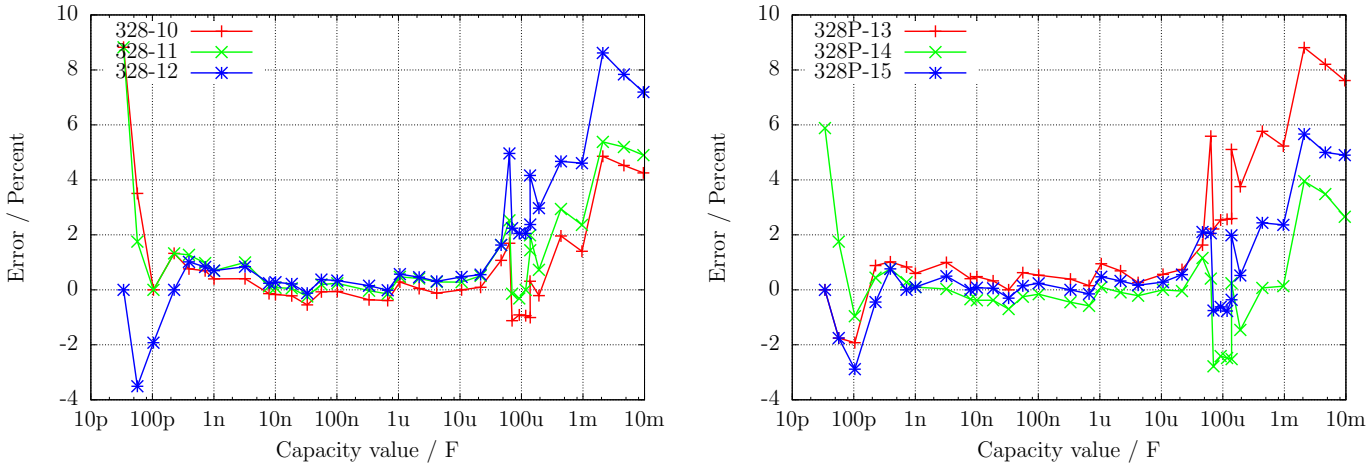


Figure 5.50. capacity measurement error of three ATmega168PA, calibrated



(a) three ATmega328

(b) three ATmega328P

Figure 5.51. capacity measurement error, calibrated

At last I will make more clear the effect of the AUTO_CAL option in the selftest program. The following figure 5.52 shows the results from the three ATmega processors with the biggest error of measurement, one measurement before the calibration and another measurement after the calibration. The points marked with the ending "unc" shows the the errors without calibration. The lines with the ending "cal" shows the error results of the **same processors** with the **same software** after the calibration in the selftest section. The reason for the measurement errors for big capacitors $>(40\mu F)$ is not yet known. All used capacitors for this series of measurements are film capacitors or ceramic capacitors ($56pF$, $100pF$ and $3.3nF$), no electrolytical capacitors are used.

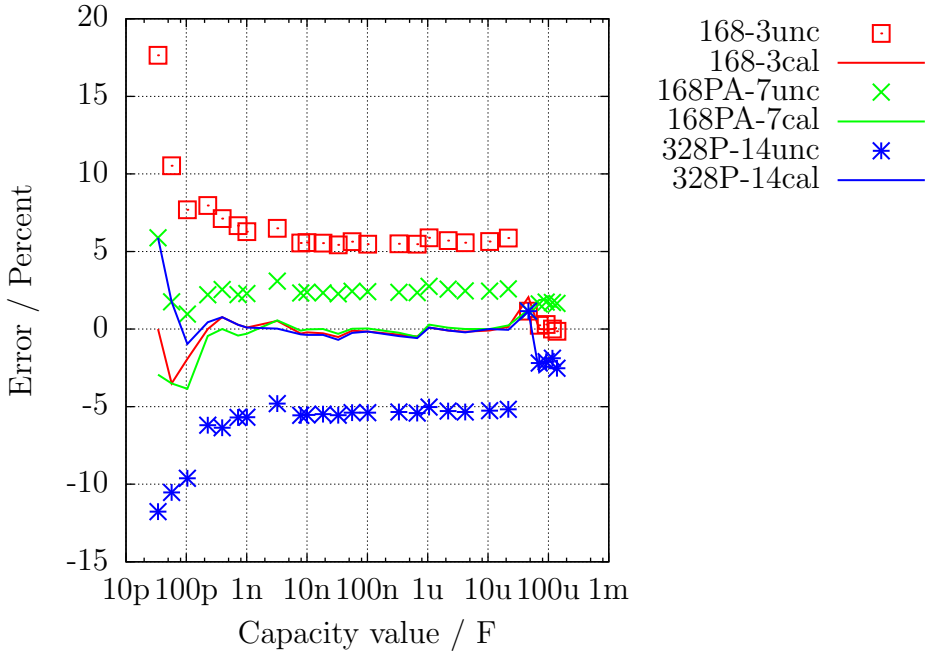


Figure 5.52. Error of capacitor measurement of three ATmega, before and after the calibration

5.4 Measurement of inductance

The measurement of inductance values will be done as separate part with all found resistors with less than 2100 Ω. The methode of measurement is based on the growing of current by formula $Il = Imax \cdot (1 - \exp \frac{-t}{\tau})$ after switching on the current. The time constant $\tau = \frac{L}{R}$ is proportional to the inductance L, but reverse proportional to the resistor R. The current can only measured indirectly with the potential drop of a resistor.

Unfortunately the time constant will be reduced additionally by the relative high resistance 680 Ω, for that the measurement of little inductance values is additionally made difficult with the 8 MHz clock. To get the time constant, the voltage at the 680 Ω resistor will be monitored by the analog comparator. If the voltage drop at the 680 Ω resistor is higher than the voltage of the internal reference, this event will be notified to the 16-bit counter, which is started at the same time of switching current on. The counter will save the state of this event. If the counter will overrun, this will be counted by the program. After the event, the counter will be stopped by the program and the total time will be build with the saved counter stage and the overflow counter. The positive side of the coil will be switched from VCC to GND and hold in this stage until monitoring of the voltages of both pins shows, that no current is detected. The figure 5.53 shown a simplified diagram of the measurement situation.

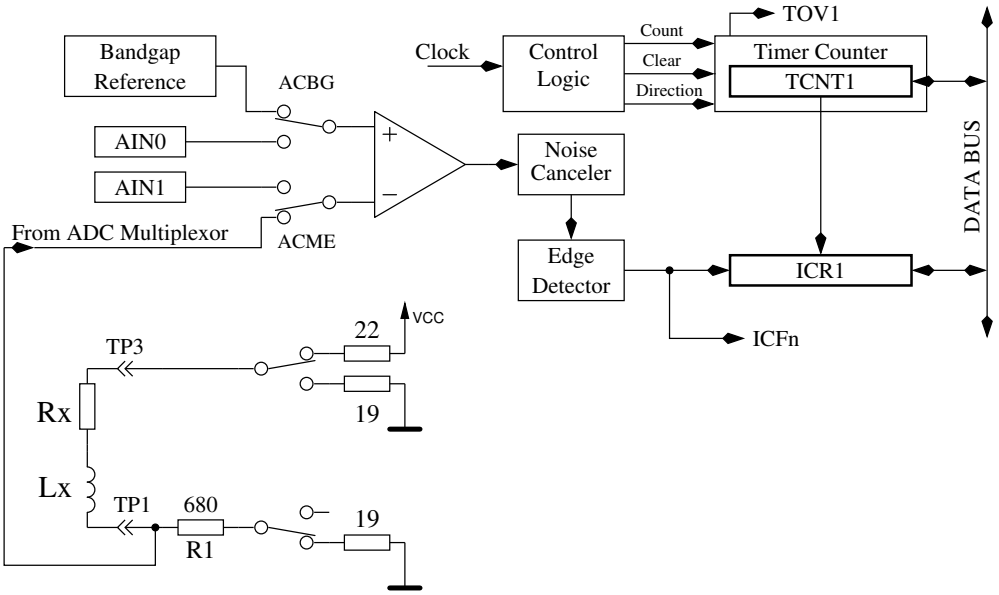


Figure 5.53. Measurement of inductances with the comparator

With the supply voltage VCC and the sum of all resistors in the electric circuit the maximum current Imax and from that the percentage of the reference voltage to the maximum voltage at the 680 Ω resistor can be calculated $Umax = Imax \cdot (680 + 19)$. With the formula $L = -\frac{t \cdot Rges}{\log(1 - \frac{Uref}{Umax})}$ the inductance can be calculated. The natural logarithm will be taken out of a build in table. A inductance resolution of 0.1mH is taken for this type of measurement.

In order to also measure lower inductance values, the 680Ω resistor will be omitted in the current loop, if the resistance value of the inductor is measured with less than 24Ω. Only the output resistance of the port (19Ω) will be used for measurement of the current. In this special case the peak current will be greater than the value, that the specification of the ATmega allows. Because this will be true only for a very short time, I expect no damage of the ATmega ports. For this type of measurement a resolution of inductance of 0.01mH is selected. To avoid a longer time with excessive current, the additional measurement with delayed start of the counter will always be done with the 680Ω resistor. To get better fitting measurement results, a zero offset of 6 is subtract from the counter reading, if

the measurement is done without the 680Ω resistor. Otherwise a zero offset of 7 or 8 is subtracted.

With great inductance values the parasitic capacity can cause a quick rise of current, so that the comparator will responce inmmediately. To get the value of the inductance anyway, the measurement will be repeated with a delayed start of the counter. With this methode the voltage grow caused by the current increase of the inductor will be detected by the analog comparator instead of the current peak of the parasitic capacity. The measurements are always done in both current directions. The program will select the higher result of measurement in the same current direction, but the lower result of the different current direction as the displayed result.

5.4.1 Results of the inductance measurements

The figure 5.54 shows the results of the measurement of different inductors. The Inductors above $1H$ are relays or primary sides of power transformers, for which measurements are difficult because the iron core has residual remanence.

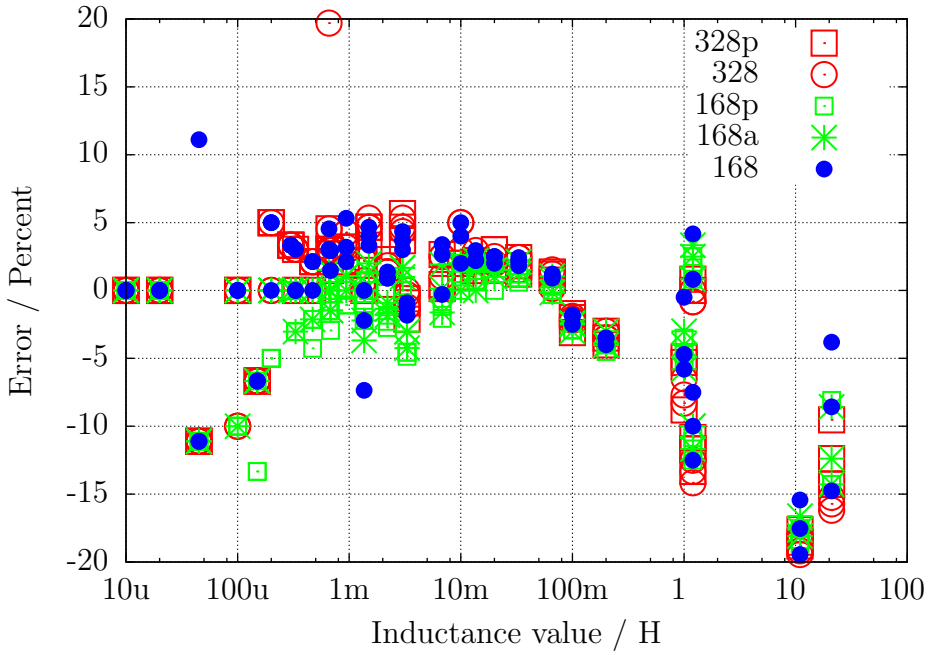


Figure 5.54. Error of inductance measurement of 15 different ATmega

5.5 Selftest Function

Beginning with release 0.9k I have implemented a self test function. Usage is very simple. If you have installed test terminal with clamps, put all clamps together to a piece of uninsulated wire and press the start button. The program notice the shorten probes and start the self test function, if you confirm within two seconds with pressing the start key. This confirmation is implemented to prevent the tester going automatically to the self test by connecting a defect transistor. After finishing the self test the transistor tester will continue with normal measurement. If no equipment is connected, the program will end with "part unknown or damaged". You can configure self test only for a ATmega168 or ATmega328. Before the test steps begin, the zero resistance of the connected probes is determined for all three combinations (T1:T3, T2:T3 and T1:T2). This zero resistances will be subtracted for the future ESR and resistance measurements below 10Ω. If the later measured resistance results fall below the particular zero resistance for more than 0.2Ω, the tester will be resetted to "uncalibrated". This will be marked by a acticated cursor during the tests. The separate steps of the self test function 1 to 7 is displayed on row 1 of the LCD display with the letter T followed by the step number. Every step is repeated 4 times, before the program continues with the next step. But if you hold the start key pressed, when the test cycle is finished, this test is not repeated any more. If you leave the key pressed the total time, every test is executed only once.

Without the AUTO_CAL option only measurement results are displayed in every step, no error analysis are done, you must interpret the results yourself. At this place I will give you an additional important hint. Never do a measurement with connected ISP plug! The ISP interface influences the measurement. Here is the list of currently implemented tests:

1. **Measurement of the 1.3V (or 1.1V) reference Voltage (band gap Reference).** In row 1 the text "Ref=" and the measured Voltage in mV is displayed. For the ATmega8 the voltage should be near to 1.3V. For the other processors the voltage should be near to 1.1V. The second row shows the resulting factor for the capacity measurement with the $470k\Omega$ resistor.

2. **Comparing of the** 680Ω **resistors.** In row 1 the cryptic text "+RL- 12 13 23" is shown. Meaning of this is as follows: The RL is the short form of Resistor Low meaning the 680Ω resistors. The 12 stand for: resistor at pin 1 is connected to VCC (+) and resistor at pin 2 is connected to GND (-). The result of this measurement is displayed in row 2 at the first place as difference to the theoretical value. In row 1 follows now a "13" which means, that the first connection of measurement 1 is still connected with 680Ω to VCC but that the resistor of pin 3 is connected to GND. The result is displayed in the middle place of row 2 as difference to the theoretical value. The last measurement of this test "23." means that now the resistor at pin 2 is connected to VCC (+) and the resistor of pin 3 is connected to GND. The result of measurement is displayed at the last place of LCR row 2 as difference to the theoretical value. Please remember, that the resolution of the ADC is about 4.88mV! The measurement situation is also shown in figure 5.55. The theoretical value with respect to the internal resistance of the pins should be: $\frac{5001 \cdot (19+680)}{(19+680+680+22)} = 2493$.

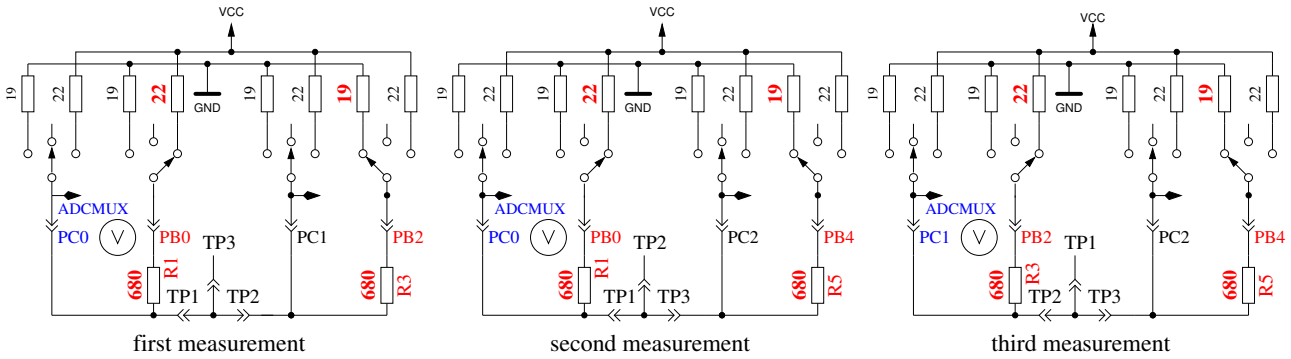


Figure 5.55. Comparison of 680Ω resistors

3. **Comparing of the** $470k\Omega$ **resistors.** Now the display shows in row 1 "+RH- 12 13 23". The same procedure as done in step 2 is repeated with the $470k\Omega$ resistors (symbols RH). All results are shown as difference to the theoretical value. The theoretical value is this time $\frac{5001\cdot(19+470000]}{(19+470000+470000+22)} = 2500$ for all combinations.

4. In this step nothing is measured, but the **order is displayed isolate Probe!**, which means that it is time to separate the probes (release from wire). This step will finish only if you release the connections between the probes.

5. **This step tests the capability of GND (-) connected** $470k\Omega$ **resistors (H) to pull the test pins to GND.** Row 1 shows the text "RH-". Row 2 should display zero for all three pins.

6. **This step tests the capability of VCC (+) connected** $470k\Omega$ **resistors (H) to pull the test pins to VCC (+).** Row 1 shows the text "RH+". The results are shown als difference to VCC and should be near zero. Great differences from the best value for test 5 and 6 are errors such as isolation problem, flux material or damaged port.

7. **This Step tests the voltages of the** $470k\Omega/680\Omega$ **resistor divider.** The voltage difference to the expected voltage of the $470k\Omega$ / 680Ω resistor dividers is shown in row 2 of the LCD for all three terminals. Differences of more than some mV can be caused by the assembly of wrong resistor values.

8. **Measuring of internal resistance of pin output switched to the GND signal.** This test and the follwing tests will only be done, if the option AUTO_CAL is selected. The internal resistance of the port C outputs switched to GND (-) are measured with the current of to VCC (+) switched 680Ω resistors, see Figure 5.56. Only the three pins of the ADC port are measured, the resistor port B (PB0,PB2 and PB4) can not be measured without hardware modification. Is is assumed that the port resistance of the different ports are nearly identical. The resistor value will be shown in the next test.

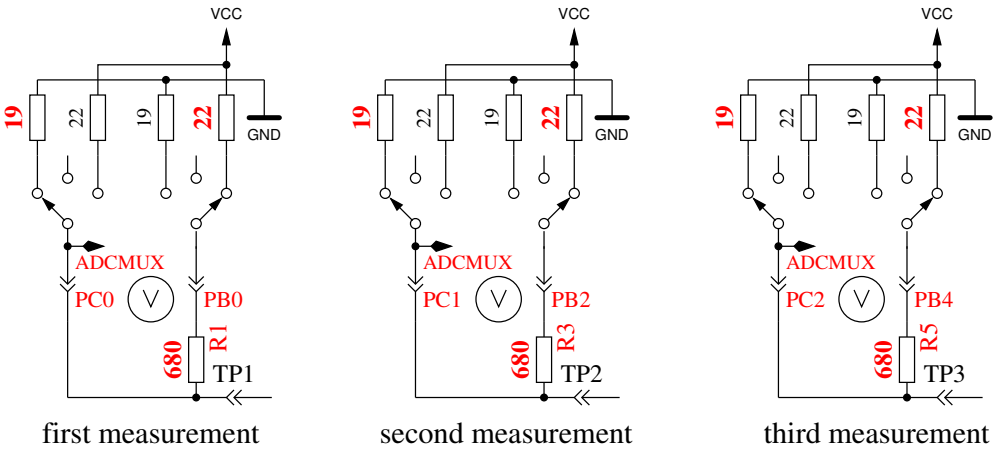


Figure 5.56. Measurement of internal resistance of Port C switched to GND

9. **Measuring of internal resistance of port outputs switched to the VCC (+)signal.** The needed current is generated with to GND connected 680Ω resistors . It are the same measurements as those in test 8 to the other side as you can see in Figure 5.57. With the following steps the resistance is computed: To get the current, the following is computed: $(VCC-(resultoftest8)-(resultoftest9))/680$. To get both resistor values, the voltage (result of test 8 or 9) is divided by this current. The result for this test will then be notified in row 1 with the text "RI_Hi=", the resistance value (Ω) to the GND side is displayed in row 2 with the text "RI_Lo=". Beginning with version 1.06k of the software, the port output resistance values are determined at the beginning of every measurement. The values are only shown by this step.

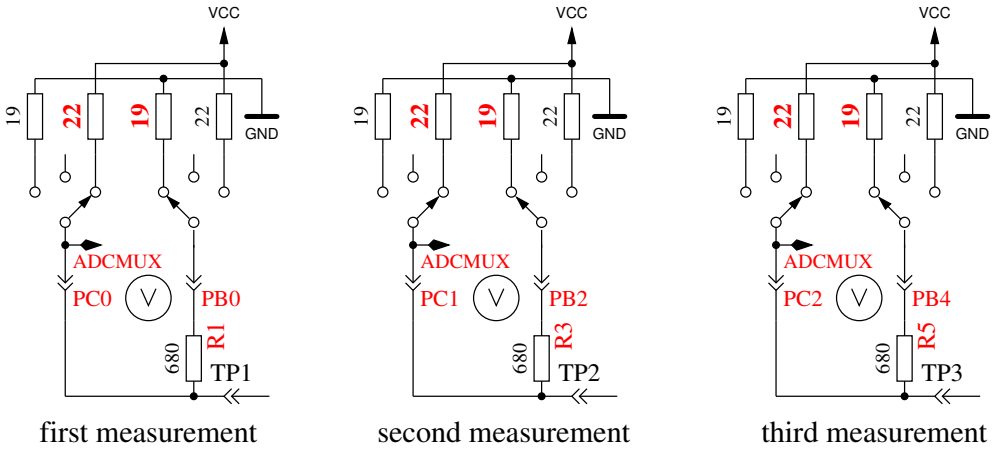


Figure 5.57. Measurement of internal resistance of Port C switched to VCC

10. **Measurement of the zero offset of the capacitor measurement.** The zero offset for the capacity measurement with pin combinations 1:3, 2:3 and 1:2 is shown in that order in display row 1 following the "C0 ". Alls three values are shown in pF units. For this measurements no predefined zero offset is respected. The zero offsets of pin combinations in opposite order is also measured. The results will be written to the EEprom, if all values are less than $190pF$. This will be notified by the output of "OK" in row 2. The found zero offsets are used for further capacity measurements with respect to the pin combination. If there is any measurement found with a capacity value 20pF below the particular zero offset, the tester will be resetted to "uncalibrated". This will be noticed by a activated LCD cursor during further tests. Please notice, that changes of the test equipment can cause a new adjustment of the zero offset. If you use wire with clips, the zero offset may be 3 pF greater compared to a empty socket.

11. **Wait for the connection of a capacitor to pin 1 and pin 3.** The message “1-C-3 >100nF” is shown in row 1 of LCD. To prepare the measurement of the comparator offset voltage, you must connect a sufficient big capacitor to pin 1 and pin 3. It should be a capacitor with a high quality factor and a capacity between $100nF$ and $20\mu F$. You should never use electrolytical capacitors, use film capacitors instead.

12. **Measurement of the comparator offset for capacitor measurement adjustment.** To get the offset of the analog comparator, a capacitor must already be connected to pin 1 and pin 3. The capacitor is needed for buffering the load voltage of a capacitor, in order to get the voltage difference of load voltage to the internal reference voltage (band gap). If measurement is successfull, the correction value is short shown with the text “REF_C=” in row 1 of the LCD and written to the EEprom. You can give a additional offset to the automatic measured value with the REF_C_KORR option.

    If you have selected the AUTOSCALE_ADC option, the gain of the ADC readings with the internal reference will be adjusted by comparing a capacitor voltage below 1 V once readed with VCC reference and once readed with the internal reference. The measurement result is shown in row 2 with the text “REF_R=”. Your REF_R_KORR value is a additional offset to this automatic find out difference value.

At the end of test function the text “Test End” is shown in row 1 and the version number of software is shown in row 2. If the Makefile option FREQUENCY_50HZ is set, a **50Hz rectangle signal** is generated on pin 2 and the same signal in opposite direction on pin 3. Pin 1 is switched to GND . The current is limited with 680Ω resistors. This will be notified by the Output of “50Hz” at the end of row 1 of the LCD display. The 50Hz signal will be generated 30 times for 2 seconds each. You can check the time of the wait calls, if you have an oscilloscope or frequency counter. Figure 5.58 shows the oscillograph curves of both 50 Hz output pins with crystal operation.

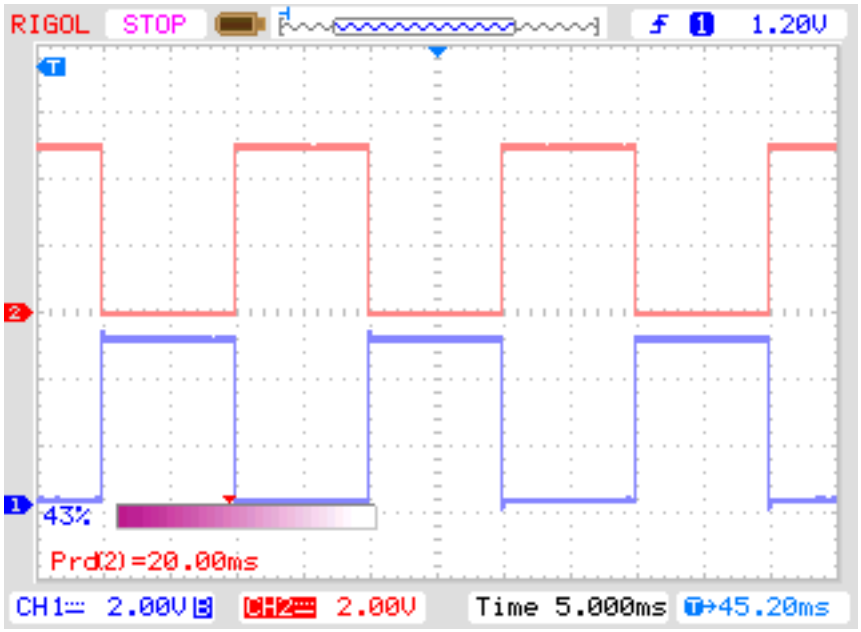


Figure 5.58. Oscillograph curve with the 50Hz outputs of Port 2 and 3

If you don’t use the crystal clock version, the result may be inexactly. A exactly clock frequency and wait time are important for measurement of capacity values. You can abort the generation of the 50Hz signal by long time pressing of the start button. Then the program continues with the normal measurement task.

5.5.1 Some Results of the Selftest Function

The results of the selftests of nine different ATmega168 processors and of six ATmega328 processors will be shown in the following figures.

Test No.	measurement typ	theoretical	figure
Test 1	band gap Ref	1100	5.59
Test 2	RL-Mean	0	5.60a
Test 3	RH-Mean	0	5.60b
Test 5	RH-Low	0	5.61a
Test 6	RH-High	0	5.61b
Test 8	R out Lo	131	5.62a
Test 9	R out Hi	151	5.62b
Test 10	Cap zero offset	30	5.63
Test 11	Reference correction	0	5.64

Table 5.6. Table of the selftest figures

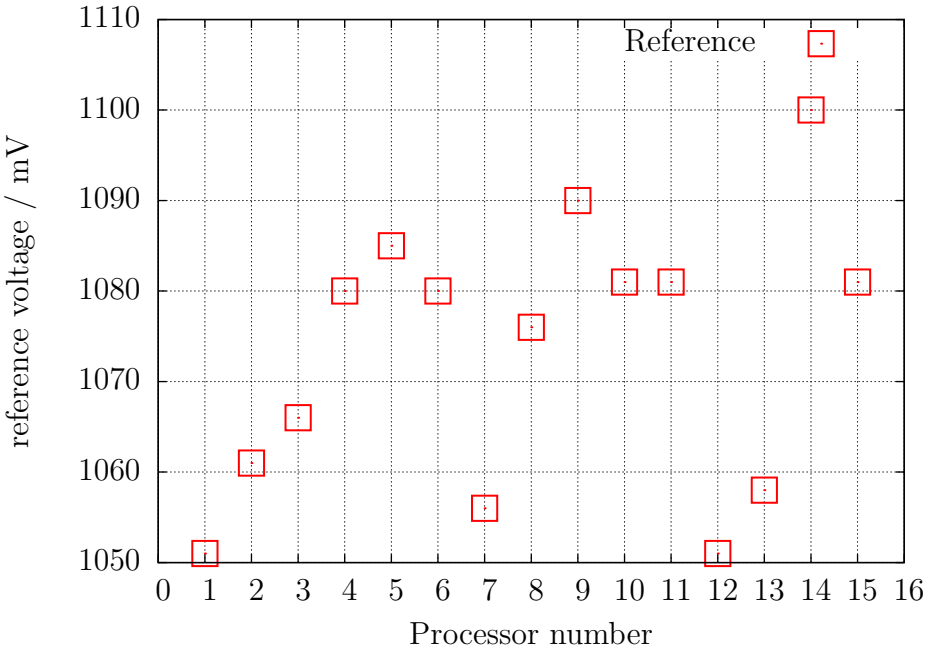
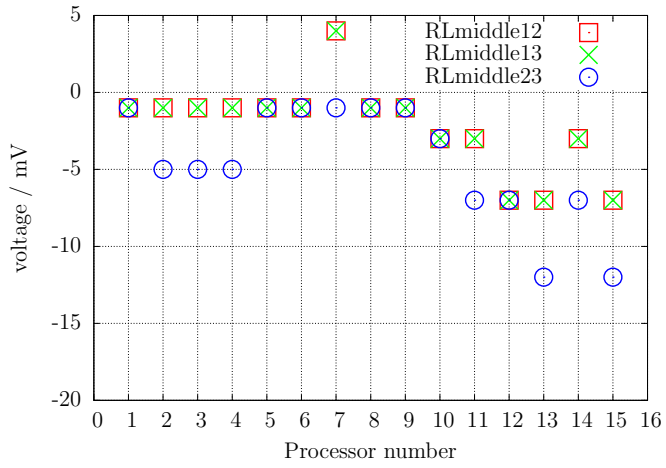
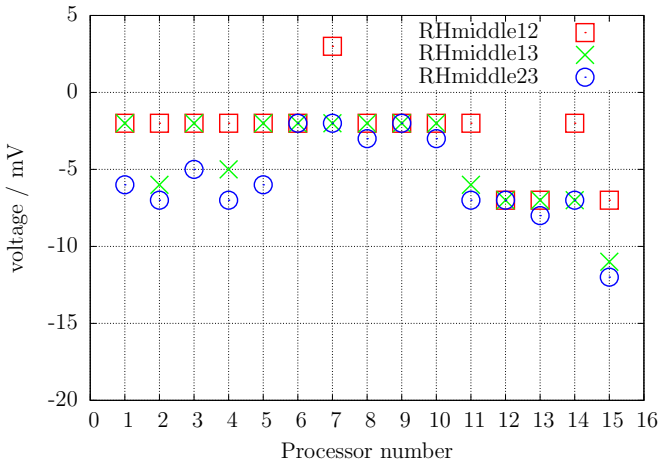


Figure 5.59. Selftest: Reference-Voltages

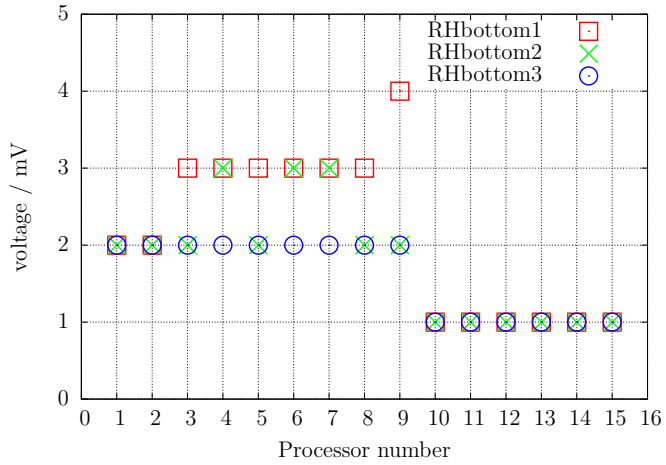


(a) with 680Ω

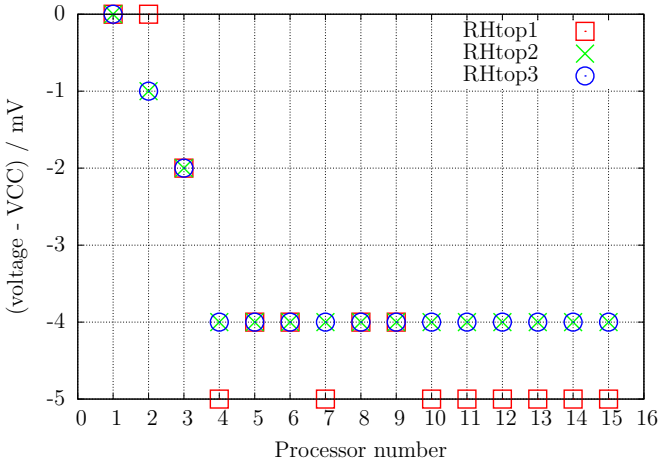


(b) with 470$k\Omega$

Figure 5.60. Selftest: difference to ideal mean voltage

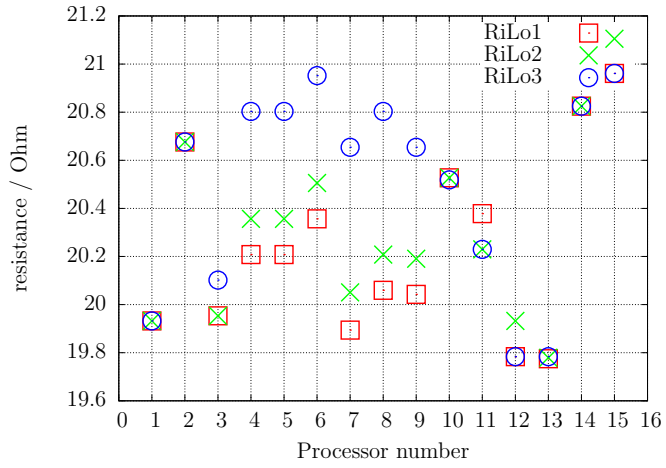


(a) with 470$k\Omega$ to 0V

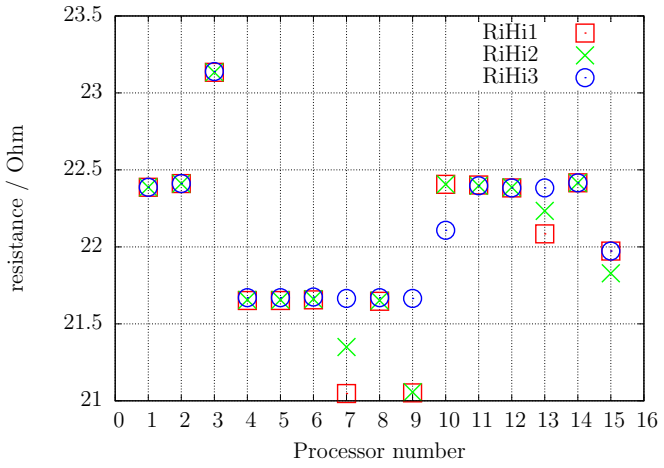


(b) with 470$k\Omega$ to 5V

Figure 5.61. Selftest: Input voltage



(a) with 680Ω to 5V



(b) with 680Ω to 0V

Figure 5.62. Selftest: Output resistance

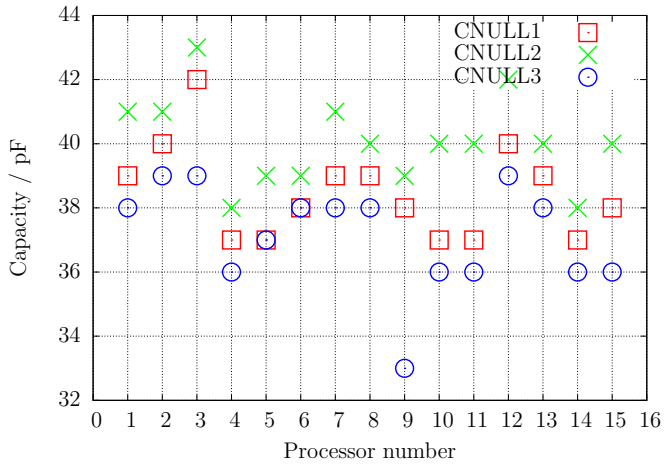


Figure 5.63. Selftest: zero offset of the capacity measurement

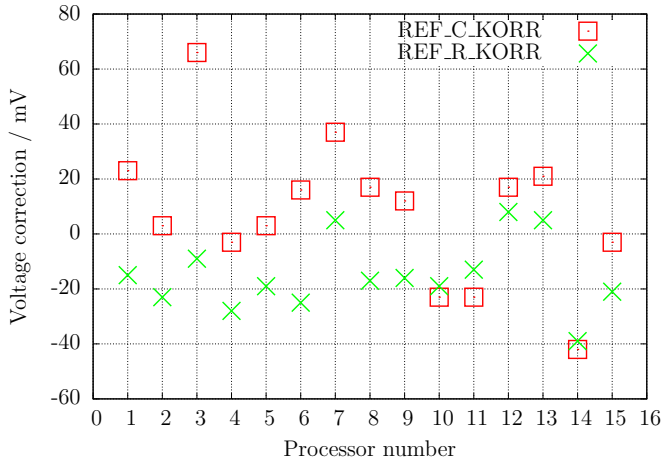


Figure 5.64. Selftest: correction values after automatic calibration

At last I would like to show you the difference voltages of the external at the AREF pin with a multimeter measured voltages and the internal with the ADC measured voltages of the reference voltages of 15 different ATmega precessors and the found correction voltages (REF_R_KORR) after the automatic calibration in figure 5.65. You can see, that the automatic calibration values nearly follow the external measured values.

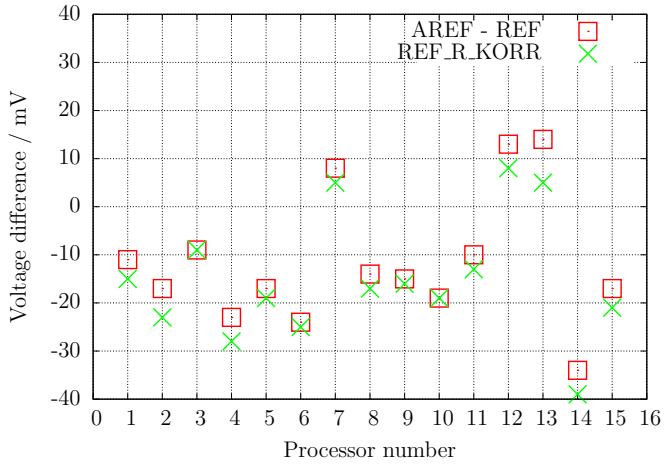


Figure 5.65. Selftest: Voltage difference of the internal reference

5.6 Measurement of frequency

Beginning with Version 1.10k the frequency measurement can be selected with a control menu. The normal frequency measurement is done with counting the falling edges of input signal T0 (PD4) with counter 0 fr one second. For maintaining of a accurate second, the counter 1 is used with a 256:1 prescaler of the CPU frequency. The 16 bit counter of the ATmega can be used up to 16 MHz CPU frequency with the prescaler to serve the second period in one pass. For the start and stop of the counter 0 ist the compare register B and A of the counter 1 used. To prevent a unstable delay by polling the compare event signals, for starting and stopping the Interrupt Service of both counter 1 compare events is used. The time delay of both Interrupt Service Routines is nearly equal. To maintain a accurate second period is a constant delay insignificant. With analysing the assembler code, the difference in time can be adjusted.

For frequencies below $10kHz$ the normal measurement is followed by a measurement of period time. This additional measurement is only followed after a normal frequency measurement. This will be done by measuring the time of a selectable count of the Pin Change interrupts of the PCINT20 (PD4) input with the counter 0. The counter 0 is used with full clock rate. This results to a resolution of $125ns$ for $8MHz$. With a greater count of measurements periods the resolution can be reduced. By using a measurement period of 125 periods, the middle resolution for one period is $1ns$. To prevent the inexactness of start and stop the counter 0, the start of counter 0 is started within the first pin change interrupt of PCINT20 and will be stopped with the last pin change interrupt with the same interrupt service routine. The count of periodes is choosed, that the measurement time is about 10 million clock tics. The part of error from one clock is only 0.1ppm with this choise. With a $8MHz$ clock the measurement time is about 1.25 seconds. Aus der so ermittelten mittleren Periode wird dann eine Frequenz mit hherer Auflsung berechnet. From this mean value of one period a frequency with better resolution is computed too.

For checking the procedure, two testers are measured against each other. First the test frequencies are generated with tester 2 and measured with tester 1. After that the testers are swapped and the measurement is repeated. Figure 5.66 shows the results of both measurement series. The nearly constant errors can be explained with a little frequency difference of both crystals. It is possible to tune the frequency offset with adjustable capacitors at the crystal. A one puls per second (1PPS) from a GPS receiver can be used to tune the crystal frequency for example.

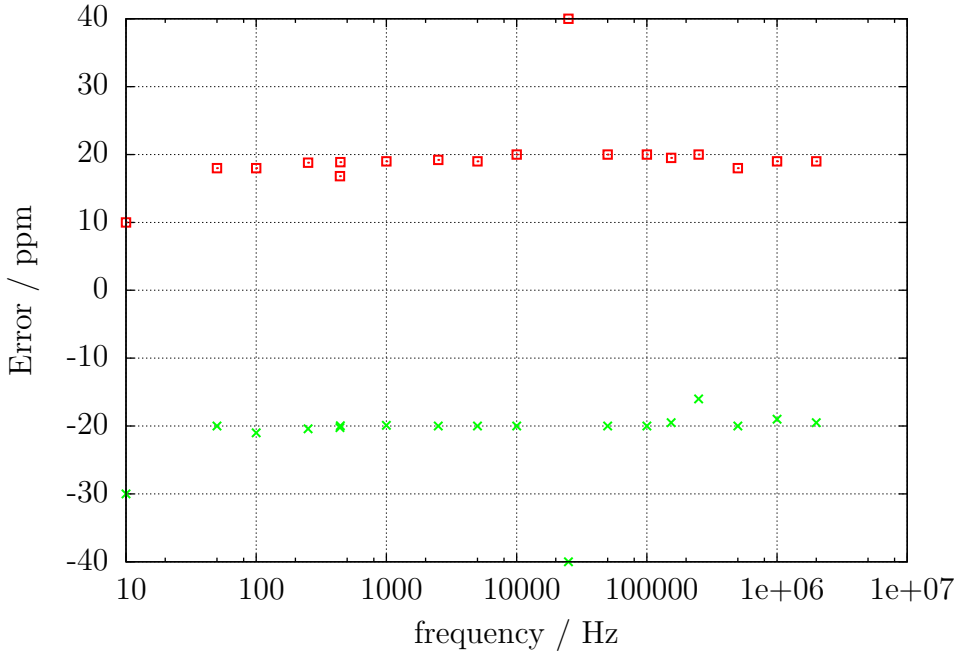


Figure 5.66. Relativ erros of frequency measurement

Chapter 6

Known errors and unsolved problems

Software Version 1.10k

1. Germanium Diodes (AC128) are not detected in all cases. This is probably caused by the residual current. Cooling of the diode can help to reduce the residual current.

2. The current amplification factor of germanium transistors can be measured too high because of the high residual current. In this case the basis emitter voltage will be very low. Cooling of the transistor can help to get a more correct current amplification factor.

3. Capacity value in reverse direction for Power Schottky Diodes such as MBR3045PT can not be measured, if only one diode is connected. The reason is a too big residual current of this diode. Sometimes the measurement is possible by cooling down the device (with cooling spray for example).

4. Here and there a wrong detection of the 2.5V precision reference is reported, when the PC4 pin (27) is unconnected. You can avoid this behaviour with a additional pull up resistor connected to VCC.

5. The diode function of a triac gate can not be examined.

6. Sometimes a problem with the Brown Out level of 4.3V is reported for ATmega168 or ATmega328 processors. This will cause a reset during capacity measurement. A reason is not known. The Resets will disappear, if the Brown Out level is set to 2.7V.

7. With the using of the sleep state of the processor, current of VCC power is changing more than using previous software versions. You should check the blocking capacitors, if you notice any problems. Ceramic capacitors with 100nF should be placed near the power pins of the ATmega. The using of sleep state can be deselected by the Makefile option INHIBIT_SLEEP_MODE.

8. The measurement of tantalum based electolytical capacitors often make trouble. They can be detected as diode or can also be not detected as known part. Sometimes the measurement with swapped connection can help.

Chapter 7

Special Software Parts

Several modifications are done to save flash memory. The LCD-Output of probe-pin numbers was done in the form "lcd_data('1'+pin)". To save the add operation for every call, the entry "lcd_testpin(uint8_t pin)" was added to the lcd_routines.c.

The pseudo calls in the form "_delay_ms(200)" are not implemented as library calls, but wait loops are implemented for every call. This will consume much memory, if you have many calls at different location in your program. All of this pseudo calls are replaced with calls to my special assembly written library, which uses only 74 bytes of flash memory (@8MHz), but enables calls from wait1us() to wait5s() in steps of 1,2,3,4,5,10,20.... The routines include the Watch Dog Reset for all calls above 50ms. Every wait call usually only need one instruction (2 Byte). Wait calls with interim value such as 8ms need two calls (5ms and 3ms or two times a 4ms call). I don't know any implementation, which is more economical if you use many wait calls in your program. The calls uses no registers, only the Stack Pointers for the return adresses in the RAM (at most 28 Byte stack space in current release) is used. The total list of functions is:
wait1us(), wait2us(), wait3us(), wait4us(), wait5us(), wait10us(),
wait20us(), wait30us(), wait30us(), wait40us(), wait50us(), wait100us(),
wait200us(), wait300us(), wait400us(), wait500us(), wait1ms(),
wait2ms(), wait3ms(), wait4ms(), wait5ms(), wait10ms(),
wait20ms(), wait30ms(), wait40ms(), wait50ms(), wait100ms(),
wait200ms(),wait300ms(), wait400ms, wait500ms(), wait1s(),
wait2s(), wait3s(), wait4s() and wait5s();
That are 36 functions with only 37 instructions inclusive Watch Dog Reset! There is really no way to shorten this library. Last not least matches the wait calls the exactly delay time, if the lowest wait call does. Only the wait calls above 50ms are one cycle per 100ms to long because of the additionally integrated watch dog reset.

Additionally the often used calling sequence "wait5ms(); ReadADC...();" is replaced by the call "W5msReadADC(...);". The same is done for the sequence "wait20ms(); ReadADC(...);" which is replaced by one "W20msReadADC(...);" call. The function ReadADC is additionally written in assembly language, so that this add-on could be implemented very effective. The functional identical C-version of the ReadADC function is also avaiable as source.

Chapter 8

To Do List and new ideas

1. Add more and better documentation.
2. Think about how we can get the real internal resistance of port B output (resistor switching port) instead of assuming, that ports are equal.
3. Can discharging of capacitors be made more quickly, if the minus pin is additionally raised with the 680Ω resistor to VCC (+)?
4. Check if the tester can use floating-point representation of values. The risk of overflow is lower. There is no need to use multiplication and division together to build a multiplication with a non integer factor. But I don't know how much flash memory must be spend for the library.
5. Write User's guide for configuring the tester with the Makefile options and description of the build chain.
6. If the holding current of a thyristor can not be reached with the 680Ω resistor, is it harmless to switch the cathode directly to GND and the anode directly to VCC for a very short time? The current could reach more than 100mA. Will the port be damaged? What is with the power supply (voltage regulator)?
7. Check the Port afterwards with self test function!
8. Warning message, if the found reference voltage is not plausible in relation to ATmega model and VCC.
9. What is about a second generation tester with a bigger ATmega which includes differential ADC-port, more flash memory . ? There is no ATxmega which have supply voltage of 5V, only the ATmega line is possible.
10. Idea for a New Projekt: USB version without LCD-Display, Power from USB, Communication to PC over a USB-Serial bridge.
11. Control of pulse width with fixed frequeny on TP2.
12. Calibration of crystal frequency. With 1PPS from GPS receiver? Tuning with adjustable capacitors?
13. Selectable separated ESR measurement. Is the "in circuit" measurement possible?
14. Selectable separated 2-pin measurement for quicker selection of parts (resiators and capacitors).
15. Support for 20x4 character display.

Bibliography

[1] Markus Frejek *AVR-Transistortester,*. Embedded Projects Journal, 11. Ausgabe, 2011

[2] Atmel Corporation *8-bit AVR with 8KBytes In-System Programmable Flash - ATmega8(L),*. Manual, 2486Z-AVR-02/11, 2011

[3] Atmel Corporation *8-bit AVR with 4/8/16/32KBytes In-System Programmable Flash - ATmega48 - ATmega328,*. Manual, 8271D-AVR-05/11, 2011

[4] Atmel Corporation *Atmel AVR126: ADC of megaAVR in Single Ended Mode,*. Application Note, 8444A-AVR-10/11, 2011

[5] Atmel Corporation *Atmel AVR121: Enhancing ADC resolution by oversampling,*. Application Note, 8003A-AVR-09/05, 2005

[6] `http://en.wikibooks.org/wiki/LaTeX` *LaTeX documentation,*. Guide to the LaTeX markup language, 2012

[7] `http://en.wikibooks.org/wiki/Gnuplot` *Gnuplot documentation,*. Documentation for the plotting tool gnuplot, 2012

[8] Wikipedia `http://de.wikipedia.org/wiki/Equivalent_Series_Resistance` *Explanation for ESR in german language*. Standardization and equivalent circuit of a capacitor, 2012

[9] `http://www.xfig.org/userman` *Xfig documentation,*. Documentation of the interactive drawing tool xfig, 2009

[10] `http://docs.gimp.org/2.6/de` *gimp documentation*. Documentation of the GNU Image Manipolation Program, 2010

[11] `http://www.mikrocontroller.net/articles/AVR-Transistortester` *Online documentation of the Transistortester,* Online Article, 2009-2011

[12] `http://www.mikrocontroller.net/articles/AVRDUDE` *Online documentation of avrdude programmer interface,* Online Article, 2004-2011

[13] `http://www.mikrocontroller.net/topic/131804` *Thread from Markus,* Forum thread, 2009

[14] `http://www.mikrocontroller.net/articles/AVR_Transistortester` *Short description of new features of the TransistorTester von Karl-Heinz K.,* Online Article, 2012

[15] `http://www.mikrocontroller.net/topic/248078` *Thread from Karl-Heinz,* Thread and new software versions, 2012

[16] `http://www.mikrocontroller.net/articles/WinAVR` *Information about WinAVR in german language,* Online Article, 2012

[17] http://winavr.sorceforge.net *Source for WinAVR package,* Download source, 2012

[18] http://www.mikrocontroller.net/topic/248078?page=5#2922341 *Patch for WinAVR, Setting of Fuses with avrdude,* Download Quelle, 2012