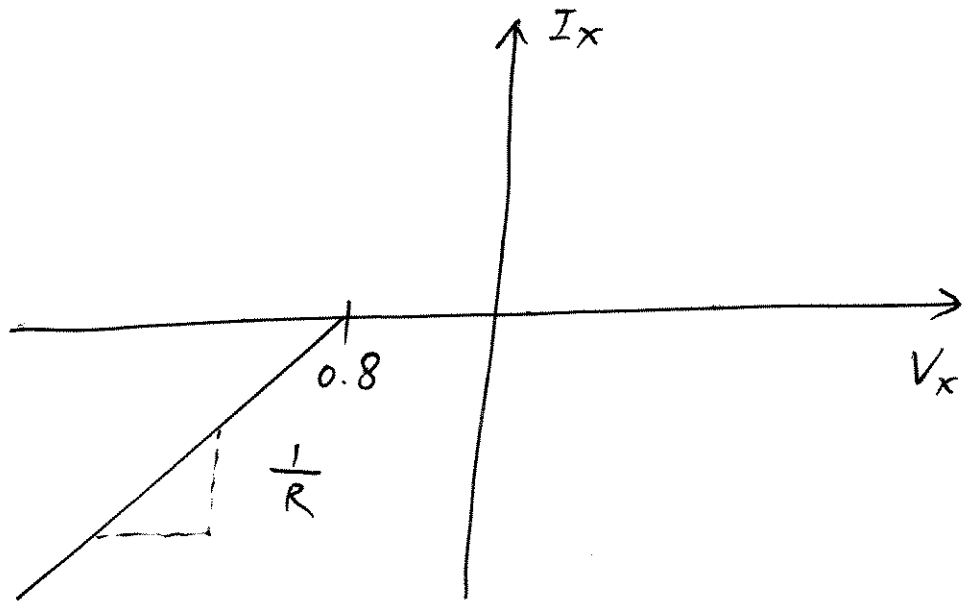
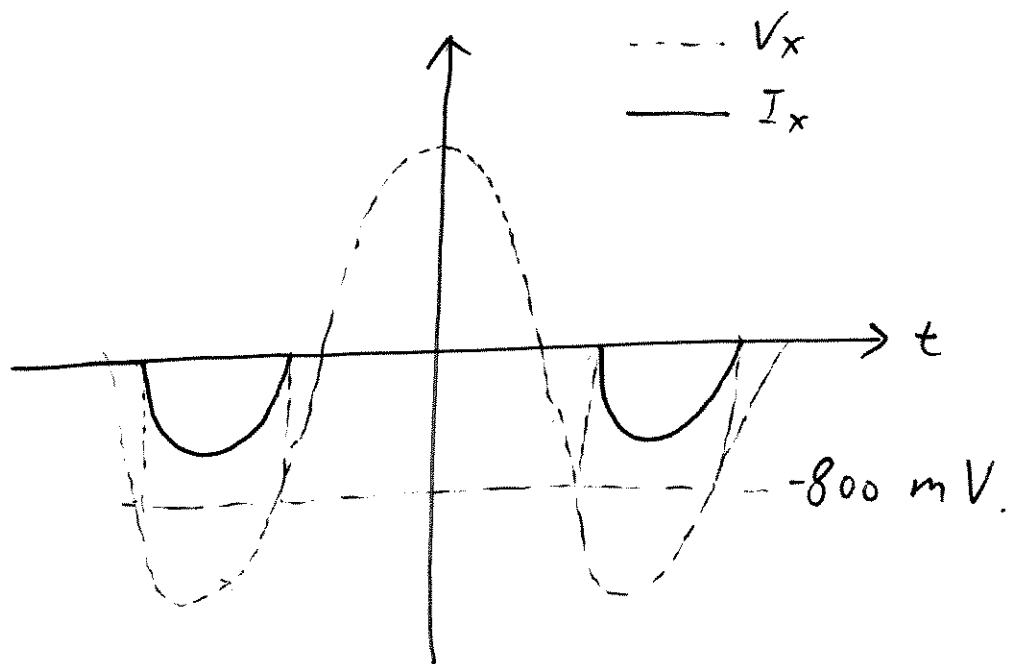


①

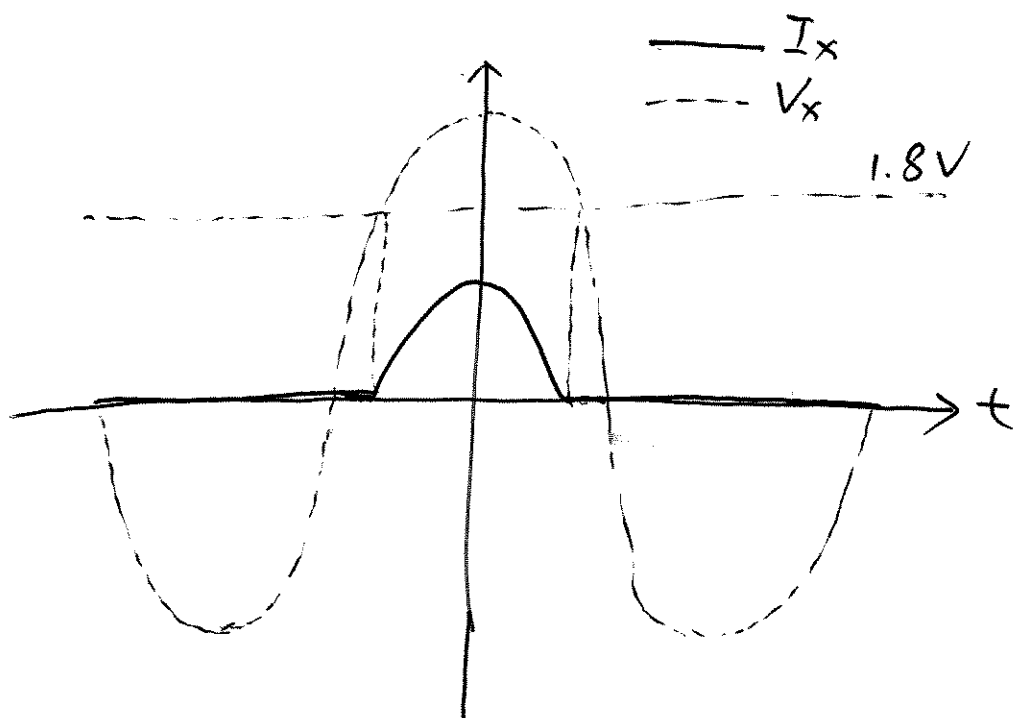
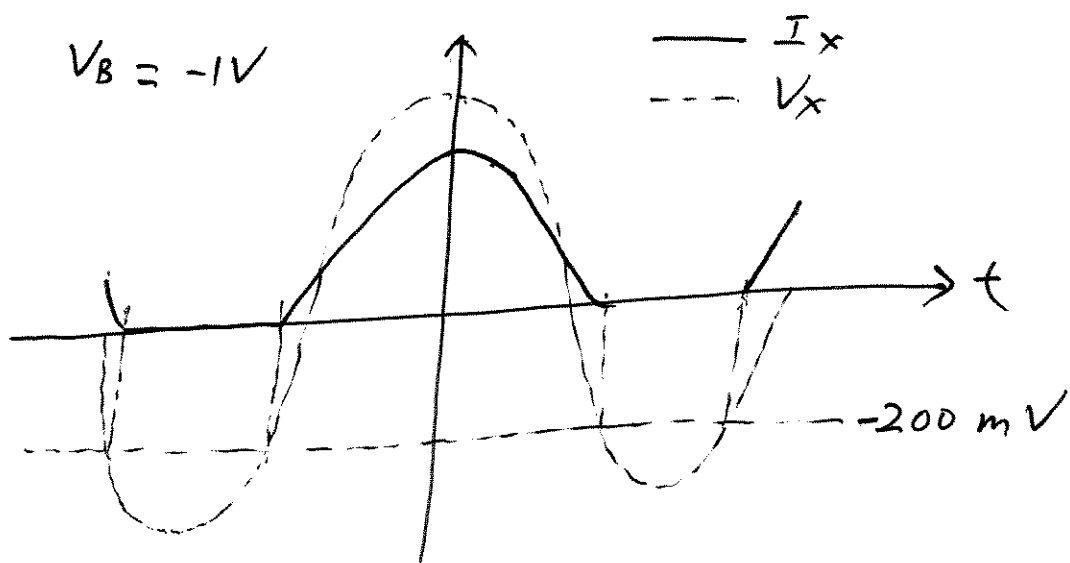


(2)

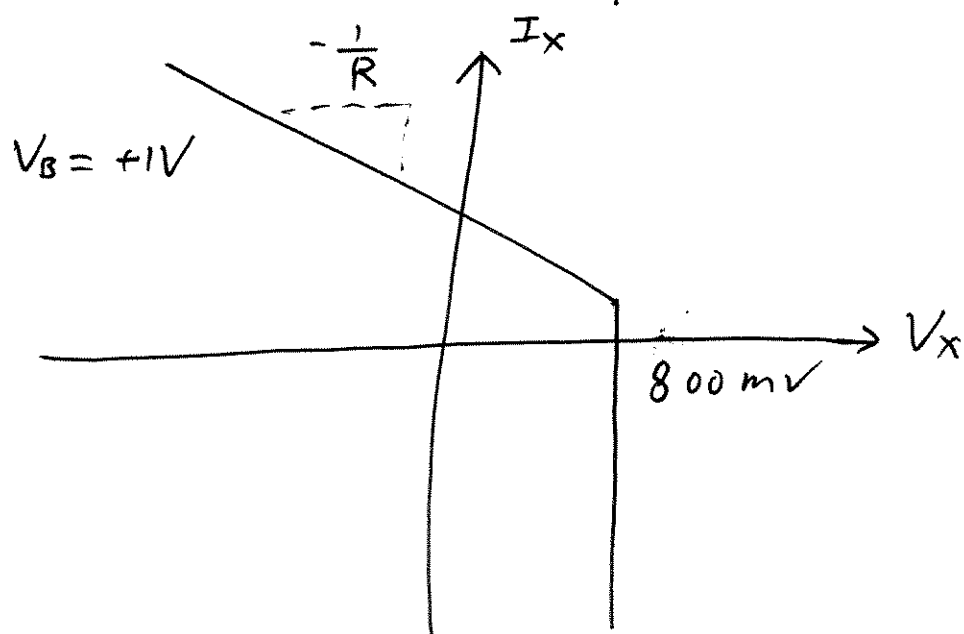
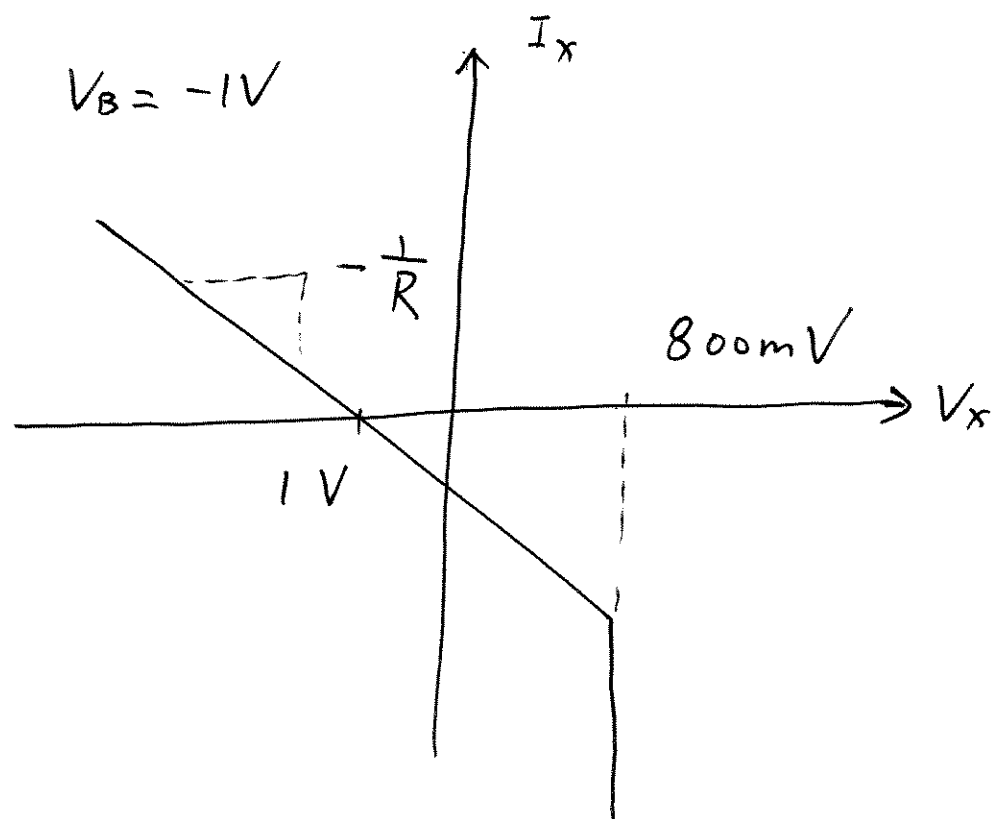


④

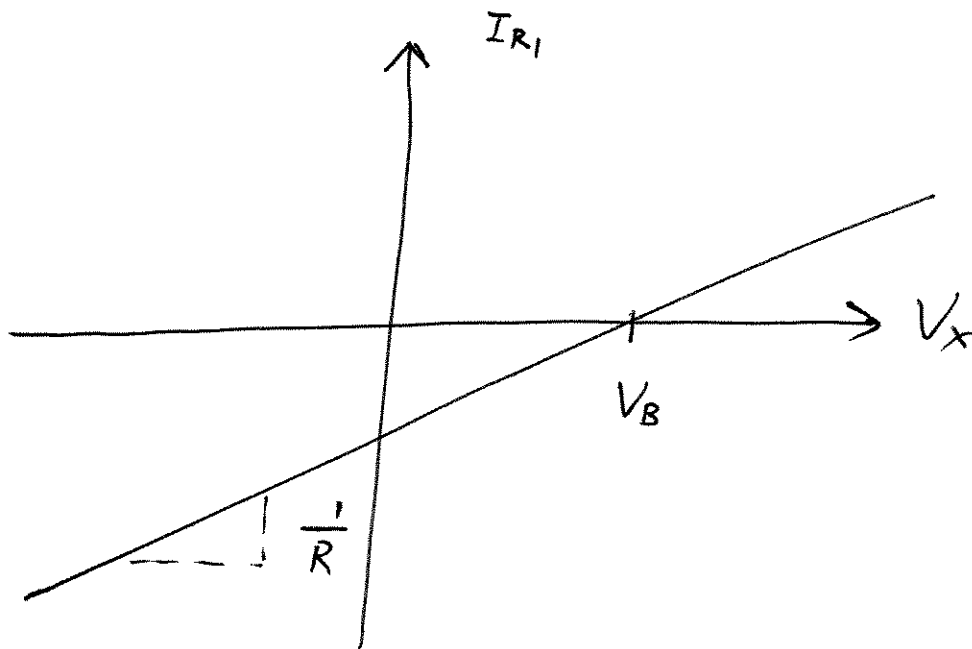
$$V_B = -1V$$



(5)



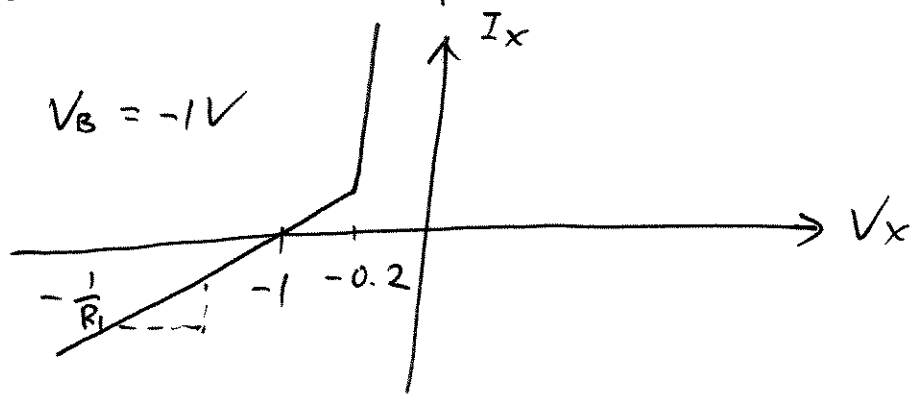
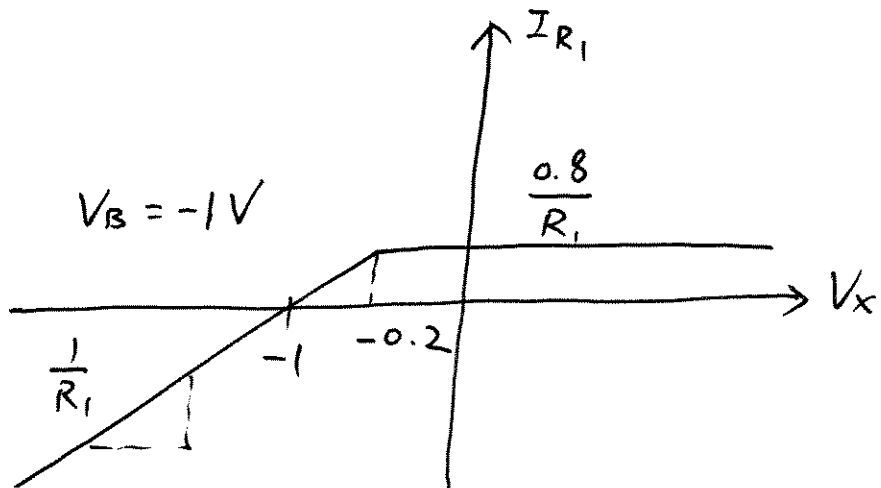
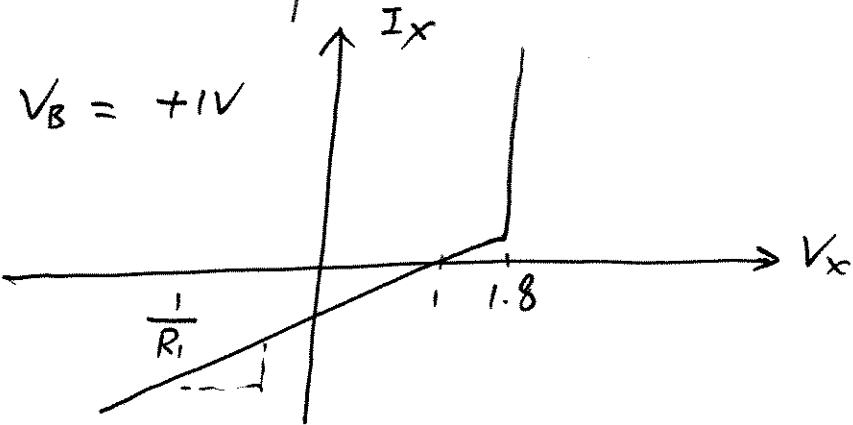
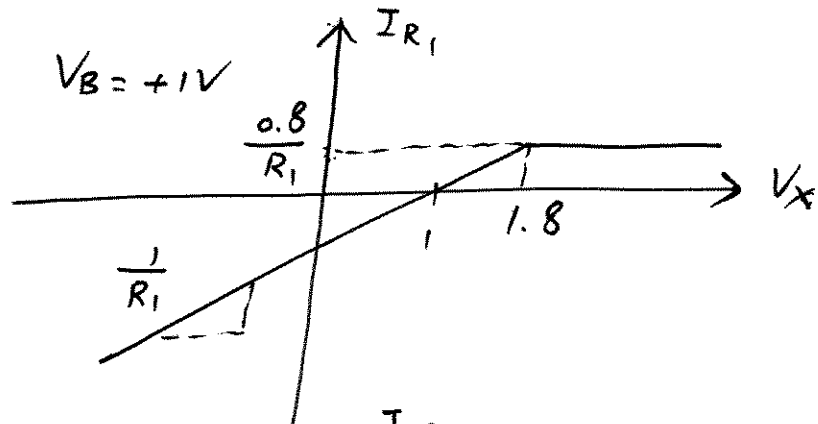
⑥



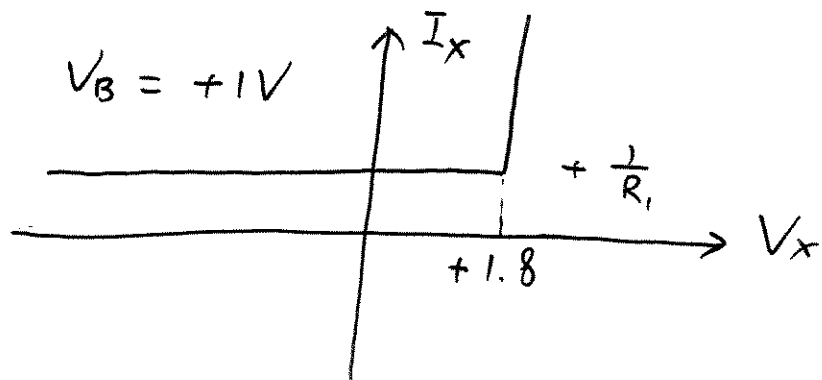
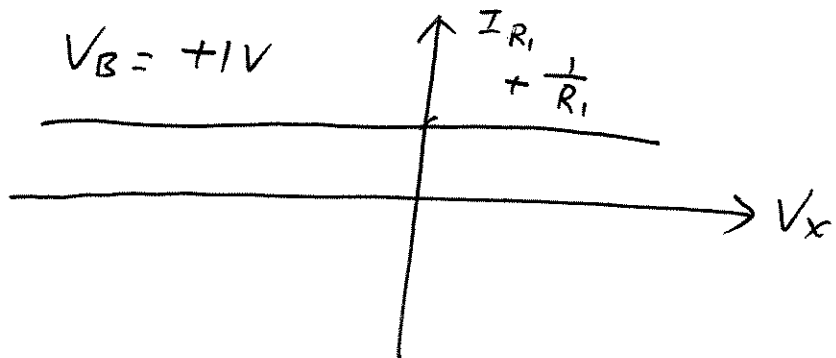
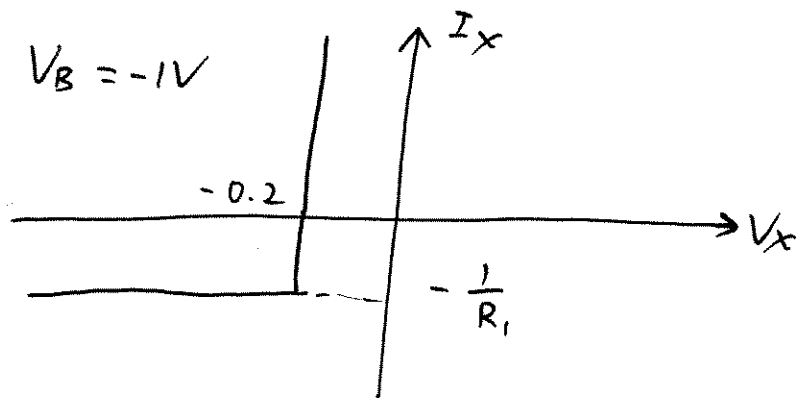
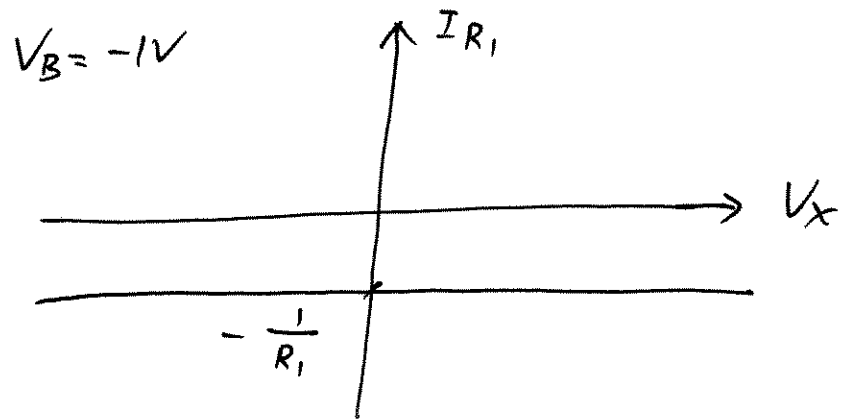
$$I_{D1} = 0 \quad \text{for all } V_x$$

($\because V_B > 0$, D_1 is reverse-biased)

(7)

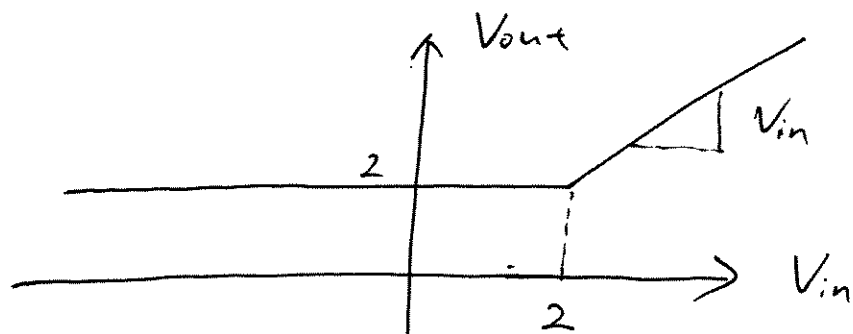


⑧

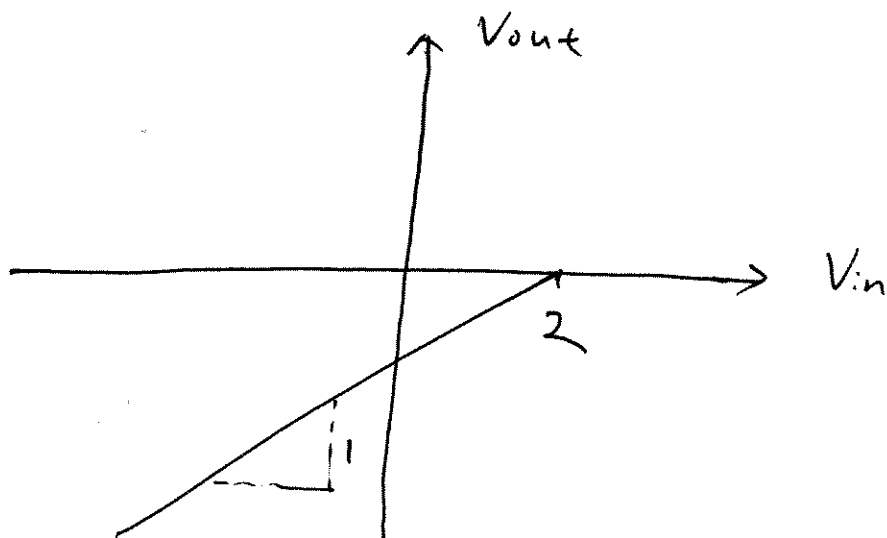


(9)

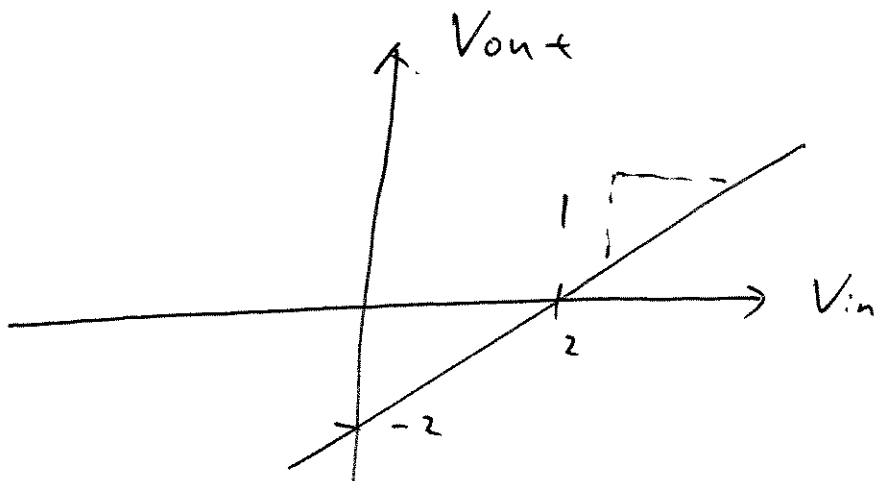
a)



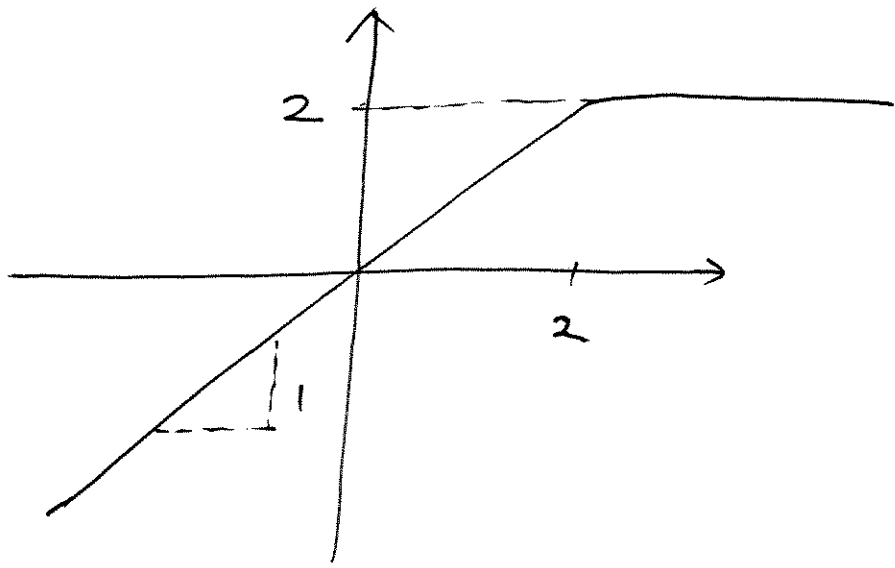
b)



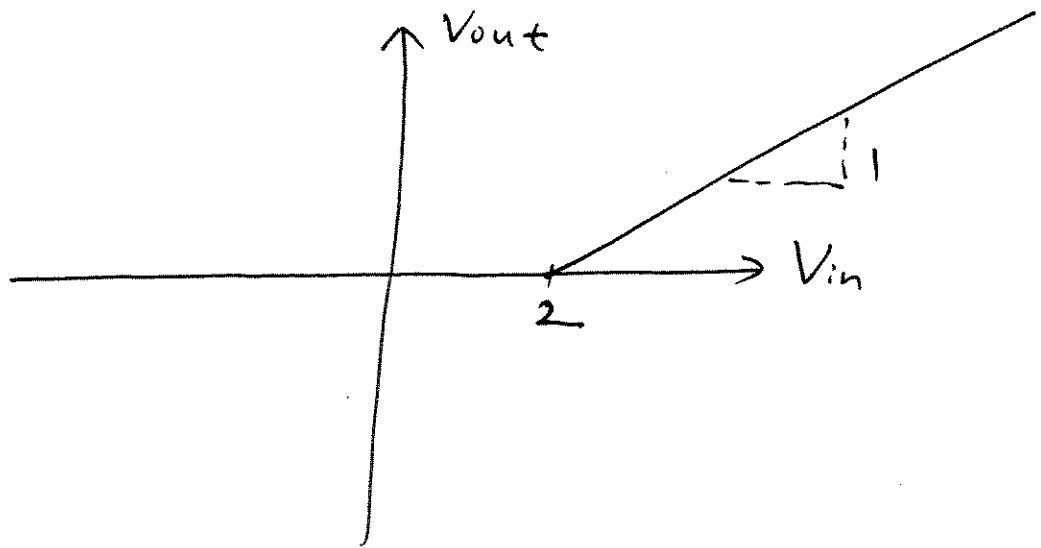
c)



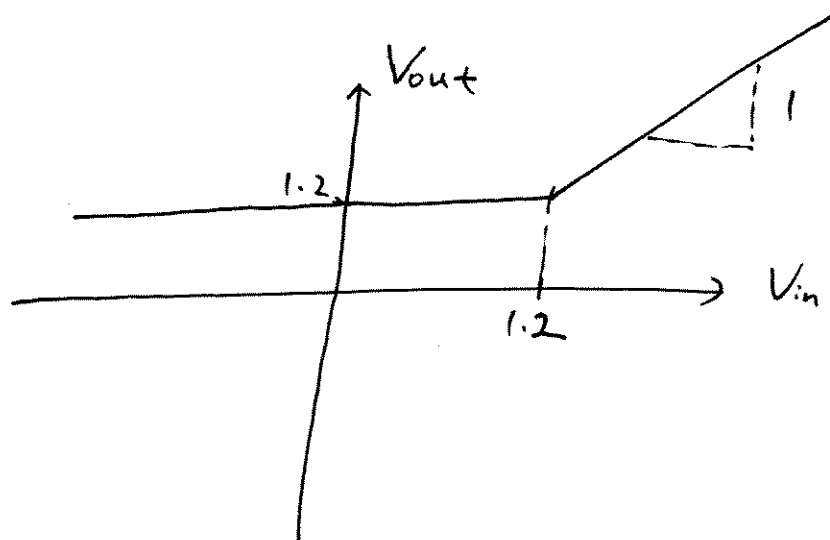
d)



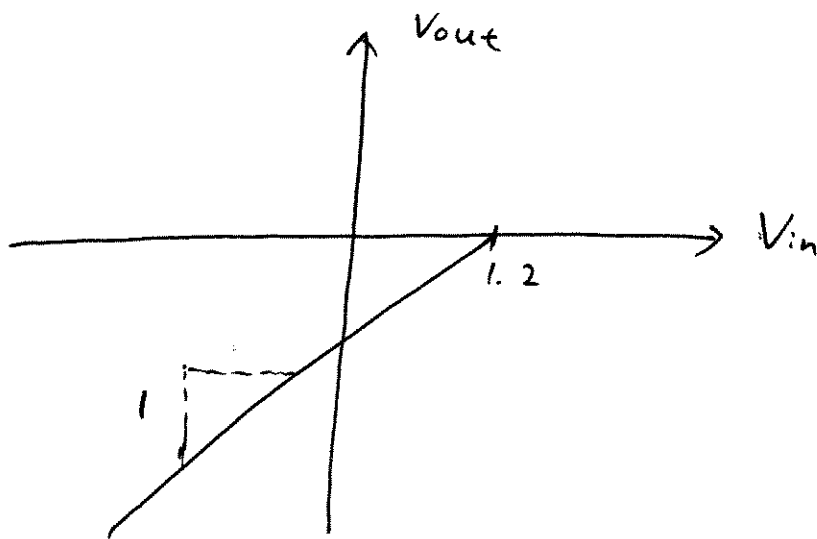
e)



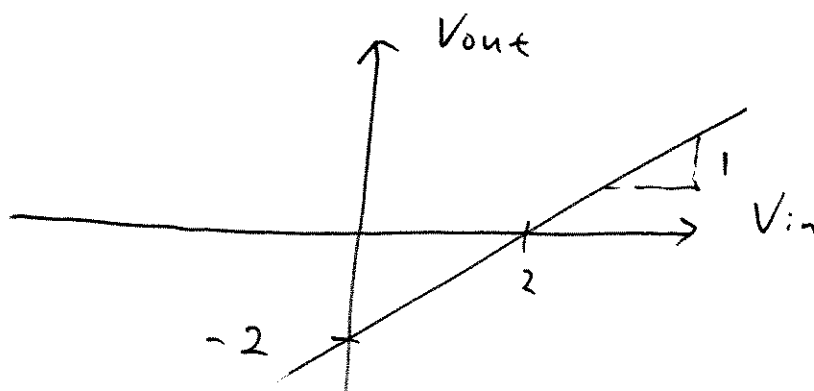
(10) a/



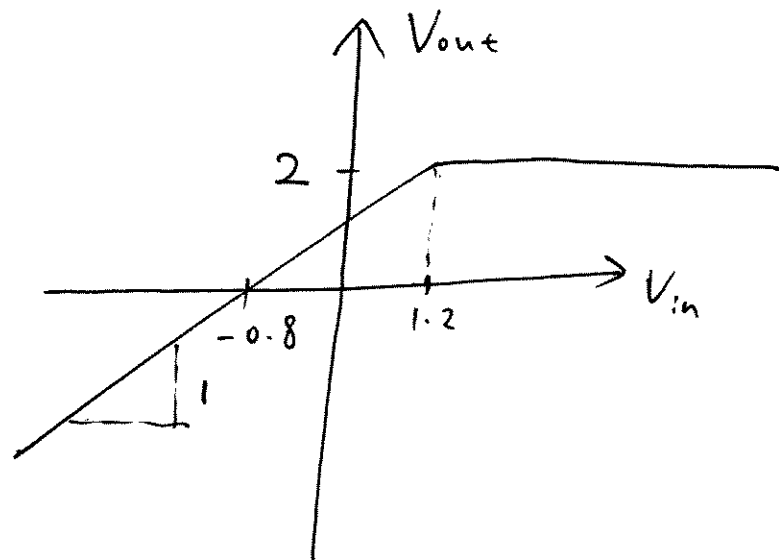
b/



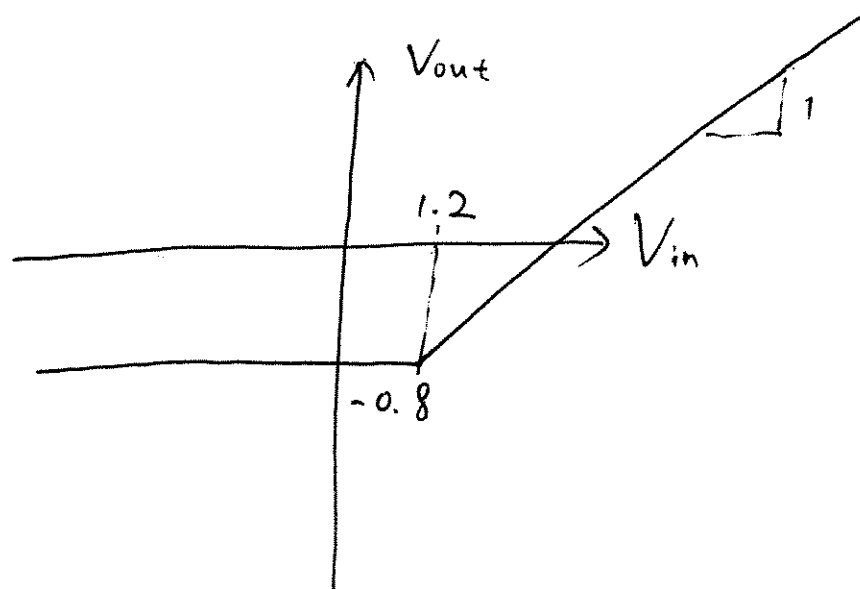
c/



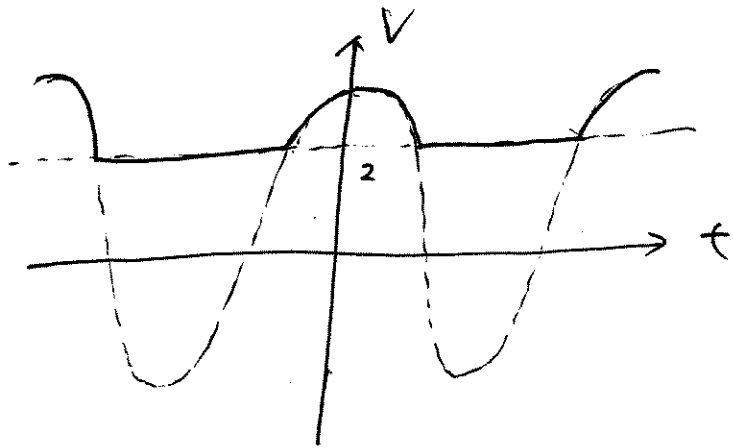
d)



e)

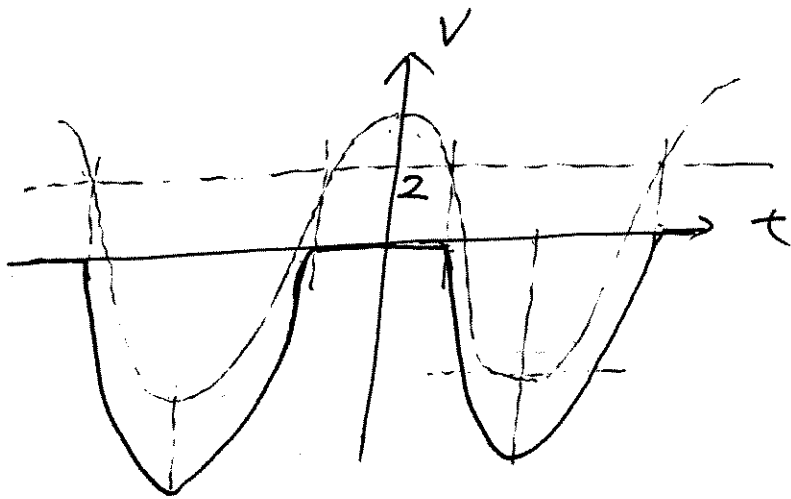


⑪ a)



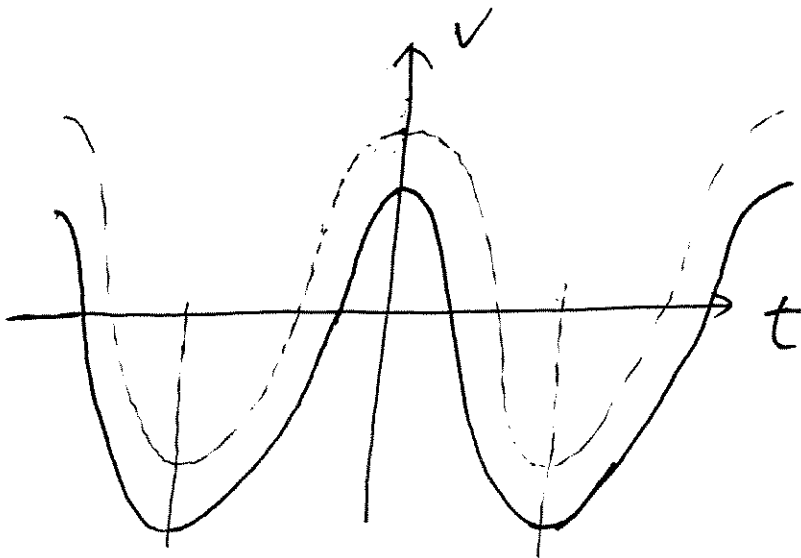
— V_{out}
--- V_{in}

b)



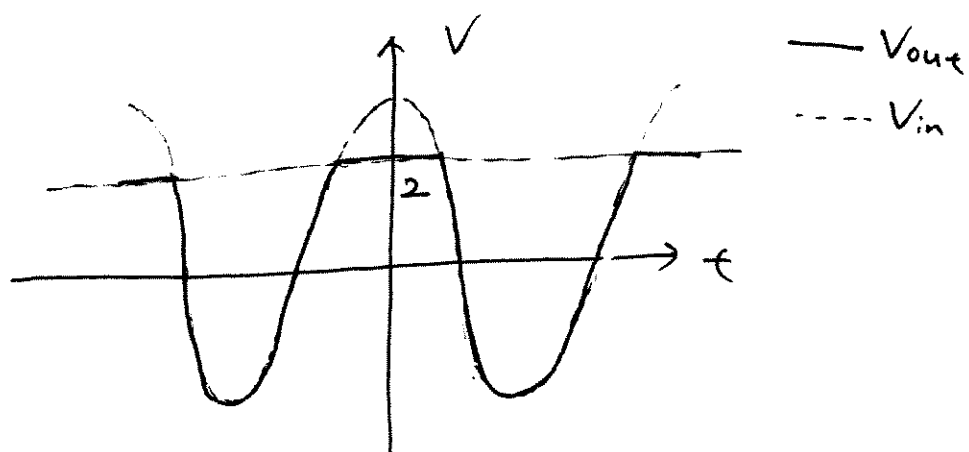
— V_{out}
--- V_{in}

c)

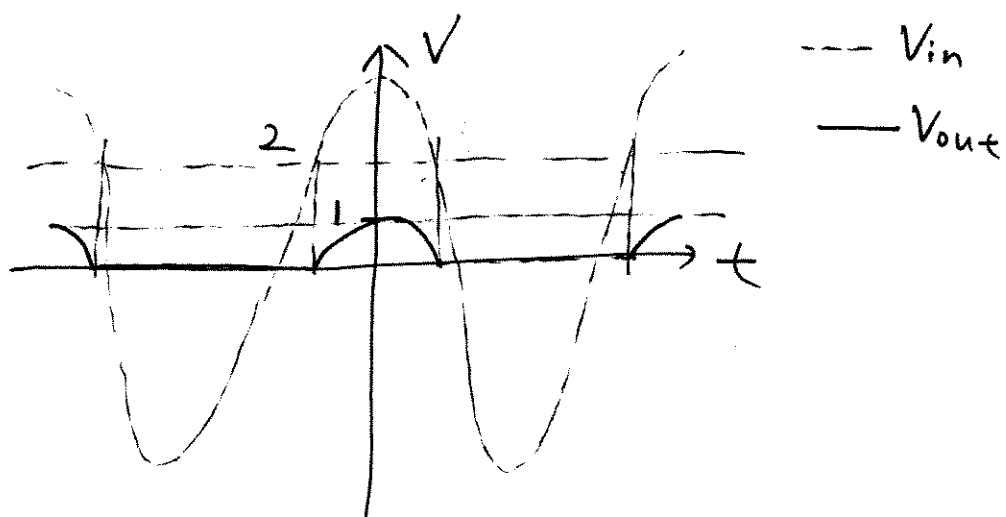


— V_{out}
--- V_{in}

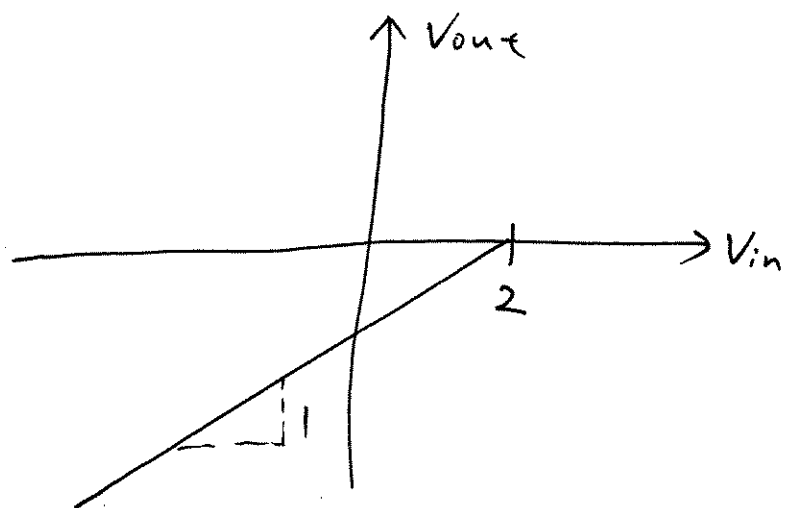
d)



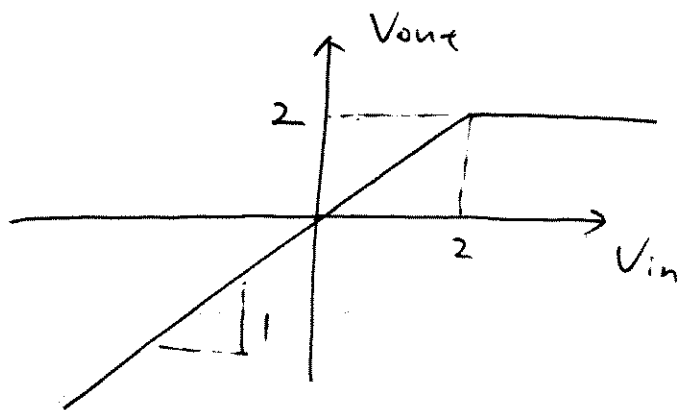
e)



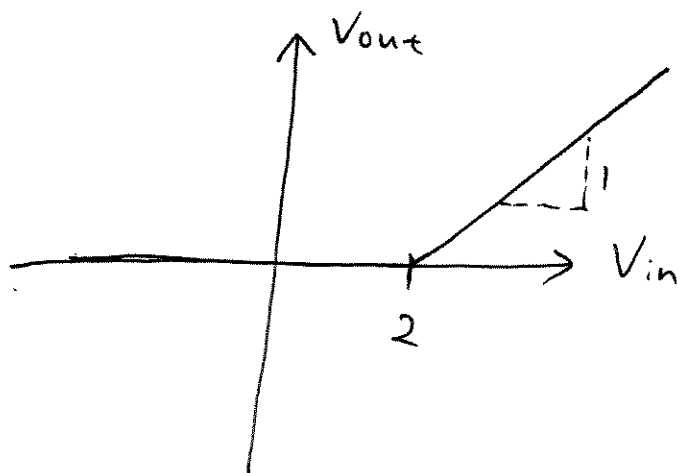
⑫ a)



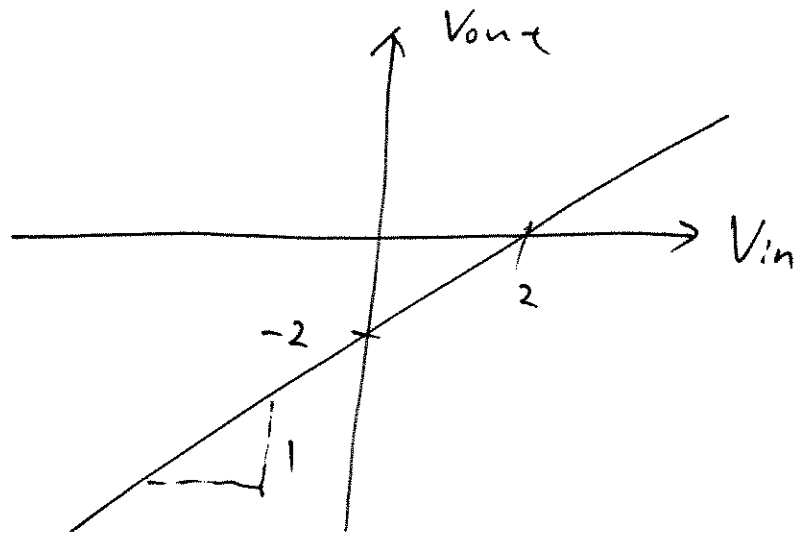
b)



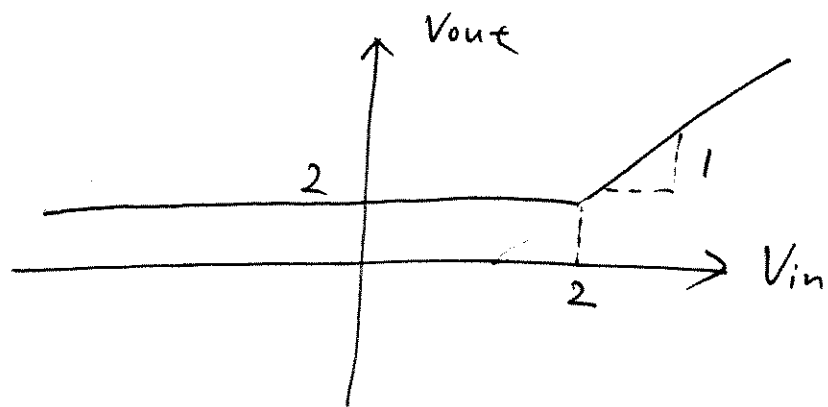
c)



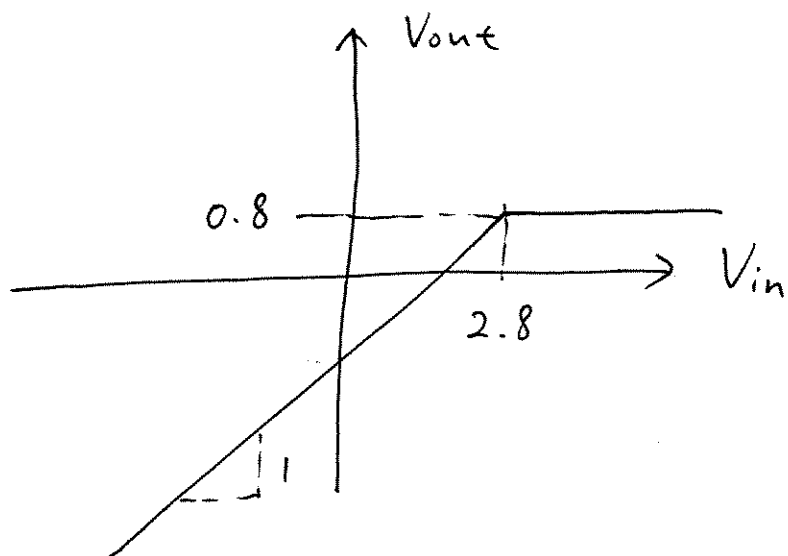
d)



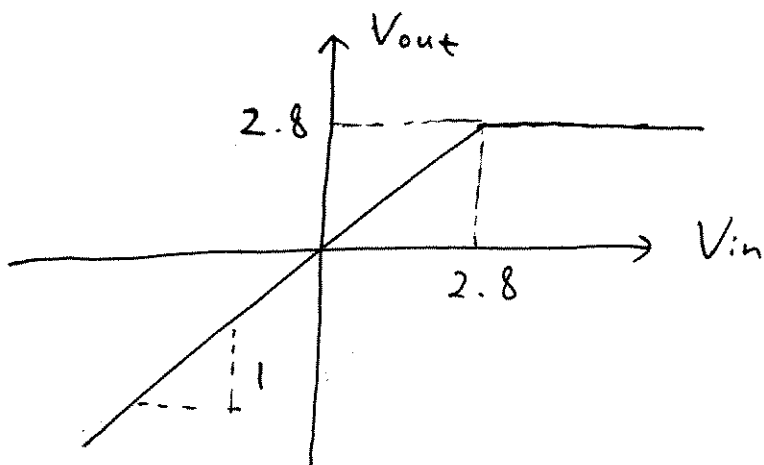
e)



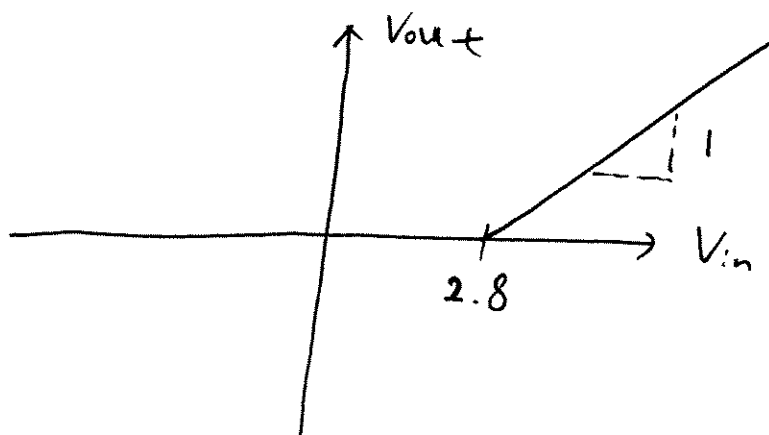
⑬ a/



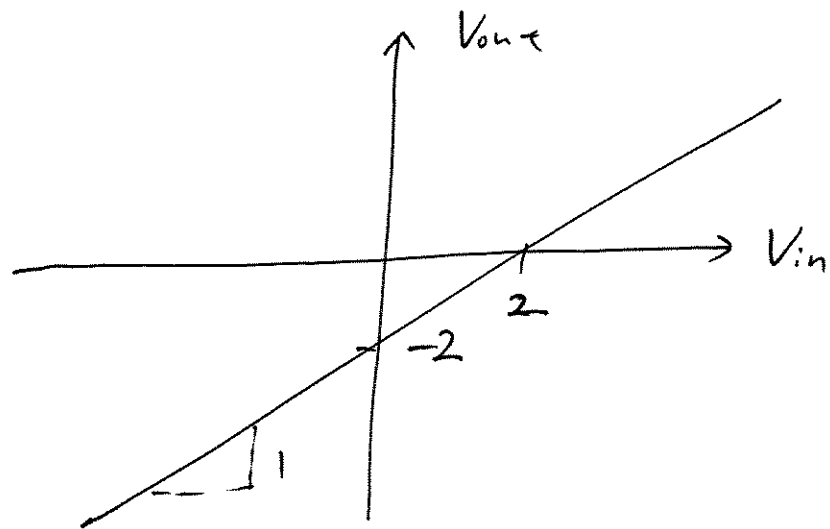
b/



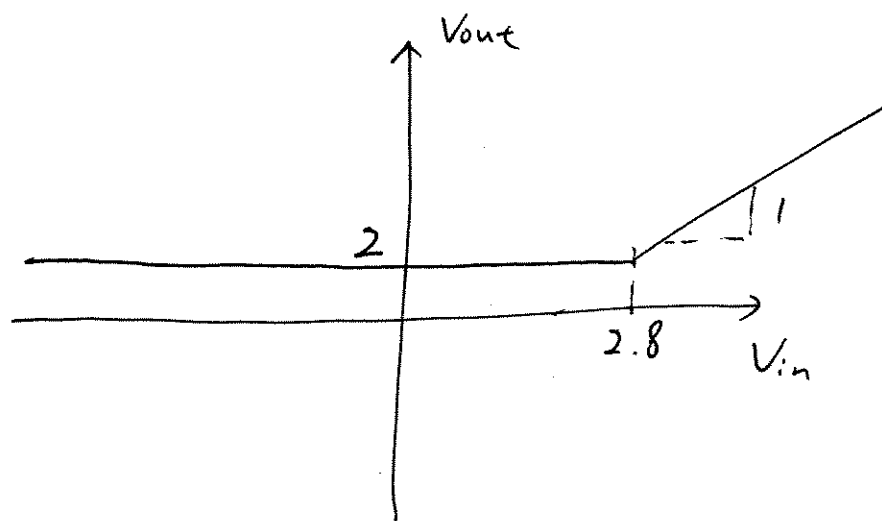
c/



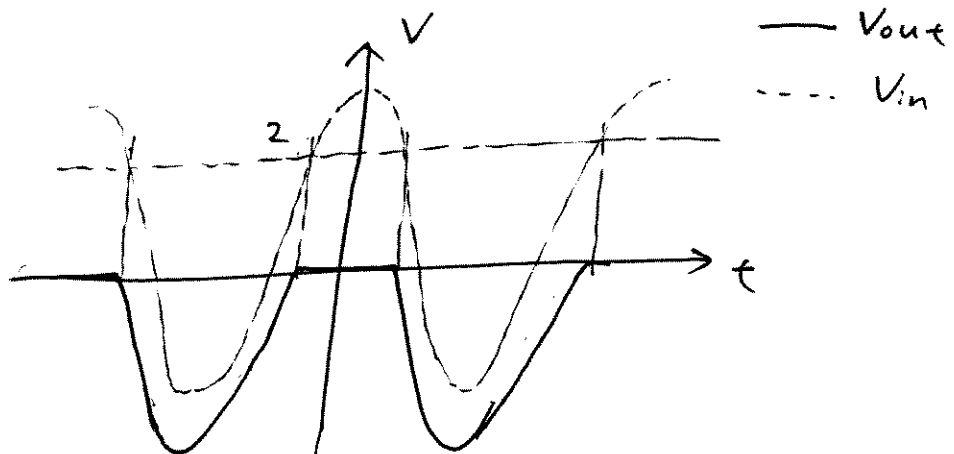
d/



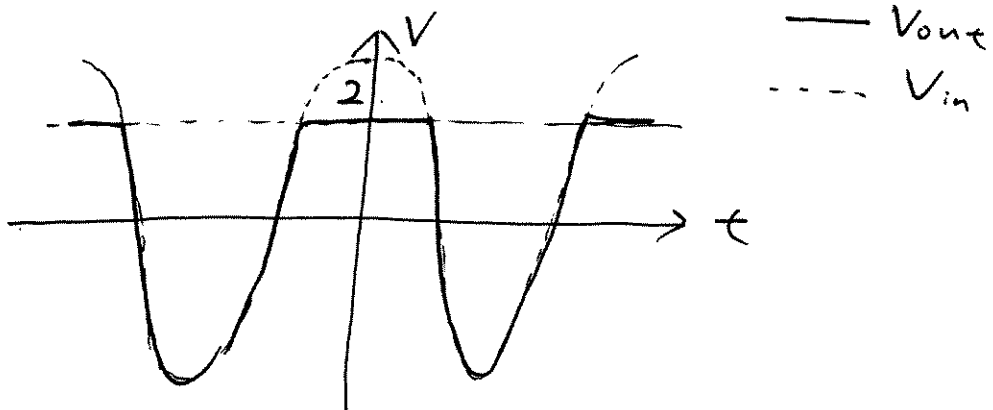
e/



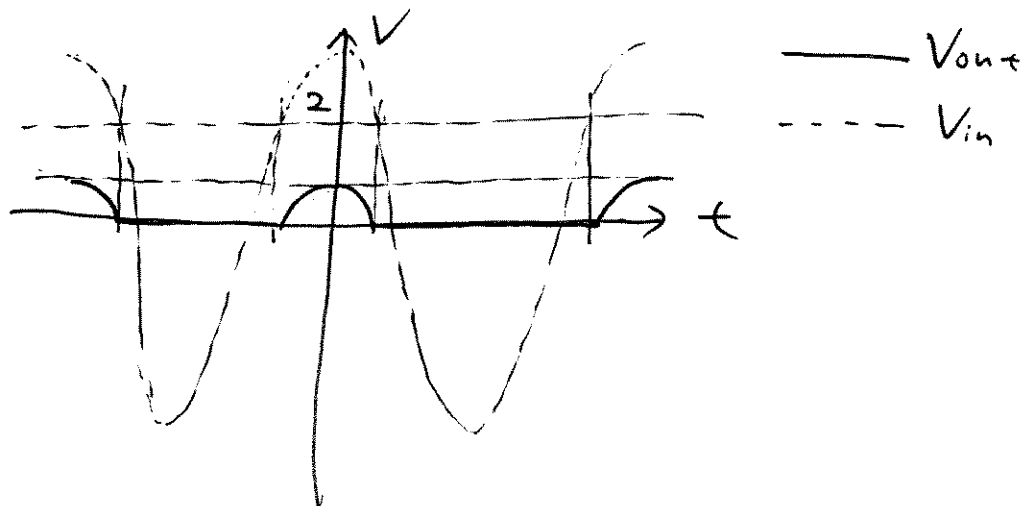
⑭ a)



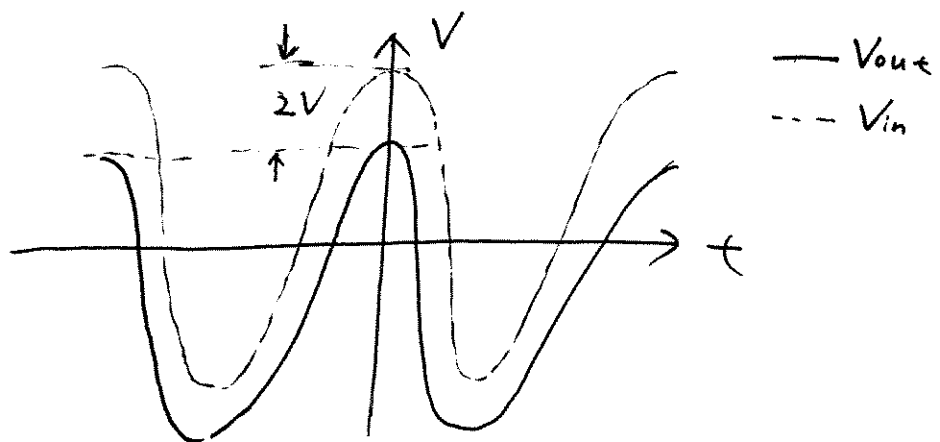
b)



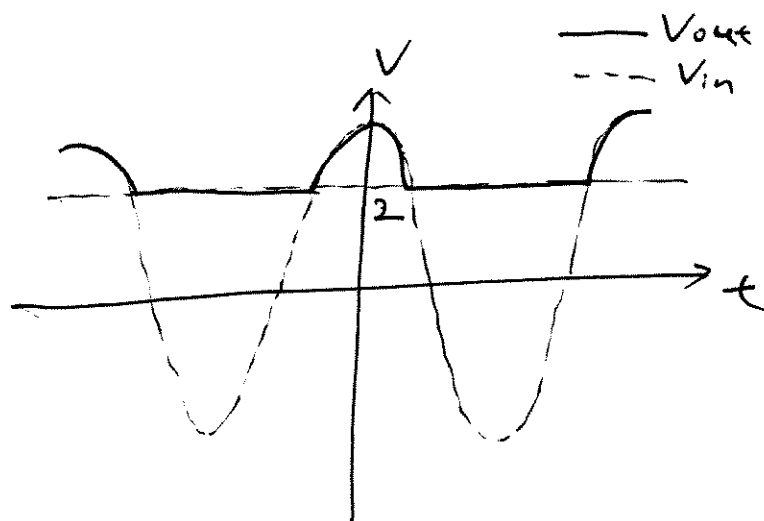
c)



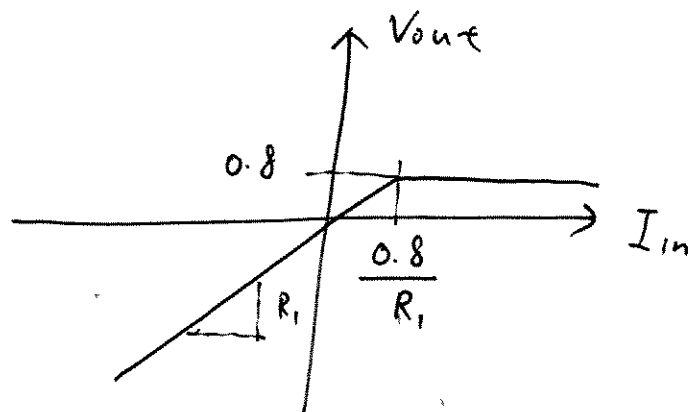
d)



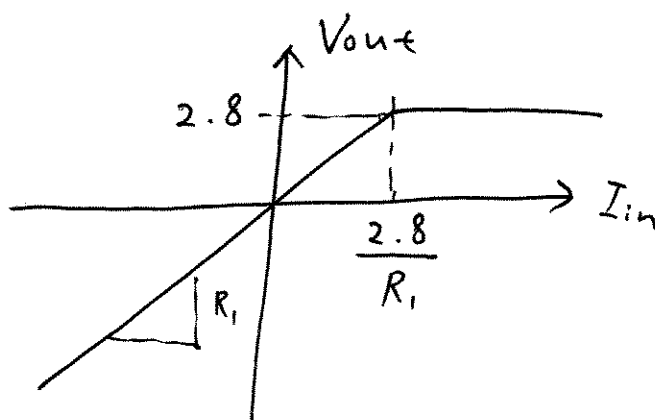
e)



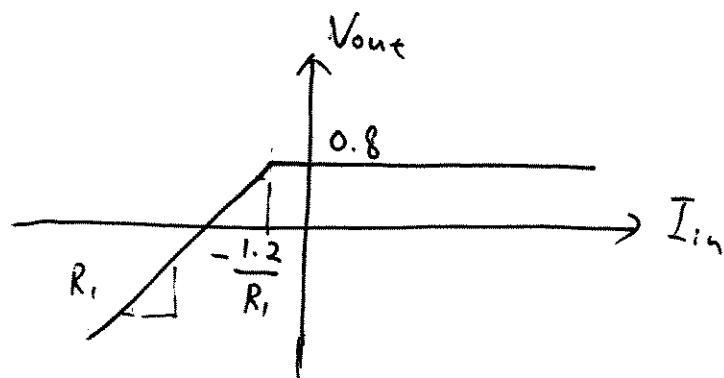
(15) a)



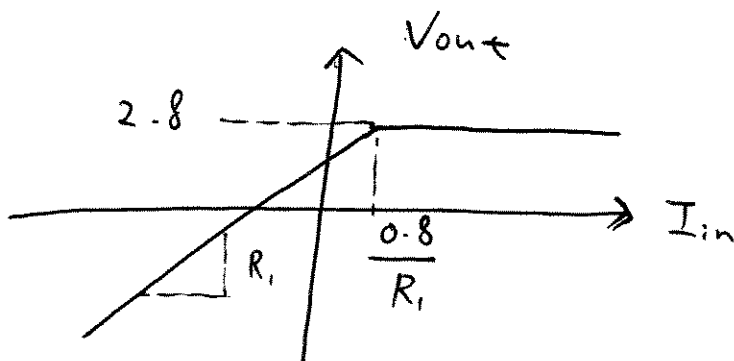
b)



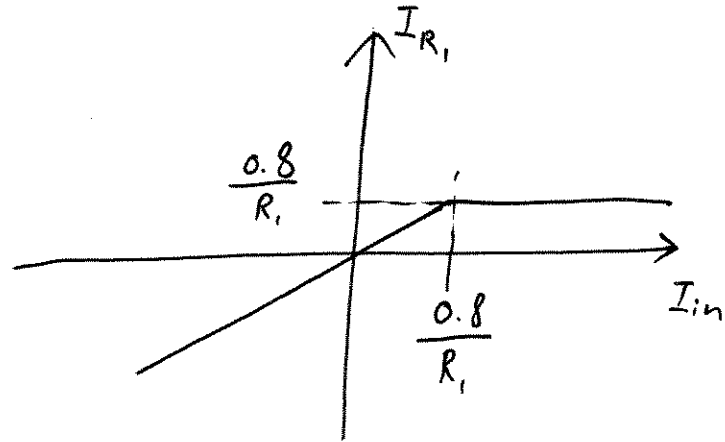
c)



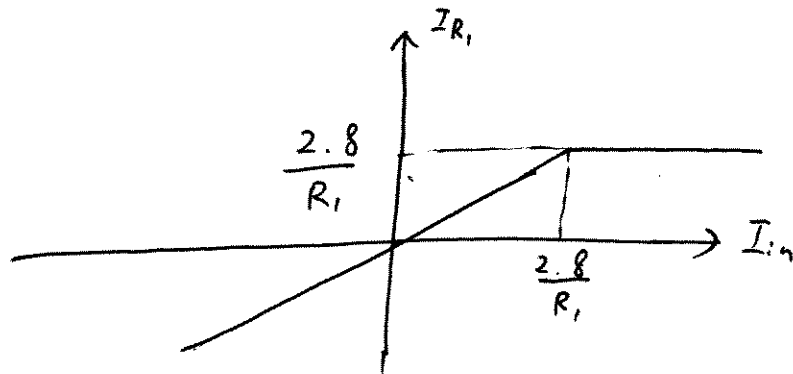
d)



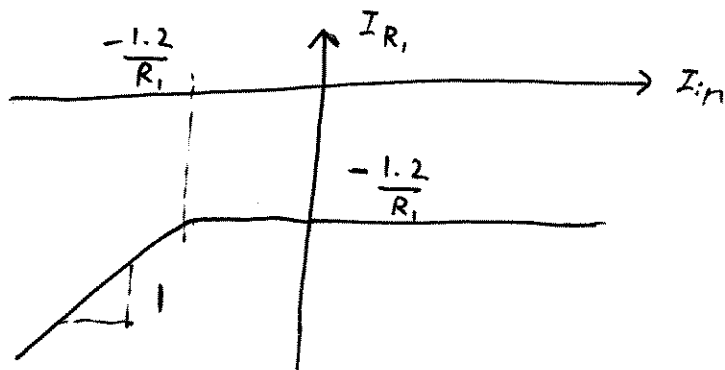
①6 a/



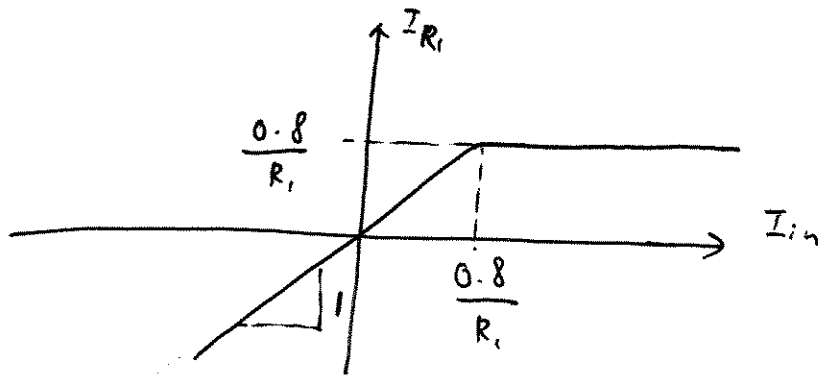
b/



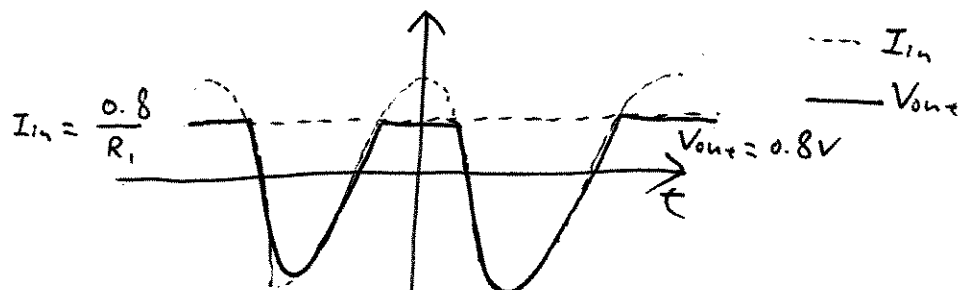
c/



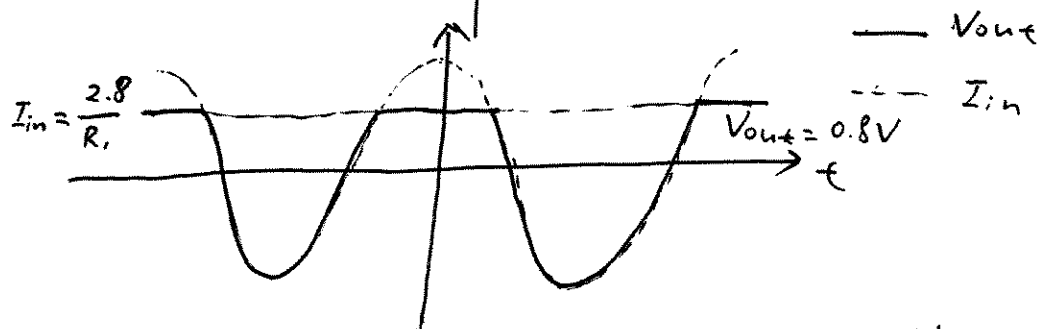
d/



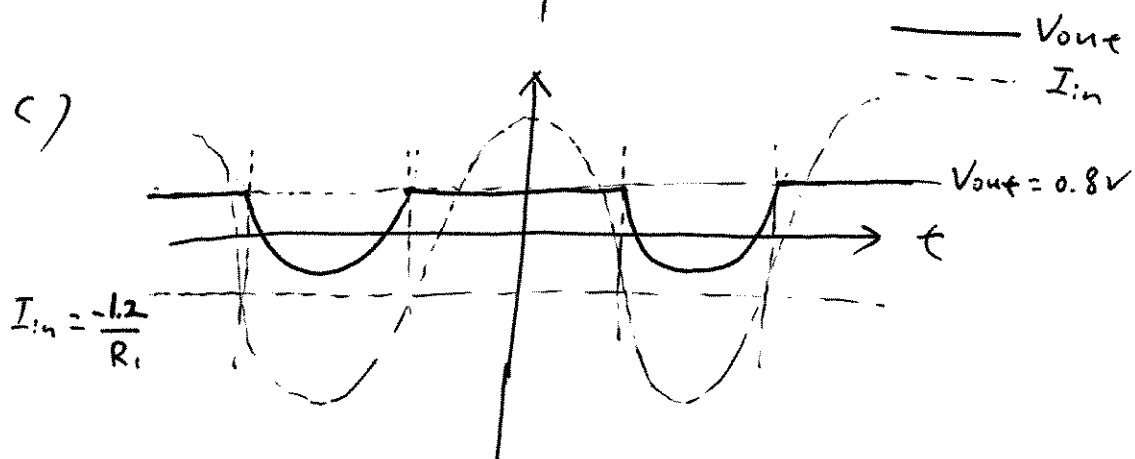
17) a)



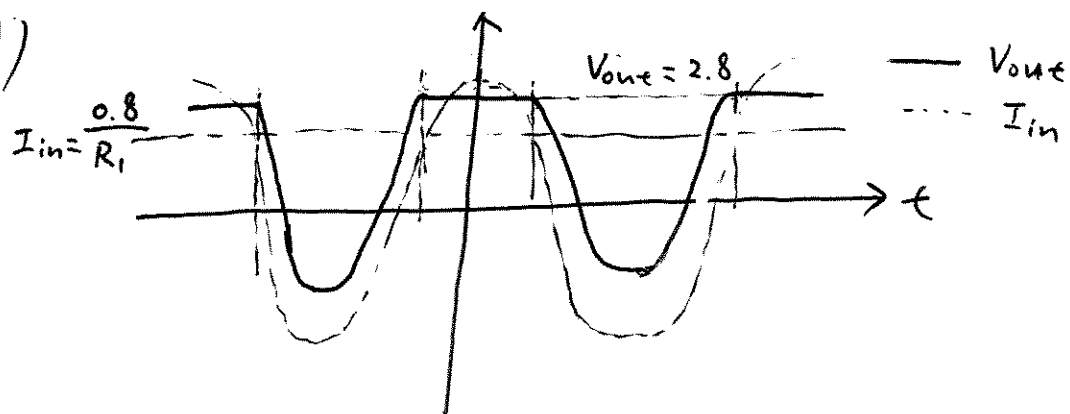
b)



c)

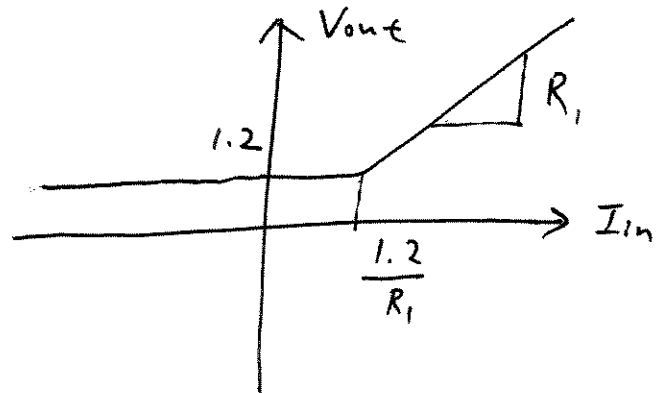


d)

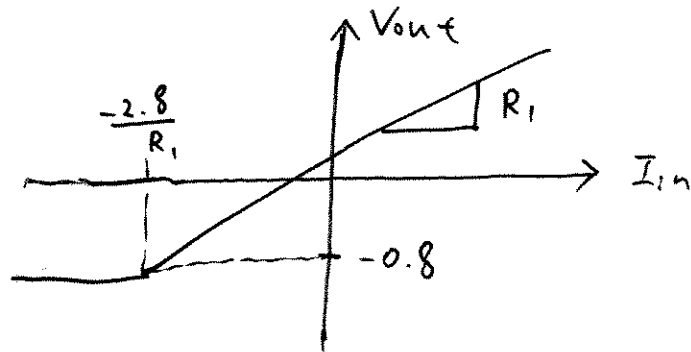


18

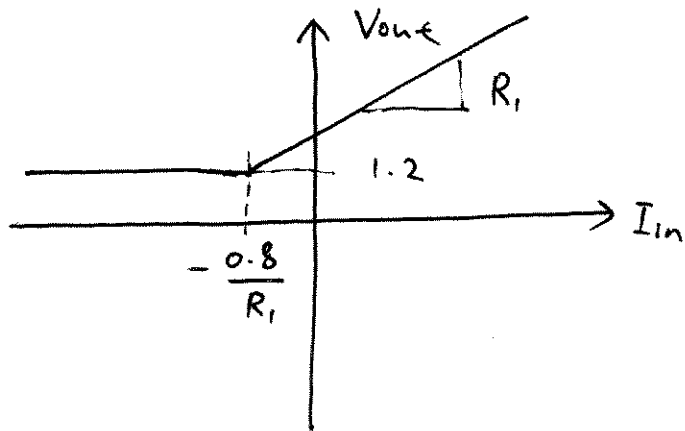
a)



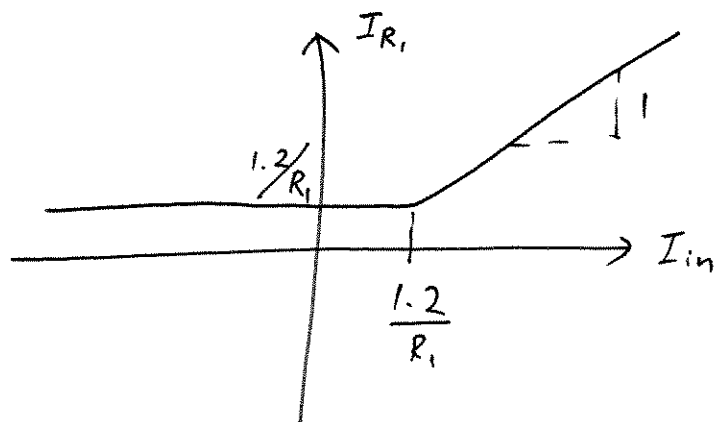
b)



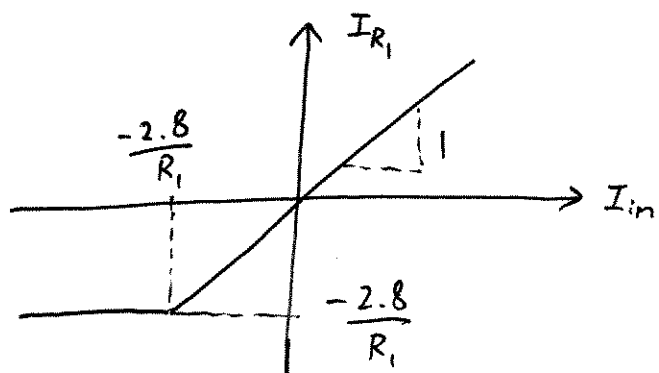
c)



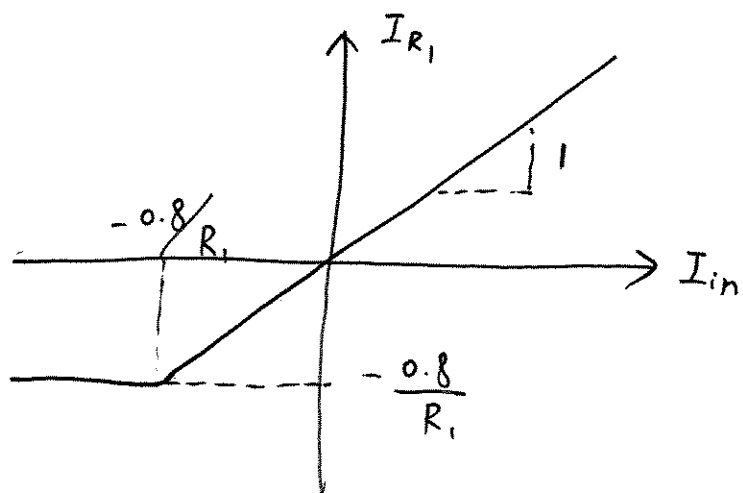
(19) a)



b)

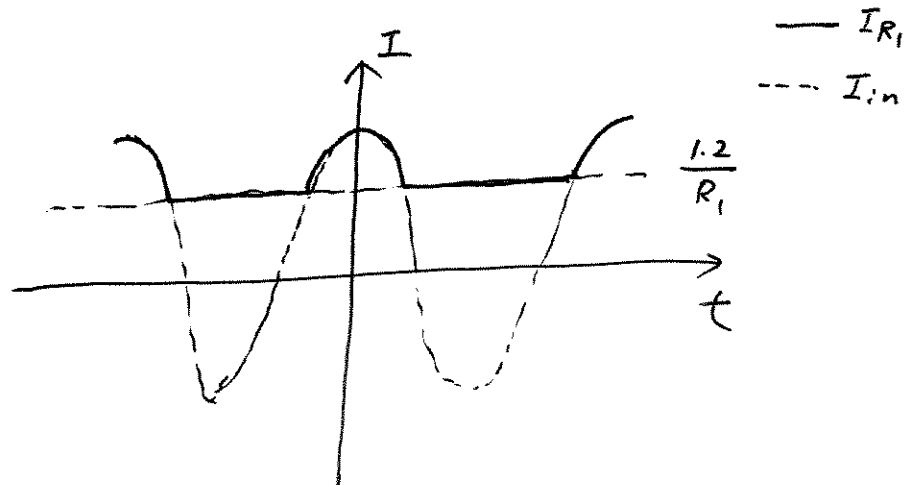


c)

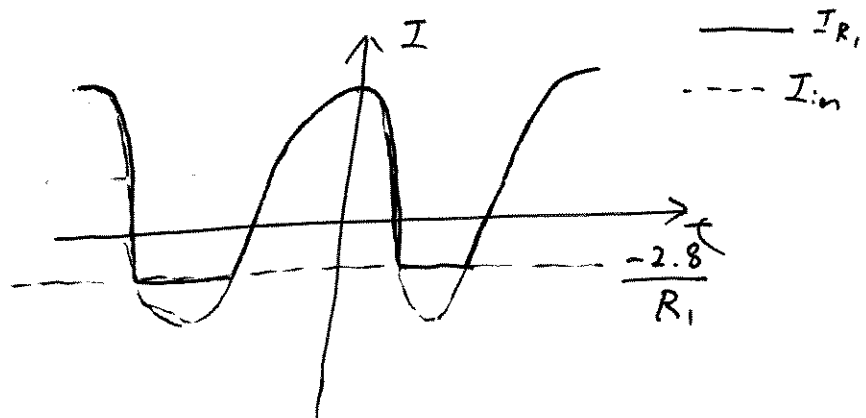


20

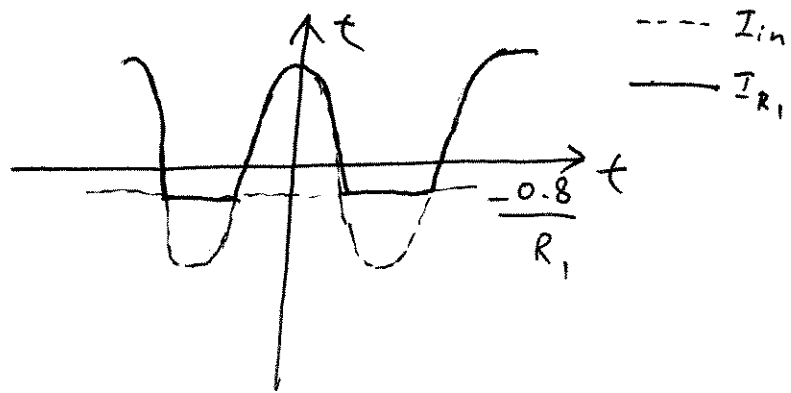
a/



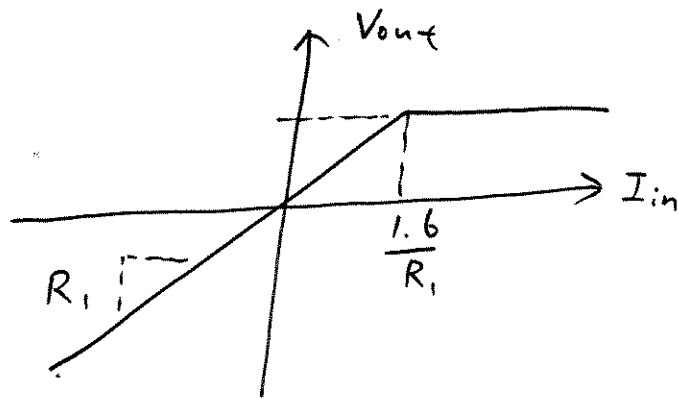
b/



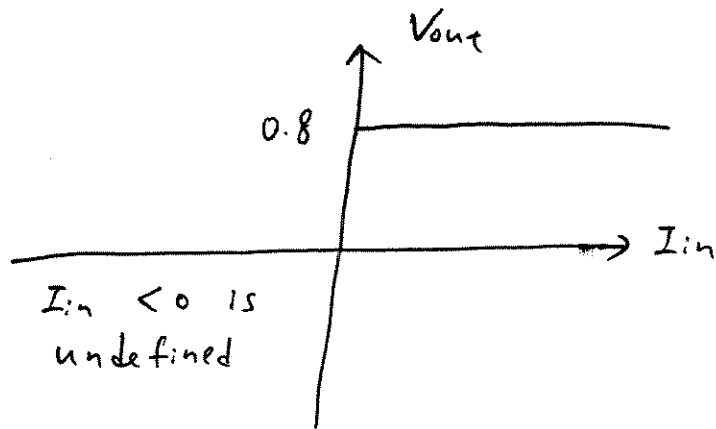
c/



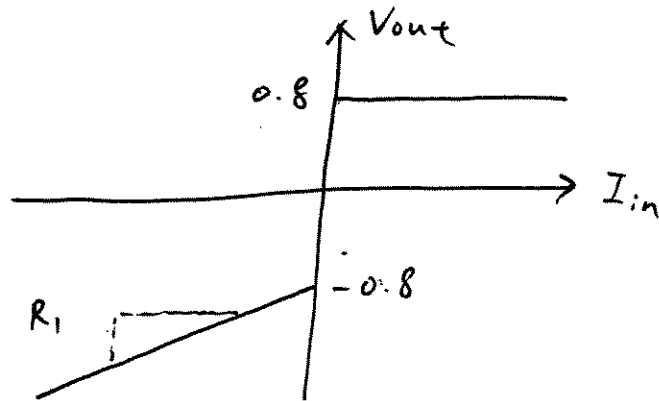
(21) a/



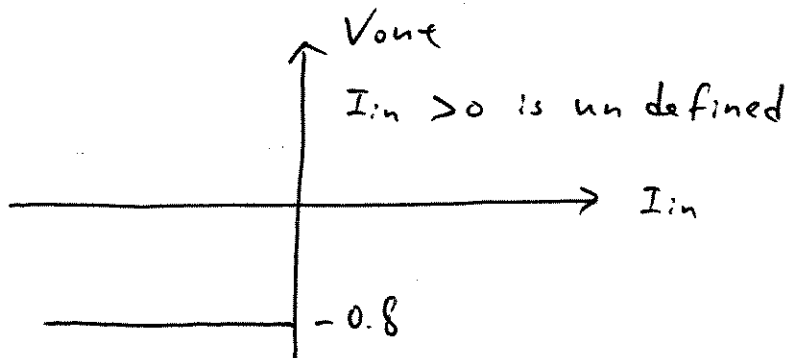
b/



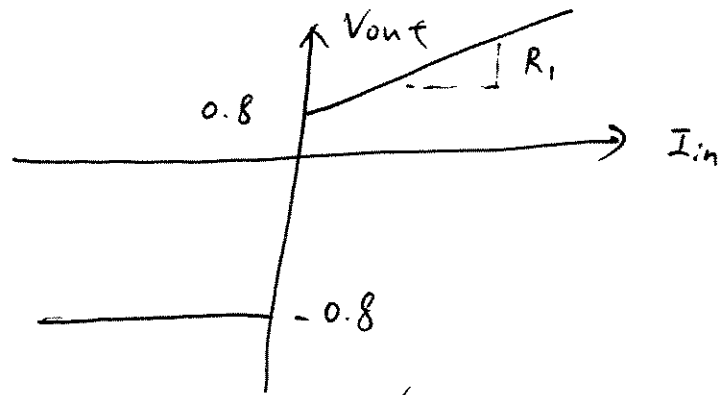
c/



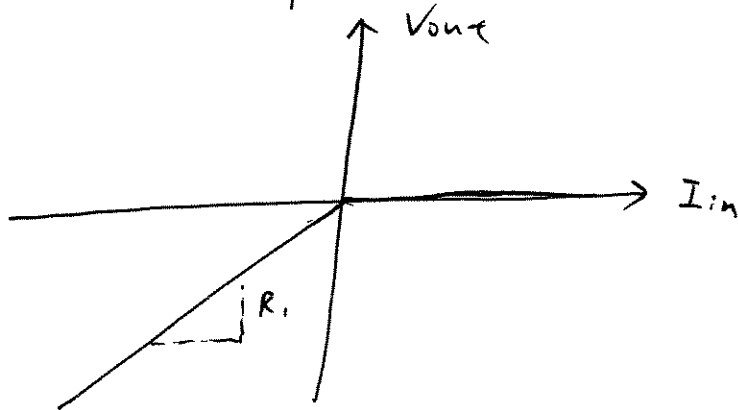
d/



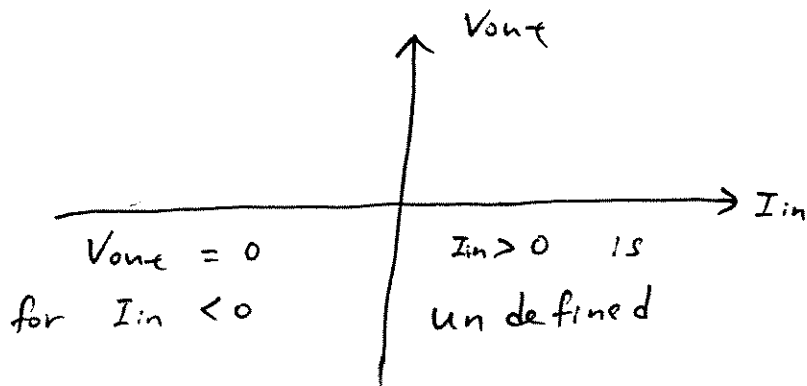
e)



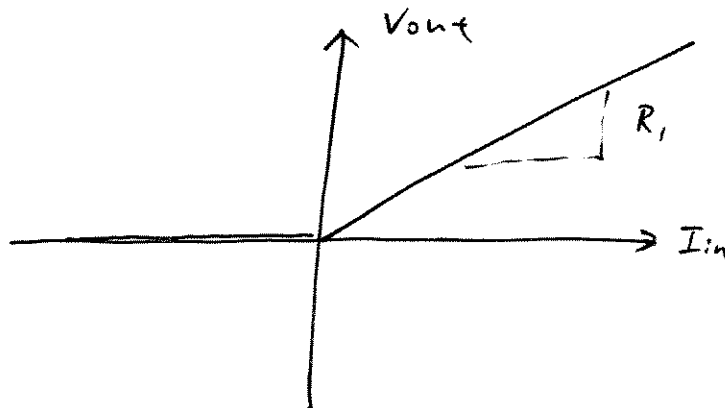
f)



g)

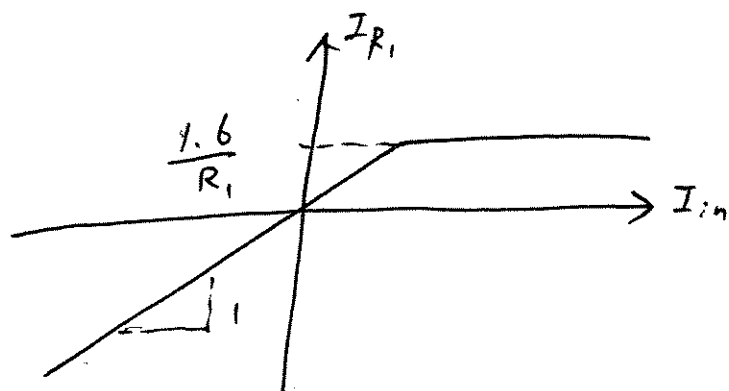


h)

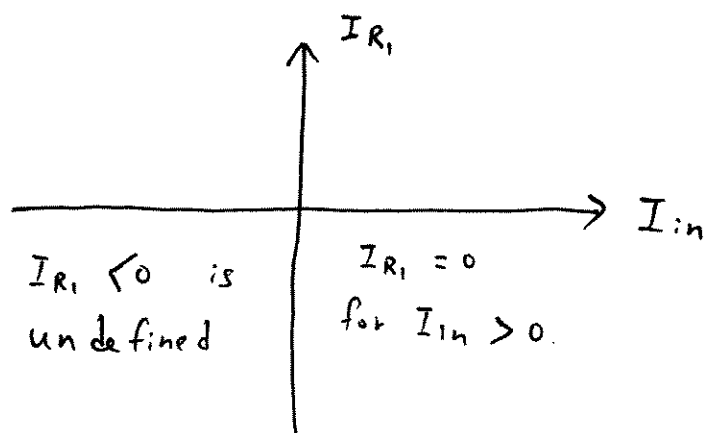


22

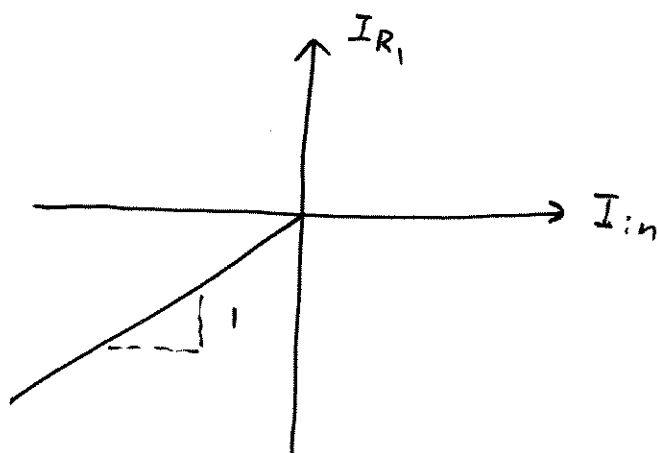
a)



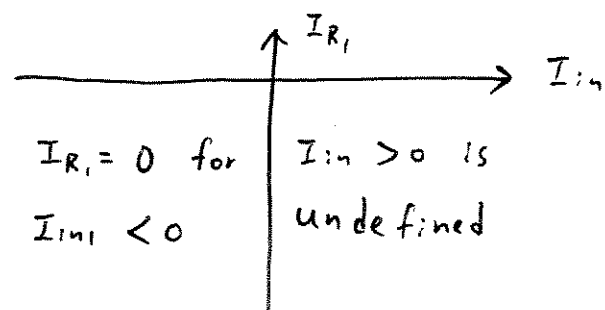
b)



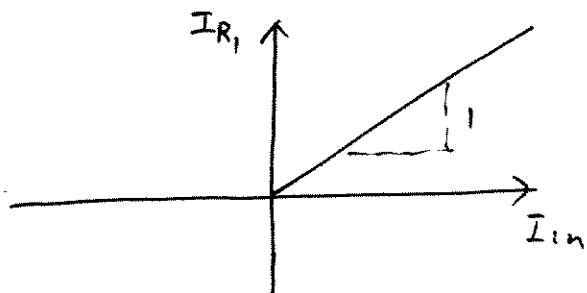
c)



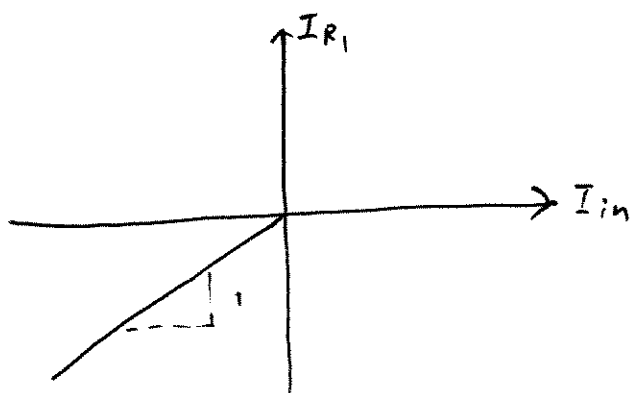
d)



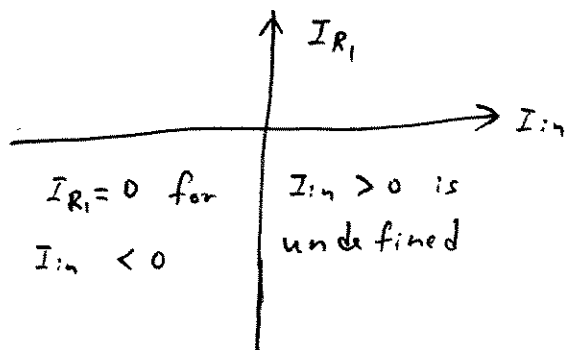
e)



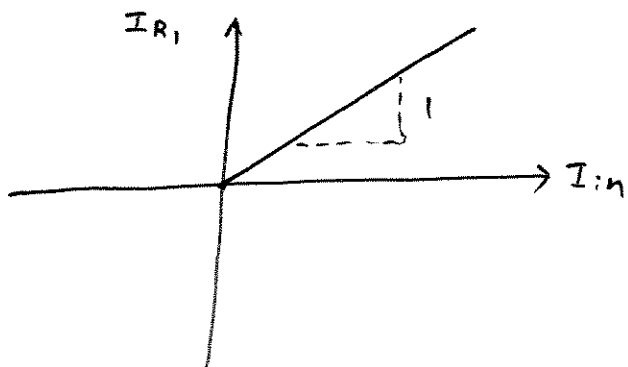
f)



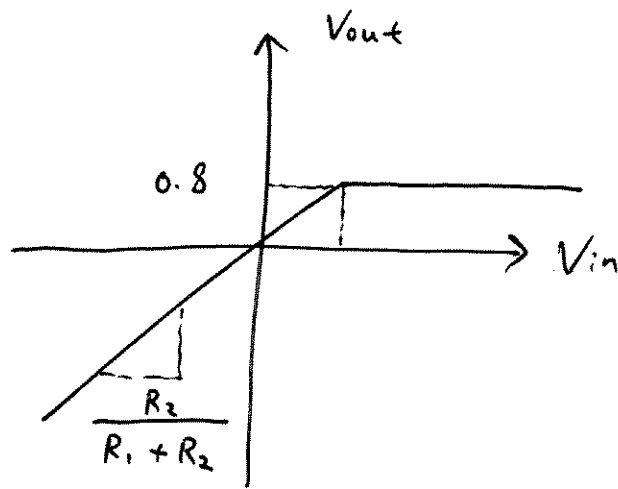
g)



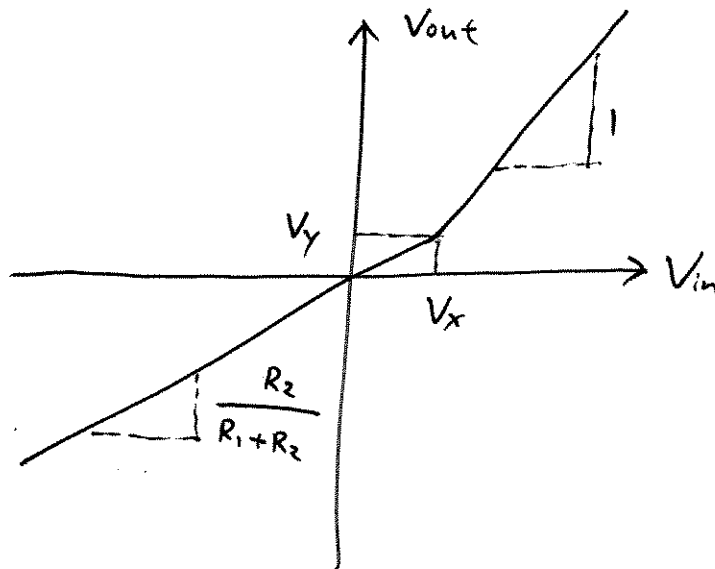
h)



23) a)



b)



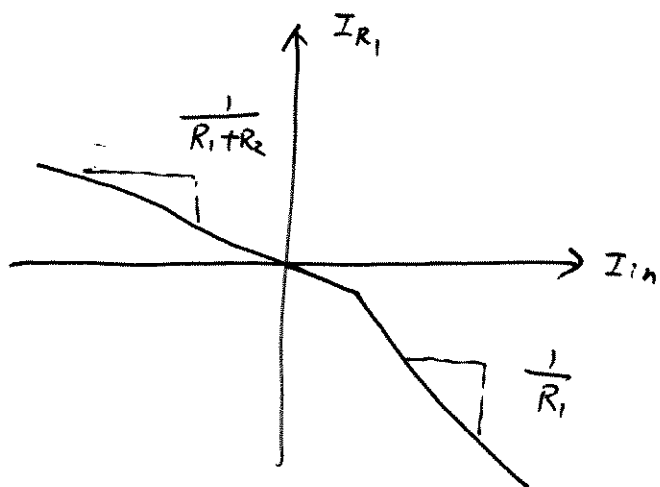
Note: at the turning point when D_1 starts to conduct, V_x, V_y need to satisfy 2 conditions:

$$V_x - V_y = 0.8 \quad \text{--- (1)}$$

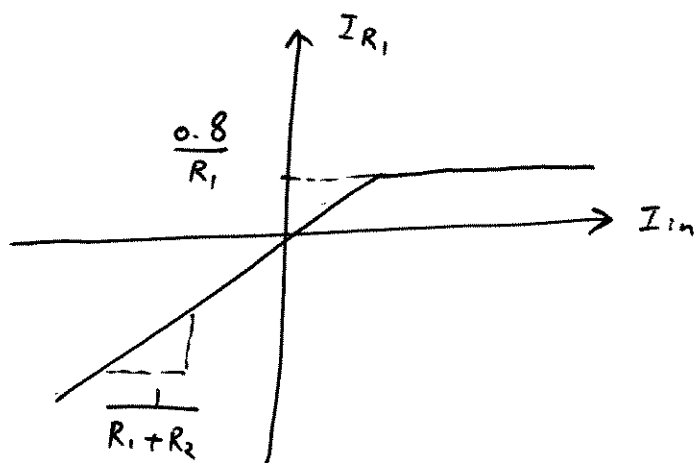
$$V_y = \frac{R_2}{R_1 + R_2} V_x \quad \text{--- (2)}$$

24

a)

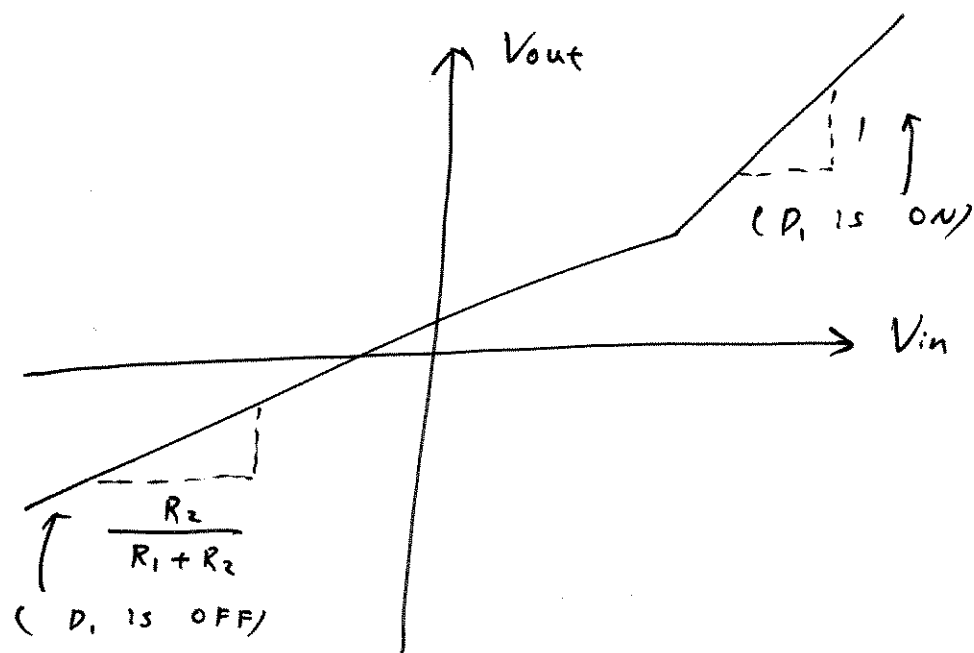


b)

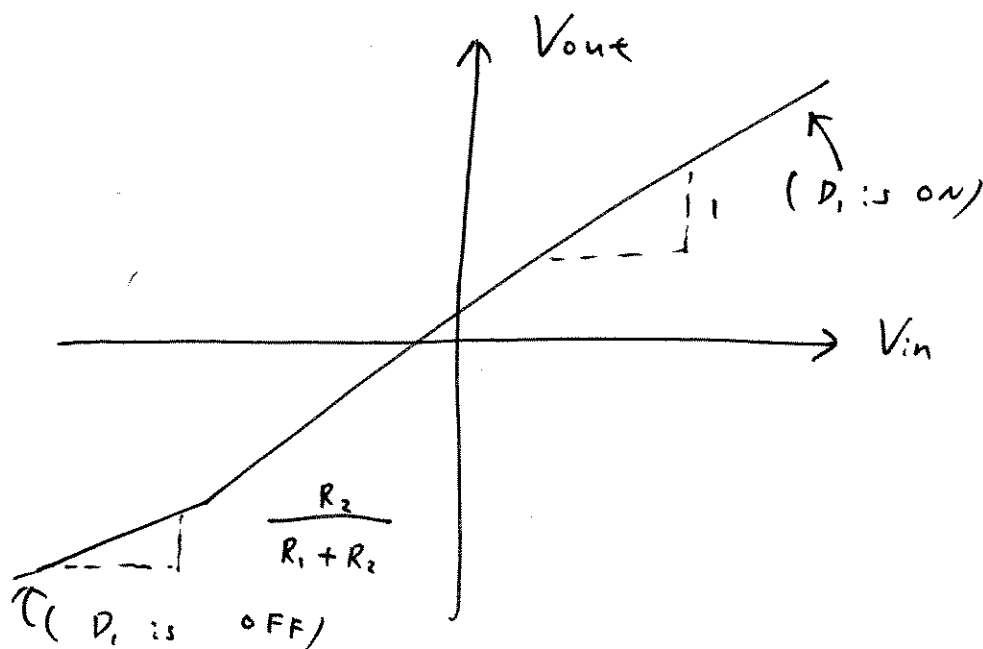


25

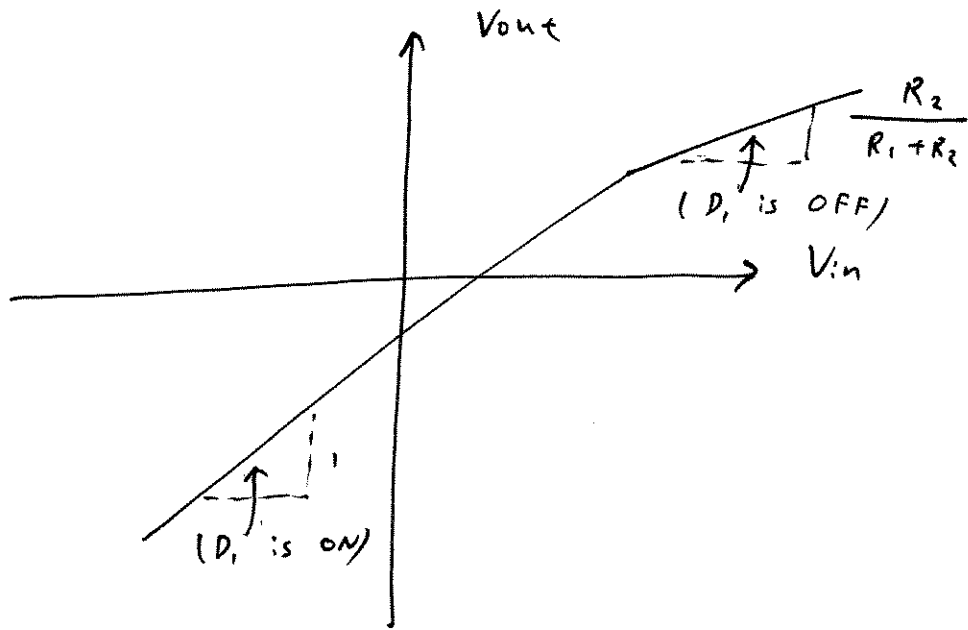
a)



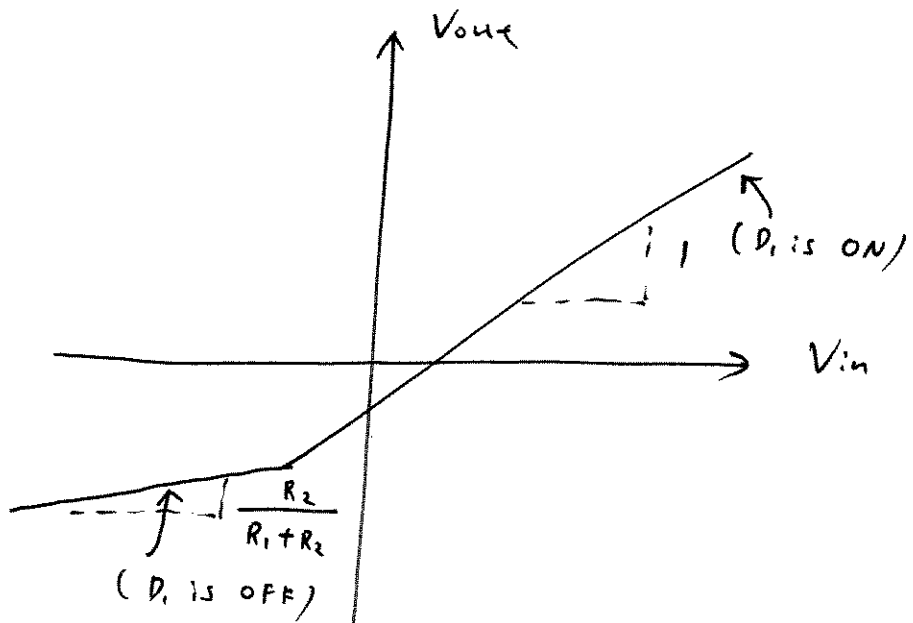
b)



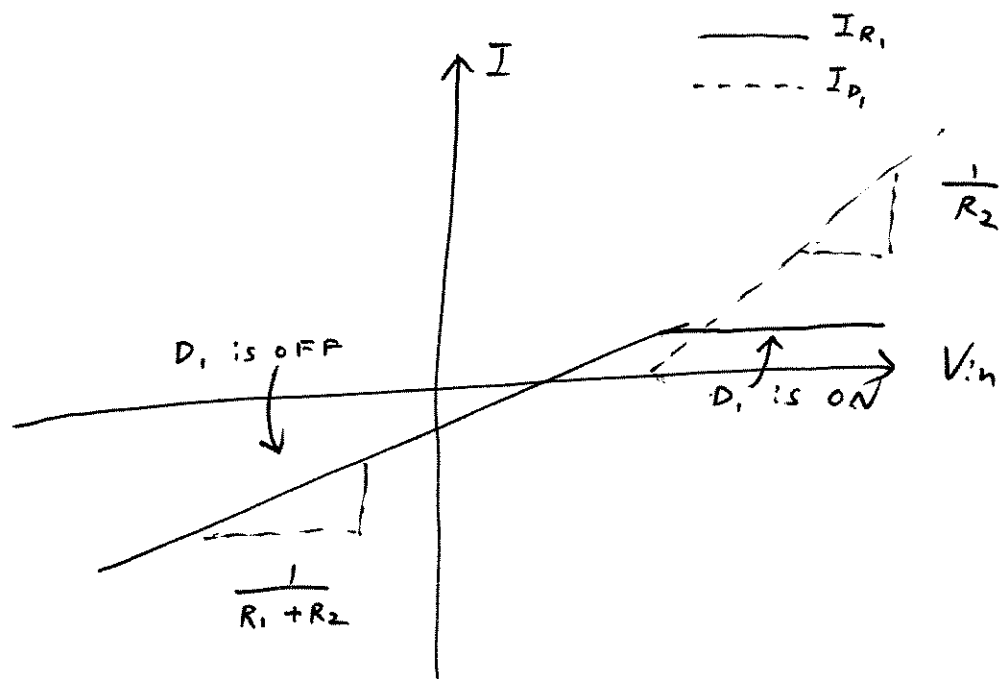
c)



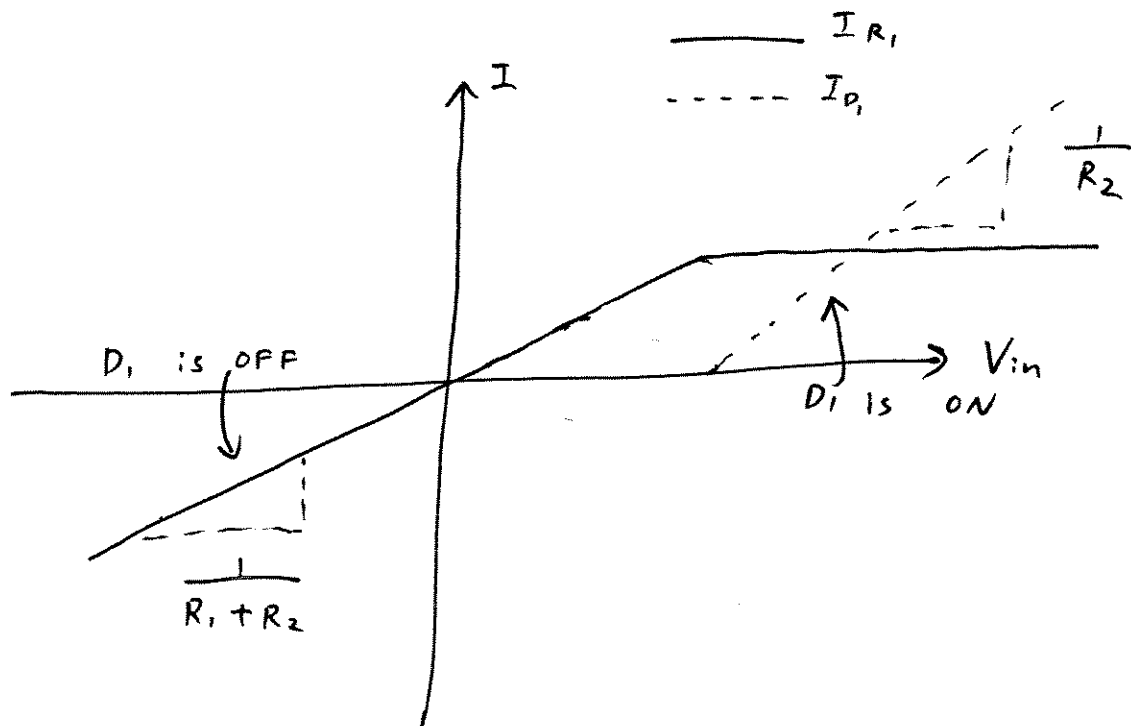
d)



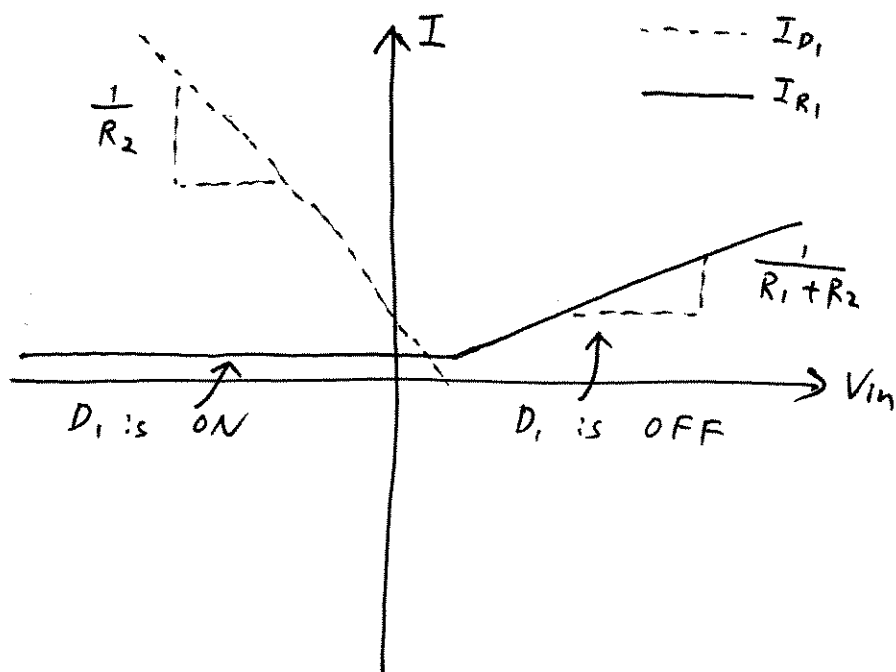
(26) a)



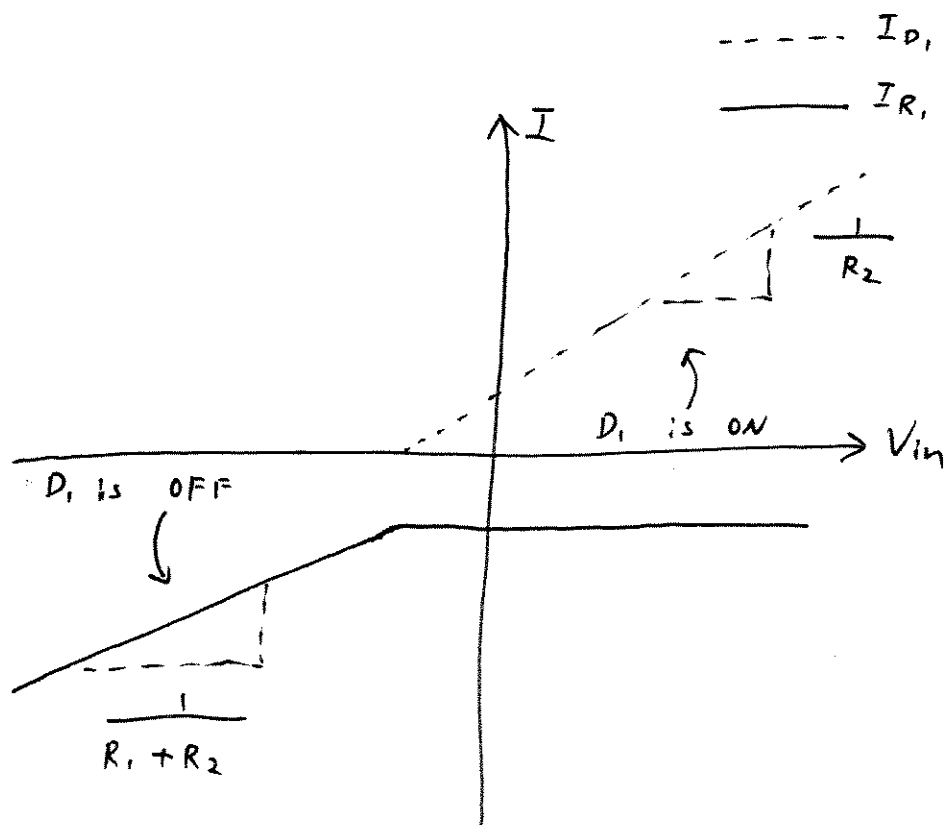
b)



c/

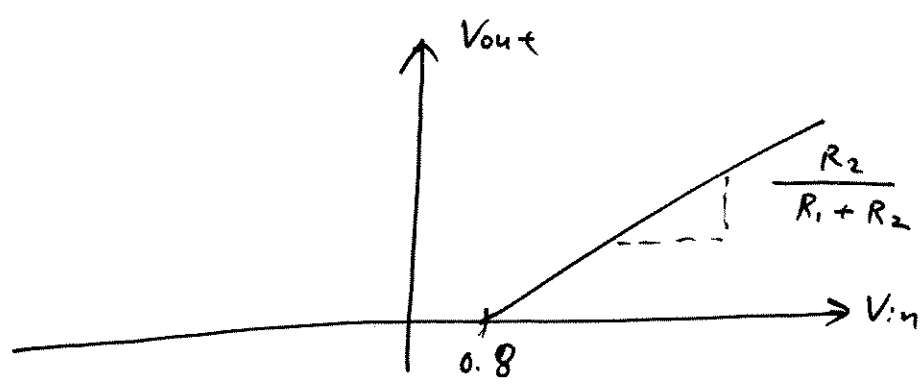


d/

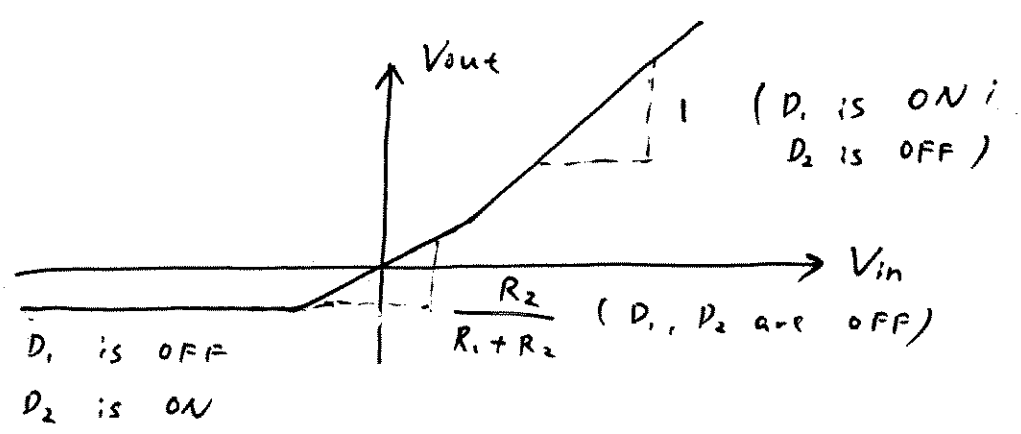


(27)

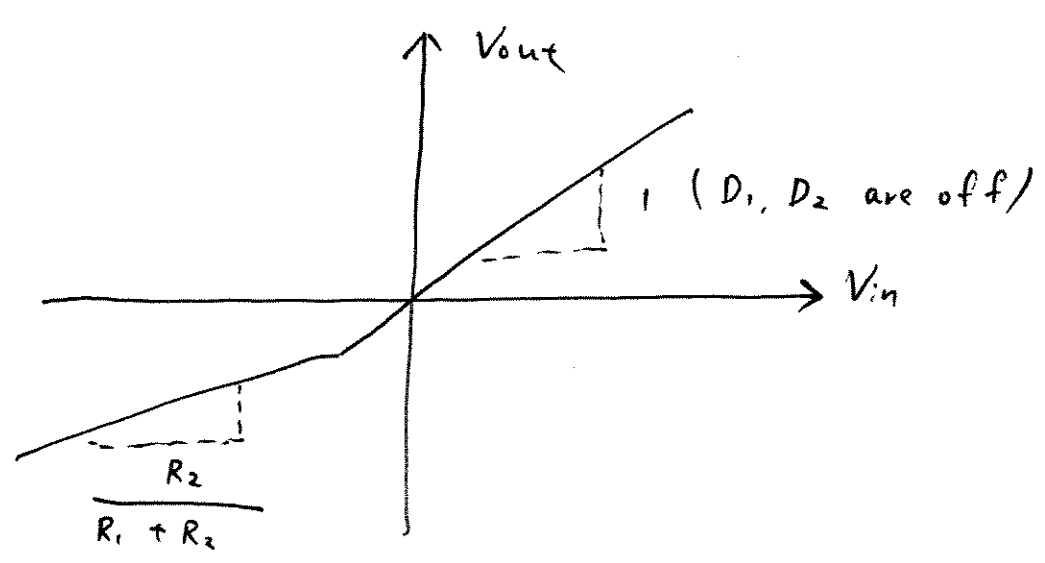
a)



b)

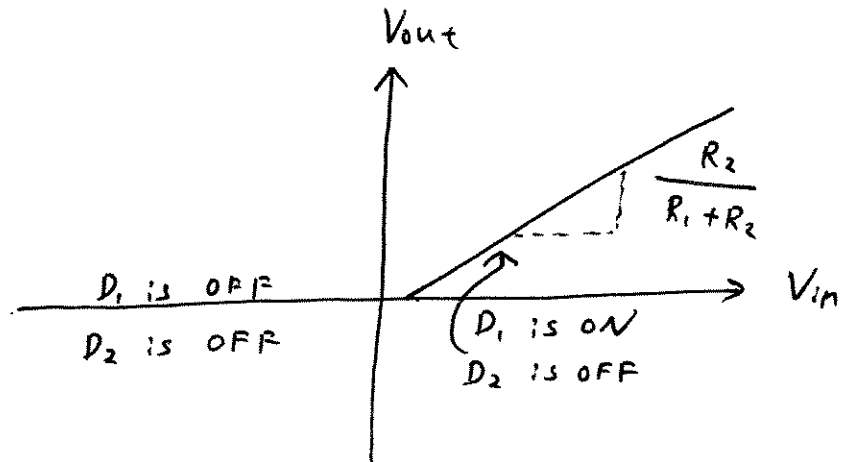


c)

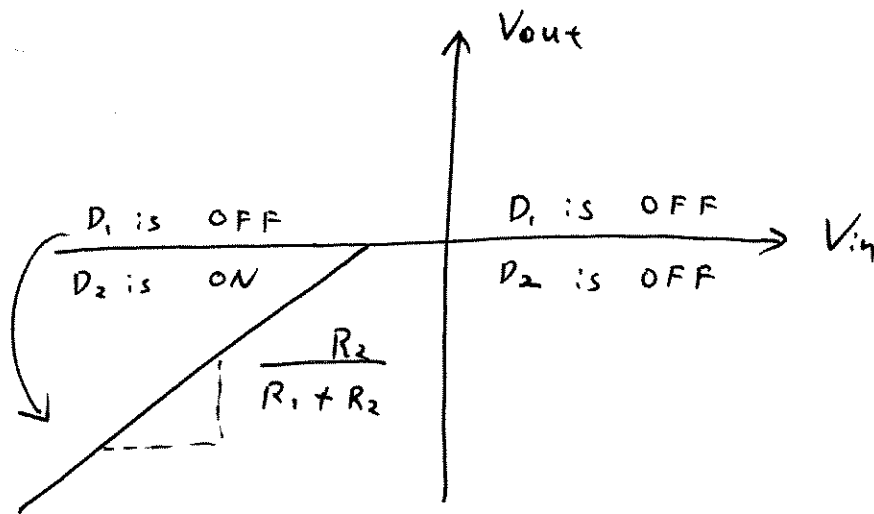


$\left(\begin{array}{l} D_1 \text{ is OFF,} \\ D_2 \text{ is ON} \end{array} \right)$

d/

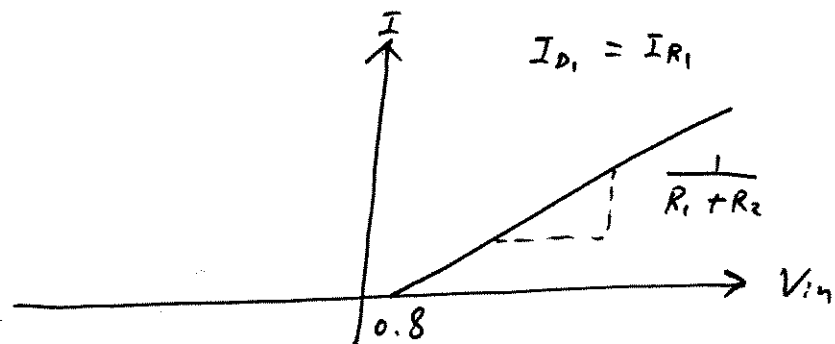


e/

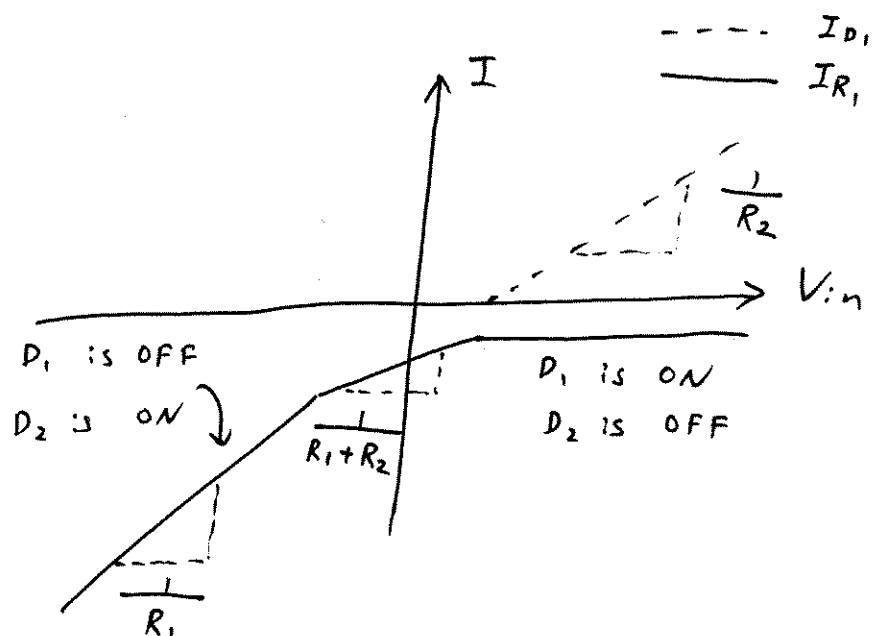


28

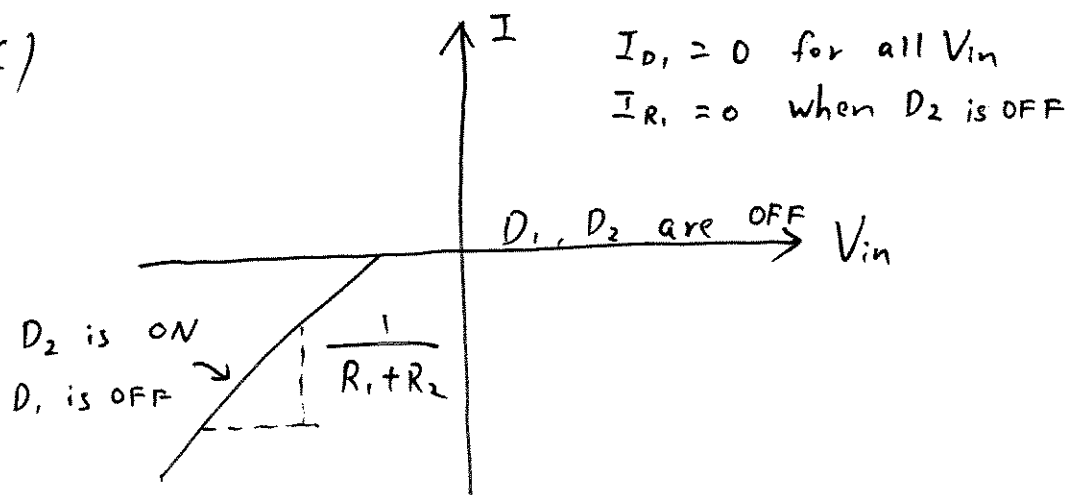
a)



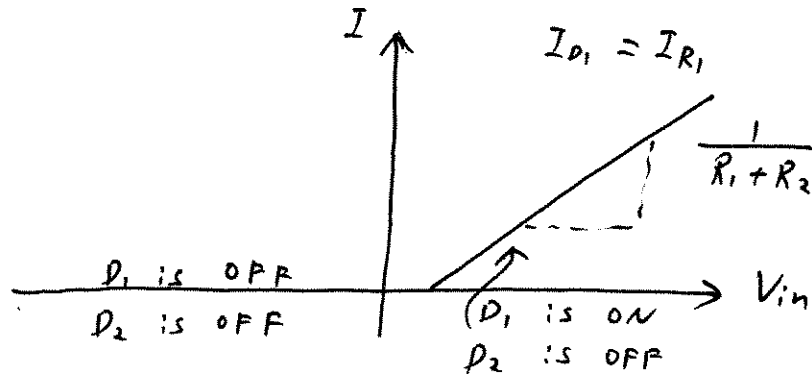
b)



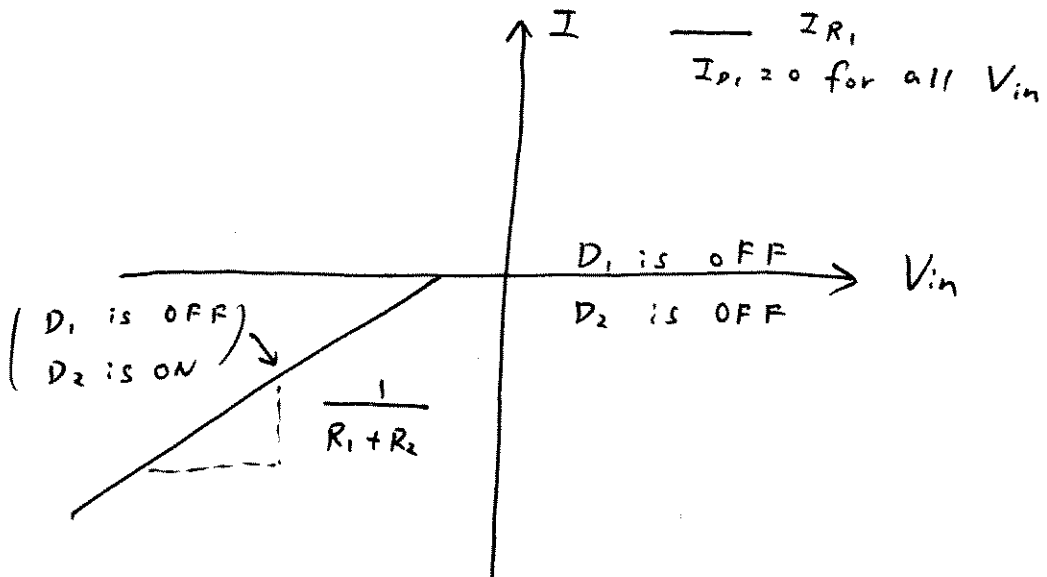
c)



d)

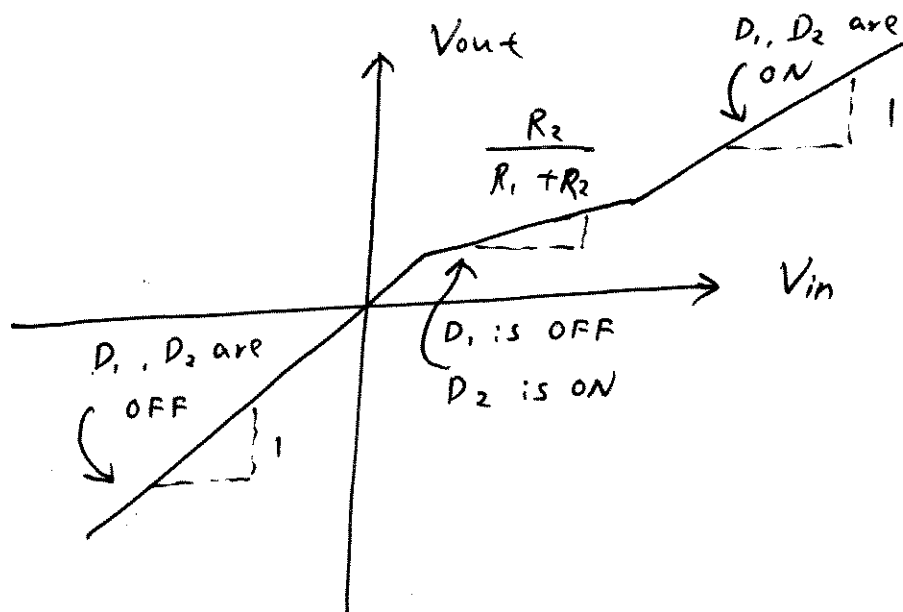


e)

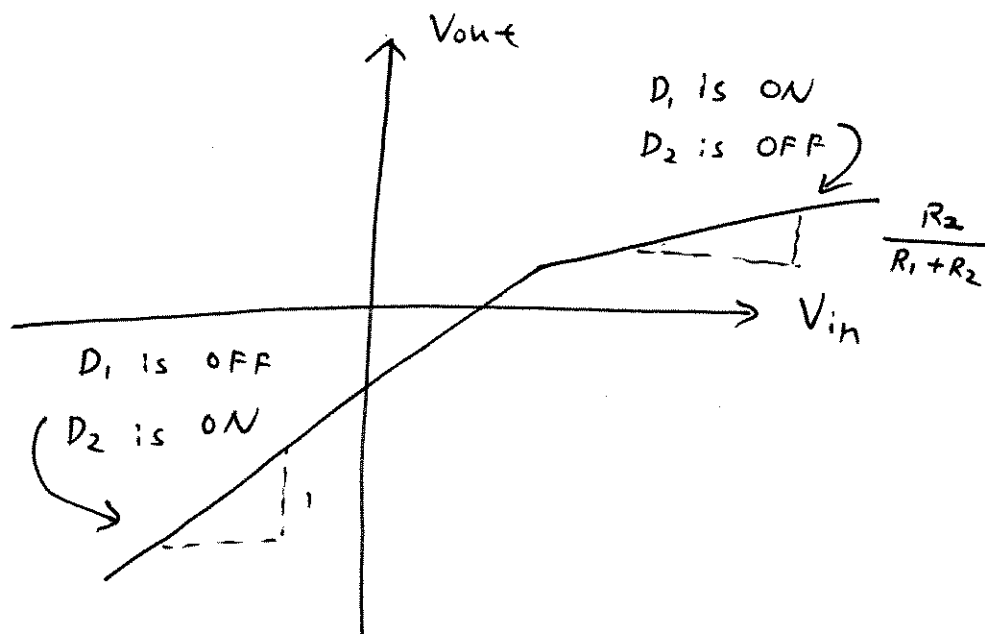


29

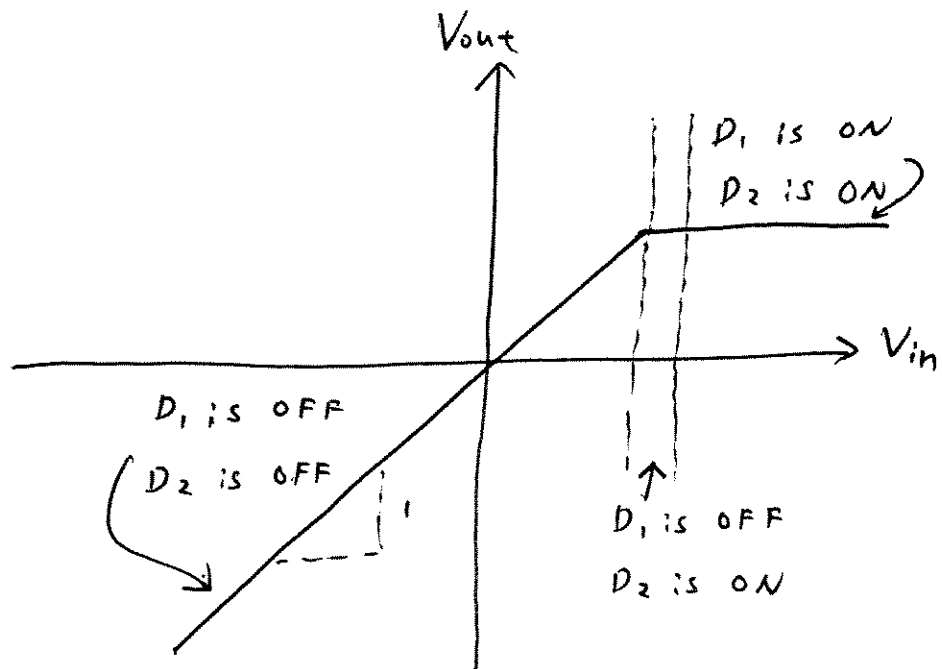
a/



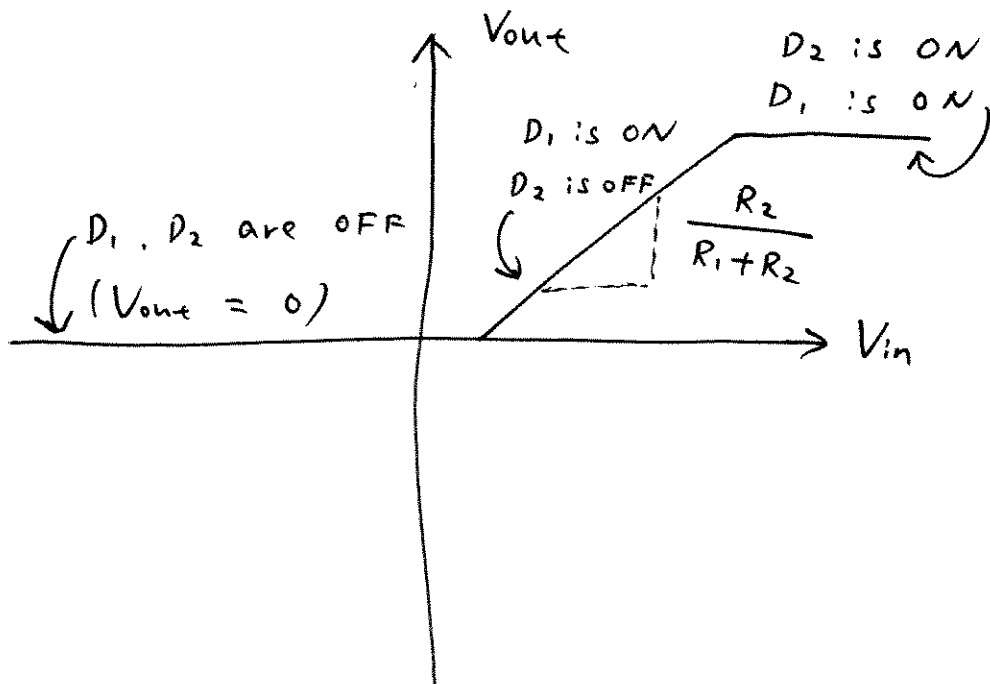
b/



c)

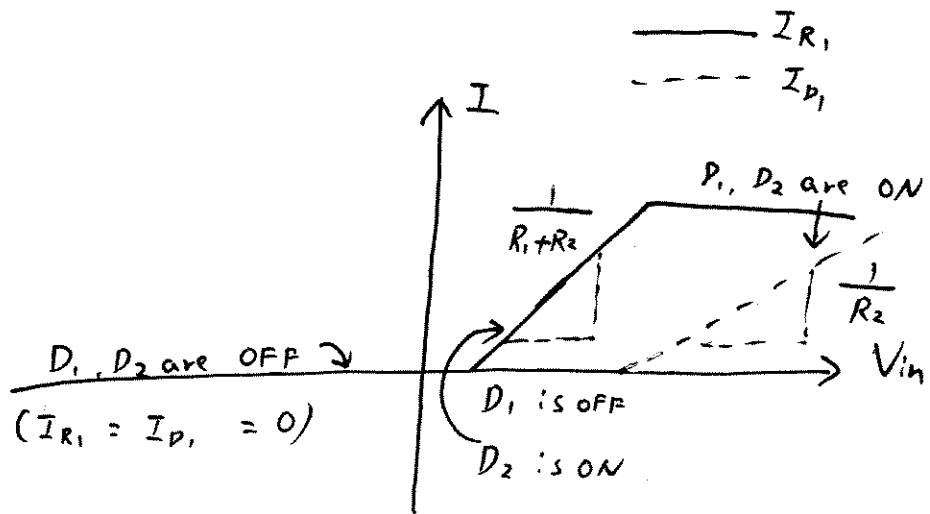


d)

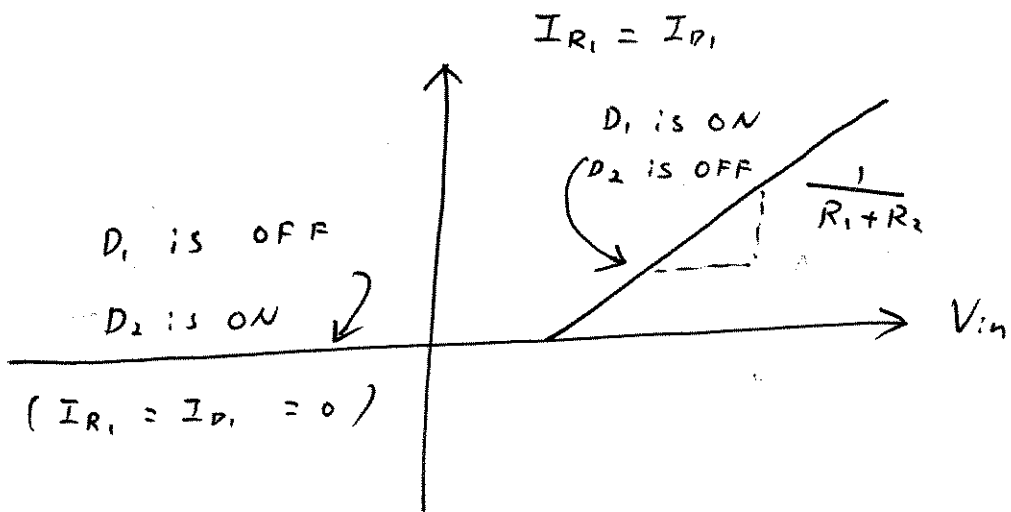


30

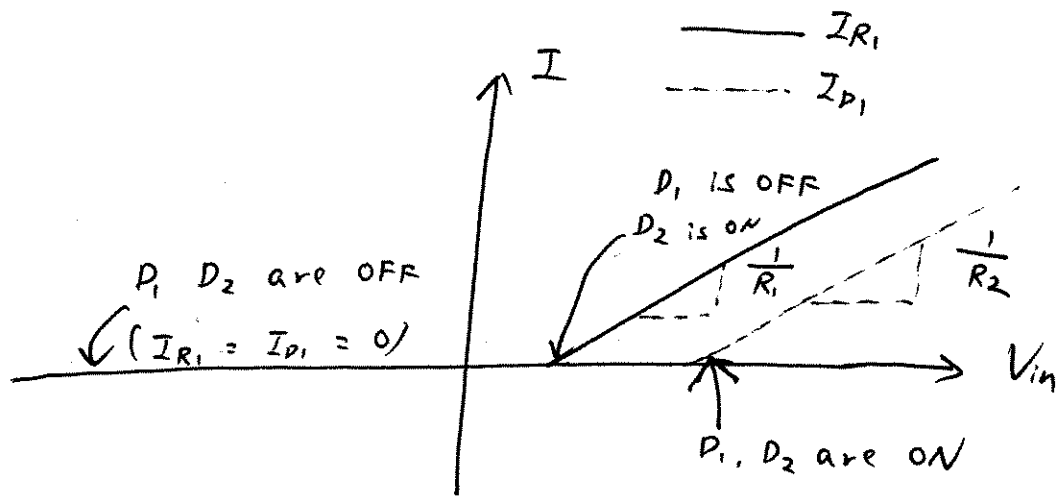
a)



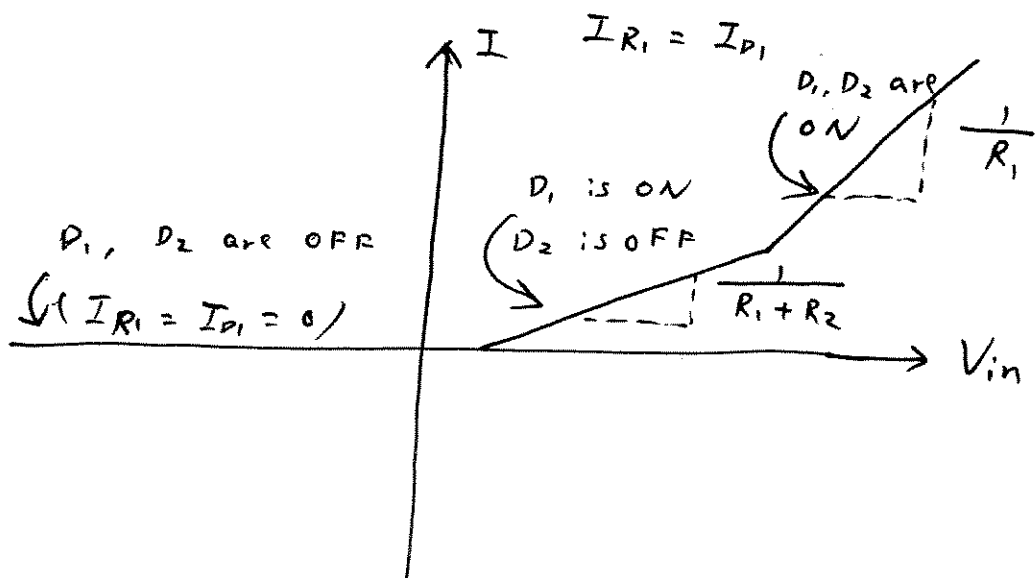
b)



c)



d)



③1 a) when V_{in} changes from $+2.4V$ to $+2.5V$,
 D_1 is ON throughout the change.

$$\therefore V_{out} \approx V_{in} - 0.8V,$$

i.e., V_{out} changes from $+1.6V$ to $+1.7V$.

b) when V_{in} changes from $+2.4V$ to $+2.5V$,
 D_1 and D_2 are both ON.

$$\therefore V_{out} = V_{in} - V_{ON, D_1},$$

i.e., V_{out} changes from $+1.6V$ to $+1.7V$.

c) when V_{in} changes from $+2.4V$ to $+2.5V$,
 D_1 and D_2 are both ON.

$$V_{out} \approx V_{ON, D_2},$$

i.e., V_{out} stays at $+0.8V$.

d) when V_{in} changes from $+2.4V$ to $+2.5V$,

D_2 is ON.

$$\therefore V_{out} \approx V_{ON, D_2},$$

i.e., V_{out} stays at $+0.8V$.

$$\begin{aligned}
 \textcircled{32} \quad a) \quad V_{out} &= i \times R_1 \\
 &= 0.1 \text{ mA} \times 1 \text{ k}\Omega \\
 &= 0.1 \text{ V}
 \end{aligned}$$

$$\begin{aligned}
 b) \quad r_{d1} = r_{d2} &= \frac{26 \text{ mV}}{3 \text{ mA}} \quad (\text{Eq. 3.58}) \\
 &\approx 8.67 \Omega.
 \end{aligned}$$

$$\begin{aligned}
 V_{out} &= i \times (R_1 + r_{d2}) \\
 &= 0.1 \text{ mA} (1.00867 \text{ k}\Omega) \\
 &\approx 1.009 \times 10^{-1} \text{ V}
 \end{aligned}$$

$$\begin{aligned}
 c) \quad V_{out} &= i \times r_{d2} \\
 &= 0.1 \text{ mA} \times 8.67 \quad (\text{from (b)}) \\
 &= 0.867 \text{ mV}
 \end{aligned}$$

$$\begin{aligned}
 d) \quad V_{out} &= i \times (R_2 \parallel r_{d2}) \\
 &\approx i \times r_{d2} \quad (\because R_2 \gg r_{d2}) \\
 &= 0.867 \text{ mV}
 \end{aligned}$$

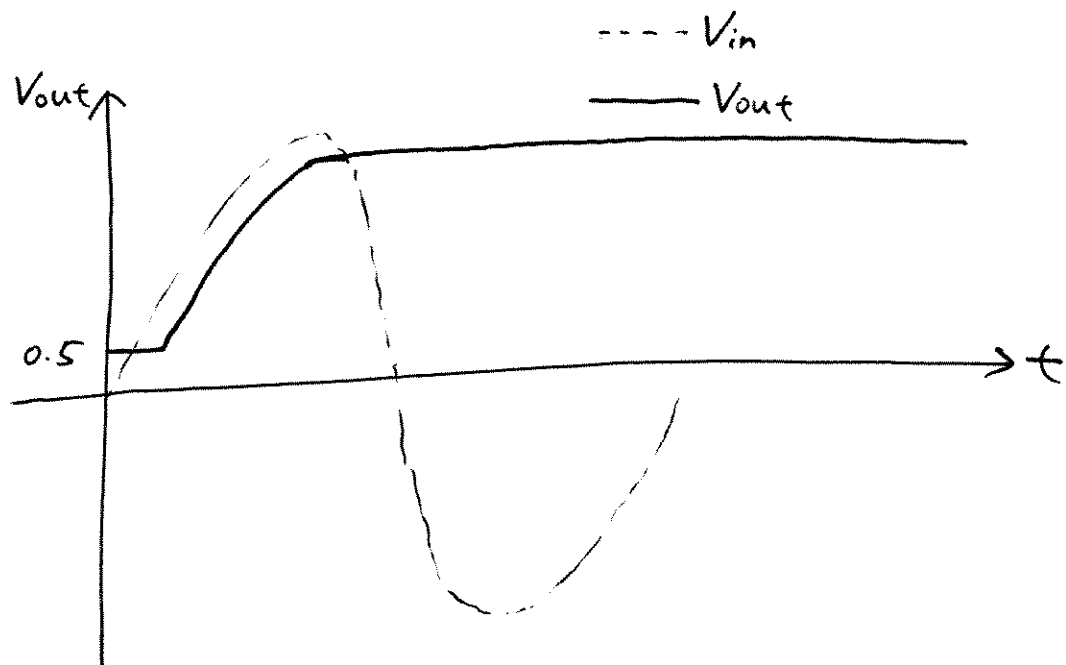
$$\textcircled{33} \text{ a) } \quad i_{r1} = i_{in} \\ = 0.1 \text{ mA}$$

$$\text{b) } \quad i_{r1} = i_{in} \\ = 0.1 \text{ mA}$$

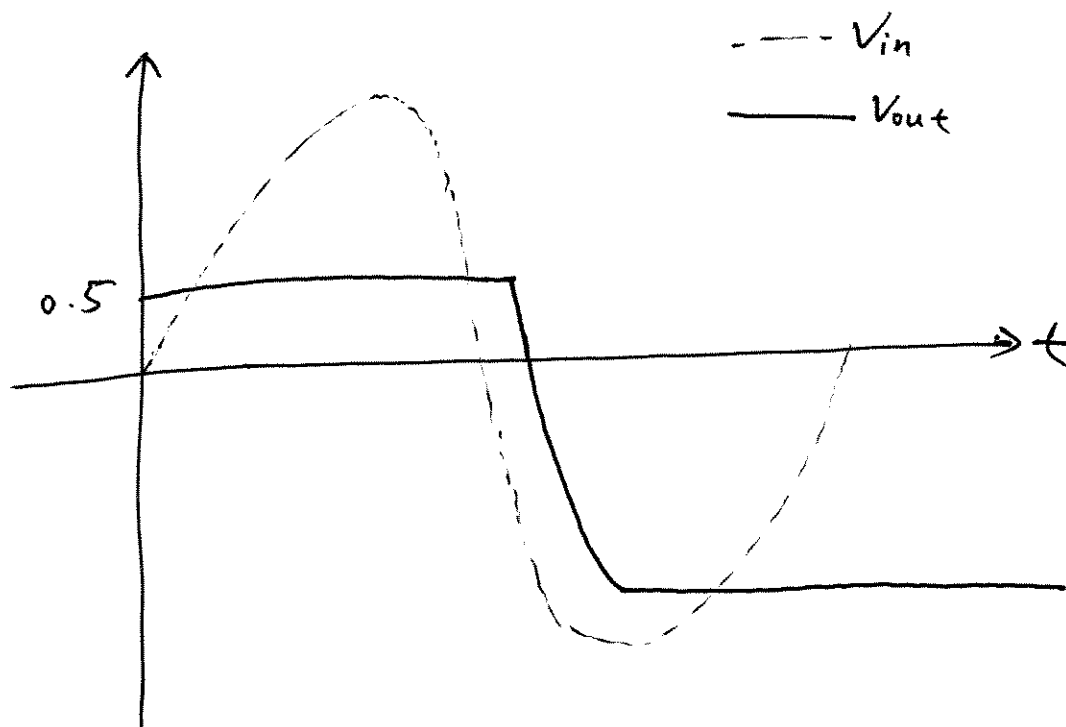
$$\text{c) } \quad i_{r1} = i_{in} \\ = 0.1 \text{ mA}$$

$$\text{d) } \quad i_{r1} = i_{in} \\ = 0.1 \text{ mA}$$

34



35



(36) From eq. (3.80),

$$\text{Ripple amplitude, } V_R \approx \frac{V_P - V_{D,on}}{R_L C f_{in}}$$

$$= \frac{3.5 - 0.8}{10 \quad 1000 \times 10^{-6} \times 60}$$

$$= 0.45 \text{ V}$$

(37)

From Eq. (3.83),

$$V_R = \frac{I_L}{C f_{in}}$$

$$\therefore V_R \leq 300 \text{ mV}$$

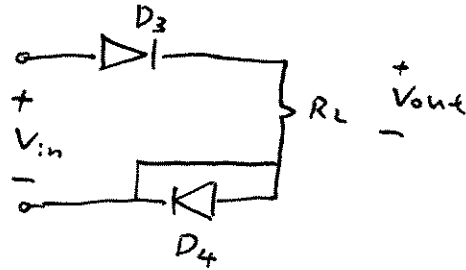
$$\frac{I_L}{C f_{in}} \leq 300 \text{ mV}$$

$$\therefore C \geq \frac{I_L}{f_{in} \times 0.3}$$

$$C \geq \frac{0.5}{60 \times 0.3}$$

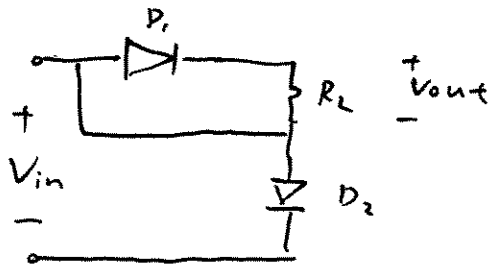
$$\text{i.e. } C \geq 0.278 \text{ F}$$

(38) In the positive half of the cycle,
when $V_{in+} > V_{in-}$, the circuit
is operating as :



D_4 is shunted, and $D_3 - R_L$ forms a
half-wave rectifier.

In the negative half of the cycle,
when $V_{in-} > V_{in+}$, the circuit becomes:



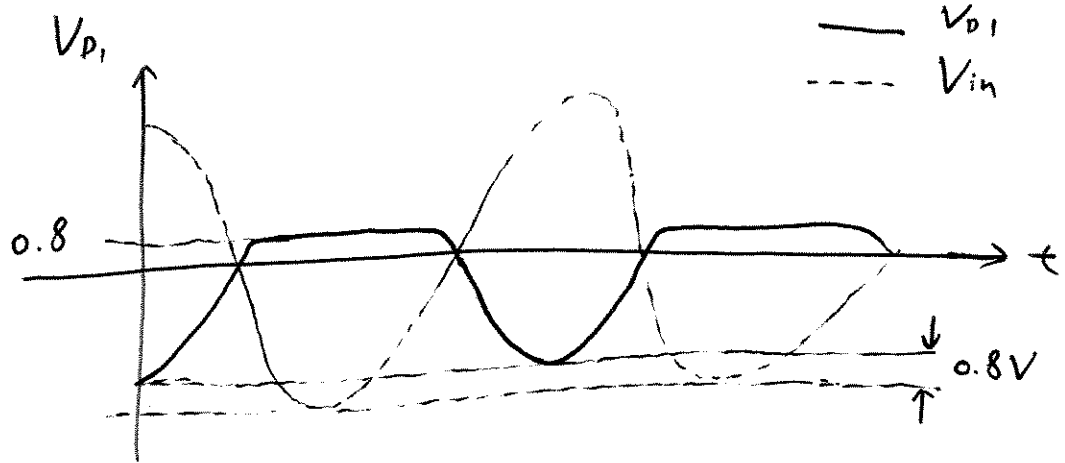
D_1 is shunted and is off.

Thus, $V_{out} = 0$.

Shunting the resistor load with a capacitor
has no effect in the above two cases.

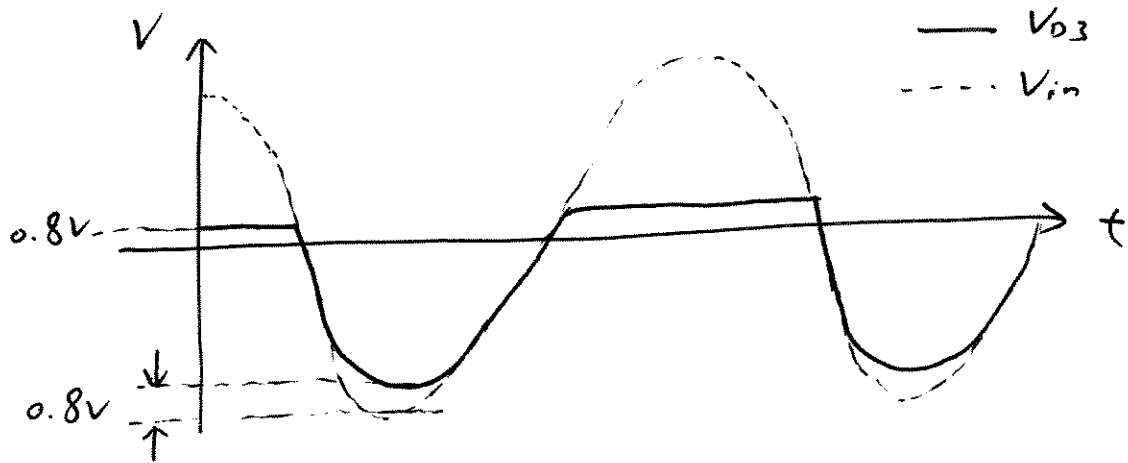
(39)

(i)

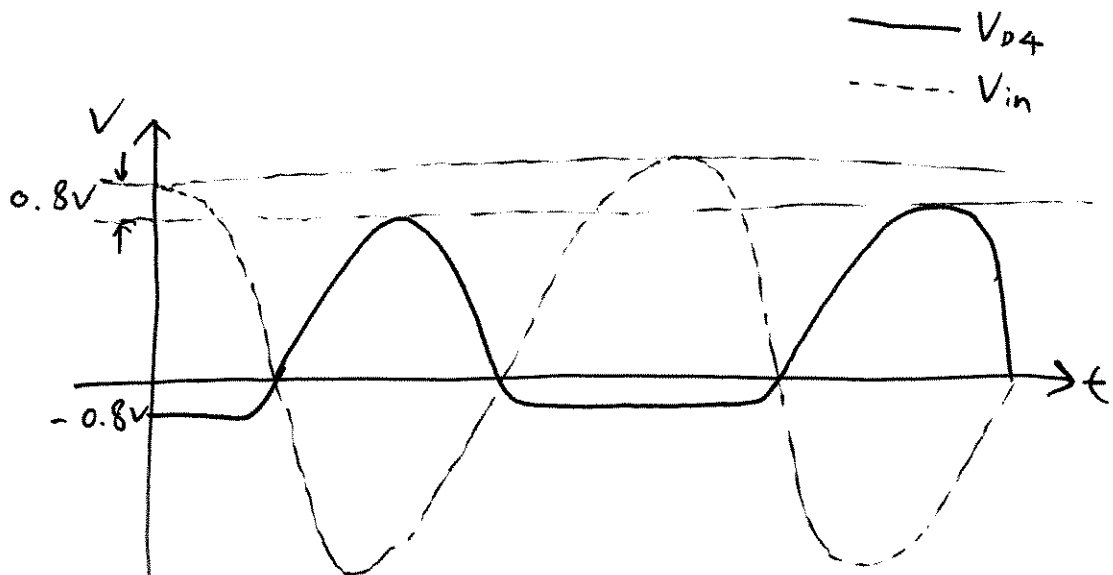


(ii) V_{D2} is same as V_{D1} (above)

(iii)



(iv)



④ - This circuit would fail to function as a full-wave rectifier.

- It only rectifies for $V_{in-} > V_{in+}$
(Current flows through D_1 and D_2)

- But for $V_{in+} > V_{in-}$, there is no conduction path through the load.

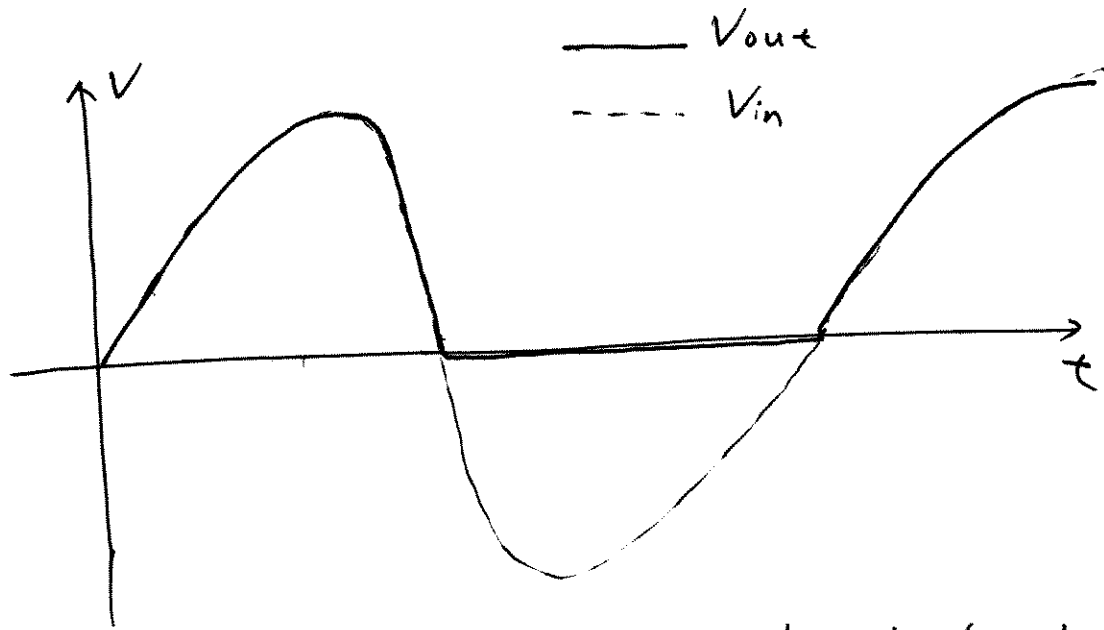
- Thus, this circuit behave like a half-wave rectifier

④ Using Eq. (3.94),

$$V_R \approx \frac{1}{2} \cdot \frac{V_P - 2 V_{P, on}}{R_L C_1 f_{in}}$$
$$= \frac{1}{2} \cdot \frac{3 - 2 \times 0.8}{30 \times 1000 \times 10^{-6} \times 60}$$

$$= 0.389V$$

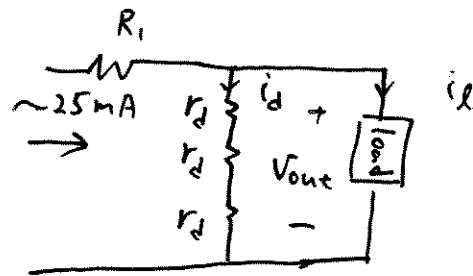
(42)



- With the two negative terminals shorted together, the circuit behaves like a half-wave rectifier.
- When $V_{in+} > V_{in-}$, D_3 and D_4 conduct as usual. There will be an additional path that bypasses D_4 , since V_{in-} and V_{out-} are shorted. But this additional path causes no change to the V_{out} waveform.
- When $V_{in-} > V_{in+}$, both V_{out+} and V_{out-} track V_{in-} . V_{out+} connects to V_{in-} through D_1 ; V_{out-} connects to V_{in-} through the additional shorted path.
- Thus $(V_{out+}) - (V_{out-}) = 0$, i.e. $V_{out} = 0$

(43)

The circuit can be simplified as:



First, find r_d :

$$r_d = \frac{V_T}{I_D} \quad (\text{from eq. 3.60/})$$

$$= \frac{26 \text{ mV}}{5 \text{ mA}}$$

$$= 5.2 \Omega$$

Since $i_L = +1 \text{ mA}$.

$$i_d = -1 \text{ mA}.$$

\therefore change in V_{out} ,

$$\text{ie. } V_{out} = (-1 \text{ mA}) (3 \times 5.2)$$

$$= -15.6 \text{ mV}$$

(44)

a) From Eq. (3.94),

$$\text{the ripple amplitude, } V_R = \frac{1}{2} \cdot \frac{V_p - 2V_{D, \text{on}}}{R_L C f_n}$$

$$= \frac{1}{2} \cdot \frac{5 - 2 \times 0.8}{1000 \times 100 \times 10^{-6} \times 60}$$

$$= 0.283 \text{ V}$$

b) The ripple across the load,

$$V_L = i \times 3r_d,$$

where i is the change in current flowing through R_L , in series with the 3 diodes.

$$\therefore r_d = \frac{V_T}{I_D}$$

$$\approx \frac{26 \text{ mV}}{5/R_L} = 5.2 \Omega$$

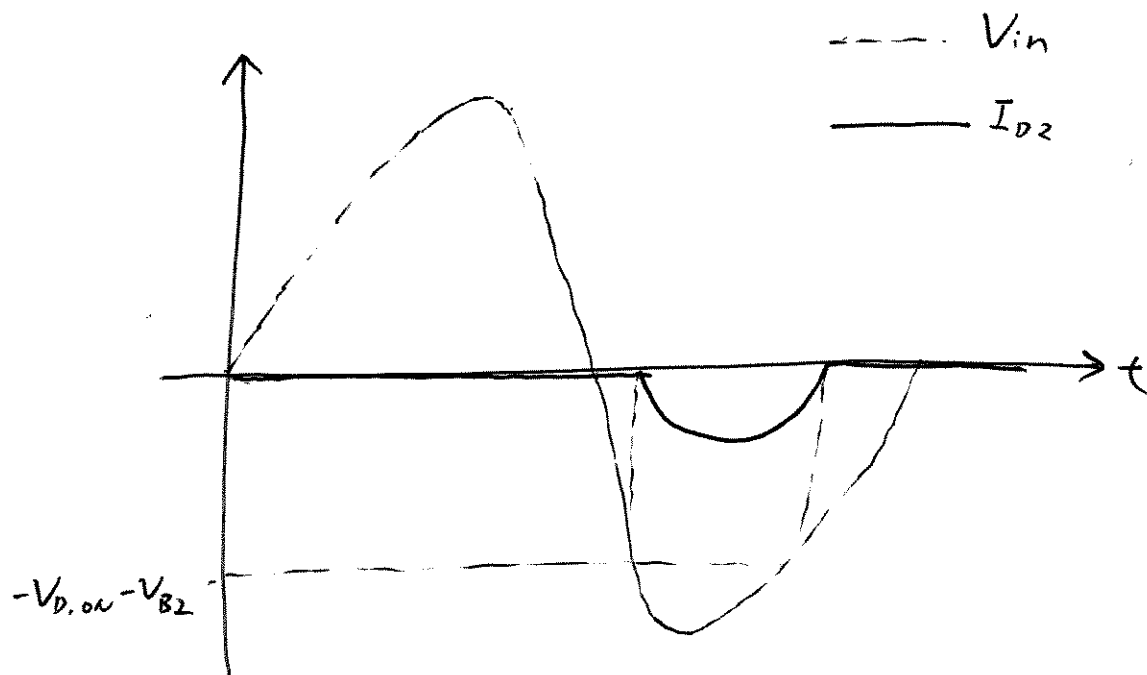
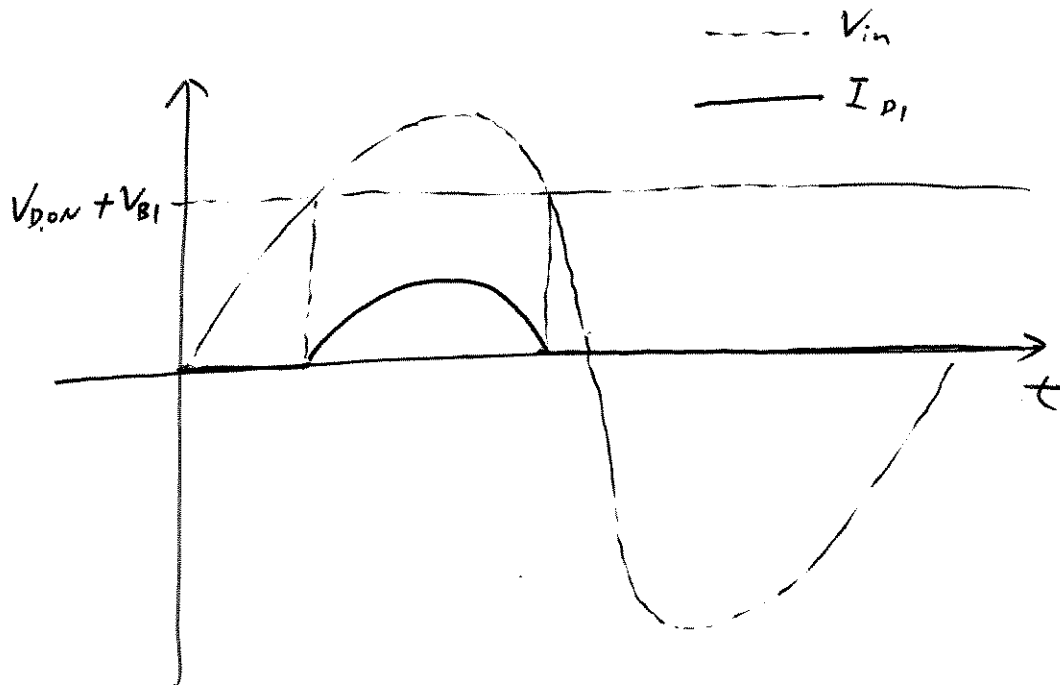
$$i \approx \frac{V_R}{R_L + 3r_d}$$

$$= 0.279 \text{ mA}$$

$$\therefore V_L = 0.279 \text{ mA} \times 3 \times 5.2$$

$$= 4.35 \text{ mV}$$

(45)



(46) With positive threshold = +2.2V,

$$\begin{aligned} V_{B1} &= 2.2 - 0.8 \\ &= +1.4V \end{aligned}$$

With negative threshold = -1.9V,

$$\begin{aligned} -V_{B2} &= -1.9 + 0.8 \\ &= -1.1V. \end{aligned}$$

$$V_{B2} = 1.1V //$$

To meet the maximum current criterion,

Since $I_{R1} = I_{D1}$ or I_{D2} ,

I_{D1} or I_{D2} is at max when

I_{R1} is at max.

I_{R1} is at max when $|V_R|$ is max,

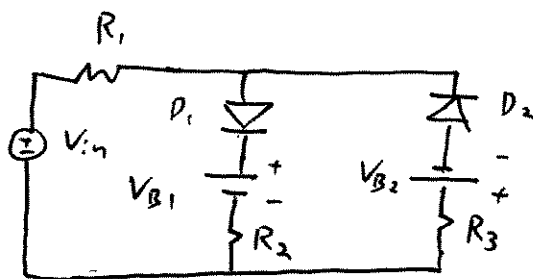
$$\begin{aligned} \text{ie. } |V_R| &= 5 - 1.9 \\ &= 3.1V. \end{aligned}$$

Since $I_{R1} \leq 2 \text{ mA}$.

$$R_1 \geq \frac{3.1}{2 \text{ mA}}, \text{ ie. } R_1 \geq 1550\Omega //$$

(47)

The required circuit is:



Similar to Example 3.34,

$$V_{B1} = V_{B2} = (2 - 0.8) \text{ V} \\ = 1.2 \text{ V}$$

To find R_2 ,

For $V_{in} > 2 \text{ V}$, $\frac{V_{out}}{V_{in}}$ has a slope of 0.5.

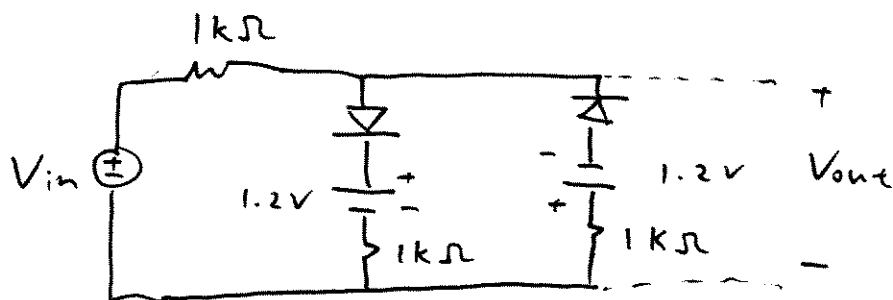
This implies $R_2 = R_1$

(R_1 and R_2 form a volt. divider).

Similarly, $R_3 = R_1$.

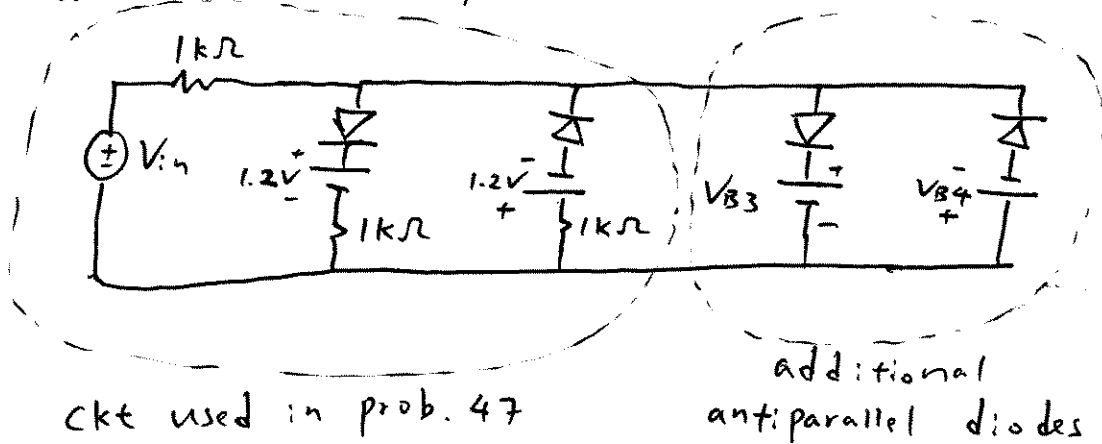
Thus, set $R_1 = R_2 = R_3 = 1 \text{ k}\Omega$.

The resulting circuit is:



(48) For $|V_{in}| < 4V$, the $V_{out} - V_{in}$ characteristic is similar to prob. (47).

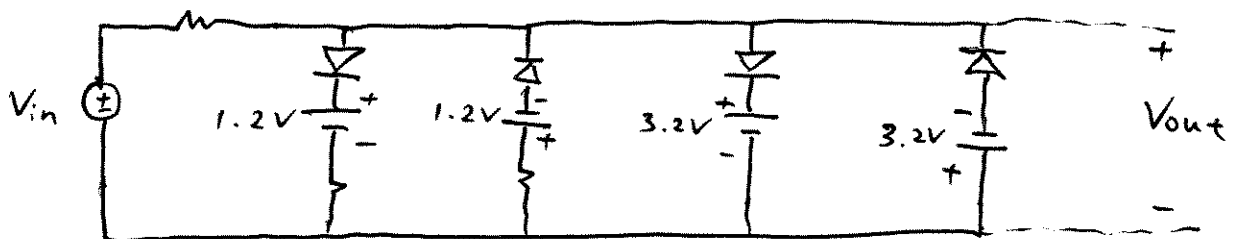
To get voltage limiting characteristic for $V_{in} > 4V$, and $V_{in} < -4V$, we can shunt the circuit used in prob(47) with two antiparallel diodes as below:



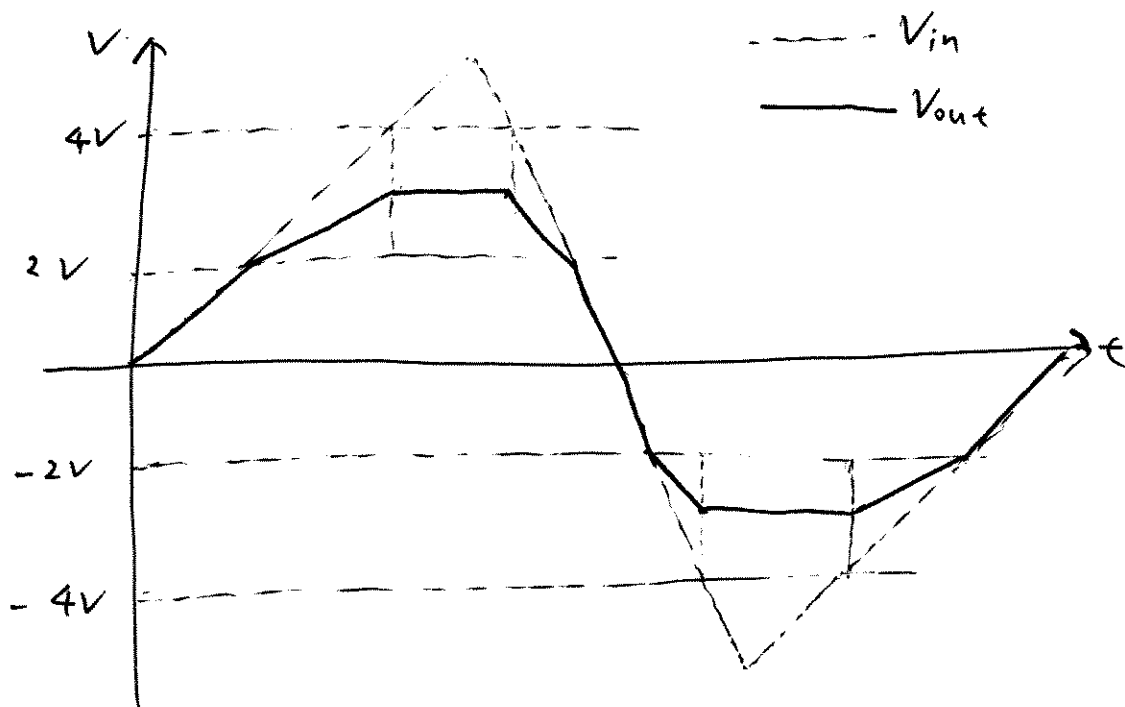
$$V_{B3} = V_{B4} = 4 - 0.8$$

$$= 3.2V$$

Resulting circuit is:



(49)



To get a better approximate of a sinusoid, the slope of the input-output characteristic should decrease more gradually from 1 to 0 through more sections.

eg :

