EE 466 Final Project Report

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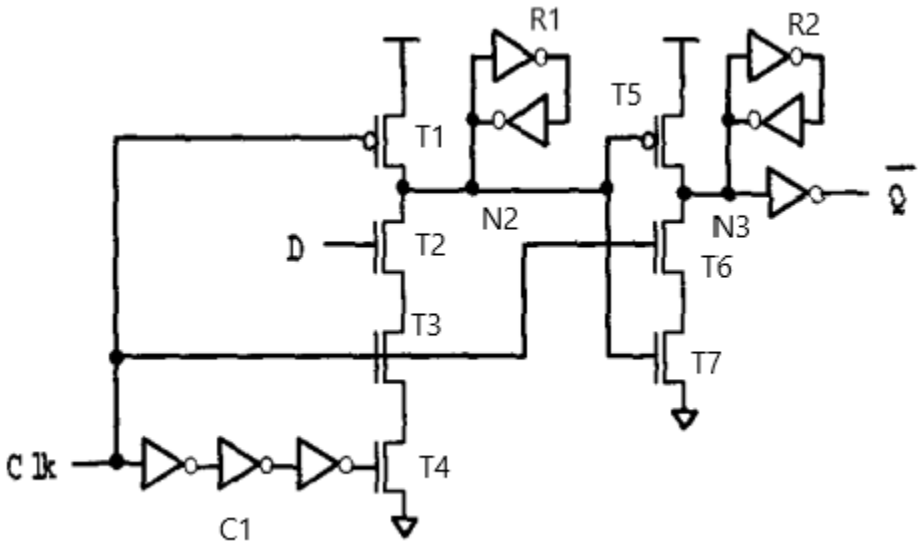
Design of an ipDCO



1. How it Works

The clock signal is fed into four parts of the circuit: T1, T3, T6 and C1. C1 acts as a pulse generator by delaying and inverting the signal, so if clock is 1, after a short delay, the output of C1 will become 0, and vice versa.

The state holder R1, and in turn node N2, are charged by Vdd when clock is 0, this in turn makes T5 turn off, and T7 turn on. This means when clock returns to a high state, node N3 drains to ground, and the state holder R2 maintains the signal. The output Qb would be a 1.

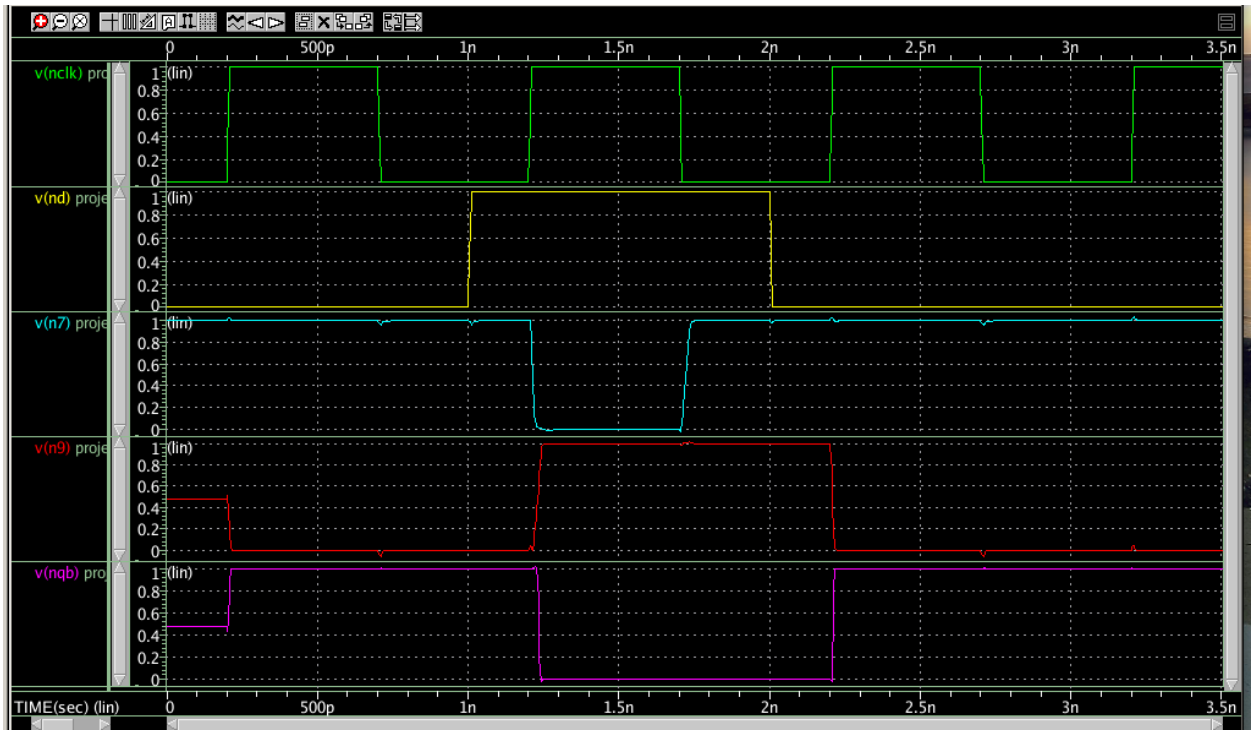
As long as D=0, the output Qb will remain a 1. But if D=1 when the clock goes from low to high, T1 will turn off, T3 will then turn on, and because of the delay, T4 will stay on for a short time. This series of events means R1 and N2 drain to ground. When this happens, T7 will turn off and T5 will turn on, this charges N3 and R2, making the output of Qb=0.

If D=1 when the clock goes from a high state to a low state, T1 will turn on, T3 will close, charging N2 and R1 to Vdd. This in turn turns on T7 and turns off T5. However, because the clock is in a low signal, T6 remains off, preventing N3 and R2 from draining to ground, this in turn keeps the Qb output being 0.

If D then switches to 0, then on the next clock up cycle, the system will return to its default state, where N2=1, allowing N3 to drain to ground, and make the output Qb=1.

The short explanation of this is, when D=1, Qb will become 0 on the next rising edge of the clock. When D=0, Qb will become 1 on the next rising edge of the clock.

The following waveform shows the clock, D, n2, n3, and Qb



(n7 and n9 in the waveform are n2 and n3 respectively)

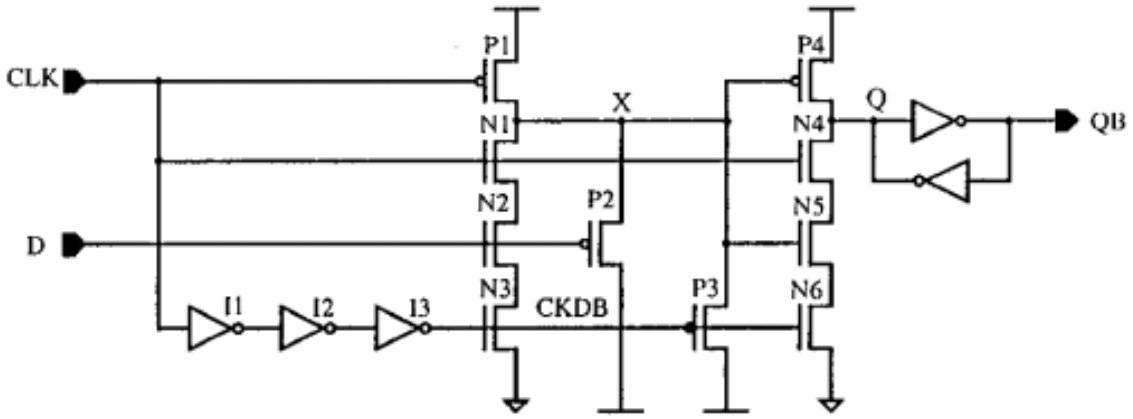
2. Performance stats

Delay: 8.3ps (falling) 5ps (rising)

Power Consumption: 5.5665uW

Total Area: 171,000 nm^2

Design of an HLFF



1. How it Works

The clock signal is fed into P1, N1, N4 and the inverter chain, starting at I1. D feeds into N2 and P2, and the inverter chain feeds into N3, P3 and N6.

Ignoring D for the moment, when clock has been low for a while, P1 is on, N1 is off, and the inverter chain will have held a steady 1 output, making N3 on and P3 off. This makes the node X go high, as it is connected to Vdd. This turns off P4, and turns on N5, the inverter chain also turns on N6, however N4 is off because the clock is low. This prevents node Q from draining to ground, and as such Q and Qb are both floating.

When clock goes high, the first thing that will happen is N4 will turn on, allowing Q to finally drain to ground, allowing Qb to output a 1. Clock going high will also turn off P1, turn on N, and after a short delay, the inverters will allow P3 to turn on. This will keep node X charged to Vdd. X being 1 means P4 is off and N5 is on. The clock being high means N4 is also on, however, the inverter is outputting a 0, preventing Q from draining to ground. The state holder will maintain Q at 0 and Qb at 1.

If D=1, and clock goes from a low state to a high state, then P1 will turn off, N1 will turn on, N2 will turn on and N3 will stay on because of the delay from the inverters. This means X will be a 0. This in turn means N5 will turn off, and P4 will turn on, allowing Q to be charged by Vdd, making Qb output a 0. The state holder will maintain these two values.

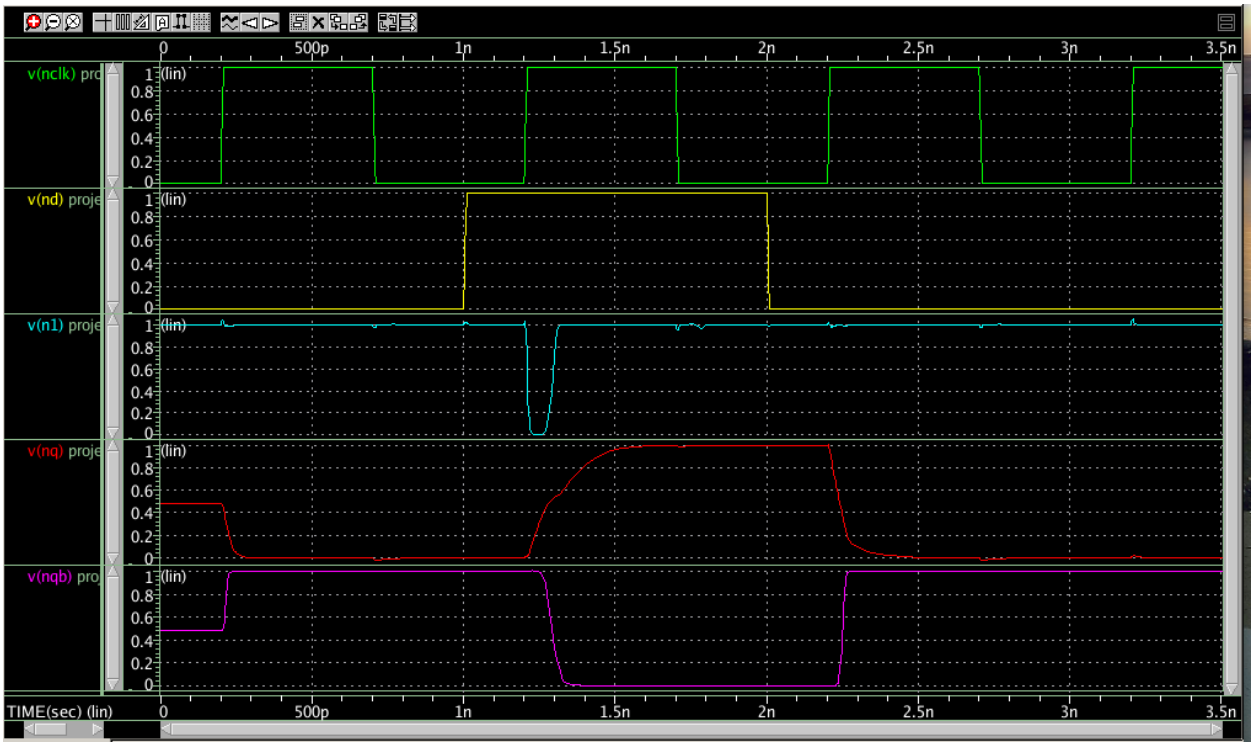
If clock holds a high state for a long period of time while D=1, then eventually the inverter will output a 0, which turns off N3, and on P3, this makes X return to being a 1. This will then turn off P4, and on N5, the inverter turns off N6. This means Q and Qb do not change, as the state holder is maintaining their values.

If D switches to 0 while the clock is high, nothing would happen, as X is already connected to Vdd. If the clock switches to low while in this state, P1 will turn on, N1 and N4 will turn off. After a short delay, the inverter will output a 1 which will turn off P3 and turn on N6. The output of the system stays the same, because the state holder keeps Q and Qb at 1 and 0 respectively.

If D=0 on the next clock up cycle, then P1 turns off, N1 turns on, and N4 turns on. N4 turning on means that Q can drain to ground, swapping the output of Qb to 1. After a short delay, the inverter will output a 0, turning off N6, but the output is maintained by the stateholder.

A simple explanation is that on a rising clock edge, Qb will go high if D=0, and Qb will go low if D=1.

Below is a waveform containing clock, D, X, Q and Qb



(n1 is standing in for node X in this waveform)

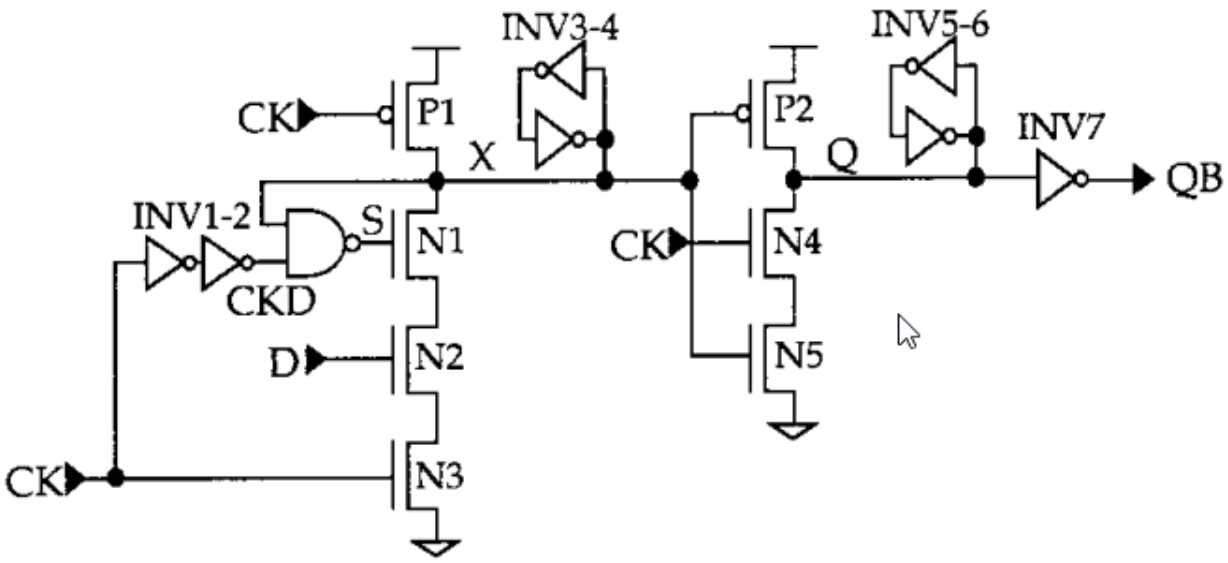
2. Performance stats

Delay: 52ps (falling) 20ps (rising)

Power Consumption: 12.059uW

Total Area: 180,000 nm^2

Design of a Semi-dynamic DFF



1. How it Works

This flip flop ultimately does the same job as the previous two, however, instead of relying on a triple inverter for a delay and to invert the clock to create a pulse, this one uses a double inverter to create a delay, and uses a NAND gate in a feedback loop.

To start off, the clock signal feeds into four parts of this circuit. It goes into transistor P1, it goes into the double inverter at Inv1, into transistor N3, and lastly into N4.

Ignore D for the moment and leave it as a 0. Clock feeds into P1, this means on a low output, P1 turns on, this in turn charges X and the state holder created by inverters 3 and 4. This makes X=1, this shuts off P2 and turns on N5, but because Q was never drained or charged, it remains in a neutral floating state. When the clock goes high for the first time, it will turn off P1, but X remains charged, N4 will now also turn on, allowing Q to drain to ground, and allow QB to output a 1. This is now the default state of the circuit. With both clock and X being 1, the NAND gate now outputs a 0, which turns off N1.

Making D=1 while the clock remains high does not change the state of the circuit. N1 remains off, meaning node X cannot drain to ground. This keeps N5 on and P2 off, preventing Q from becoming charged by Vdd.

If the clock drops to a low signal while D=1, transistor N3 turns off as well, again, preventing node X from draining. It does however also turn off N4, meaning if X became a 0, P2 could turn on and charge node Q. Because clock is now low, the double inverter system after a short while will output a 0 as well, making the NAND gate switch to outputting a 1, turning N1 on. This means the only thing stopping node X from draining to ground is clock going high once more.

While D1=1 when the clock goes high, N1, N2, and N3 are all going to be on, while P1 will switch off. This means that X will drain to 0. This turns off N5 and on P2, allowing node Q and the state holder to become charged by Vdd. This in turn swaps output QB to 0.

If D=1 when the clock again drops to a low signal, X will become charged by Vdd as N3 will turn off and P1 will turn on. However, this does not affect the state of Q and QB, because the clock going low turns off N4. So even if N5 turns on and P2 turns off, Q cannot drain to ground, and as such QB remains a 0.

Making D=0 while the clock is low means that X will remain as a 1 as it now longer has a path to drain to ground, as N2 will now be off. However, if the clock switches from a low signal to a high signal while D is off, then N4 will turn on, and with P2 being off and N5 also being on, node Q can then drain to ground, switching output QB to 1.

This flip flop is like the previous two, where on a rising edge, QB becomes the inversion of D, and remains as such until the next rising edge.

Below is the waveform of this flip flop. It contains the clock, D, X, Q and QB

(N1 in this waveform is node X in the diagram)

2. Performance stats

Delay: 18ps (falling) 12ps (rising)

Power Consumption: 11.341uW

Total Area: 160,875 nm^2