COMP 2432 Operating Systems
Tutorial 9 Solution

1. Virtual Memory.

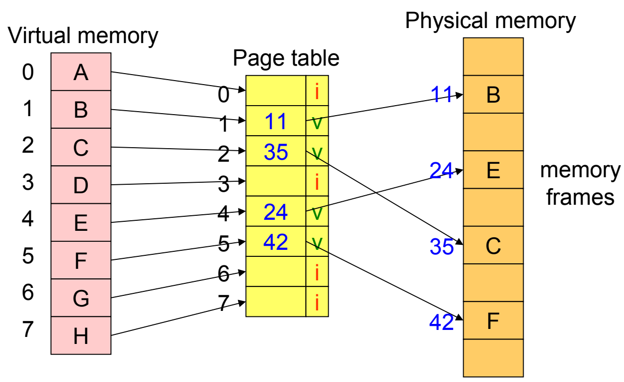
(*a*) There are 24 bits for the address. It can address up to a space of 2^{24}, i.e. **16 MB**.
(*b*) Physical memory has a size of 32KB. It needs an address length of **15 bits**, since 32K = 2^{15}.
(*c*) Page size (and frame size) is 2KB. It would imply an offset length *n* of **11 bits**, since 2K = 2^{11}.
(*d*) Logical address length $m = 24$. Page offset length $n = 11$. Page number length is thus 24–11 = **13 bits**.
(*e*) Physical memory has a size of 32KB and each frame has a size of 2KB. Number of frames is 32K / 2K = **16**.
(*f*) There are 16 frames. Thus, 4 bits are needed for frame number, since 16 = 2^4. Alternatively, physical address has a length of 15 bits. The offset length $n = 11$. Therefore frame number has 15–11 = 4 bits.

2. Virtual Memory.

(*a*) **4 GB** [2^{32}]
(*b*) **16 bits** [64K = 2^{16}]
(*c*) **10 bits** [1K = 2^{10}]
(*d*) **22 bits** [32 – 10]
(*e*) **64** [64K / 1K = 64]
(*f*) **6 bits** [16 – 10]
(*g*) **4 MB** [6 bits for frame number, 2 additional bits ⇒ 1 byte / entry, 4G/1K pages ⇒ 4M entries]
(*h*) **1 KB** that can be fit into ***one single page*** [1M/1K ⇒ 1K page table entries ⇒ 1KB page table size]

3. Page Table in Virtual Memory.

Page Ref	1	3	0	2	3	5	1	5	0	4
Frame 1	1	1	1	1	1	5	5	5	5	**5**
Frame 2	-	3	3	3	3	3	1	1	1	**1**
Frame 3	-	-	0	0	0	0	0	0	0	**4**
Frame 4	-	-	-	2	2	2	2	2	2	**2**



4. Memory Access Time.

Effective memory access time = cache access time + (2 – *h*) × memory access time.
With $h = 0.95$, we have 20 + (2 – 0.95) × 100 = 125 ns.
With $h = 0.99$, we have 20 + (2 – 0.99) × 100 = 121 ns.

Effective virtual memory access time = (1 – *f*) × memory access time + *f* × page fault service time. Note that without TLB, memory access time is 200 ns = 0.2 μs.
With $f = 0.01$, we have (1–0.01) × 0.2 + 0.01 × 5000 = 50.198 μs.
With $f = 0.001$, we have (1–0.001) × 0.2 + 0.001 × 5000 = 5.1998 μs.

Making use of the adjusted memory access time with TLB, when page fault rate is 1% and TLB hit rate of 95%, effective virtual memory access time = (1–0.01) × 0.125 + 0.01 × 5000 = 50.1238 μs.

When page fault rate is 0.1% and TLB hit rate of 99%, the effective virtual memory access times = (1–0.001) × 0.121 + 0.001 × 5000 = 5.12088 μs. It can be seen that the impact of TLB is much smaller with this amortized cost computation, since I/O dominates the cost. In real scenario, the page fault service time could largely be absorbed by the waiting time for CPU scheduling, in particular with round-robin scheduling.