4I68
ANYTHING I/O
MANUAL

1.4

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GENERAL

DESCRIPTION

The MESA 4I68 is a general purpose programmable I/O card for the PC/104-PLUS bus. The 4I68 uses a 200K or 400K gate Xilinx Spartan3 FPGA for all logic, so it is truly an "Anything I/O" card. The FPGA is downloadable from the PC/104-PLUS bus side, allowing creation of almost any kind of specialized I/O function, even including micro-controllers in the FPGA.

Several pre-made functions are provided, including a 72 bit parallel I/O card with three 24 bit ports a 12 channel host based servo motor controller, a 8 channel micro-controller based servo motor controller (*Soft*DMC), and a 8 channel, 32 bit timer counter card capable of running at 100 MHz. VHDL source is provided for all examples.

A bus mastering PCI bridge is used to support high bandwidth I/O. 10 LVDS pairs are available on one I/O connector for high speed card-card interfaces.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 4I68 card is oriented in an upright position, that is, with the PC/104-PLUS connector on the top and the white PCB markings right side up.

PC/104-PLUS SLOT NUMBER

PC104-PLUS cards have a slot number setting that cooresponds to the physical PCI slots on standard PCI systems. No two I/O cards in a PC104-PLUS stack can have the same slot number. The slot numbers are assigned with jumpers W3 and W4. The following table shows 4I68 slot numbers:

W3	W4	SLOT
DOWN	DOWN	0
DOWN	UP	1
UP	DOWN	2
UP	UP	3

HARDWARE CONFIGURATION

EEPROM ENABLE

The PLX9054 PCI-Local bus bridge chip is configured at power up via a serial EEPROM. If the EEPROM is somehow mis-programmed or corrupted, it can be impossible to re-write the EEPROM from the PC/104-PLUS bus. To avoid this problem, The EEPROM can be temporarily disabled. W2 controls the EEPROM enable function, When W2 is in the up position (default) the EEPROM is enabled. When W2 is in the down position, the EEPROM is disabled. To fix a broken EEPROM setup, you must power up the 4I68 card with the EEPROM disabled, Enable the EEPROM, and re-write the EEPROM.

CONNECTOR POWER

The power connection on the I/O connectors can supply either 3.3V or 5V power. Supplied power should be limited to 400 mA total.

W6 selects the power supplied to P1. (The right hand I/O connector) When W6 is in the up position, 5V power is supplied to P1. When W6 is in the down position, 3.3v power is supplied to P1.
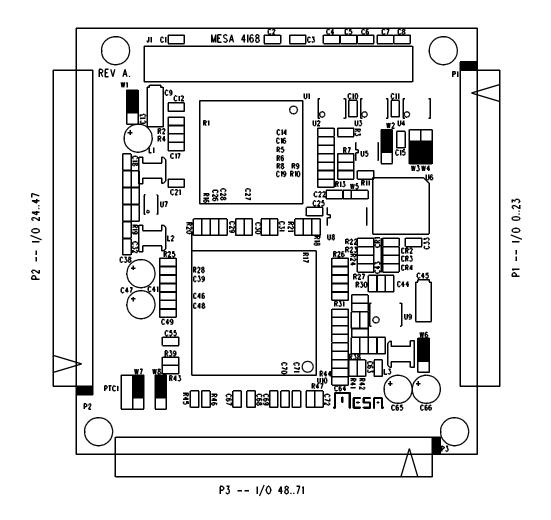
W1 selects the power supplied to P2. (The left hand I/O connector) When W1 is in the left position, 5V power is supplied to P2. When W1 is in the right position, 3.3v power is supplied to P2.

W7 selects the power supplied to P3. (The bottom I/O connector) When W7 is in the up position, 5V power is supplied to P3. When W7 is in the down position, 3.3V power is supplied to P3.

P3 IOVCC

The IO bank that connects to P3 can have 3.3V or 2.5V power. This is intended to allow LVDS operation on connector P3. Jumper W8 selects the IOVCC for this bank. When W8 is in the up position, 3.3V IOVCC is selected for the bank connected to P3. When W8 is in the down position, 2.5V is selected for the bank connected to P3.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS

CONNECTORS

I/O CONNECTORS

P1, P3, and P4 are the 4I68's I/O connectors. These are 50 pin box headers that mate with standard 50 conductor female IDC connectors. For information on which I/O pin connects to which FPGA pin, please see the 4I68IO.PIN file on the 4I68 distribution disk. 4I68 IO connector pinouts are as follows:

P1 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO0	2	GND	3	IO1	4	GND
5	IO2	6	GND	7	IO3	8	GND
9	IO4	10	GND	11	IO5	12	GND
13	IO6	14	GND	15	IO7	16	GND
17	IO8	18	GND	19	IO9	20	GND
21	IO10	22	GND	23	IO11	24	GND
25	IO12	26	GND	27	IO13	28	GND
29	IO14	30	GND	31	IO15	32	GND
33	IO16	34	GND	35	IO17	36	GND
37	IO18	38	GND	39	IO19	40	GND
41	IO20	42	GND	43	IO21	44	GND
45	IO22	46	GND	47	IO23	48	GND
49	POWER	50	GND				

CONNECTORS

I/O CONNECTORS

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO24	2	GND	3	IO25	4	GND
5	IO26	6	GND	7	IO27	8	GND
9	IO28	10	GND	11	IO29	12	GND
13	IO30	14	GND	15	IO31	16	GND
17	IO32	18	GND	19	IO33	20	GND
21	IO34	22	GND	23	IO35	24	GND
25	IO36	26	GND	27	IO37	28	GND
29	IO38	30	GND	31	IO39	32	GND
33	IO40	34	GND	35	IO41	36	GND
37	IO42	38	GND	39	IO43	40	GND
41	IO44	42	GND	43	IO45	44	GND
45	IO46	46	GND	47	IO47	48	GND
49	POWER	50	GND				

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO48/DN0	2	GND	3	IO49/DP0	4	GND
5	IO50/DN1	6	GND	7	IO51/DP1	8	GND
9	IO52/DN2	10	GND	11	IO53/DP2	12	GND
13	IO54/DN3	14	GND	15	IO55/DP3	16	GND
17	IO56/DN4	18	GND	19	IO57/DP4	20	GND
21	IO58/DN5	22	GND	23	IO59/DP5	24	GND
25	IO60/DN6	26	GND	27	IO61/DP6	28	GND
29	IO62/DN7	30	GND	31	IO63/DP7	32	GND
33	IO64/DN8	34	GND	35	IO65/DP8	36	GND
37	IO66/DN9	38	GND	39	IO67/DP9	40	GND
41	IO68	42	GND	43	IO69	44	GND
45	IO70	46	GND	47	IO71	48	GND
49	POWER	50	GND				

DIFFERENTIAL PAIRS

The 4I68 supports LVDS signaling on 10 pairs of the P3 I/O connector. The pairs are marked DPx and DPx in the table above. These signals are connected to the FPGA with 100 ohm impedance differential traces on the 4I68 PCB. Note that when LVDS is used, P3's VCCIO must be set to 2.5V.

OPERATION

FPGA

The 4I68 use a Xilinx Spartan-III 200K or 400K gate FPGA in a 208 pin QFP package: XC3S200-PQ208 or XC3S400-PG208.

FPGA PINOUT

The local bus and I/O interface FPGA pinouts are described in the 4I68INFC.PIN and 4I68IO.PIN files in CONFIGS directory of the distribution disk. The 4I68IO.PIN file may be used as a template for custom configurations.

MEMORY AND I/O REGIONS

The PLX9054 PCI bridge local configuration registers can be accessed via I/O or memory. These are used to setup the PCI bridge, and for manipulating the I/O bits when configuring the FPGA.

BAR	MEM - I/O	WIDTH	RANGE
BAR 0	MEMORY	32 BITS	128 BYTES
BAR 1	I/O	32 BITS	128 BYTES

The PLX9054 PCI bridge allows for 2 separate memory and I/O regions to be mapped to the local bus that connects to the FPGA. The default EEPROM configuration sets these up as follows:

BAR	ADDRESS SPACE	MEM - I/O	WIDTH	RANGE
BAR 2	0	I/O	32 BITS	256 BYTES
BAR 3	1	MEMORY	32 BITS	64K BYTES

LOCAL BUS INTERFACE

The 4I68 uses the multiplexed local bus option of the PLX9054 bridge chip to save FPGA pins. Because of the multiplexed bus, the FPGA interface logic must latch the LAD bus when ADS is active to create an internal address

OPERATION

CONFIGURATION

Before the 4I68 can do anything useful it must have its FPGA configuration data downloaded from the host CPU to the FPGA on the 4I68. This is done by writing a series of bytes from the configuration file to the 4I68 card's configuration data register. Configuration data is written a byte at a time (Right justified) to any of the I/O or memory bus space regions mapped to the 4I68s local bus.

The FPGA configuration control bits must be manipulated before configuration data can be sent to the FPGA. These control bits are controlled via GPIO pins of the PLX9054 PCI bridge. The PLX9054s GPIO pins are connected to the following FPGA configuration pins:

GPIO	DIRECTION	FPGA	ALTERNATE
GPI	IN	DONE	/DACK
GPO	IN	/PROGRAM	/DREQ

Note that the DONE and /PROGRAM bits are multiplexed with DMA control lines. If these DMA control lines are needed, the DISABLECONF pin on the FPGA needs to be asserted or a /DREQ signal will reset the FPGA.

UNUSED PINS

Due to the preferred idle local bus state on the 4I68, unused FPGA pins must be pulled up. This can be set in the 'Generate Programming File" properties box, configuration options tab, Unused IOB selection list.

SC4I68

A utility program SC4I68.EXE is provided to send configuration files to the 4I68. The Pascal and C source for this program is available on the distribution disk, and can be used as an example for writing a custom version of download software. SC4I68 is invoked with the FPGA configuration file and the 4I68 configuration base address on the command line:

```
SC4I68 FPGAFILE.BIN
```

SC4I68 uses binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC4I68 utility sends PROM files directly to the 4I68. BIT files have their headers stripped and are bit reversed before being sent to the 4I68.

OPERATION

CONFIGURATION

SC4I68W

Another utility SC4I68W is provided for Windows 2000 and Windows XP This utility requires the PLX9054.SYS driver and PLXAPI.DLL API SHIM to work. The source for SC4I68W can be used as an example of how to access the configured 4I68cards under Windows 2K or XP.

SC4I68 and SC4I68W use binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC4I68 utility sends PROM files directly to the 4I68. BIT files have their headers stripped and are bit reversed before being sent to the 4I68.

IO4I68

IO4I68 is a DOS demo program that accesses the IOPR24 configuration.

IO4I68W

IO4I68W is a Windows NT/2K/XP demo program that accesses the IOPR24 configuration and can be used as an example of low level card access on Windows systems, that use the PLX9054.SYS driver.

OPERATION

CLOCK SIGNALS

The FPGA has one on card clock source and 4 available clock inputs on I/O connector P3. The on card clock is 48 MHz routed to GCLK3. This functions as the FPGA system clock and the local bus interface clock. P3 I/O bits 56,57,58, and 59 correspond to GCLKs 7,6,5, and 4.

LEDS

The 4I68 has 4 FPGA driven user LEDs. The user LEDs can be used for any purpose, and can be helpful as a simple debugging feature. A low output signal from the FPGA lights the LED. See the 4I68IO.PIN file for FPGA pin locations of the LED signals.

IO LEVELS

The FPGA used on the 4I68 is a Spartan3. The Spartan3 supports many I/O standards. The 4I68 does not support use of the I/O standards that require input reference voltages, also VCCIO on the banks that connect to P1 and P2 are fixed at 3.3V so only 5 I/O options can be used on P1 and P2. The available I/O options for P1 and P2 are are LVTTL, LVCMOS_33, LVDCI_33, and LVDCI_33_DV2 . P3 can use a 2.5V VCCIO which adds the following I/O standards: LVCMOS_25, LVCMOS_25_DCI, LVDS_25, LVDS_25_DCI, LVDSEXT_25, LVDSEXT_25_DCI.

Note that the Spartan3 chip is _NOT_ 5V tolerant and should not have signals exceeding 3.3V applied to its inputs.

TERMINATION

The FPGAs used on the 4I68 support series and parallel termination that can be programmed on a pin-for-pin basis. This feature is called DCI. The 4I68 supports DCI on all I/O pins. The DCI reference resistors are all 100 Ohm 1%.

POWER SUPPLY

The 4I68 uses on card switching regulators to supply the 3.3VCC, 2.5VAUX/VIO and 1.2VCORE core power for the FPGA. The core power supply is rated at 1 Amp. The 3.3V and 2.5V power are limited to 600 mA. All power supplies are sourced from the 5V bus power.

SUPPLIED CONFIGURATIONS

IOPR12

The IOPR12 configuration creates a simple 72 bit parallel I/O port. IOPR12 is a word device, all accesses read or write 16 bit words. IOPR12 creates six 12 bit ports, 2 ports per I/O connector. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the IOPR12 configuration, see the regmap file in the /configs/IOPR12 directory of the 4I68 distribution disk.

IOPR24

The IOPR24 configuration creates a simple 72 bit parallel I/O port. IOPR24 is 32 bit device, all accesses read or write 16 bit words. IOPR24 creates three 24 bit ports, one port per I/O connector.. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the IOPR24 configuration, see the regmap file in the /configs/IOPR24 directory of the 4I68 distribution disk.

4I68LOOP

The IOPR24 configuration provides a simple way to check that all the I/O pins are OK and that most of the host interface is working. A loopback program (4I68LOOP) is provided for doing this testing. 4I68LOOP depends on an external loopback cable between I/O connectors P2, P3, and P4. 4I68LOOP perform a rotating bit test with one I/O connector programmed as outputs and the other two as inputs. All combinations of inputs and outputs are tested. In addition, a 32 bit register readback test is performed to verify 32 bit local data bus functionality.

HOSTMOT

The HOSTMOT configuration is a 12 channel host based servo motor controller. Host based controllers depend on the host CPU to "close" the servo loop. This has advantages and disadvantages. One advantage is that less hardware is needed, since host based software does all the math and handles all the control bits. Another advantage is that since the host based software is easily examined and modified, it is more amenable to customization and is more useful as a teaching tool. One disadvantage is that host based motor controllers depend on fast interrupt response time, since the control loop is an interrupt driven background task. This means that host based motor controllers don't tend to work well with multitasking operating systems such as Windows or Unix. They will work with real-time operating systems or simple operating systems like DOS.

SUPPLIED CONFIGURATIONS

HOSTMOT

The HOSTMOT configuration consists of twelve 32 bit quadrature counters to measure motor position, twelve 12 bit PWM generators for driving the motor, plus miscellaneous control and interrupt generation logic. For information on the register map of the HOSTMOT configuration, see the regmap file in the /configs/hostmot directory of the 4I68 distribution disk.

Demonstration software provided with the 4I68 implements a PID + feedforward control loop, plus a ramp-up, slew, ramp-down, profile generator for position control applications. Demo program (newmove.exe) and sources are located in the /configs/hostmot/support directory of the 4I68 distribution disk.

*SOFT*DMC

The *Soft*DMC configuration creates a 4 or 8 axis processor based servo motor controller, with the processor embedded in the FPGA. The *Soft*DMC configuration has the advantage that the embedded processor takes care of all time critical functions, so it can control motor position and motions without host intervention.

The *Soft*DMC configuration has programmable sample and PWM rates, and can operate 4 axis at up to 50 KHz sample rate and 8 axis at up to 25 KHz sample rate.

The control loop is a PID+F loop (F=feedforward) with 16 bit tuning parameters. Position and Velocity use 32 bit parameters for wide range.

The profile generator supports position,velocity, and homing modes. Position mode includes ramp-up, slew, ramp-down motions. Velocity mode supports breakpoints and a linked list parameter loading system for accurate profiling. Profile generator uses 48 bit accumulator to allow velocities from 2 turns per day (500 line - 2000 count encoder, 4 KHz sample rate) to 60,000 RPM.

There is a separate manual available for the *Soft*DMC motion controller.

Demo programs, and tuning program (dmctune.exe) and sources are located in the /configs/softdmc/support directory of the 4I68 distribution disk.

REFERENCE

SPECIFICATIONS

POWER	MIN	MAX	NOTES:
POWER SUPPLY	4.5V	5.5V	
POWER CONSUMPTION:	----	450 mA	Depends on FPGA Configuration
MAX 5V CURRENT TO I/O CONNS	---	500 mA	Total of all three
MAX 3.3V CURRENT TO I/O CONNS	---	300 mA	Total of all three
TEMPERATURE RANGE -C version	0 ^{o}C	+70 ^{o}C	
TEMPERATURE RANGE -I version	-40 ^{o}C	+85 ^{o}C	