Computer Organization Lab3

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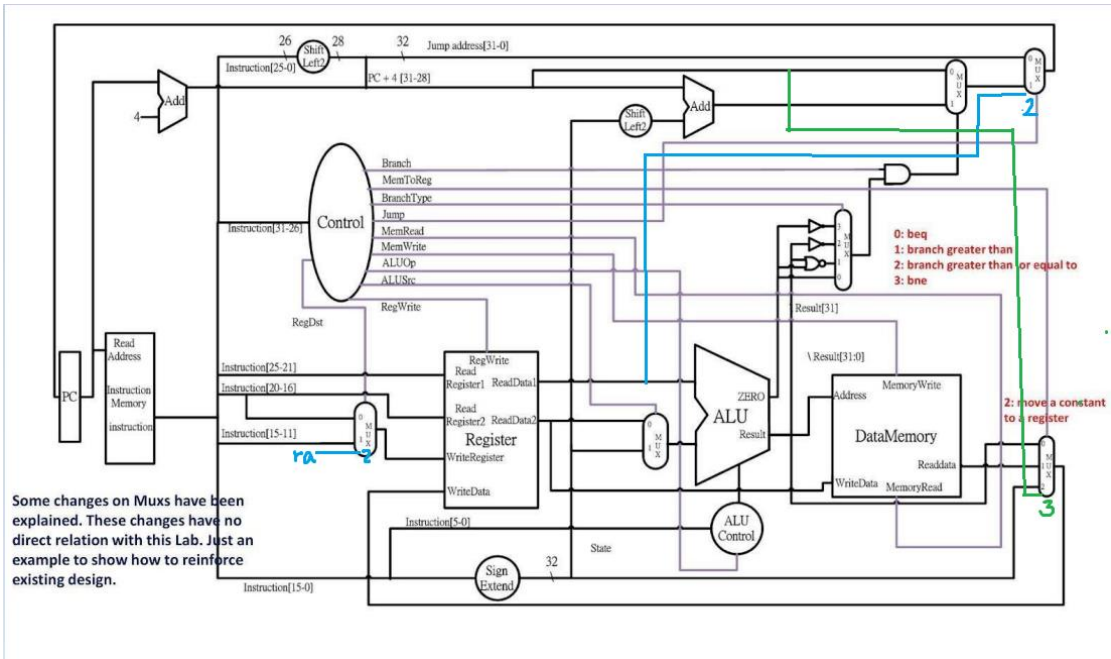
Architecture diagrams:



Hardware module analysis:

Simple_Single_CPU:整個 CPU 的架構，將 modules 用對應的線連接起來。裡面的 module 除了用到 lab2 的所有 module，還新增了 MUX_4to1，使得有些地方可以有 3 或 4 個輸入。整個 Simple_Single_CPU 用到 2 個 Adder、1 個 Decoder、1 個 Decoder、1 個 ALU、1 個 Decoder、1 個 Sign_Extend、2 個 Shift_Left_Two_32、2 個 MUX_2to1、4 個 MUX_4to1

Adder:兩個輸入等於輸出，用來算地址

Decoder:把從 Instr_Memory 得到的訊息分析得出 ALUOp, ALUSrc, branch, RegWrite, RegDst, MemToReg, BranchType, Jump, MemRead ,MemWrite

ALU_Ctrl:把輸入的訊息換成 ALU 要做的運算方式

ALU:依照 ALU_Ctrl 的輸出做運算

Sign_Extend:將 16bits 變成 32bits

Shift_Left_Two_32:往左移兩個 bits

MUX_2to1:依照輸入的 select 從兩個 data 中選擇一個輸出

MUX_4to1:依照輸入的 select 從四個 data 中選擇一個輸出

Finished part:

Testcase1 和 testcase2 跑出預期的結果

```
- Register File -
 r0 =    0  r1 =    1  r2 =    2  r3 =    3
 r4 =    4  r5 =    5  r6 =    1  r7 =    2
 r8 =    4  r9 =    2 r10 =    0 r11 =    0
r12 =    0 r13 =    0 r14 =    0 r15 =    0
r16 =    0 r17 =    0 r18 =    0 r19 =    0
r20 =    0 r21 =    0 r22 =    0 r23 =    0
r24 =    0 r25 =    0 r26 =    0 r27 =    0
r28 =    0 r29 =  128 r30 =    0 r31 =    0

- Memory Data -
 m0 =    1  m1 =    2  m2 =    0  m3 =    0
 m4 =    0  m5 =    0  m6 =    0  m7 =    0
 m8 =    0  m9 =    0 m10 =    0 m11 =    0
m12 =    0 m13 =    0 m14 =    0 m15 =    0
m16 =    0 m17 =    0 m18 =    0 m19 =    0
m20 =    0 m21 =    0 m22 =    0 m23 =    0
m24 =    0 m25 =    0 m26 =    0 m27 =    0
m28 =    0 m29 =    0 m30 =    0 m31 =    0
```

```
- Register File -
 r0 =    0  r1 =    0  r2 =    5  r3 =    0
 r4 =    0  r5 =    0  r6 =    0  r7 =    0
 r8 =    0  r9 =    1 r10 =    0 r11 =    0
r12 =    0 r13 =    0 r14 =    0 r15 =    0
r16 =    0 r17 =    0 r18 =    0 r19 =    0
r20 =    0 r21 =    0 r22 =    0 r23 =    0
r24 =    0 r25 =    0 r26 =    0 r27 =    0
r28 =    0 r29 =  128 r30 =    0 r31 =   16

- Memory Data -
 m0 =    0  m1 =    0  m2 =    0  m3 =    0
 m4 =    0  m5 =    0  m6 =    0  m7 =    0
 m8 =    0  m9 =    0 m10 =    0 m11 =    0
m12 =    0 m13 =    0 m14 =    0 m15 =    0
m16 =    0 m17 =    0 m18 =    0 m19 =    0
m20 =   68 m21 =    2 m22 =    1 m23 =   68
m24 =    2 m25 =    1 m26 =   68 m27 =    4
m28 =    3 m29 =   16 m30 =    0 m31 =    0
```

Problems you met and solutions:

這次 lab 中發現若曾經出現錯誤，修正完錯誤還是會出現錯誤訊息，因為仍可以正常模擬，所以可能之前都沒有發現。

[USF-XSim-62] 'compile' step failed with error(s). Please check the Tcl console output or 'C:/Users/sammy/Desktop/Computer Organization/lab3/lab3/lab3.sim/sim_1/behav/xsim/xvlog.log' file for more information.

[Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.

上網查後，只要重新開啟 Vivado 錯誤訊息就會消失了。

Summary:

這次的 lab 又比上次更加複雜，主要花時間在修改 decoder，只透過輸出很難判斷哪裡有錯，所以這次在除錯的時候練習觀察波形圖。此外這次新增了 MUX 4to1，但只有 3 個輸入的 MUX 就會有一個輸入沒有用到，目前先暫時填 0。