Exploring the Design Space of Mixed Swing QuadRail for Low-Power Digital Circuits

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***Abstract*—This paper describes and explores the design space of a mixed voltage swing methodology for lowering the energy per switching operation of digital circuits in standard submicron complementary metal–oxide–semiconductor (CMOS) fabrication processes. Employing mixed voltage swings expands the degrees of freedom available in the power-delay optimization space of static CMOS circuits. In order to study this design space and evaluate the power-delay tradeoffs, analytical posynomial formulations for power and delay of mixed swing circuits are derived and HSPICE simulation results are presented to demonstrate their accuracy. Efficient voltage scaling and transistor sizing techniques based on our analytical formulations are proposed for optimizing energy/operation subject to target delay constraints; up to 2.2× improvement in energy/operation is demonstrated for an ISCAS'85 benchmark circuit using these techniques. Experimental results from HSPICE simulations and measurements from an And-Or-Invert (AOI222) test chip fabricated in the Hewlett-Packard 0.5 μm process are presented to demonstrate up to 2.92× energy/operation savings for optimized mixed swing circuits compared to static CMOS.**

***Index Terms*—Digital circuit design, modeling, and optimization, mixed voltage swing techniques.**

I. Introduction

THE portable communications industry has been one of the fastest growing consumer market segments over the last five years, and is expected to grow even further in the near future. This growth has been accelerated by the strong demand for portable devices performing multimedia tasks, i.e., interfacing with information from the real-world environment (e.g., handwriting and speech recognition, image understanding) [1], [2]. With the primary bottleneck to portability being battery space and weight, there has been strong interest in exploring innovative low power digital circuit design techniques to prolong battery life between charges [3]. Even for desktop computing machines, rapidly increasing integration density and the accompanying onboard heat dissipation issues have made power reduction a top priority in the traditional performance-area-reliability design space. Most low-power circuit design methodologies have focused on using fully static complementary metal–oxide–semiconductor (CMOS) logic and lowering the power supply voltage below the maximum process-permitted voltage (voltage scaling) [4]. Voltage scaling represents the most effective means of power reduction, because of its quadratic influence on dynamic power consumption, typically the dominant component of total power in static CMOS circuits. However, scaling power supply voltage also leads to reduced drive currents, causing to increase gate delays steeply making them a substantial critical path delay contributor. This effectively imposes a lower bound on static CMOS voltage scaling. Architectural [4] and technological [5]–[7] solutions have been proposed to overcome this bottleneck and extend the lower bound. However, they have their limitations [4], [8]–[13], and more work is required toward exploring methodologies for lowering the power consumption of static CMOS circuits.

In this paper, we describe a multiple power-supply-voltage circuit methodology, that enables more aggressive voltage scaling than the fully static CMOS approach in a standard submicron bulk-CMOS fabrication process. Our methodology, called *Mixed Swing QuadRail* [14], [15], requires *four* power supply rails to be distributed to all circuits sharing this signalling methodology, in order to expand the degrees of freedom available in the power-delay optimization space of static CMOS circuits. Logic is performed in multiple stages by intermixing high and low swing signals and substantial savings in dynamic power compared to static CMOS is obtained by driving capacitive loads at reduced voltage swings.

In order to study Mixed Swing QuadRail's multiple voltage swing design space and evaluate the power-delay tradeoffs, analytical posynomial models for power and delay are developed. Sections II and III describe the QuadRail gate architecture and our power and delay models, respectively. Section III also describes comparisons of our power and delay models with HSPICE simulations to assess the models' accuracy and an analysis of QuadRail's power-delay tradeoffs. In Section IV, we propose efficient voltage scaling and transistor sizing techniques for optimizing QuadRail circuit performance and demonstrate their effectiveness. In Section V, experimental results from HSPICE simulations and measurements on an And-Or-Invert (AOI222) QuadRail test chip fabricated in the Hewlett-Packard (HP) 0.5 μm process are presented to study power-delay tradeoffs between QuadRail and static CMOS. Finally, our conclusions are presented in Section VI.

II. The Mixed Swing QuadRail Methodology

A. Gate Architecture

The essence of the Mixed Swing QuadRail methodology is that it allows the digital circuit designer to exploit the

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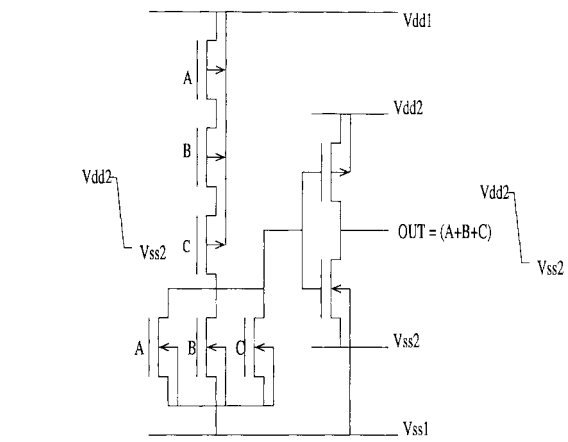
best aspects of both voltage scaling and full swing static CMOS logic. Fig. 1(a) shows the basic two-stage QuadRail gate architecture, consisting of a logic stage operating between the high swinging power supply rails (i.e., $Vdd1 - Vss1 = V_{\text{logic}}$) and a driver/buffer stage operating between the low swinging power supply rails (i.e., $Vdd2 - Vss2 = V_{\text{buffer}}$). The buffer stage is essentially a CMOS inverter, with high swinging inputs (V_{logic}) and low swinging outputs (V_{buffer}), both approximately centered to maximize noise margins and equalize rising and falling delays in either stage. PMOS devices in both stages are ratioed wider than the NMOS devices to roughly equalize their respective drive capabilities. The buffer transistor widths are ratioed by a factor $k(\geq 1)$ relative to that of logic stage transistors for improved buffer current over-drive. Each stage has its own N-well in order to minimize body effect on the PMOS devices, whereas the NMOS devices reside in the native P-substrate because our target fabrication process is an N-well process. Since the buffer devices are driven by approximately $(V_{\text{logic}}+V_{\text{buffer}})/2$, the on-drive currents remain quite high. This enables Vbuffer to be scaled well below the sum of the threshold voltages of the NMOS and PMOS devices while retaining good switching performance. In addition, the rise/fall times of the output nodes are improved due to the reduced voltage swings across them. The logic stage is identical to a CMOS inverting gate topology, except its inputs have reduced voltage swings (i.e., V_{buffer}). This is tolerable because the transition region in a static CMOS gate is smaller than the input range. The voltage swings are optimally selected to allow a small static current to flow in the logic stage, striking a balance between static power dissipation and performance. The high and low swing supplies are generated off-chip using efficient low voltage switching power supplies [16]. No dc path exists between supplies, ensuring a nearly quadratic reduction in dynamic power with the low voltage swing.

The Mixed Swing QuadRail methodology can be extended to three (or more) stages as shown in Fig. 1(b) to allow larger voltage differences between the highest and lowest swing stages by using intermediate logic stages. The intermediate stages can be either CMOS inverters or logic gates. Because the buffer's input swing is increased, the gate's output drive is greater for a given buffer size. Any number of high voltage logic stages can be cascaded to form more complex functions, and followed by a buffer to deliver the output to the next gate. This is desirable because grouping of several clustered gates into a single more complex gate reduces area, delay, and power.

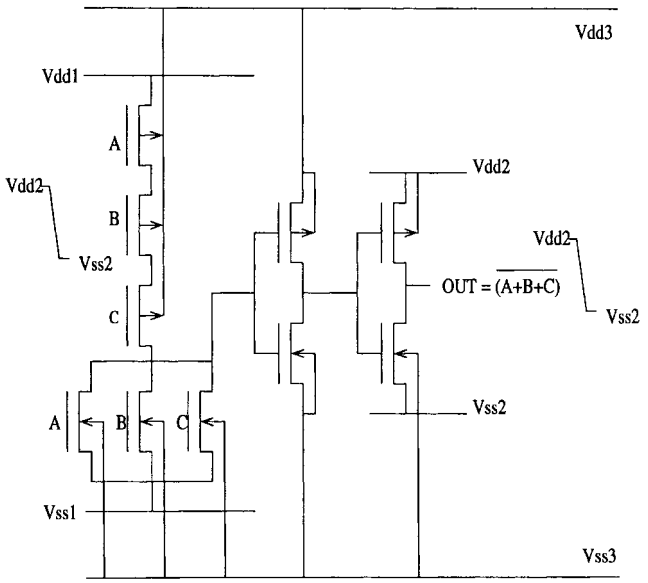
The analysis presented in the ensuing sections is specific to the two-stage QuadRail gate architecture [Fig. 1(a)], but it can be extended to three or more number of stages.

B. Noise Margin Analysis

As feature sizes continue to scale rapidly, noise immunity of submicron digital circuits, particularly at reduced power supply voltages, has become a metric of comparable importance as performance and power [17]. Noise immunity is particularly of concern in mixed voltage swing methodologies since buffer voltages (and hence I/O swings) are scaled well below the



(a)



(b)

Fig. 1. Mixed Swing QuadRail (a) two-stage and (b) three-stage gate architecture.

sum of the threshold voltages of the NMOS and PMOS transistors. Fig. 2 shows the two-stage QuadRail (logic and buffer stage) dc transfer characteristics for $V_{\text{logic}} = 2.2$ V and $V_{\text{buffer}} = 0.8$ V, obtained through HSPICE simulations using Level13, BSIM1 models in the HP 0.5 μm process (nominal NMOS and PMOS threshold voltages are 0.7 and -0.9 V, respectively). Despite considerable static current in the logic stage, the transfer characteristics are observed to be sharp, with fully restored outputs, due to multiple stages of gain and essentially Class-B switching. High and Low noise margins are almost equal and are approximately half of the I/O voltage swing $(V_{\text{buffer}}/2)$. Therefore, the lower bound on V_{buffer} is set by the minimum permissible noise margin constraints [18]. Note that the logic stage has a finite short circuit current due to the totempole current path between $Vdd1$ and $Vss1$ during switching. The buffer stage's short circuit current is negligible since V_{buffer} is smaller than the sum of the NMOS and PMOS threshold voltages.

Because of the high on-drive currents in both logic and buffer stages and steep output edges, primary sources of digital

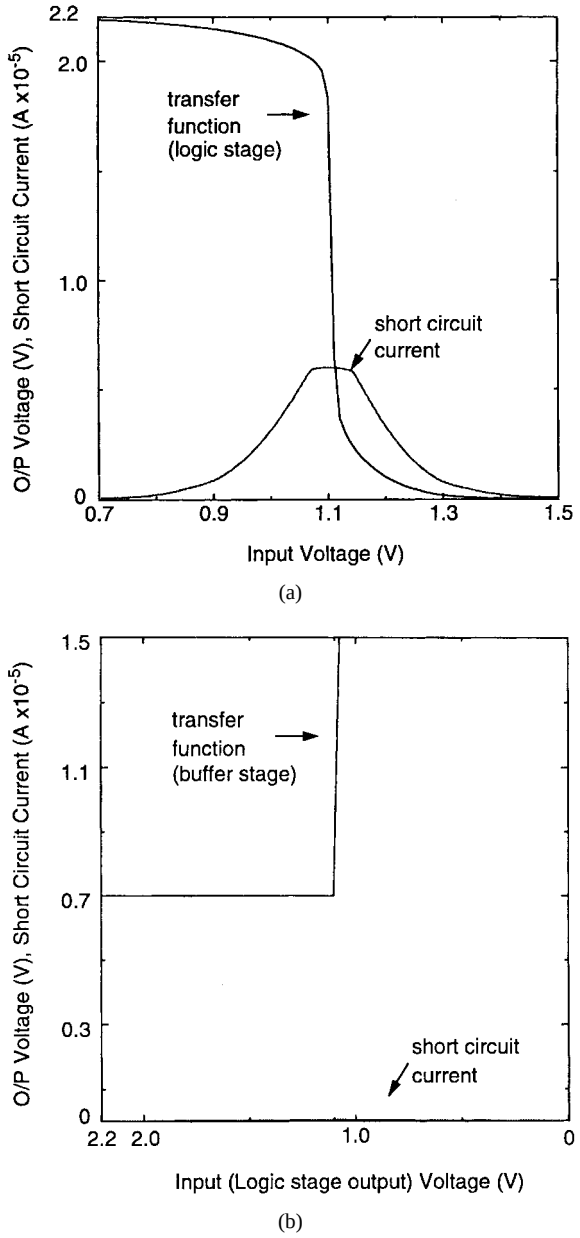


Fig. 2. Mixed swing QuadRail (a) logic stage and (b) buffer stage dc transfer characteristics.

circuit noise such as power/ground bounce due to simultaneous switching, substrate coupling, and crosstalk (particularly from high swing to low swing signals along the periphery of CMOS and QuadRail circuits) need to be carefully controlled in order to enable reliable voltage scaling. These concerns are best addressed by employing traditional noise reduction techniques (e.g., power/ground line despiking capacitors, segregation/shielding, and isolated substrate/well rails) [19] and developing CAD tools that can assess these problems and can design to meet noise margin specifications [20].

III. Mixed Swing QuadRail Power and Delay Models

Since Mixed Swing QuadRail performs multistaged logic and employs multiple voltage swings, additional degrees of freedom are introduced into the power-delay optimization space. Specifically, in two-stage QuadRail, the logic and buffer stage transistor sizes and voltage swings are our additional degrees of freedom. While the transistor sizes are local to every QuadRail circuit on-chip, the voltage swings are global across all QuadRail circuits on-chip. In this work, we assume the logic stage transistors to be unit-sized (1× NMOS, 2.5× PMOS) for minimum gate capacitance loading on the previous stage drivers.[1] Hence, the buffer transistor sizes and the two voltage swings are our available degrees of freedom, whose impact on QuadRail's power-delay space over a range of power supply voltages will be explored. The first step toward this goal is to develop analytical models for QuadRail power and delay in terms of both design factors and process parameters. Such models are essential because they enable 1) rapidly studying the power-delay tradeoffs in current and future fabrication processes and 2) casting and solving any QuadRail design optimization problem, particularly for large circuits. In this section, we develop QuadRail power and delay models from MOSFET I-V equations, compare their accuracy to HSPICE simulations, and evaluate power-delay tradeoffs in QuadRail circuits. We propose to model both QuadRail power and delay as posynomial functions[2] of buffer transistor size. Posynomial models for power and delay are widely used for solving transistor sizing and gate sizing optimization problems in static CMOS circuits [22]–[26].

One traditional approach employed in transistor-level optimization problems to model CMOS circuits is by modeling CMOS gates as RC-trees [19]. However, these models can deviate significantly from SPICE simulations, yielding suboptimal solutions [23], [24]. This is primarily due to not considering MOSFET short-channel effects which become significant at submicron feature sizes. On the other hand, developing accurate analytical models requires the usage of more precise MOSFET models, which are not only time-consuming but also require special device parameter extraction procedures [27]. Shockley's square-law MOSFET model [19] is widely used for simple analytical treatment of CMOS circuits but does not account for short-channel effects. The nth-Power Law MOSFET model [27], [28] has been proposed as an extension to the square-law model and accounts for carrier velocity saturation and channel length modulation, both of which are dominant short-channel effects in submicron devices. Here, n is the velocity saturation index, a process-dependent parameter extracted from device I-V characteristics and is approximately 1.0–1.5 for submicron processes [28]. This model has shown good agreement to measured I-V characteristics at least down to 0.25 μm feature sizes for

[1] We define 1× NMOS and 2.5× PMOS as the unit-size in the HP 0.5 μm process. This approximately equalizes drive capabilities of the NMOS and PMOS devices, giving roughly equal rising/falling delays and high/low noise margins for a static CMOS inverter in this process.

[2] From geometric programming, a posynomial function P of a positive variable $k \in R^m$ is defined as [21]

$$P(k) = \sum_j a_j \cdot \prod_{i=1}^{m} k_i^{b_{ij}} \tag{1}$$

and exhibits the distinct property that a local minimum of this function is a guaranteed global minimum. The coefficients a_j must be positive and b_{ij} must be real.

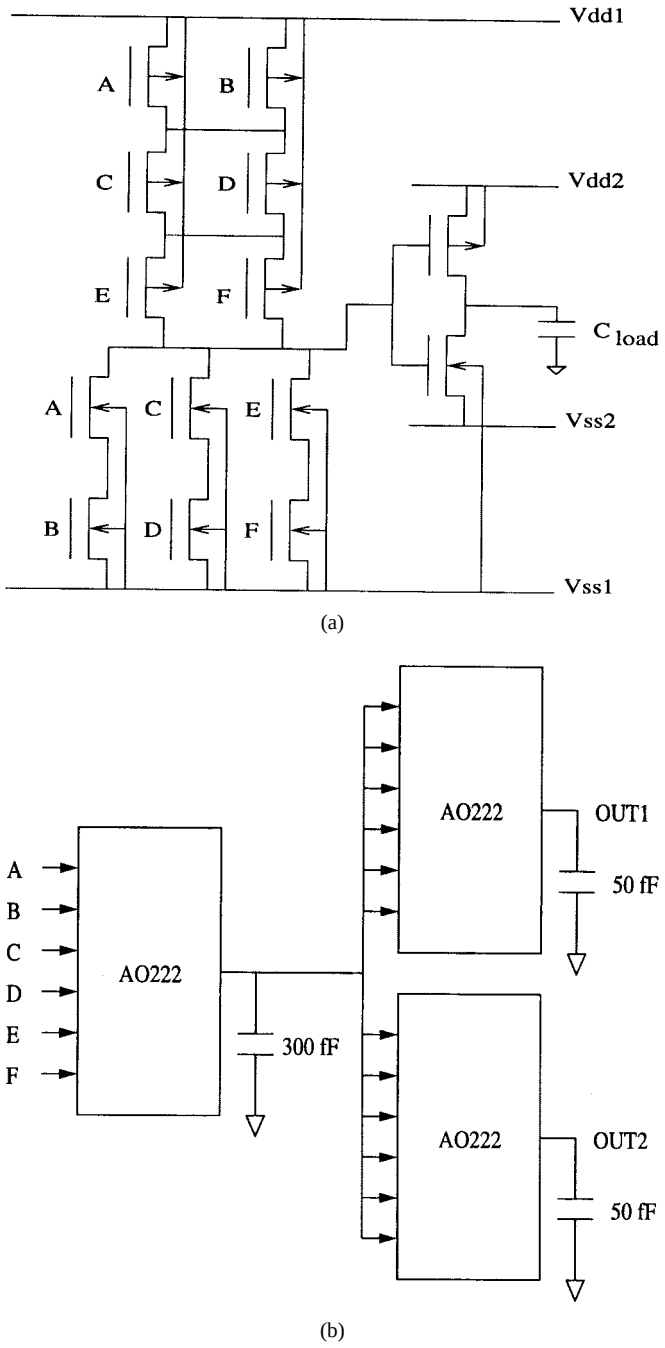


Fig. 3. QuadRail six-input AND-OR (AO222) gate and AO222 experimental circuit setup.

power supply voltages at or very close to the maximum process-permitted voltage [27]. At reduced voltages, since maximum gate-source and drain-source voltages are reduced, carriers are subjected to lesser electric fields both parallel and perpendicular to the channel. This significantly mitigates velocity saturation [29], increasing n from approximately 1.0 to 1.5 toward 2.0 at low voltages.

We propose to employ the nth-Power Law model I-V equations to develop our analytical formulations for QuadRail power and delay. Furthermore, we take into consideration input waveform slope (approximated as a ramp signal), because of its significant contribution to gate delay at low voltages and short circuit power dissipation [30]. Our models are derived as functions of n, and hence they may be used to explore QuadRail's design space in various current and future submicron processes. In Section III-C, we will demonstrate that our models show good agreement with HSPICE simulations using Level 13, BSIM1 models [31] in the HP 0.5 μm process.

A. Analytical Power Model

The dynamic power dissipated by a QuadRail gate driving a load capacitance Cload can be expressed as the sum of the energies drawn by each stage from their respective supply rails over one clock cycle [4], i.e.

$$P_{\text{dyn}} = \alpha \cdot k \cdot C_{\text{in}} (V_{\text{logic}})^2 \cdot f_{\text{clk}} + \alpha \cdot C_{\text{load}} \cdot (V_{\text{buffer}})^2 \cdot f_{\text{clk}} \quad (2)$$

where C_{in} is the input gate capacitance of a unit-sized buffer (1× NMOS +2.5× PMOS), α is the switching activity, f_{clk} is the input signal frequency, and k is the width of the buffer transistors relative to a unit-sized buffer, such that $k.C_{\text{in}}$ is the buffer stage's input capacitance. Parasitic source/drain capacitances for each stage are accounted for in C_{load} and kC_{in}. The short circuit power in the logic stage is derived for QuadRail similar to the static CMOS case in [28] and is approximately given by[3]:

$$P_{sc} = \frac{1}{n+1} \cdot \frac{1}{2^{n-1}} \cdot \frac{\beta_1}{2} \cdot (V_{\text{drive}} - 2V_{t1})^{n+1} \cdot t_T \cdot f_{\text{clk}} \quad (3)$$

where n is the velocity saturation index, β_1 is the equivalent transconductance gain factor of the logic stage for short channel devices [29], V_{drive} is the gate-source on-drive voltage, i.e., $(V_{\text{logic}} + V_{\text{buffer}})/2$, V_{t1} is the logic stage threshold voltage,[4] and t_T is the input rise/fall time. Note that (3) converges to the static CMOS short circuit power expression in [28] when $V_{\text{buffer}} = V_{\text{logic}}$. Static power dissipation in the logic stage is given by

$$P_{\text{static}} = I_{\text{off}} \cdot V_{\text{logic}} \quad (4)$$

where I_{off} is the logic stage off-current. If the logic stage gate-source off-drive voltage, i.e., $(V_{\text{logic}} - V_{\text{buffer}})/2$, is less (greater) than V_{t1}, the off devices are in subthreshold (strong inversion) and I_{off} is as defined in [4] (see also [27]). Both short circuit and static power dissipation are negligible for the buffer stage due to its reduced voltage swing and negative off-drive voltage respectively. As the buffer transistor size (k) increases, logic stage loading increases, increasing its dynamic power. This, however, decreases the buffer's switching time, reducing short circuit power in all receivers (this reduction is more significant for large fanouts). Then, total QuadRail power consumption may be modeled as

$$P_{\text{total}} = P_{\text{dyn}} + P_{\text{static}} + P_{\text{sc}} = A \cdot k + B + \frac{C}{k}. \quad (5)$$

[3] We will later (Section IV-A) develop an optimal voltage scaling approach for QuadRail and show that $V_{\text{logic}}, V_{\text{buffer}}$, and V_{t1} (which affects logic-stage off-currents) are not independent of each other, i.e., V_{drive} is related to V_{t1}.

[4] Similar to [28], we assume NMOS and PMOS threshold voltages to be equal in our derivation. For unequal threshold voltages, $2V_{t1}$ in (3) is replaced by $V_{t1\text{NMOS}} + |V_{t1\text{PMOS}}|$.

From (1) and (5) we observe that *QuadRail power dissipation is a posynomial function of buffer transistor size* (k) and there exists a global *power optimum* at which power is minimized.

B. Analytical Delay Model

Defining Δ as the separation between rails,[5] i.e., $Vdd1 - Vdd2 = Vss2 - Vss1$ from Fig. 1(a) and λ as the channel length modulation factor, the differential equation governing the logic stage's output node charging/discharging is given by [27]

$$k \cdot C_{\text{in}} \cdot \frac{dV_{\text{out}}}{dt} = \frac{\beta_1}{2} \cdot \left(\Delta + V_{\text{buffer}} \cdot \frac{t}{t_T} - V_{t1}\right)^n \cdot (1 + \lambda \cdot V_{\text{out}}) \tag{6}$$

where V_{out} is the time varying voltage across the buffer stage input capacitance. Solving the above first order differential equation yields the expression for 50% rising/falling delay of the logic stage as follows:

$$\begin{aligned}\text{Delay}_{\text{logic}} = {} & \frac{2 \cdot k \cdot C_{\text{in}}}{\beta_1 \cdot \lambda} \cdot \frac{1}{(\Delta + V_{\text{buffer}} - V_{t1})^n} \cdot \ln\left(\frac{V_{\text{logic}} + \frac{1}{\lambda}}{\frac{V_{\text{logic}}}{2} + \frac{1}{\lambda}}\right) \\ & t_T - \\ & + \left[\frac{t_T}{(n+1) \cdot V_{\text{buffer}}} \cdot \frac{1}{(\Delta + V_{\text{buffer}} - V_{t1})^n} \cdot \left((\Delta + V_{\text{buffer}} - V_{t1})^{n+1} - (\Delta - V_{t1})^{n+1}\right)\right].\end{aligned} \tag{7}$$

Similarly, the buffer stage 50% rising/falling delay expression is derived from its governing charging/discharging differential equation and is given by

$$\begin{aligned}\text{Delay}_{\text{buffer}} = {} & \left[\frac{C_{\text{load}}}{k \cdot \beta \cdot (\Delta + V_{\text{buffer}} - V_{t2})^{n-1}} \cdot \ln\left(\frac{4 \cdot (\Delta + V_{\text{buffer}} - V_{t2}) - V_{\text{buffer}}}{2 \cdot (\Delta + V_{\text{buffer}} - V_{t2}) - V_{\text{buffer}}}\right)\right] \\ & + m \cdot t_{1(r/f)}\end{aligned} \tag{8}$$

where $t_{1(r/f)}$ is the first stage outputs' 10–90% rise/fall time, given by

$$t_{1(r/f)} = \left[\frac{2 \cdot k \cdot C_{\text{in}}}{\beta_1 \cdot \lambda} \cdot \frac{1}{(\Delta + V_{\text{buffer}} - V_{t1})^n} \cdot \ln\left(\frac{0.9V_{\text{logic}} + \frac{1}{\lambda}}{\Delta + V_{\text{buffer}} - V_{t1} + \frac{1}{\lambda}}\right)\right]$$

$$\begin{aligned} & + t_T - \left[\frac{t_T}{(n+1) \cdot V_{\text{buffer}}} \cdot \frac{1}{(\Delta + V_{\text{buffer}} - V_{t1})^n} \cdot \left((\Delta + V_{\text{buffer}} - V_{t1})^{n+1} - (\Delta - V_{t1})^{n+1}\right)\right] \\ & + \left[\frac{k \cdot C_{\text{in}}}{\beta_1 \cdot (\Delta + V_{\text{buffer}} - V_{t2})^{n-1}} \cdot \ln\left(\frac{2 \cdot (\Delta + V_{\text{buffer}} - V_{t2}) - 0.1V_{\text{logic}}}{0.1V_{\text{logic}}}\right)\right]\end{aligned} \tag{9}$$

β is the transconductance gain factor of a unit-sized (1× NMOS, 2.5× PMOS) transistor, V_{t2} is the buffer stage threshold voltage,[6] and m is an empirically fitted constant for a given set of voltage swings.[7]

Increasing the buffer transistor size (k) leads to increased loading on the logic stage and hence logic stage delay. This, however, improves the buffer current drive, thereby decreasing buffer stage delay. Thus, *QuadRail delay is also a posynomial function of buffer transistor size* (k) and there exists a *delay optimum* at which delay is minimized.

C. Accuracy of Power, Delay models

In this paper, we will focus our study of power-delay tradeoffs in QuadRail in the HP 0.5 μm process. Through measurements on a QuadRail test chip fabricated in this process (to be described in Section V) and HSPICE simulations using Level13, BSIM1 models, we determined the value of n for this process to be approximately 2.0 for power supply voltages $\leq$3.0 V. In this section, we present comparisons of our models with HSPICE simulations using Level13, BSIM1 models. An experimental two-stage QuadRail circuit setup is considered for our comparisons as shown in Fig. 3. The setup consists of a six-input And-Or (AO222) gate cascade circuit. The driving gate drives all the fanout gates' inputs in addition to a capacitive load of 300 fF (corresponding to approximately 2500 μm of metal1 interconnect in the 0.5 μm process). The fanout gates have unit-sized buffer transistors. Fig. 4 shows the power (at 50 MHz with $\alpha = 1$) and delay for this setup obtained at one operating point: $V_{\text{logic}} = 2.2$ V and $V_{\text{buffer}} = 0.8$ V. Our models show good agreement to HSPICE simulation results; the optimal buffer transistor sizes (*power optimum and delay optimum*) predicted by our models is within 2% of HSPICE results over a range of operating voltage swings (up to 3.0 V) and capacitive loads, with the accuracy improving with reducing voltage swings. Note that both our models and HSPICE simulations correctly show a less steeper delay penalty for oversizing than undersizing as expected. This is due to the relative dominance of the logic and buffer stage delays in the total delay [(7) and (8), respectively].

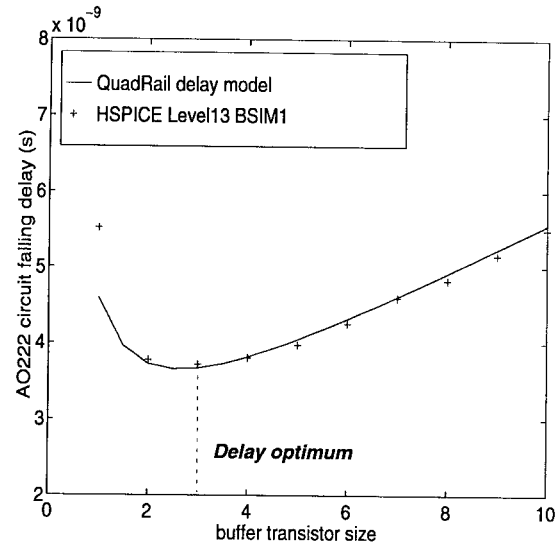
D. QuadRail Power, Delay Tradeoffs Analysis

In this section, we will employ our power and delay models to study the impact of our degrees of freedom on QuadRail's

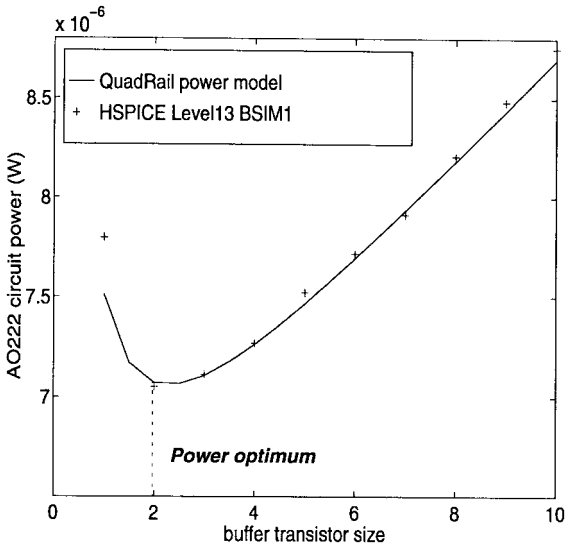
[5] For simplicity, we assume a single Δ in our derivation. The resulting delay model can be modified for unequal NMOS and PMOS threshold voltages by substituting Δ with $\Delta_1 = Vdd1 - Vdd2$ for pull-up delay and $\Delta_2 = Vss2 - Vss1$ for pull-down delay, for both logic and buffer stages.

[6] Logic and buffer stage threshold voltages, i.e., V_{t1} and V_{t2} are different because opposite type devices are in conduction in either stage for any input combination that causes a transition at the output.

[7] Since only a portion of the logic stage output's slope affects the buffer stage delay, the input waveform slope's contribution is empirically fitted through HSPICE Level13, BSIM1 models in our analysis.



(a)



(b)

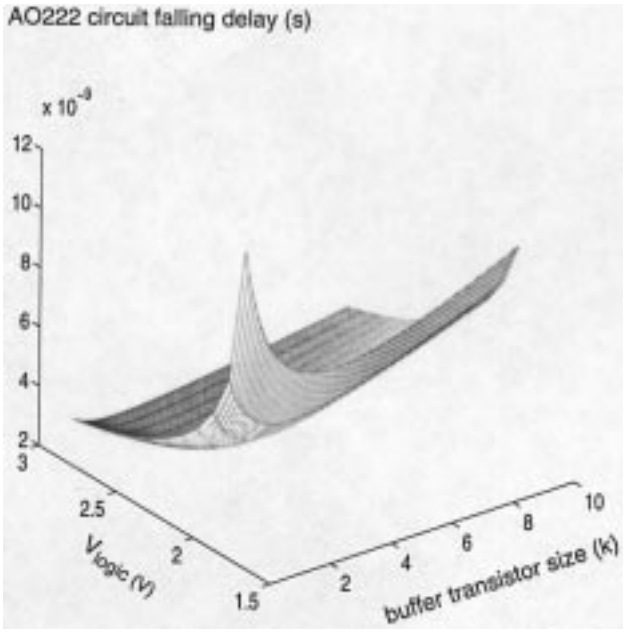
Fig. 4. QuadRail delay and power models compared to HSPICE Level13, BSIM1 model simulations.

power-delay space and evaluate the power delay tradeoffs in the HP 0.5 μm process. Fig. 5 shows the power and delay for the same circuit setup as in Fig. 3 obtained from our models with $V_{\text{buffer}} = 0.8$ V, buffer transistor size (k) for the driving gate varying from $1\times$ (unit-sized buffers) upto $10\times$, and V_{logic} varying from 1.5 to 3.0 V. Some important conclusions can be drawn from these graphs as follows.

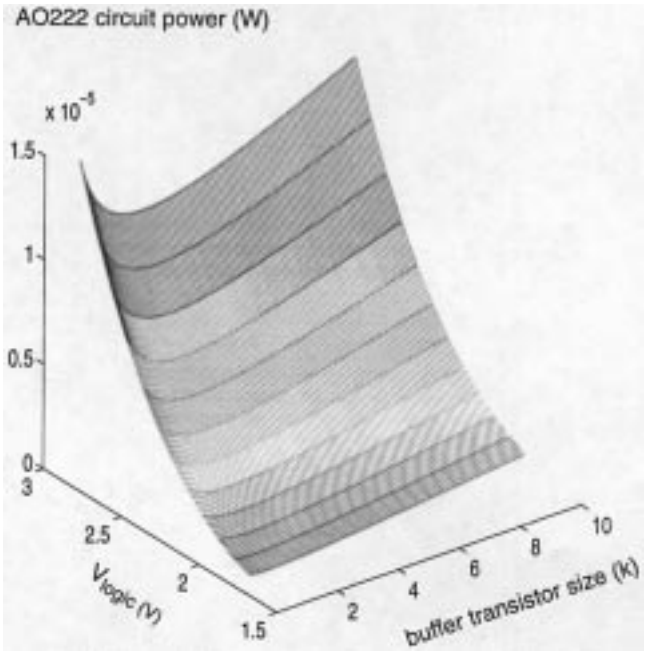
- As V_{logic} approaches 3.0 V, on-drive currents of both logic and buffer stages is increased, leading to reduced delays, despite an increase in the off-currents. Scaling V_{logic} toward 1.5 V causes a hyperbolic delay increase in both logic and buffer stages, consistent with Fig. 5(a) and classical to static CMOS-based gate topologies [19].
- As V_{logic} approaches 3.0 V, the increased buffer drive currents flatten the delay curve, i.e, the delay becomes less convex with increasing V_{logic}. Hence, although an optimal buffer transistor size exists at high logic stage voltage swings, the delay improvement obtained is not significant. Scaling V_{logic} toward 1.5 V, i.e., tighter logic stage turn-off, causes steep delay penalties for nonoptimal sizing, both for over- and undersized buffers. The delay penalties for not sizing the buffer transistors at their *delay optimum* become more severe with even smaller buffer voltage swings (i.e., $<$0.8 V) or increased capacitive loads. Section IV-B describes our approach for optimal buffer transistor sizing in QuadRail.
- As V_{logic} approaches 3.0 V, short circuit dissipation of the fanout gates is a significant component of total circuit power. This is particularly true with unit-sized buffers. When buffer transistor size is increased beyond unit size, the driving gate's output edge becomes steeper lowering the short circuit power of the fanout gates and hence total power, consistent with Fig. 5(b). When buffer size increases beyond the *power optimum*, dynamic power due to increased capacitive load dominates and total power starts increasing monotonically with buffer transistor size. Scaling V_{logic} toward 1.5 V diminishes short circuit power cubically, and power penalty due to unit-sized buffers also diminishes. Thus, at reduced power supply voltage swings, although there exists a *power optimum*, it is very close to unit-size.
- As V_{logic} approaches 3.0 V, separation between logic and buffer stage swings is increased. Consequently, totempole off-currents in logic stage are substantially increased beyond nominal leakage currents. The increased static power dissipation may dominate total power, consistent with Fig. 5(b). Moreover, the increased static currents reduce the steepness of the transfer characteristics and degrade noise margins. Scaling V_{logic} toward 1.5 V causes improved turn-off lowering both static and dynamic power dissipation. Thus, selection of V_{logic} for a given V_{buffer} involves careful consideration of static currents and noise margin degradation. Selection of a global V_{buffer} itself is determined by minimum noise margin requirements and target clock frequency constraints. Section IV-A describes our approach for optimal voltage scaling in QuadRail.

E. QuadRail Power-Delay Product, Energy-Delay Product Tradeoffs Analysis

We now examine the effect of our degrees of freedom on QuadRail circuit power-delay product (PDP), i.e., power * delay, and energy-delay product (EDP), i.e., power * $(\text{delay})^2$. Fig. 6 shows the PDP and EDP for the same experimental setup as in Fig. 3. Since V_{logic} has orthogonal effects on power and delay, and since both QuadRail power and delay are posynomial functions of buffer transistor size, QuadRail PDP and EDP are two-dimensional (2-D) convex functions [21] of V_{logic} and buffer transistor size, i.e., there exists global optimal V_{logic} and k values at which PDP and EDP are minimized. Both nonoptimal voltage scaling and buffer transistor sizing causes steep PDP/EDP penalties, emphasizing the importance of optimally selecting these quantities both from power and delay perspectives.

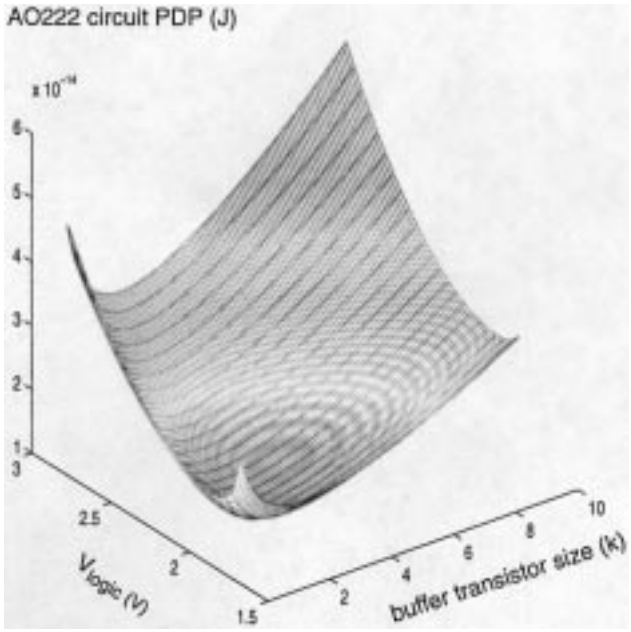


(a)

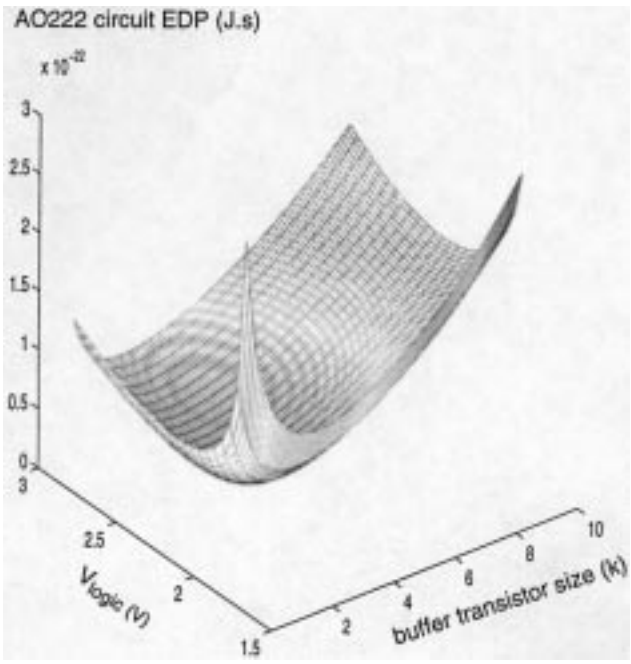


(b)

Fig. 5. AO222 circuit (a) falling delay and (b) power versus V_{logic} and buffer transistor size (k).



(a)



(b)

Fig. 6. AO222 circuit (a) PDP and (b) EDP versus V_{logic} and buffer transistor size (k).

IV. Mixed Swing Quadrail Circuit Optimization

For Mixed Swing QuadRail circuits, we assume the buffer voltage swing and hence I/O swing to be globally uniform to ensure I/O compatibility between different QuadRail modules on-chip as well as off-chip. From a power savings point of view we would like to operate at the absolute smallest V_{buffer} possible under noise margin constraints. Unfortunately, aggressive delay constraints may require using larger V_{buffer}'s for increased buffer drive currents, forcing us to pay the quadratic dynamic power penalty. Given a global V_{buffer} specification, we describe in this section, approaches to optimally select V_{logic} and buffer transistor sizes, and demonstrate their efficiency in optimizing the energy/operation of an ISCAS'85 combinational benchmark circuit given various target clock frequencies. We do not place a constraint on total active area, but this feature can be introduced easily at the cost of obtaining suboptimal solutions [24].

A. Optimal Voltage Scaling

As mentioned in Section III-D, selection of V_{logic} for a given V_{buffer} in QuadRail is critical for optimizing static power as well as noise margin degradation. In order to ensure

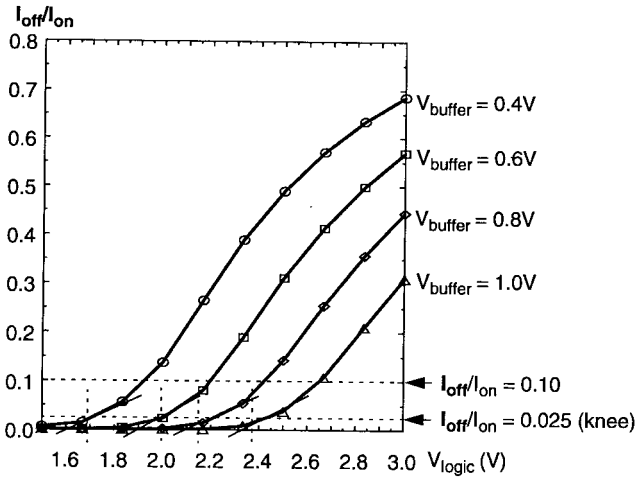


Fig. 7. Off- to on-drive current ratios versus logic stage voltage.

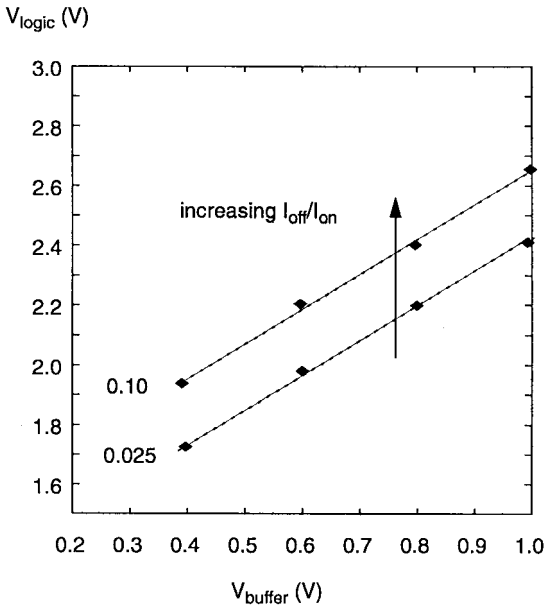


Fig. 8. Logic versus buffer stage voltage swing with $I_{\rm off}/I_{\rm on} = 0.025$ and 0.10.

adequately turned-off devices in the logic stage, we must restrict the off-currents to a small fraction of the average on-drive currents, striking a balance between static and dynamic power. Fig. 7 shows the ratio of logic stage totempole off-current $(I_{\rm off})$ to the worst-case on-drive current $(I_{\rm on})$ versus $V_{\rm logic}$ for $V_{\rm buffer}$ from 0.4 to 1.0 V for the three-input OR gate [see Fig. 1(a)] obtained through HSPICE simulations. It is observed that all graphs have two distinct regions—a steeply falling region where $I_{\rm off}$ falls quadratically with $V_{\rm logic}$ due to strong inversion, and a flat region where $I_{\rm off}$ falls exponentially with $V_{\rm logic}$, due to subthreshold conduction. Ion falls linearly with $V_{\rm logic}$ in both regions. Selecting an $I_{\rm off}/I_{\rm on}$ ratio defines unique logic voltage swings at these buffer voltage swings; the smaller this ratio, the better the turn-off.

If α is the circuit switching activity, N_d is the average logic gate depth per pipeline stage, and f_{clk} is the maximum operating clock frequency for a QuadRail circuit, then the QuadRail logic stage's average on-drive current can be written similar to [32] as

$$I_{\rm on} = N_d \cdot (k \cdot C_{\rm in}) \cdot V_{\rm logic} \cdot f_{\rm clk} \tag{10}$$

where $k \cdot C_{\rm in}$ is as defined in Section III-A. Then, the optimal $I_{\rm off}/I_{\rm on}$ ratio to balance static power, $I_{\rm off} \cdot V_{\rm logic}$ and dynamic power, $\alpha \cdot (k \cdot C_{\rm in}) \cdot V_{\rm logic}^2 \cdot f_{\rm clk}$, is given by

$$\left.\frac{I_{\rm off}}{I_{\rm on}}\right|_{\rm optimal} = \frac{\alpha}{N_d}. \tag{11}$$

Our result is the same as that derived in [32] for static CMOS circuits; since the QuadRail gate's logic stage is identical to a static CMOS gate topology, the expressions for optimal $I_{\rm off}/I_{\rm on}$ ratio are identical as well.

As an example, $I_{\rm off}/I_{\rm on}$ ratios of 0.025 (corresponding to the "knee" points) and 0.1 are chosen from Fig. 7, corresponding to $\alpha = 0.025$ and 0.1 respectively (since we are considering a single QuadRail gate in Fig. 7, $N_d = 1$ for this case). The static currents are approximately 2.5% and 10% of the average on-drive currents. Fig. 8 shows these example points on a $V_{\rm logic}$ versus $V_{\rm buffer}$ plot. It is observed that the graphs are approximately linear, and each point on this line defines a unique pair of voltage swings satisfying the desired $I_{\rm off}/I_{\rm on}$ ratio. In general, any QuadRail circuit with an activity factor α and an average gate depth N_d is mapped onto the $V_{\rm logic}$ vs. $V_{\rm buffer}$ space as an approximate linear plot, having the form

$$V_{\rm logic} \approx V_{\rm buffer} + \delta \cdot \left.\frac{I_{\rm off}}{I_{\rm on}}\right|_{\rm optimal} \cdot 2V_{t1} \tag{12}$$

where δ is an empirically fitted constant and the optimal $I_{\rm off}/I_{\rm on}$ ratio for that circuit is defined by (11) and is the same at every point on the linear plot. Note that as the $I_{\rm off}/I_{\rm on}$ ratio approaches zero, $V_{\rm logic}$ approaches $V_{\rm buffer}$, i.e., fully static CMOS operation. Exactly which operating point $(V_{\rm buffer}, V_{\rm logic})$ is selected on this line depends on the designer's target clock frequency specifications; tighter delay constraints will force selection of higher voltage swings requiring higher power penalties. Thus, scaling down operating logic and buffer voltage swings along this line offers an efficient technique for simultaneous reduction of static and dynamic power, without degrading noise margins while ensuring adequately tight turn-off characteristics.

B. Optimal Buffer Transistor Sizing

From (8) it is seen that for large load capacitances, typical along critical delay paths of digital circuits, unit-sized buffers have inadequate current drives and high delays. Since QuadRail delay is modeled as a posynomial function, there exists an optimal buffer transistor size for which delay is minimized. This *delay optimum* is computed for every critical path gate as follows:

From (7) to (9), total QuadRail gate delay can be expressed as

$$\text{Delay}_{\rm total} = A \cdot k + B + C \cdot \frac{1}{k} \tag{13}$$

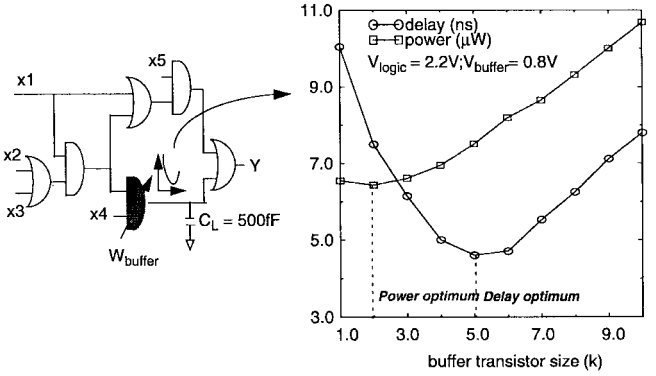


Fig. 9. Optimal buffer transistor sizing for an example critical circuit delay path.

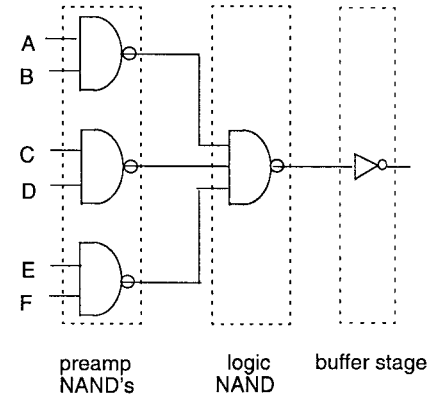


Fig. 11. Three-stage AOI222 gate construction.

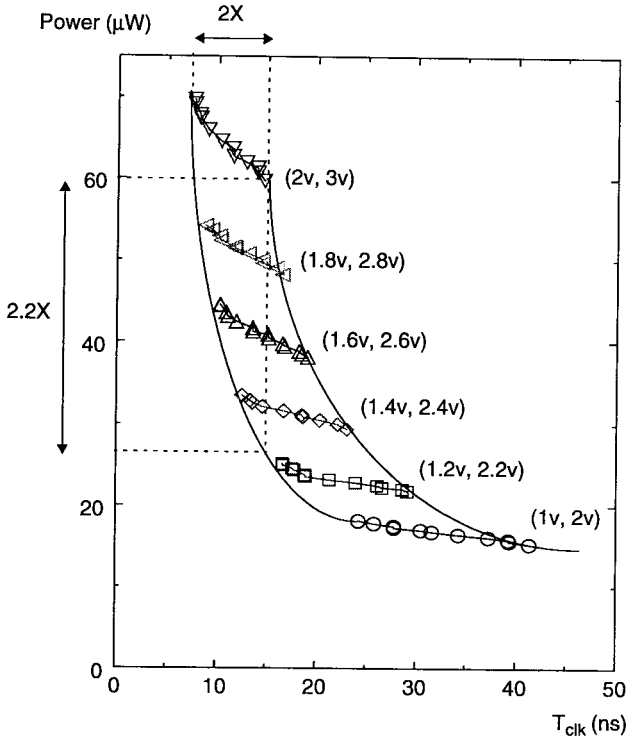


Fig. 10. Effect of optimal voltage scaling and buffer transistor sizing on QuadRail power-delay characteristics.

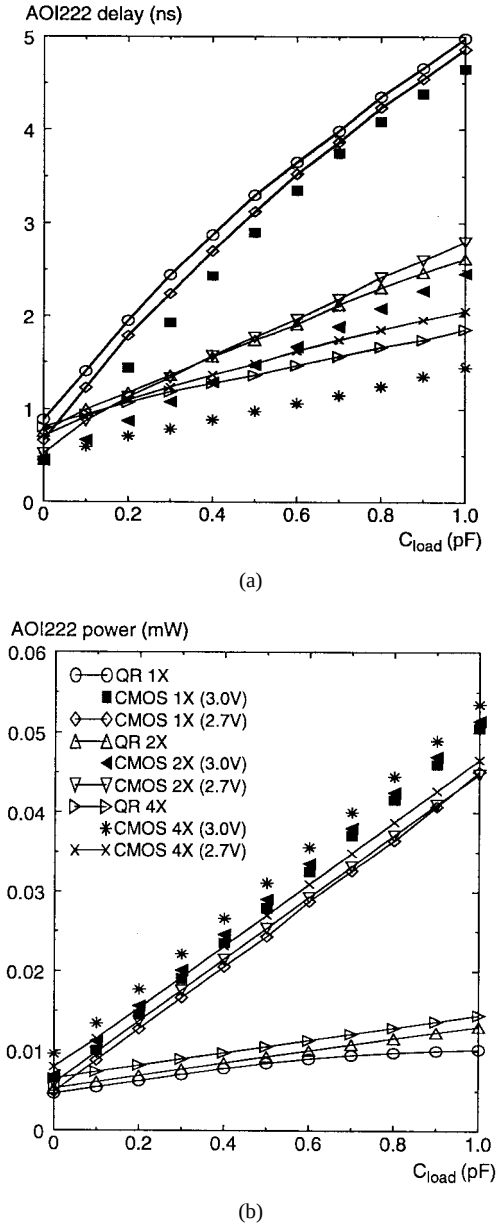


Fig. 12. QuadRail versus CMOS power-delay tradeoffs: AOI222 delay and power versus C_{load} for 1×, 2×, and 4× buffers.

where A, B, and C are the other design factors and process parameters independent of k from (7) to (9). This posynomial expression has a global minimum, which is the *delay optimum*, given by

$$k_{\mathrm{optimum}} = \sqrt{\frac{C}{A}}. \tag{14}$$

The optimal buffer transistor size depends on $\sqrt{C_{\mathrm{load}}}, \sqrt{\beta_1}$, and is a nonlinear function of the voltage swings. Since QuadRail power is also a posynomial function of buffer size, there exists a value of k, for which power is also minimized. This *power optimum* can be determined if the interconnect loading on a gate, and the logic and buffer transistor sizes of the fanout gates are known. In general, larger the fanout, larger the power reduction obtained due to sizing the driving buffers at this *power optimum.* Thus, a QuadRail circuit with all transistors sized minimally is neither delay optimal nor power optimal, and increasing the

TABLE I
AOI222 TEST CHIP POWER AND DELAY MEASUREMENTS

interconnect length (mm)	QuadRail power (μW)	CMOS power (μW)	QuadRail delay (ns)	CMOS delay (ns)
0.25	206	383	32.82	18.24
0.50	214	418	33.80	19.24
1.00	275	450	34.99	20.81
2.00	289	896	39.81	37.62

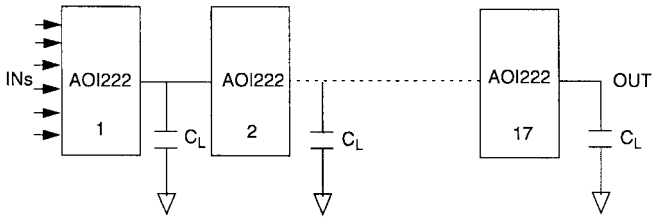


Fig. 13. QuadRail AOI222 test chip circuit setup.

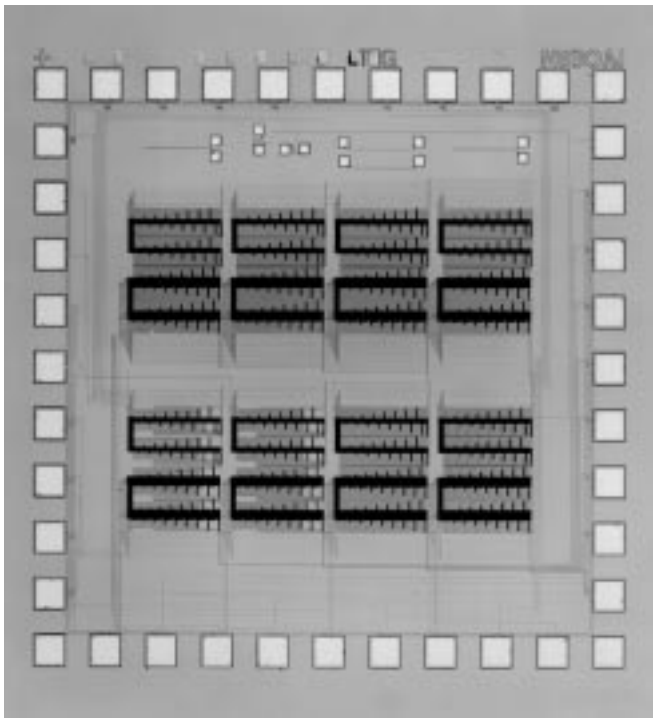


Fig. 14. Microphotograph of QuadRail AOI222 test chip.

buffer transistor size toward the *delay optimum* simultaneously offers a delay and power reduction. This continues until power starts to increase monotonically beyond the *power optimum.* Fig. 9 illustrates this behavior for an example critical circuit delay path containing a two-input AND gate driving a 500 fF capacitive load in addition to a single fanout. Also shown are the *power* and *delay optima* for the AND gate for $V_{\text{logic}} = 2.2$ V and $V_{\text{buffer}} = 0.8$ V in the HP 0.5 μm process. Increasing the AND gate's buffer transistor size beyond unit-size to its *power optimum* of $2\times$ offers only a slight reduction ($<2\%$) in its contribution to total power. However, sizing the buffer transistors at their *delay optimum* of $5\times$ offers a substantial reduction ($2.2\times$) in its contribution to critical path delay. Increasing the AND gate's buffer transistor size beyond the *power optimum* to the *delay optimum* costs additional dynamic power in its logic stage; the power penalty due to delay optimal sizing is 15% higher than with minimum sized buffers. Note that since the *power* and *delay optima* are functions of the voltage swings, they need to be recomputed for different global choices of logic and buffer voltage swings.

The effect of optimal voltage scaling and buffer transistor sizing on QuadRail's power-delay characteristics is demonstrated for an ISCAS'85 combinational benchmark circuit c17 [33], implemented in two-stage Mixed Swing QuadRail in the HP 0.5 μm process. Sensitivity of critical path gates is defined as $(-\Delta\text{delay}/\Delta k)$, i.e., reduction in delay per unit increase in buffer transistor size, and represents the gates most sensitive to optimal sizing. A range of logic and buffer voltage swings is considered ($V_{\text{logic}} = 2.0 - 3.0$ V and $V_{\text{buffer}} = 1.02.0$ V), governed by the linear relationship $V_{\text{logic}} = V_{\text{buffer}} + 1.0$, corresponding to an optimal $I_{\text{off}}/I_{\text{on}}$ ratio of 0.01. Through HSPICE simulations, this value of $I_{\text{off}}/I_{\text{on}}$ was found to balance static and dynamic power for this benchmark circuit. Starting with all buffers unit-sized, the buffers of critical path gates are optimally sized in decreasing order of their sensitivities to meet different target clock frequencies over our range of voltage swings. This is done until no further critical path delay improvement is obtained at each operating point $(V_{\text{buffer}}, V_{\text{logic}})$. Fig. 10 shows the power-delay characteristics for unit-sized buffer transistors (right), and with buffer transistors sized for the smallest delay constraint that could be met (left), over our range of voltage swings. Optimal scaling and sizing is observed to offer an essentially horizontal movement of the power-delay characteristics toward the origin, i.e., significant reduction in power for a target critical path delay specification. Alternately, this can be viewed as a significant improvement in maximum operable speed for a target power consumption budget. From Fig. 10, we observe that our optimization techniques offer up to $2.2\times$ reduction in energy/operation (at a target clock period of 15 ns) and a nearly $2\times$ improvement in maximum operable speed for this benchmark circuit.

V. MIXED SWING QUADRAIL VERSUS STATIC CMOS POWER-DELAY TRADEOFFS

In the previous sections, we studied power-delay tradeoffs and developed optimization techniques for the Mixed Swing QuadRail methodology. We now study power-delay tradeoffs between optimized QuadRail and static CMOS circuits, and demonstrate that the QuadRail methodology can offer substantial power savings in CMOS circuits where interconnect capacitance dominates gate capacitance.

The basis for our comparison is a six-input And-Or-Invert (AOI222) complex gate, constructed in a NAND-NAND-INVERT configuration in three stages (Fig. 11). The QuadRail AOI222 gate operates at $V_{\text{preamp}} = 2.0$ V and $V_{\text{logic}} = 3.0$ V. The buffer stage supply voltage and I/O swings are 1.0 V. The static CMOS AOI222 operates at $V_{dd} = 3.0$ V and at a

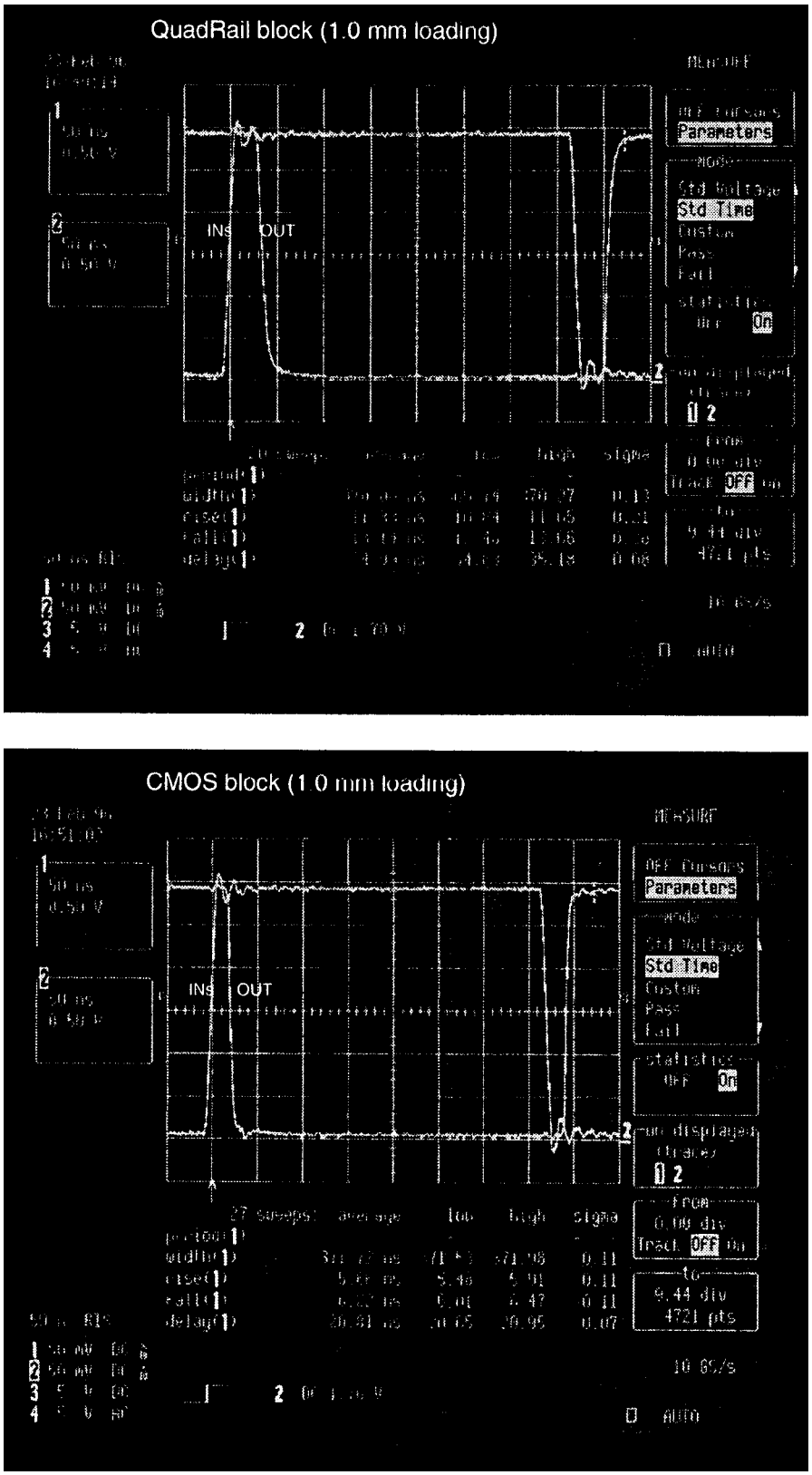


Fig. 15. QuadRail AOI222 test chip sample measured waveforms.

V_{dd} for which QuadRail and CMOS delays are approximately equalized at any load capacitance ($V_{dd} = 2.7$ V). Load capacitances in the range from 0 to 1 pF and buffer sizes of 1×, 2×, and 4× are considered for both cases. Fig. 12 shows the worst-case delay and power consumption (at 100 MHz with $\alpha = 1$) of the CMOS and QuadRail AOI222, obtained through HSPICE simulations in the HP 0.5 μm process. Some important conclusions can be drawn from these graphs.

- Increasing the buffer transistor size from 1× (unitsize) to 4× (optimal size at $C_{\text{load}} = 1$ pF) causes a steep delay

reduction for both the QuadRail and CMOS gates. The delay reduction increases linearly with load capacitance, and at $C_{\text{load}} = 1$ pF, QuadRail (CMOS) delay improves by 63% (57%) due to optimal sizing.

- With increasing load capacitance, both QuadRail and CMOS delays increase with the same steepness, but QuadRail's power increases less steeply than CMOS due to the reduced load voltage swing. Thus, at $C_{\text{load}} = 1$ pF, with equal delays a 3.3× power reduction is obtained compared to CMOS, and a 3.8× power reduction is obtained compared to CMOS at $V_{dd} = 3.0$ V (corresponding delay penalty = 22%), when both are sized optimally for that load (4×). The power savings are even higher as load capacitance increases beyond our range of analysis. At small loads (<50 fF), CMOS and QuadRail power dissipation are almost equal at equal delays: this is due to QuadRail's significant logic stage static power dissipation.
- In submicron digital circuits, the power dissipated in driving interconnect capacitance loads can be a substantial component of total power consumption. As feature sizes continue to shrink, this component will grow even higher because interconnect capacitance, predominantly due to coupling and fringing, scales more slowly than gate capacitance. This implies that the buffer stage's input gate capacitance becomes less significant compared to the fraction of total load capacitance that is due to interconnect. Since the low swinging buffer stage drives these interconnect loads, QuadRail will demonstrate even higher power reduction at reduced feature sizes. The ratio of interconnect load to buffer input gate capacitance sets an upper bound on the amount of power savings achievable compared to full swing static CMOS.

To demonstrate these conclusions, a six-input AOI222 QuadRail test chip was fabricated in the HP 0.5 μm process. The experimental setup (Fig. 13) consists of 17 AOI222 gates cascaded together with each AOI222 driving the next AOI222's six inputs and an additional load of 0.25, 0.50, 1.0, and 2.0 mm of metal2 interconnect capacitance. The AOI222 gates are constructed as shown in Fig. 11. The QuadRail AOI222 cascade operating voltage swings are $V_{\text{preamp}} = 2.0$ V, $V_{\text{logic}} = 3.0$ V, and $V_{\text{buffer}} = 1.0$ V. The static CMOS AOI222 cascade operates at $V_{dd} = 3.0$ V. The buffer transistors are sized 2.5× for both CMOS and QuadRail gates. Table I summarizes the measured power (at 10 MHz with $\alpha = 1$) and input-pin to output-pin delay for the QuadRail and CMOS AOI222 blocks. It is observed that the power savings improve with increasing interconnect loading; a 3.1× power savings is achieved for QuadRail compared to CMOS for the 2 mm interconnect loading, corresponding to a capacitive load of approximately 200 fF in this process. At this load, QuadRail delay is 6% higher than CMOS, offering an overall energy/operation reduction of 2.92×. HSPICE fullchip simulation results are within 10% of these experimental measurements. The AOI222 test chip microphotograph is shown in Fig. 14. Sample measured waveforms from the QuadRail and CMOS blocks for the 1.0 mm interconnect capacitance loading are shown in Fig. 15.

VI. Conclusions

We have described and explored the design space of a mixed voltage swing methodology called Mixed Swing QuadRail. Analytical posynomial models for QuadRail power and delay are derived, that enable rapid evaluation of power-delay tradeoffs and casting and solving of optimization problems for large QuadRail circuits. The accuracy of these models is demonstrated through comparisons with HSPICE simulations using Level13, BSIM1 models in the HP 0.5 μm process. On the basis of conclusions drawn from these models, techniques are proposed for optimal voltage scaling and buffer transistor sizing of QuadRail circuits, and up to 2.2× improvement in energy/ operation is demonstrated for an ISCAS'85 benchmark circuit utilizing these techniques. Furthermore, experimental results from HSPICE simulations and an AOI222 test chip fabricated in the HP 0.5 μm process show that the QuadRail methodology can offer significant energy/operation savings compared to static CMOS in digital circuits where the interconnect capacitance dominates gate capacitance.

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