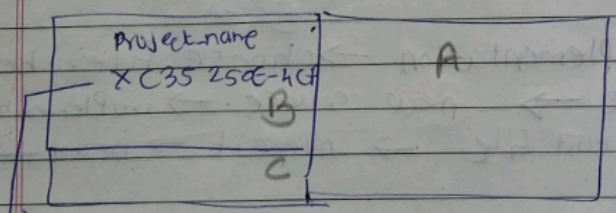
Exp-01

Click on ISE design suit 14 ⇒ from Xilinx (प्रोग्राम्स)

file → New project → name → next → finish

Property name	value
Evaluation dev Board	none
Product category	All
family	SPartan3E
Device	XC3S250E
Package	CP132
Speed	-4
TOP level Source type	HDL
Synthesis Tool	XST
Simulator	ISim
Preferred lang	VHDL
Property Specific	Store all value
VHDL Source analysis standard	VHDL-93



→ click this → right click → new source
→ VHDL model → give filename → next

Port name	Direction
a, b	in
sel	in
op	out

next → finish → write code

Select the file below device
→ save
Now in C Part → Synthesis →
check syntax → after all
errors gone → again synthesis
→ view RTL schematic → start
with explor results → ok →
add → create ⊙ schematic

Select file below device → New source →
VHDL Testbench → name it → next → finish
→ write code
go to simulator in B →
ISim - Simulator

① → Behavioural check
Syntax
② → simulate behavioural
model

implementation → choose file below
device → new source → implementation
constraint file → name it → next → finish

Select second file from device below
→ user constraint → edit constraint
→ write code

Select file below device →
implement design → Run
in C

generate programming file in C

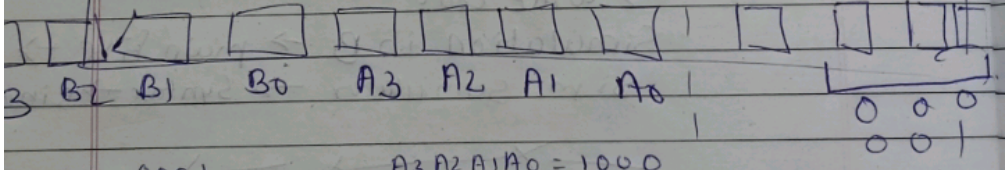
digilent software (D)

Connect the Board Basys2

FPGA
XC3S250E

PROM

(2) Program
(1) Browse (select the main file below device)



Suppose 0001 A3 A2 A1 A0 = 1000

1 + 8 = 9 while push button 0000

EXP-04

new source → VHDL

Port name | Direction | Bus | MSB | LSB

→ clk, rst, enr, enW | in | X | MSB 3 — 0

↓ enable read ↓ enable write

→ datain | in | ✓ | 3 | 0

→ dataout | out | ✓ | 3 | 0

→ full, emply | out

→ write code in A → click main file → synthesis → check syntax → synthesis → view RTL schematic → ok → add → create schematic

main file → New source → VHDL

testbench → name it → Finish

→ write code

Simulation in B → main file → sim simulator → syntax → simulate