

nRF51822

Multiprotocol *Bluetooth*® 4.0 low energy/2.4 GHz RF SoC

Product Specification v1.3

Key Features

- 2.4 GHz transceiver
 - -93 dBm sensitivity in *Bluetooth*® low energy mode
 - 250 kbps, 1 Mbps, 2 Mbps supported data rates
 - TX Power -20 to +4 dBm in 4 dB steps
 - TX Power -30 dBm Whisper mode
 - 13 mA peak RX, 10.5 mA peak TX (0 dBm)
 - RSSI (1 dB resolution)
- ARM® Cortex™-M0 32 bit processor
 - 275 µA/MHz running from flash memory
 - 150 µA/MHz running from RAM
 - Serial Wire Debug (SWD)
- S100 series SoftDevice ready
- Memory
 - 256 kB or 128 kB embedded flash program memory
 - 16 kB RAM
- Support for non-concurrent multiprotocol operation
 - On-air compatibility with nRF24L series
- Flexible Power Management
 - Supply voltage range 1.8 V to 3.6 V
 - 2.5 µs wake-up using 16 MHz RCOSC
 - 0.4 µA @ 3 V OFF mode
 - 0.5 µA @ 3 V in OFF mode + 1 region RAM retention
 - 2.3 µA @ 3 V ON mode, all blocks IDLE
- 8/9/10 bit ADC - 8 configurable channels
- 31 General Purpose I/O Pins
- One 32 bit and two 16 bit timers with counter mode
- SPI Master
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Decoder (QDEC)
- AES HW encryption
- Real Timer Counter (RTC)
- Package variants
 - QFN48 package, 6 x 6 mm
 - WLCSP package, 3.50 x 3.83 mm

Applications

- Computer peripherals and I/O devices
 - Mouse
 - Keyboard
 - Multi-touch trackpad
- Interactive entertainment devices
 - Remote control
 - 3D Glasses
 - Gaming controller
- Personal Area Networks
 - Health/fitness sensor and monitor devices
 - Medical devices
 - Key-fobs + wrist watch
- Remote control toys

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Datasheet Status

Status	Description
Objective Product Specification (OPS)	This product specification contains target specifications for product development.
Preliminary Product Specification (PPS)	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product Specification (PS)	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Revision History

Date	Version	Description
May 2013	1.3	Updated schematics and BOMs in Section 11.3 on page 61 .
April 2013	1.2	Added chip variant nRF51822-CEAA. Updated feature list on front page. Updated <i>Section 3.2.1 on page 15, Section 3.2.2 on page 15, Chapter 6 on page 28, Section 10.4 on page 52, and Section 10.5.1 on page 53.</i> Added <i>Section 2.2.2 on page 10, Section 7.1 on page 29, Section 9.2 on page 50, and Section 11.3 on page 61.</i> Removed PCB layouts in <i>Chapter 11 on page 54</i> .
March 2013	1.1	Added chip variant nRF51822-QFAB. Added 32 MHz crystal oscillator feature. Updated feature list on front page. Moved subsection 'Calculating current when the DC/DC converter is enabled' from chapter 8 to the nRF51 Reference Manual. Updated <i>Chapter 1 on page 6, Section 2.2 on page 8, Section 3.2 on page 14, Section 3.5 on page 18, Section 3.5.1 on page 19, Section 4.2 on page 23, Chapter 5 on page 26, Section 8.1 on page 30, Section 8.1.2 on page 31, Section 8.1.5 on page 33, Section 8.2 on page 35, Section 8.3 on page 37, Section 8.5.3 on page 39, Section 8.8 on page 43, Section 8.9 on page 44, Section 8.10 on page 45, Section 8.14 on page 46, Chapter 10 on page 51, Section 11.2.3 on page 59, Section 11.2.1 on page 55, and Section 11.2.2 on page 57.</i> Added <i>Section 3.5.4 on page 21, Section 8.1.3 on page 32, and Section 11.1 on page 54.</i>
November 2012	1.0	Changed from PPS to PS. Updated feature list on front page. Updated <i>Table 13 on page 28, Table 14 on page 29, Table 16 on page 31, Table 18 on page 33, Table 19 on page 33, Table 20 on page 34, Table 23 on page 36, Table 24 on page 37, Table 26 on page 38, Table 27 on page 38, Table 28 on page 39, Table 32 on page 42, Table 33 on page 43, Table 35 on page 44, Table 38 on page 45, Table 39 on page 46, Table 42 on page 47, Table 45 on page 48, Table 46 on page 48, Table 61 on page 53, and Figure 15 on page 59.</i>

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1 Introduction

nRF51822 is an ultra-low power 2.4 GHz wireless System on Chip (SoC) integrating the nRF51 series 2.4 GHz transceiver, a 32 bit ARM® Cortex™-M0 CPU, flash memory, and analog and digital peripherals. nRF51822 can support *Bluetooth*® low energy and a range of proprietary 2.4 GHz protocols, such as Gazell from Nordic Semiconductor.

Fully qualified *Bluetooth* low energy stacks for nRF51822 are implemented in the S100 series of SoftDevices. The S100 series of SoftDevices are available for free and can be downloaded and installed on nRF51822 independent of your own application code.

nRF51822 is available in different package and memory variants. When data in this product specification does not apply to all variants, those variants it does apply to will be clearly stated. An example of a variant name is nRF51822-QFAA. If no variant name is stated, or if just nRF51822 is used, the data will apply to all versions of nRF51822.

1.1 Required reading

The *nRF51 Reference Manual* is required reading.

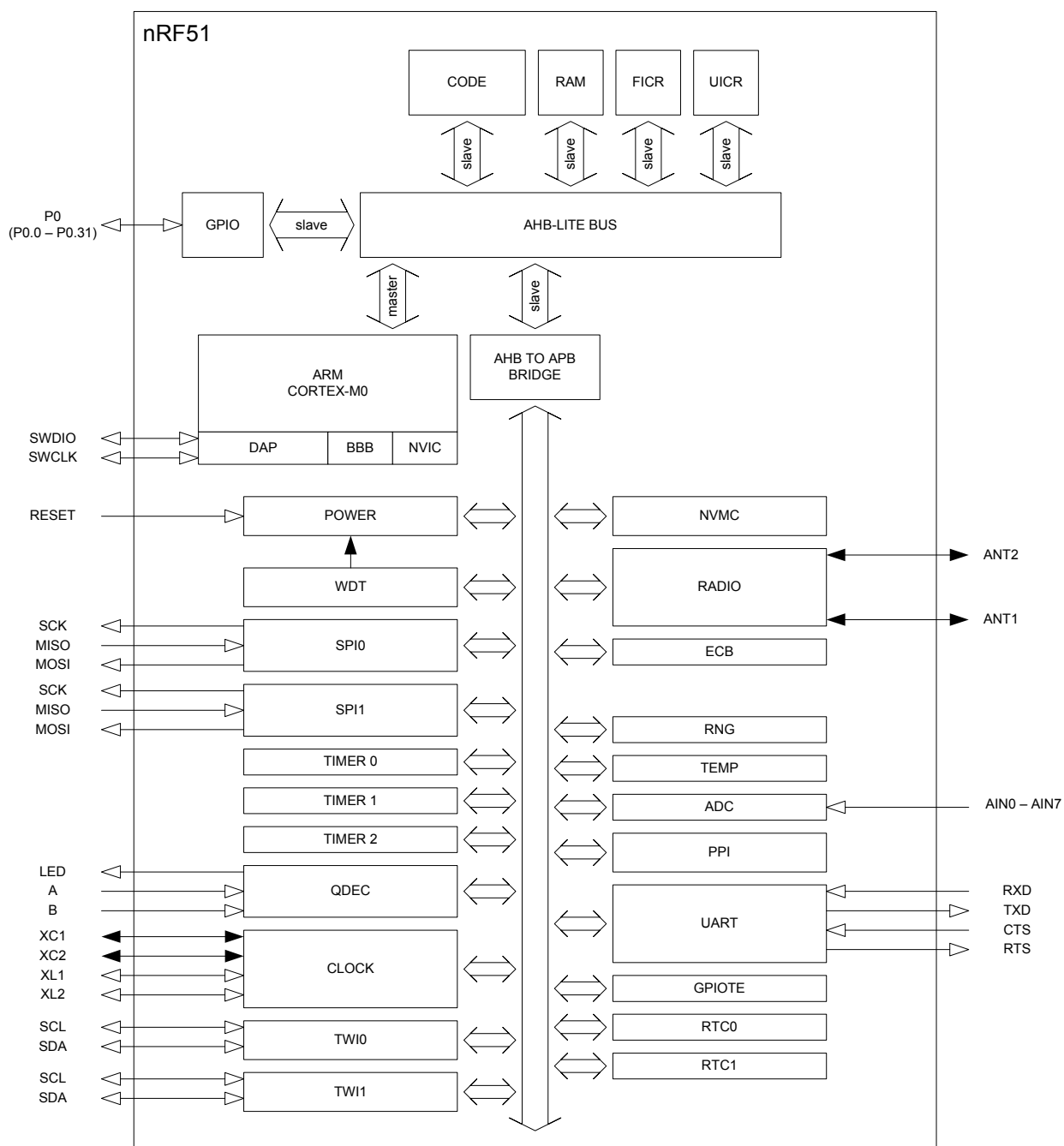
1.2 Writing conventions

This product specification follows a set of typographic rules to ensure that the document is consistent and easy to read. The following writing conventions are used:

- Command, event names, and bit state conditions, are written in `Lucida Console`.
- Pin names and pin signal conditions are written in `Consolas`.
- File names and User Interface components are written in **bold**.
- Internal cross references are italicized and written in ***semi-bold***.
- Placeholders for parameters are written in italic regular text font. For example, a syntax description of Connect will be written as:
`Connect(TimeOut, AdvInterval)`.
- Fixed parameters are written in regular text font. For example, a syntax description of Connect will be written as:
`Connect(0x00F0, Interval)`.

2 Product overview

2.1 Block diagram



Note: RESET is disabled by default.

Figure 1 nRF51822 block diagram

2.2 Pin assignments and functions

This section describes the pin assignment and the pin functions for the different packet types.

2.2.1 nRF51822 QFN48

2.2.1.1 Pin assignment

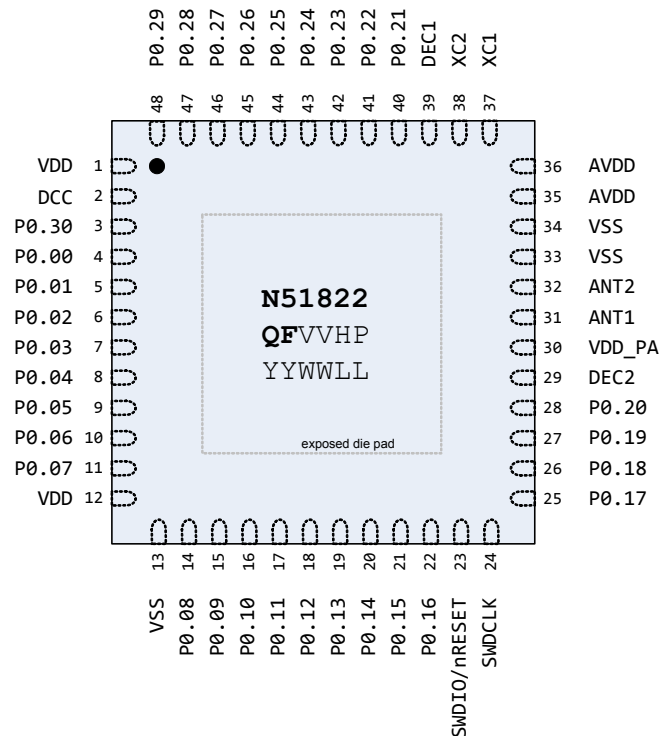


Figure 2 Pin assignment - nRF51822 QFN48 packet

Note: VV = Variant code, HP = Build code, YYWWLL = Tracking code.
For more information, see **Section 10.4 on page 52**.

2.2.1.2 Pin functions

Pin	Pin name	Pin function	Description
1	VDD	Power	Power supply
2	DCC	Power	DC/DC output voltage to external LC filter
3	P0.30	Digital I/O	General purpose I/O pin
4	P0.00 AREF0	Digital I/O Analog input	General purpose I/O pin ADC Reference voltage
5	P0.01 AIN2	Digital I/O Analog input	General purpose I/O pin ADC input 2
6	P0.02 AIN3	Digital I/O Analog input	General purpose I/O pin ADC input 3
7	P0.03 AIN4	Digital I/O Analog input	General purpose I/O pin ADC input 4
8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O pin ADC input 5
9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O pin ADC input 6
10	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O pin ADC input 7 ADC Reference voltage
11	P0.07	Digital I/O	General purpose I/O pin
12	VDD	Power	Power supply
13	VSS	Power	Ground (0 V) ¹
14 to 22	P0.08 to P0.16	Digital I/O	General purpose I/O pin
23	SWDIO/nRESET	Digital I/O	System reset (active low). Also HW debug and flash programming I/O
24	SWDCLK	Digital input	HW debug and flash programming I/O
25 to 28	P0.17 to P0.20	Digital I/O	General purpose I/O pin
29	DEC2	Power	Power supply decoupling
30	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp
31	ANT1	RF	Differential antenna connection (TX and RX)
32	ANT2	RF	Differential antenna connection (TX and RX)
33, 34	VSS	Power	Ground (0 V)
35, 36	AVDD	Power	Analog Power supply
37	XC1	Analog input	Connection for 16/32 MHz crystal or external 16 MHz clock reference
38	XC2	Analog output	Connection for 16/32 MHz crystal
39	DEC1	Power	Power supply decoupling

Pin	Pin name	Pin function	Description
40 to 44	P0.21 to P0.25	Digital I/O	General purpose I/O pin
45	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O pin ADC input 0 Connection for 32.768 kHz crystal
46	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O pin ADC input 1 Connection for 32.768 kHz crystal or external 32.768 kHz clock reference
47, 48	P0.28 and P0.29	Digital I/O	General purpose I/O pin

1. The exposed center pad of the QFN48 package must be connected to supply ground for proper device operation.

Table 1 Pin functions nRF51822 QFN48 packet

2.2.2 nRF51822 WLCSP

2.2.2.1 Ball assignment

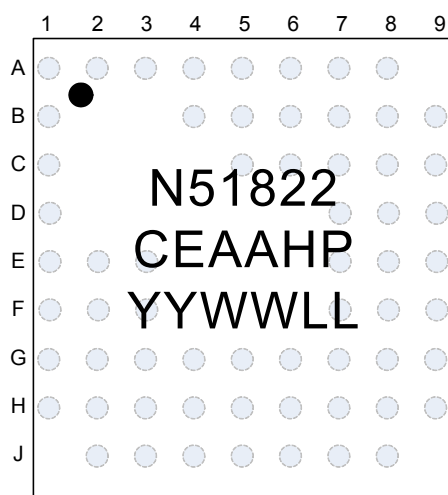


Figure 3 Ball assignment nRF51822-CEAA packet (top side view)

Note: HP = Buildcode, YYWWLL = Tracking code
Solder balls not visible on the top side. Dot denotes A1 corner.

2.2.2.2 Ball functions

Ball	Name	Function	Description
A1	AVDD	Power	Analog power supply
A2	XC1	Analog input	Crystal connection for 16/32 MHz crystal oscillator or external 16/32 MHz crystal reference
A3	XC2	Analog output	Crystal connection for 16/32 MHz crystal
A4	DEC1	Power	Power supply decoupling
A5	P0.21	Digital I/O	General purpose I/O
A6	P0.24	Digital I/O	General purpose I/O
A7	P0.26	Digital I/O	General purpose I/O
	AIN0	Analog input	ADC input 0
	XL2	Analog output	Crystal connection for 32.768 kHz crystal oscillator
A8	P0.27	Digital I/O	General purpose I/O
	AIN1	Analog input	ADC input 1
	XL1	Analog input	Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference
B1	VSS	Power	Ground (0 V)
B4	VSS	Power	Ground (0 V)
B5	P0.22	Digital I/O	General purpose I/O
B6	P0.23	Digital I/O	General purpose I/O
B7	P0.28	Digital I/O	General purpose I/O
B8	VDD	Power	Power supply
B9	DCC	Power	DC/DC output voltage to external LC filter
C1	ANT2	RF	Differential antenna connection (TX and RX)
C5	P0.25	Digital I/O	General purpose I/O
C6	N.C.	No Connection	Must be soldered to PCB
C7	P0.29	Digital I/O	General purpose I/O
C8	VSS	Power	Ground (0 V)
C9	P0.00	Digital I/O	General purpose I/O
	AREF0	Analog input	ADC Reference voltage
D1	ANT1	RF	Differential antenna connection (TX and RX)
D7	VSS	Power	Ground (0 V)
D8	P0.30	Digital I/O	General purpose I/O
D9	P0.02	Digital I/O	General purpose I/O
	AIN3	Analog input	ADC input 3
E1	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp
E2	N.C.	No Connection	Must be soldered to PCB
E3	N.C.	No Connection	Must be soldered to PCB
E7	N.C.	No Connection	Must be soldered to PCB
E8	P0.31	Digital I/O	General purpose I/O
E9	P0.01	Digital I/O	General purpose I/O
	AIN2	Analog input	ADC input 2

Ball	Name	Function	Description
F1	DEC2	Power	Power supply decoupling
F2	P0.19	Digital I/O	General purpose I/O
F3	N.C.	No Connection	Must be soldered to PCB
F7	N.C.	No Connection	Must be soldered to PCB
F8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O ADC input 5
F9	P0.03 AIN4	Digital I/O Analog input	General purpose I/O ADC input 4
G1	P0.20	Digital I/O	General purpose I/O
G2	P0.17	Digital I/O	General purpose I/O
G3	N.C.	No Connection	Must be soldered to PCB
G4	N.C.	No Connection	Must be soldered to PCB
G5	N.C.	No Connection	Must be soldered to PCB
G6	VSS	Power	Ground (0 V)
G7	N.C.	No Connection	Must be soldered to PCB
G8	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O ADC input 7 ADC Reference voltage
G9	VSS	Power	Ground (0 V)
H1	P0.18	Digital I/O	General purpose I/O
H2	SWDCLK	Digital input	HW debug and flash programming I/O
H3	VSS	Power	Ground (0 V)
H4	P0.14	Digital I/O	General purpose I/O
H5	P0.13	Digital I/O	General purpose I/O
H6	P0.10	Digital I/O	General purpose I/O
H7	P0.07	Digital I/O	General purpose I/O
H8	VDD	Power	Power supply
H9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O ADC input 6
J2	SWDIO/ nRESET	Digital I/O	System reset (active low). Also HW debug and flash programming I/O
J3	P0.16	Digital I/O	General purpose I/O
J4	P0.15	Digital I/O	General purpose I/O
J5	P0.12	Digital I/O	General purpose I/O
J6	P0.11	Digital I/O	General purpose I/O
J7	P0.09	Digital I/O	General purpose I/O
J8	P0.08	Digital I/O	General purpose I/O

Table 2 Ball functions for nRF51822-CEAA

3 System blocks

The nRF51822 contains system-level features common to all nRF51 series devices including clock control, power and reset, interrupt system, Programmable Peripheral Interconnect (PPI), watchdog, and GPIO.

System blocks which have a register interface and/or interrupt vector assigned are instantiated in the device address space. The instances of system blocks, their associated ID (for those with interrupt vectors) and base address are found in **Table 12 on page 26**. Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Reference Manual*.

3.1 CPU

The ARM® Cortex™-M0 CPU has a 16 bit instruction set with 32 bit extensions ([Thumb-2® technology](#)) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, a 3-stage pipeline and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M0 CPU makes program execution simple and highly efficient.

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex-M processor series is implemented and available for M0 CPU. Code is forward compatible with ARM Cortex M3 based devices.

3.2 Memory

All memory and registers are found in the same address space as shown in the Device Memory Map, see **Figure 4**. Devices in the nRF51 series use flash based memory in the code, FICR, and UICR regions. The RAM region is SRAM.

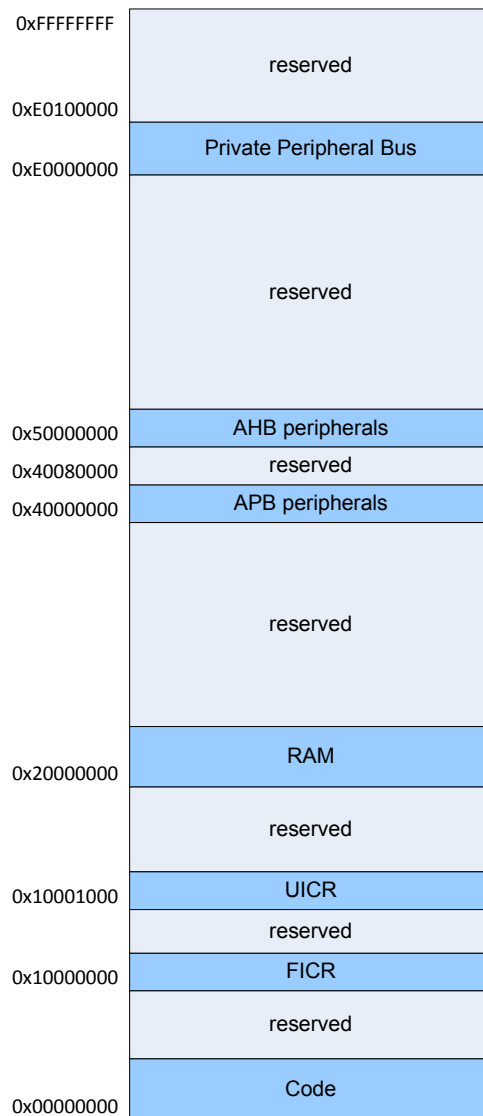


Figure 4 Device Memory Map

The embedded flash memory for program and static data can be programmed using In Application Programming (IAP) routines from RAM through the SWD interface, or in-system from a program executing from code area. The Non-Volatile Memory Controller (NVMC) is used for program/erase operations. It is also possible to set up the device to have readback protection on all or part of the code area by enabling readback protection in the UICR.

3.2.1 Code organization

Chip variant	Code size	Page size	No of pages
nRF51822-QFAA	256 kB	1024 byte	256
nRF51822-CEAA			
nRF51822-QFAB	128 kB	1024 byte	128

Table 3 Code organization

3.2.2 RAM organization

RAM is divided into blocks for separate power management as described in the *nRF51 Series Reference Manual*.

The RAM power management is controlled by the POWER System Block.

Chip variant	RAM size	Block	Start address	Size
nRF51822-QFAA	16 kB	Block0	0x20000000	8 kB
nRF51822-QFAB		Block1	0x20002000	8 kB
nRF51822-CEAA				

Table 4 RAM organization

3.3 Power management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, Radio Transceiver, and peripherals having separate power state control in addition to the global System ON and OFF modes. In System OFF mode, RAM can be retained and the device state can be changed to System ON through reset or GPIO signal. When in System ON mode, all functional blocks will independently be in IDLE or RUN mode depending on needed functionality.

Power management features:

- System ON/OFF modes
- Brownout reset
- Power fail comparator
- Pin wake-up from System OFF
- Functional block RUN/IDLE modes
- 2-region RAM retention in System OFF mode

Power supply features:

- Supervisor HW to manage power on reset, brownout, and power fail
- 1.8 to 3.6 V supply voltage range using internal LDO regulator
- 1.75 to 1.95 V low voltage mode (external voltage regulator is required)
- 2.1 to 3.6 V supply voltage range using internal buck DC/DC converter

3.3.1 Low voltage mode

Devices can be used in low voltage mode where a steady 1.8 V supply is available externally. To use the device in the low voltage mode, the circuit must be modified as per the reference circuitry provided in *Section 11.2.2 on page 57*.

3.3.2 DC/DC converter

The nRF51 DC/DC buck converter transforms battery voltage to lower internal voltage with minimal power loss. The converted voltage is then available to the linear regulator input. The DC/DC converter can be disabled when the supply voltage drops to the lower limit of the voltage range so the LDO can be used for low supply voltages. When enabled, the DC/DC converter operation is automatically suspended when only the low current regulator is needed internally.

This feature is particularly useful for applications using battery technologies with higher nominal cell voltages. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. Used with a 3 V coin-cell battery, the peak current drawn from the battery is reduced by approximately 30%.

Note: Three external passive components are required in order to use the DC/DC converter. See *Section 11.2.3 on page 59* for details on the schematic differences.

3.4 Programmable Peripheral Interconnect (PPI)

The Programmable Peripheral Interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. This feature allows precise synchronization between peripherals when application real-time constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

Instance	Number of channels	Number of groups
PPI	16	4

Table 5 PPI properties

3.5 Clock management (CLOCK)

The advanced clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. This prevents large clock trees being active and drawing power when no system modules needing this clock reference are active.

If an application enables a module that needs a clock reference without the corresponding oscillator running, the clock management system will automatically enable the RC oscillator option and provide the clock. When the module goes back to idle, the clock management will automatically set the oscillator to idle as well. To avoid delays involved in starting a given oscillator, or if a specific oscillator is required, the application can override the automatic oscillator management so it keeps oscillators active when no system modules require the clock reference.

Clocks are only available in System ON mode and can be generated by the following sources:

Clock	Source	Frequency options
High Frequency Clock (HFCLK) ¹	External Crystal (XOSC)	16/32 MHz ²
	External clock reference ³	16 MHz
	Internal RC Oscillator (RCOSC)	16 MHz
Low Frequency Clock (LFCLK)	External Crystal (XOSC)	32.768 kHz
	External clock reference ³	32.768 kHz
	Synthesized from HFCLK	32.768 kHz
	Internal RC Oscillator (RCOSC)	32.768 kHz

1. External Crystal must be used for Radio operation
2. The HFCLK will be 16 MHz for both the 16 and 32 MHz crystal option
3. See nRF51 reference manual for more details on external clock reference

Table 6 Clock properties

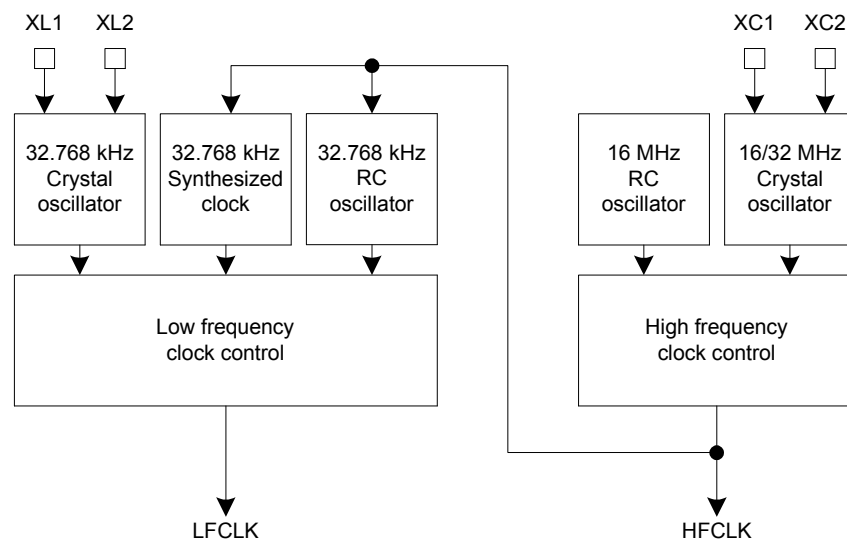


Figure 5 Clock management

3.5.1 16/32 MHz crystal oscillator

The crystal oscillator can be controlled either by a 16 MHz or a 32 MHz external crystal. However, the system clock is always 16 MHz, see the *nRF51 Reference Manual* for more details. The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. **Figure 6** shows how the crystal is connected to the 16/32 MHz crystal oscillator.

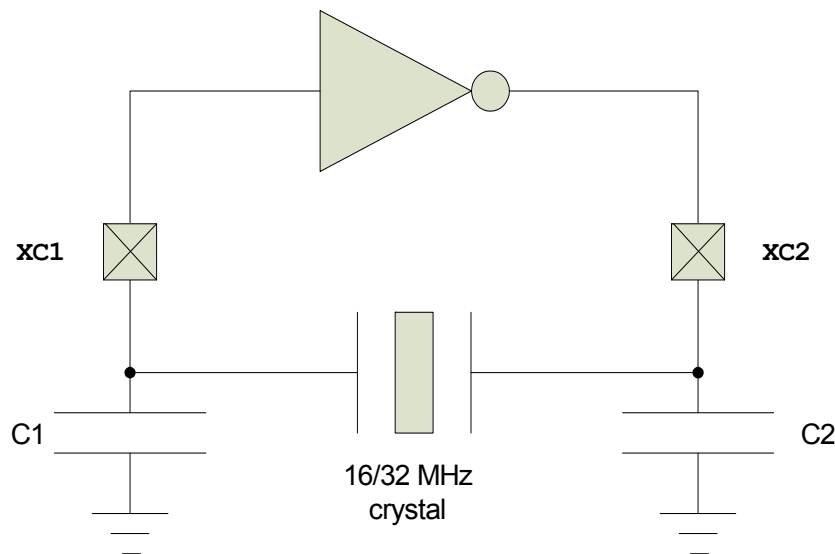


Figure 6 Circuit diagram of the 16/32 MHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2}¹ are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins, see **Table 16 on page 31** (16 MHz) and **Table 17 on page 32** (32 MHz). The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance (R_{S,X16M}/R_{S,X32M}), and drive level must comply with the specifications in **Table 16 on page 31** (16 MHz) and **Table 17 on page 32** (32 MHz). It is recommended to use a crystal with lower than maximum R_{S,X16M}/R_{S,X32M} if the load capacitance and/or shunt capacitance is high. This will give faster startup and lower current consumption. A low load capacitance will reduce both startup time and current consumption.

1. See **Chapter 11 on page 54** for the capacitance value used for C_{pcb1} and C_{pcb2} in reference circuitry.

3.5.2 32.768 kHz crystal oscillator

The 32.768 kHz crystal oscillator is designed for use with a quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. **Figure 7** shows how the crystal is connected to the 32.768 kHz crystal oscillator.

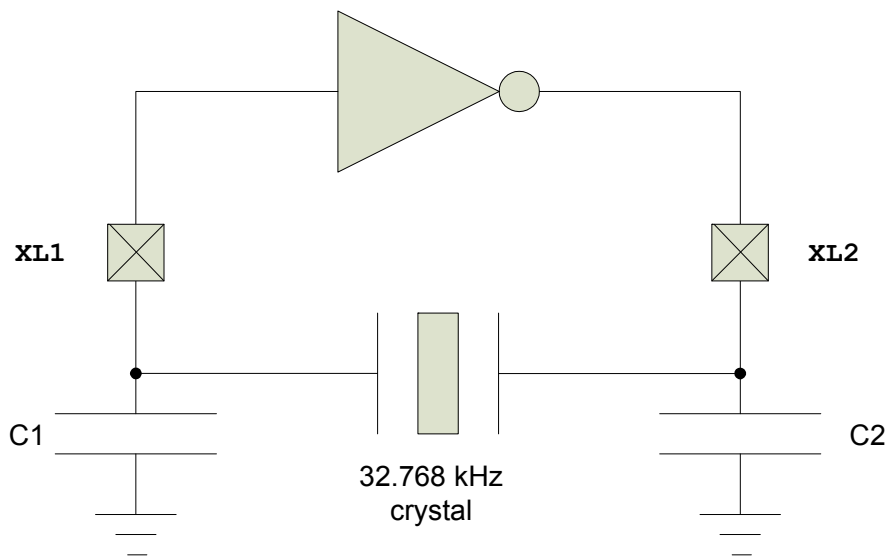


Figure 7 Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins, see **Table 19 on page 33**. The load capacitors C1 and C2 should have the same value.

3.5.3 32.768 kHz RC oscillator

The 32.768 kHz RC low frequency oscillator may be used as an alternative to the 32.768 kHz crystal oscillator. It has a frequency accuracy of ± 250 ppm in a stable temperature environment or when calibration is periodically performed in changing temperature environments. The 32.768 kHz RC oscillator does not require external components.

2. See **Chapter 11 on page 54** for the capacitance value used for C_{pcb1} and C_{pcb2} in reference circuitry.

3.5.4 Synthesized 32.768 kHz clock

The low frequency clock can be synthesized from the high frequency clock. This saves the cost of a crystal but increases average power consumption as the high frequency clock source will have to be active.

3.6 GPIO

The Flexible general purpose I/O is organized as one port with up to 32 I/Os (dependant on package) enabling access and control of up to 32 pins through one port. Each GPIO can also be accessed individually and each has the following user configured features.

- Input/output direction
- Output drive strength
- Internal pull up and pull down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE modules
- All pins can be individually configured to carry serial interface or quadrature demodulator signals

3.7 Debugger support

The 2-pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) in conjunction with the Nordic Trace Buffer (NTB) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support.

4 Peripheral blocks

Peripheral blocks which have a register interface and/or interrupt vector assigned are instantiated, one or more times, in the device address space. The instances, associated ID (for those with interrupt vectors), and base address of features are found in **Table 12 on page 26**. Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Reference Manual*.

4.1 2.4 GHz radio (RADIO)

The nRF51 series 2.4 GHz RF transceiver is designed and optimized to operate in the worldwide ISM frequency band at 2.400 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with *Bluetooth*® low energy (BLE), ANT™, Enhanced ShockBurst™, and other 2.4 GHz protocol implementations.

The transceiver receives and transmits data directly to and from system memory for flexible and efficient packet data management.

- General modulation features
 - GFSK modulation
 - Data whitening
 - 7 bit linear feedback shift register (programmable IV)
 - On-air data rates
 - 250 kbps
 - 1 Mbps
 - 2 Mbps
- Transmitter with programmable output power of +4 dBm to -20 dBm, in 4 dB steps
- Transmitter whisper mode: -30 dBm
- RSSI function (1 dB resolution, ± 6 dB accuracy)
- Receiver with integrated channel filters achieving maximum sensitivity
 - -96 dBm @ 250 kbps
 - -93 dBm @ 1 Mbps BLE
 - -90 dBm @ 1 Mbps
 - -85 dBm @ 2 Mbps
- RF Synthesizer
 - 1 MHz frequency programming resolution
 - 1 MHz non-overlapping channel spacing at 1 Mbps and 250 kbps
 - 2 MHz non-overlapping channel spacing at 2 Mbps
 - Works with low-cost ± 60 ppm 16 MHz crystal oscillators
- Baseband controller
 - EasyDMA³ RX and TX packet transfer directly to and from RAM
 - Dynamic payload length
 - On-the-fly packet assembly/disassembly and AES CCM payload encryption
 - 8 bit, 16 bit, and 24 bit CRC check (programmable polynomial and initial value)

3. EasyDMA - is an integrated DMA implementation requiring no configuration to take advantage of flexible data management and avoid copy operations to and from RAM.

4.2 Timer/counters (TIMER)

The TIMER timer/counter runs on the high-frequency clock source (HFCLK) and includes a 4 bit ($1/2^X$) prescaler that can divide the HFCLK.

The extensive TIMER task/event and interrupt features make it possible to use the PPI system for timing/count tasks to/from any system peripheral including any GPIO of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE modules.

Instance	Bit-width	Capture/Compare registers
TIMER0	32	4
TIMER1	16	4
TIMER2	16	4

Table 7 Timer / Counter properties

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit ($1/X$) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

Instance	Capture/Compare registers
RTC0	4
RTC1	3

Table 8 RTC properties

4.4 AES-ECB encryption (ECB)

The ECB encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. It operates with EasyDMA access to system RAM for in-place operations on cleartext and ciphertext during encryption.

4.5 Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers based on internal thermal noise. These random numbers are suitable for cryptographic purposes. The RNG does not require a seed value.

4.6 Watchdog Timer (WDT)

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.7 Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device with 0.25° C resolution.

4.8 SPI (SPI)

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SCK, MISO, MOSI) bidirectional bus with fast data transfers to and from multiple slaves. Individual chip select signals will be necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of GPIO signals. I/O data is double buffered.

The GPIOs used for each SPI interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and enables efficient use of printed circuit board space and signal routing.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

Instance	Master/Slave
SPI0	Master
SPI1	Master

Table 9 SPI properties

4.9 Two-wire interface (TWI)

The Two-wire interface can interface a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 128 individually addressable devices. The interface is capable of clock stretching and data rates of 100 kbps and 400 kbps are supported.

The GPIOs used for each Two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin-out and enables efficient use of board space and signal routing.

Instance	Master/Slave
TWI0	Master
TWI1	Master

Table 10 Two-wire properties

4.10 UART (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1 Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and enables efficient use of board space and signal routing.

4.11 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors with an optional LED output signal and input debounce filters. The sample period and accumulation are configurable to match application requirements.

4.12 Analog to Digital Converter (ADC)

The 10 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8, 9, and 10 bit).

4.13 GPIO Task Event blocks (GPIOTE)

A GPIO TE block enables GPIOs on Port 0 to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system.

Instance	Number of GPIOs
GPIOTE	4

Table 11 GPIOTE properties

5 Instance table

The peripheral instantiation of the nRF51822 is shown in the table below.

ID	Base address	Peripheral	Instance	Description
0	0x40000000	POWER	POWER	Power Control
0	0x40000000	CLOCK	CLOCK	Clock Control
1	0x40001000	RADIO	RADIO	2.4 GHz Radio
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/Transmitter
3	0x40003000	SPI	SPIM0	SPI0
3	0x40003000	TWI	TWI0	I2C compatible Two-Wire Interface 0
4	0x40004000	SPI	SPI1	SPI1
4	0x40004000	TWI	TWI1	I2C compatible Two-Wire Interface 1
5				Unused
6	0x40006000	GPOTE	Port 0 Task and events	GPIO Tasks and events
7	0x40007000	ADC	ADC	Analog-to-Digital Converter
8	0x40008000	TIMER	TIMER0	Timer/Counter 0
9	0x40009000	TIMER	TIMER1	Timer/Counter 1
10	0x4000A000	TIMER	TIMER2	Timer/Counter 2
11	0x4000B000	RTC	RTC0	Real Time Counter 0
12	0x4000C000	TEMP	TEMP	Temperature Sensor
13	0x4000D000	RNG	RNG	Random Number Generator
14	0x4000E000	ECB	ECB	Crypto AES ECB
15	0x4000F000	CCM	CCM	AES Crypto CCM
15	0x4000F000	AAR	AAR	Accelerated Address Resolver
16	0x40010000	WDT	WDT	Watchdog Timer
17	0x40011000	RTC	RTC1	Real Time Counter 1
18	0x40012000	QDEC	QDEC	Quadrature Decoder
19				Unused
20				Reserved as software input
21				Reserved as software input
22				Reserved as software input
23				Reserved as software input
24				Reserved as software input
25				Reserved as software input
26				Unused
27				Unused
28				Unused
29				Unused
30	0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller
31	0x4001F000	PPI	PPI	Programmable Peripheral Interconnect
NA	0x50000000			General Purpose Input and Output
NA	0x10000000	FICR	FICR	Factory Information Configuration Registers
NA	0x10001000	UICR	UICR	User Information Configuration Registers

Table 12 Peripheral instance reference

Note: Some peripherals will not be available when a SoftDevice is programmed. See the applicable SoftDevice specification for resource usage.

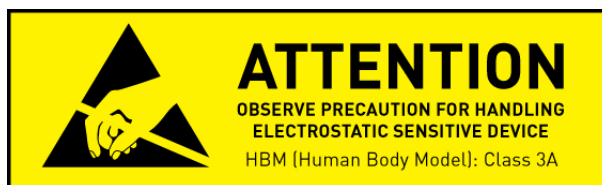
6 Absolute maximum ratings

Maximum ratings are the extreme limits to which nRF51822 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the nRF51822. **Table 13** specifies the absolute maximum ratings for nRF51822.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD		-0.3	+3.6	V
DEC2 ¹			2	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental QFN48 package				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model		4	kV
ESD CDM	Charged Device Model		750	V
Environmental WLCSP package				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		1	
ESD HBM	Human Body Model		4	kV
ESD CDM	Charged Device Model		500	V
Flash memory				
Endurance		20 000		write/erase cycles
Retention		10 years at 40 °C		
Number of times an address can be written between erase cycles			2	times

1. Forced in low voltage mode

Table 13 Absolute maximum ratings



7 Operating conditions

The operating conditions are the physical parameters that nRF51822 can operate within as defined in *Table 14*.

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage, normal mode		1.8	3.0	3.6	V
VDD	Supply voltage, normal mode, DC/DC converter output voltage 1.9 V		2.1	3.0	3.6	V
VDD	Supply voltage, low voltage mode	1	1.75	1.8	1.95	V
t _{R_VDD}	Supply rise time (0 V to 1.8 V)	2			60	ms
T _A	Operating temperature		-25	25	75	°C

1. DEC2 shall be connected to VDD in this mode.
2. The on-chip power-on reset circuitry may not function properly for rise times outside the specified interval.

Table 14 Operating conditions

Nominal operating conditions (NOC) - conditions under which nRF51822 is operated and tested are the typical (Typ.) values in *Table 14*.

Extreme operating conditions (EOC) - conditions under which nRF51822 is operated and tested are the minimum (Min.) and maximum (Max.) values in *Table 14*.

7.1 nRF51822 WLCSP light sensitivity

The nRF51822 WLCSP package variant is sensitive to visible and near infrared light which means a final product design must shield the chip properly. The marking side is covered with a light absorbing film, while the side edges of the chip and the ball side must be protected by coating or other means.

8 Electrical specifications

This chapter contains electrical specifications for device interfaces and peripherals including radio parameters and current consumption.

The test levels referenced are defined in *Table 15*.

Test level	Description
1	Simulated, calculated, by design (specification limit) or prototype samples tested at NOC
2	Parameters have been verified at Test level 1 and in addition: Prototype samples tested at EOC
3	Parameters have been verified at Test level 2 and in addition: Production samples tested at EOC in accordance with JEDEC47
4	Parameters have been verified at Test level 3 and in addition: Production devices are limit tested at NOC

Table 15 Test level definitions

8.1 Clock sources

8.1.1 16/32 MHz crystal startup

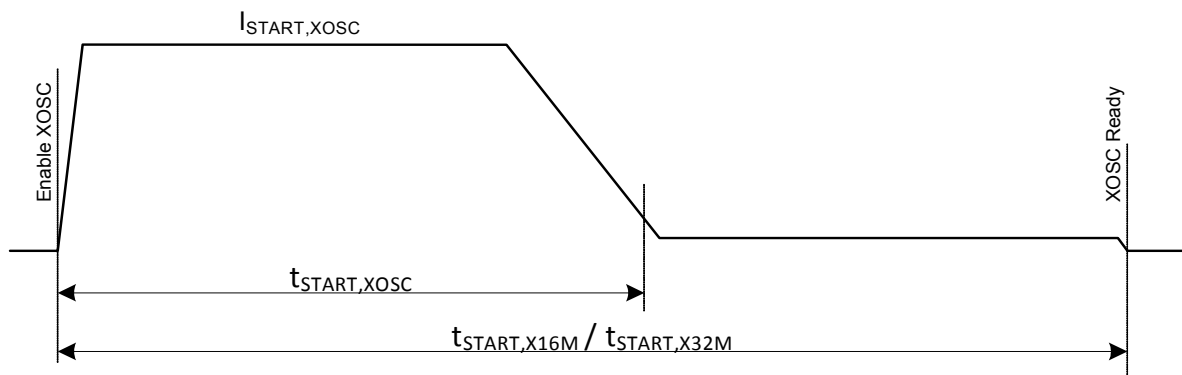


Figure 8 Current drawn at oscillator startup

This figure shows the current drawn by the crystal oscillator (XOSC) at startup. The $t_{START,XOSC}$ period is the time needed for the oscillator to start clocking. The length of $t_{START,XOSC}$ is depending on the crystal specifications.

The period following $t_{START,XOSC}$ to the end of $t_{START,X16M} / t_{START,X32M}$ is fixed. This is the debounce period where the clock stabilizes before it is made available to rest of the system.

8.1.2 16 MHz crystal oscillator (16M XOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM},\text{X16M}}$	Crystal frequency			16		MHz	N/A
$f_{\text{TOL},\text{X16M}}$	Frequency tolerance ¹				$\pm 60^2$	ppm	N/A
$f_{\text{TOL},\text{X16M},\text{BLE}}$	Frequency tolerance, <i>Bluetooth</i> low energy applications				$\pm 40^2$	ppm	N/A
$R_{\text{S},\text{X16M}}$	Equivalent series resistance	$C_0 \leq 7 \text{ pF}, C_{\text{L},\text{MAX}} \leq 16 \text{ pF}$	50	100		Ω	N/A
		$C_0 \leq 5 \text{ pF}, C_{\text{L},\text{MAX}} \leq 12 \text{ pF}$	75	150		Ω	N/A
		$C_0 \leq 3 \text{ pF}, C_{\text{L},\text{MAX}} \leq 12 \text{ pF}$	100	200		Ω	N/A
$P_{\text{D},\text{X16M}}$	Drive level				100	μW	N/A
C_{pin}	Input capacitance on XC1 and XC2 pads			4		pF	1
I_{X16M}	Run current for 16 MHz crystal oscillator	With SMD 2520 $CL = 8 \text{ pF}$		400 ³		μA	1
$I_{\text{STBY},\text{X16M}}$	Standby current for 16 MHz crystal oscillator ⁴	With SMD 2520 $CL = 8 \text{ pF}$		35		μA	1
$I_{\text{START},\text{XOSC}}$	Startup current for 16 MHz crystal oscillator			1.1		mA	3
$t_{\text{START},\text{XOSC}}$	Startup time for 16 MHz crystal oscillator	With SMD 2520 $CL = 8 \text{ pF}$		400	500 ⁵	μs	2
$t_{\text{START},\text{X16M}}$	Total startup time ($t_{\text{START},\text{XOSC}}$ + debounce period) ⁶	With SMD 2520 $CL = 8 \text{ pF}$		800		μs	1

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See **Table 28 on page 39**.
2. Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 16M, meaning there is no clock management active (see **Table 24 on page 37**). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.

Table 16 16 MHz crystal oscillator

8.1.3 32 MHz crystal oscillator (32M XOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM},\text{X32M}}$	Crystal frequency			32		MHz	N/A
$f_{\text{TOL},\text{X32M}}$	Frequency tolerance ¹				$\pm 60^2$	ppm	N/A
$f_{\text{TOL},\text{X32M,BLE}}$	Frequency tolerance, <i>Bluetooth</i> low energy applications				$\pm 40^2$	ppm	N/A
$R_{\text{S},\text{X32M}}$	Equivalent series resistance	$C_0 \leq 7 \text{ pF}, C_{\text{L},\text{MAX}} \leq 12 \text{ pF}$	30	60		Ω	N/A
		$C_0 \leq 5 \text{ pF}, C_{\text{L},\text{MAX}} \leq 12 \text{ pF}$	40	80		Ω	N/A
		$C_0 \leq 3 \text{ pF}, C_{\text{L},\text{MAX}} \leq 9 \text{ pF}$	50	100		Ω	N/A
$P_{\text{D},\text{X32M}}$	Drive level				100	μW	N/A
C_{pin}	Input capacitance on XC1 and XC2 pads			4		pF	1
I_{X32M}	Run current for 32 MHz crystal oscillator	With SMD 2520 $CL = 8 \text{ pF}$		440 ³		μA	1
$I_{\text{STBY},\text{X32M}}$	Standby current for 32 MHz crystal oscillator ⁴	With SMD 2520 $CL = 8 \text{ pF}$		43		μA	1
$I_{\text{START},\text{XOSC}}$	Startup current for 32 MHz crystal oscillator			1.1		mA	3
$t_{\text{START},\text{XOSC}}$	Startup time for 32 MHz crystal oscillator	With SMD 2520 $CL = 8 \text{ pF}$		300	400 ⁵	μs	1
$t_{\text{START},\text{X32M}}$	Total startup time ($t_{\text{START},\text{XOSC}}$ + debounce period) ⁶	With SMD 2520 $CL = 8 \text{ pF}$		750		μs	1

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See **Table 28 on page 39**.
2. Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 32M, meaning there is no clock management active (see **Table 24 on page 37**). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.

Table 17 32 MHz crystal oscillator

8.1.4 16 MHz RC oscillator (16M RCOSC)

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM,RC16M}}$	Nominal frequency		16		MHz	N/A
$f_{\text{TOL,RC16M}}$	Frequency tolerance		± 1	± 5	%	3
I_{RC16M}	Run current for 16 MHz RC oscillator		750 ¹		μA	1
$t_{\text{START,RC16M}}$	Startup time for 16 MHz RC oscillator		2.5	3.5	μs	1
$I_{\text{RC16M, START}}$	Startup current for 16 MHz RC oscillator		400		μA	1

1. This number includes the current used by the automated power and clock management system.

Table 18 16 MHz RC oscillator

8.1.5 32.768 kHz crystal oscillator (32k XOSC)

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM,X32k}}$	Crystal frequency		32.768		kHz	N/A
$f_{\text{TOL,X32k}}$	Frequency tolerance			± 250	ppm	N/A
$C_{\text{L,X32k}}$	Load capacitance			12.5	pF	N/A
$C_{\text{0,X32k}}$	Shunt capacitance			2	pF	N/A
$R_{\text{S,X32k}}$	Equivalent series resistance		50	80	$\text{k}\Omega$	N/A
$P_{\text{D,X32k}}$	Drive level			1	μW	N/A
C_{pin}	Input capacitance on XL1 and XL2 pads		4		pF	1
I_{X32k}	Run current for 32.768 kHz crystal oscillator		0.4	1	μA	1
$I_{\text{START,X32k}}$	Startup current for 32.768 kHz crystal oscillator		1.3	1.8	μA	1
$t_{\text{START,X32k}}$	Startup time for 32.768 kHz crystal oscillator		0.3	1	s	2

Table 19 32.768 kHz crystal oscillator

8.1.6 32.768 kHz RC oscillator (32k RCOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM,RC32k}}$	Nominal frequency			32.768		kHz	N/A
$f_{\text{TOL,RC32k}}$	Frequency tolerance			± 2		%	3
$f_{\text{TOL,CAL,RC32k}}$	Frequency tolerance for 32.768 kHz RC oscillator after calibration	Calibration interval 4 s at constant temperature			± 250	ppm	1
I_{RC32k}	Run current for 32.768 kHz RC oscillator		0.5	0.8	1.1	μA	1
$t_{\text{START,RC32k}}$	Startup time for 32.768 kHz RC oscillator			100		μs	1

Table 20 32.768 kHz RC oscillator

8.1.7 32.768 kHz Synthesized oscillator (32k SYNT)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM,SYNT32k}}$	Nominal frequency			32.768		kHz	1
$f_{\text{TOL,SYNT}}$	Frequency tolerance			$f_{\text{TOL,XO16M}} \pm 8$		ppm	1
I_{SYNT32k}	Run and startup current for 32.768 kHz Synthesized clock			40		μA	1
$t_{\text{START,SYNT32k}}$	Startup time for 32.768 kHz Synthesized clock			100		μs	1

Table 21 32.768 kHz Synthesized oscillator

8.2 Power management

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
VPOF	Nominal power level warning thresholds (falling supply voltage)	Accuracy as defined by V_{TOL}		2.1 2.3 2.5 2.7		V	N/A
V_{TOL}	Threshold voltage tolerance				±5	%	3
V_{HYST}	Threshold voltage hysteresis	2.1 V 2.3 V 2.5 V 2.7 V		46 62 79 100		mV	3

Table 22 Power Fail Comparator

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$t_{POR, 1\mu s}$	Time Reset is active from VDD reaches 1.7 V with 1 μs rise time		0.2	2.7		ms	1
$t_{POR, 50 ms}$	Time Reset is active from VDD reaches 1.7 V with 50 ms rise time		6.5	29		ms	1
I_{OFF}	Current in SYSTEM-OFF, no RAM retention			0.4		μA	1
$I_{OFF, 8 k}$	Current in SYSTEM-OFF mode 8 kB SRAM retention			0.6		μA	1
$I_{OFF, 16 k}$	Current in SYSTEM-OFF mode 16 kB SRAM retention			0.8		μA	1
I_{OFF2ON}	OFF to CPU execute transition current			400		μA	1
t_{OFF2ON}	OFF to CPU execute			9.6	10.6	μs	1
I_{ON}	SYSTEM-ON base current			2.3		μA	2
I_{1V2}	Current drawn by 1V2 regulator			290		μA	2
t_{1V2}	Startup time for 1V2 regulator			2.3		μs	1
I_{1V7}	Current drawn by 1V7 regulator			90		μA	2
t_{1V7}	Startup time for 1V7 regulator			2	3.6	μs	1
$I_{1V2RC16}$	Current drawn by 1V2 regulator and 16 MHz RCOSC when both are on at the same time	See Table 24		830 ¹		μA	1

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{1V2XO16}$	Current drawn by 1V2 regulator and 16 MHz XOSC when both are on at the same time	See <i>Table 24</i>		740 ¹		μA	1
I_{DCDC}	Current drawn by DC/DC converter			300		μA	1
F_{DCDC}	DC/DC converter current conversion factor		0.65 ²		1.2 ²		1
$t_{\text{START,DCDC}}$	DC/DC converter startup time		10 ²		425 ²	μs	1

1. This number includes the current used by the automated power and clock management system.
2. F_{DCDC} and $t_{\text{START,DCDC}}$ will vary depending on VDD and device internal current consumption (I_{DD}). The range of values stated in this specification is for VDD between 2.1 V and 3.6 V, and I_{DD} between 4 mA and 20 mA. Please refer to the *nRF51 Series Reference Manual*, v1.1 or later, for a method to calculate these numbers based on VDD and I_{DD} .

Table 23 Power management

8.3 Block resource requirements

Block	ID	Required resources			Comment
		1V2+16M	16M	32k	
Radio	1	x			Requires 16M XOSC
UART	2	x			
SPI	3, 4	x			
2W	3, 4	x			
GPIOTE	6		x		Only in input mode
ADC	7	x			Requires 16M XOSC
TIMER	8, 9, 10		x		
RTC	11, 17		x	x	16M will only be requested if the 32.768 kHz clock is synthesized from the 16 MHz clock
TEMP	12	x			Requires 16M XOSC
RNG	13	x			
ECB	14	x	x		
WDT	16			x	
QDEC	18	x			
CPU		x			

Table 24 Clock and power requirements for different blocks

8.4 CPU

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$I_{\text{CPU, Flash}}$	Run current at 16 MHz, Executing code from flash memory		4.4 ¹		mA	2
$I_{\text{CPU, RAM}}$	Run current at 16 MHz, Executing code from RAM		2.4 ²		mA	1
$I_{\text{START, CPU}}$	CPU startup current		600		μA	1
$t_{\text{START, CPU}}$	IDLE to CPU execute	0	³		μs	1

1. Includes CPU, flash, 1V2, 1V7, RC16M

2. Includes CPU, RAM, 1V2, RC16M

3. t_{1V2} if 1V2 regulator is not running already

Table 25 CPU specifications

8.5 Radio transceiver

8.5.1 General radio characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
f_{OP}	Operating frequencies	1 MHz channel spacing	2400		2483	MHz	N/A
PLL_{res}	PLL programming resolution			1		MHz	N/A
Δf_{250}	Frequency deviation @ 250 kbps			± 170		kHz	2
Δf_{1M}	Frequency deviation @ 1 Mbps			± 170		kHz	2
Δf_{2M}	Frequency deviation @ 2 Mbps			± 320		kHz	2
Δf_{BLE}	Frequency deviation @ BLE		± 225	± 250	± 275	kHz	4
bps_{FSK}	On-air data rate		250		2000	kbps	N/A

Table 26 General radio characteristics

8.5.2 Radio current consumption

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{TX,+4dBm}$	TX only run current @ $P_{OUT} = +4$ dBm	1		16		mA	4
$I_{TX,0dBm}$	TX only run current @ $P_{OUT} = 0$ dBm	1		10.5		mA	4
$I_{TX,-4dBm}$	TX only run current @ $P_{OUT} = -4$ dBm	1		8		mA	2
$I_{TX,-8dBm}$	TX only run current @ $P_{OUT} = -8$ dBm	1		7		mA	2
$I_{TX,-12dBm}$	TX only run current @ $P_{OUT} = -12$ dBm	1		6.5		mA	2
$I_{TX,-16dBm}$	TX only run current @ $P_{OUT} = -16$ dBm	1		6		mA	2
$I_{TX,-20dBm}$	TX only run current @ $P_{OUT} = -20$ dBm	1		5.5		mA	2
$I_{TX,-30dBm}$	TX only run current @ $P_{OUT} = -30$ dBm	1		5.5		mA	2
$I_{START,TX}$	TX startup current	2		7		mA	1
$I_{RX,250}$	RX only run current @ 250 kbps			12.6		mA	1
$I_{RX,1M}$	RX only run current @ 1 Mbps			13		mA	4
$I_{RX,2M}$	RX only run current @ 2 Mbps			13.4		mA	1
$I_{START,RX}$	RX startup current	3		8.7		mA	1

1. Valid for data rates 250 kbps, 1 Mbps, and 2 Mbps
2. Average current consumption (at 0 dBm TX output power) for TX startup (130 μ s), and when changing mode from RX to TX (130 μ s).
3. Average current consumption for RX startup (130 μ s), and when changing mode from TX to RX (130 μ s).

Table 27 Radio current consumption

8.5.3 Transmitter specification

Symbol	Description	Min.	Typ.	Max.	Units	Test level
P_{RF}	Maximum output power		4		dBm	4
P_{RFC}	RF power control range	20	24		dB	2
$PRFCR$	RF power accuracy			± 4	dB	1
P_{WHISP}	RF power whisper mode		-30		dBm	2
P_{BW2}	20 dB bandwidth for modulated carrier (2 Mbps)		1800	2000	kHz	2
P_{BW1}	20 dB bandwidth for modulated carrier (1 Mbps)		950	1100	kHz	2
P_{BW250}	20 dB bandwidth for modulated carrier (250 kbps)		700	800	kHz	2
$P_{RF1.2}$	1 st Adjacent Channel Transmit Power 2 MHz (2 Mbps)			-20	dBc	2
$P_{RF2.2}$	2 nd Adjacent Channel Transmit Power 4 MHz (2 Mbps)			-45	dBc	2
$P_{RF1.1}$	1 st Adjacent Channel Transmit Power 1 MHz (1 Mbps)			-20	dBc	2
$P_{RF2.1}$	2 nd Adjacent Channel Transmit Power 2 MHz (1 Mbps)			-40	dBc	2
$P_{RF1.250}$	1 st Adjacent Channel Transmit Power 1 MHz (250 kbps)			-25	dBc	2
$P_{RF2.250}$	2 nd Adjacent Channel Transmit Power 2 MHz (250 kbps)			-40	dBc	2
$t_{TX,30}$	Maximum consecutive transmission time, $f_{TOL} < \pm 30$ ppm			16	ms	1
$t_{TX,60}$	Maximum consecutive transmission time, $f_{TOL} < \pm 60$ ppm			4	ms	1

Table 28 Transmitter specification

8.5.4 Receiver specification

Symbol	Description	Min.	Typ.	Max.	Units	Test level
Receiver operation						
PRX _{MAX}	Maximum received signal strength at < 0.1% PER		0		dBm	1
PRX _{SENS,2M}	Sensitivity (0.1% BER) @ 2 Mbps		-85		dBm	2
PRX _{SENS,1M}	Sensitivity (0.1% BER) @ 1 Mbps		-90		dBm	2
PRX _{SENS,250k}	Sensitivity (0.1% BER) @ 250 kbps		-96		dBm	2
P _{SENS IT} 1 Mbps BLE	Receiver sensitivity: Ideal transmitter		-93		dBm	2
P _{SENS DT} 1 Mbps BLE	Receiver sensitivity: Dirty transmitter		-91		dBm	2
RX selectivity - modulated interfering signal¹						
2 Mbps						
C/I _{CO}	C/I co-channel		12		dB	2
C/I _{1ST}	1 st ACS, C/I 2 MHz		-4		dB	2
C/I _{2ND}	2 nd ACS, C/I 4 MHz		-24		dB	2
C/I _{3RD}	3 rd ACS, C/I 6 MHz		-28		dB	2
C/I _{6th}	6 th ACS, C/I 12 MHz		-44		dB	2
C/I _{Nth}	N th ACS, C/I f _i > 25 MHz		-50		dB	2
1 Mbps						
C/I _{CO}	C/I co-channel (1 Mbps)		12		dB	2
C/I _{1ST}	1 st ACS, C/I 1 MHz		4		dB	2
C/I _{2ND}	2 nd ACS, C/I 2 MHz		-24		dB	2
C/I _{3RD}	3 rd ACS, C/I 3 MHz		-30		dB	2
C/I _{6th}	6 th ACS, C/I 6 MHz		-40		dB	2
C/I _{12th}	12 th ACS, C/I 12 MHz		-50		dB	2
C/I _{Nth}	N th ACS, C/I f _i > 25 MHz		-53		dB	2

Symbol	Description	Min.	Typ.	Max.	Units	Test level
250 kbps						
C/I_{CO}	C/I co-channel		4		dB	2
C/I_{1ST}	1 st ACS, C/I 1 MHz		-10		dB	2
C/I_{2ND}	2 nd ACS, C/I 2 MHz		-34		dB	2
C/I_{3RD}	3 rd ACS, C/I 3 MHz		-39		dB	2
C/I_{6th}	6 th ACS, C/I $f_i > 6$ MHz		-50		dB	2
C/I_{12th}	12 th ACS, C/I 12 MHz		-55		dB	2
C/I_{Nth}	N th ACS, C/I $f_i > 25$ MHz		-60		dB	2
Bluetooth Low Energy RX selectivity						
C/I_{CO}	C/I co-channel		10		dB	2
C/I_{1ST}	1 st ACS, C/I 1 MHz		1		dB	2
C/I_{2ND}	2 nd ACS, C/I 2 MHz		-25		dB	2
C/I_{3+N}	ACS, C/I (3+n) MHz offset [$n = 0, 1, 2, \dots$]		-51		dB	2
C/I_{Image}	Image blocking level		-30		dB	2
$C/I_{Image \pm 1MHz}$	Adjacent channel to image blocking level (± 1 MHz)		-31		dB	2
RX intermodulation²						
$P_{IMD_{2Mbps}}$	IMD performance, 2 Mbps, 3rd, 4th and 5th offset channel		-41		dBm	2
$P_{IMD_{1Mbps}}$	IMD performance, 1 Mbps, 3rd, 4th and 5th offset channel		-40		dBm	2
$P_{IMD_{250kbps}}$	IMD performance, 250 kbps, 3rd, 4th and 5th offset channel		-36		dBm	2
$P_{IMD_{BLE}}$	IMD performance, 1 Mbps BLE, 3rd, 4th and 5th offset channel		-39		dBm	2

1. Wanted signal level at $P_{IN} = -67$ dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented.
2. Wanted signal level at $P_{IN} = -64$ dBm. Two interferers with equal input power are used. The interferer closest in frequency is unmodulated, the other interferer is modulated equal with the wanted signal. The input power of interferers where the sensitivity equals BER = 0.1% is presented.

Table 29 Receiver specification

8.5.5 Radio timing parameters

Symbol	Description	250 k	1 M	2 M	BLE	Jitter	Units
t_{TXEN}	Time between TXEN task and READY event	132	132	132	140	0	μs
$t_{TXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX	10	4	3	4	1	μs
t_{RXEN}	Time between the RXEN task and READY event	130	130	130	138	0	μs
$t_{RXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX	0	0	0	0	1	μs
$t_{TXCHAIN}$	TX chain delay	5	1	0.5	1	0	μs
$t_{RXCHAIN}$	RX chain delay	12	2	2.5	3	0	μs

Table 30 Radio timing

8.6 RSSI specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$RSSI_{ACC}$	RSSI accuracy	Valid between: -50 dBm and -80 dBm			± 6	dB	2
$RSSI_{RESOLUTION}$	RSSI resolution			1		dB	1
$RSSI_{PERIOD}$	Sample period		8.8			μs	1
$RSSI_{CURRENT}$	Current consumption in addition to I_{RX}			250		μA	1

Table 31 RSSI specifications

8.7 UART specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{UART1M}	Run current @ max baud rate			230		μA	1
$I_{UART115k}$	Run current @ 115200 bps			220		μA	1
$I_{UART1k2}$	Run current @ 1200 bps			210		μA	1
f_{UART}	Baud rate for UART		1.2		921.6	kbps	N/A

Table 32 UART specifications

8.8 SPI specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$I_{SPI125K}$	Run current for SPI master @ 125 kbps		180		μA	1
I_{SPI8M}	Run current for SPI master @ 8 Mbps		200		μA	1
f_{SPI}	Bit rates for SPI	0.125		8	Mbps	N/A

Table 33 SPI specifications

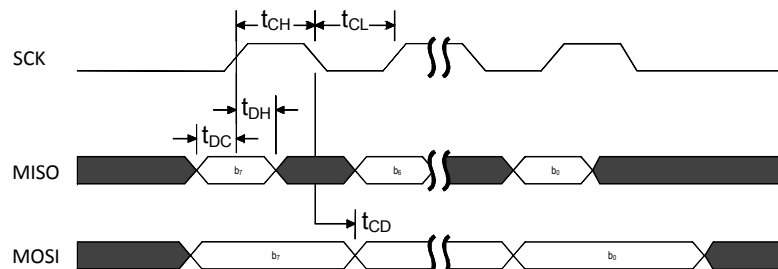


Figure 9 SPI timing diagram, one byte transmission, SPI mode 0

Symbol	Description	Note	Min.	Max.	Units	Test level
t_{DC}	Data to SCK setup		10		ns	1
t_{DH}	SCK to Data hold		10		ns	1
t_{CD}	SCK to Data valid	$C_{LOAD} = 0 \text{ pF}$ $C_{LOAD} = 5 \text{ pF}$ $C_{LOAD} = 10 \text{ pF}$ $C_{LOAD} = 35 \text{ pF}$		60 66 68 78	ns	1
t_{CL}	SCK Low time		40		ns	1
t_{CH}	SCK High time		40		ns	1
f_{SCK}	SCK Frequency		0.125	8	MHz	1
t_R, t_F	SCK Rise and Fall time			100	ns	1

Table 34 SPI timing parameters

8.9 TWI specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{2W100K}	Run current for TWI @ 100 kbps		380		μA	1
I_{2W400K}	Run current for TWI @ 400 kbps		400		μA	1
f_{2W}	Bit rates for TWI	100		400	kbps	N/A

Table 35 TWI specifications

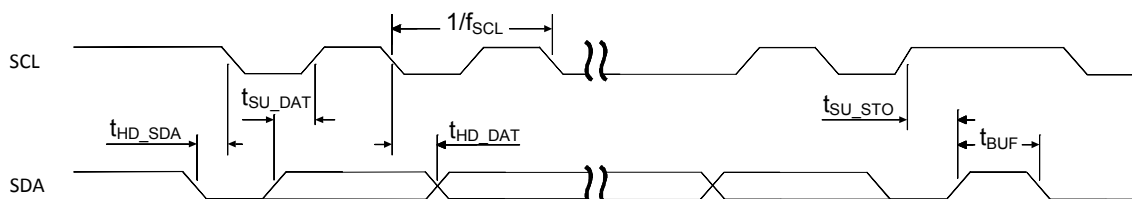


Figure 10 SCL/SDA timing

Symbol	Description	Standard		Fast		Units	Test level
		Min.	Max.	Min.	Max.		
f_{SCL}	SCL clock frequency		100		400	kHz	1
t_{HD_STA}	Hold time for START and repeated START condition	5200		1300		ns	1
t_{SU_DAT}	Data setup time before positive edge on SCL	300		300		ns	1
t_{HD_DAT}	Data hold time after negative edge on SCL	300		300		ns	1
t_{SU_STO}	Setup time from SCL goes high to STOP condition	5200		1300		ns	1
t_{BUF}	Bus free time between STOP and START conditions	4700		1300		ns	1

Table 36 TWI timing parameters

8.10 GPIOTE specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$I_{\text{GPIOTE,IN}}$	Run current with GPIOTE active in Input mode		100		μA	1
$I_{\text{GPIOTE,OUT}}$	Run current with GPIOTE active in Output mode		0.1		μA	1

Table 37 GPIOTE specifications

Note: Setting up one or more GPIO DETECT signals to generate PORT EVENT, that again could be used either as a wakeup source or to give an interrupt, will not lead to an increase of the current consumption.

8.11 Analog-to-Digital Converter (ADC) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$\text{DNL}_{10\text{b}}$	Differential non-linearity (10 bit mode)			< 1		LSB	2
$\text{INL}_{10\text{b}}$	Integral non-linearity (10 bit mode)			2		LSB	2
V_{OS}	Offset error		-2		+2	%	2
e_{G}	Gain error		-2		+2	%	2
$V_{\text{REF_INT}}$	Internal reference voltage		-1.5	1.20 V	+1.5	%	2
$\text{TC}_{\text{REF_INT}}$	Internal reference voltage drift		-200		+200	ppm/°C	2
$V_{\text{REF_EXT}}$	External reference voltage		0.83	1.2	1.3	V	1
$t_{\text{ADC}10\text{b}}$	Time required to convert a single sample in 10 bit mode			68		μs	1
$t_{\text{ADC}9\text{b}}$	Time required to convert a single sample in 9 bit mode			36		μs	1
$t_{\text{ADC}8\text{b}}$	Time required to convert a single sample in 8 bit mode			20		μs	1
I_{ADC}	Current drawn by ADC during conversion			290		μA	1
ADC_ERR_1V8	Absolute error when used for battery measurement at 1.8 V, 2.2 V, 2.6 V, 3.0 V and 3.4 V	Internal reference, input from VDD/3 10 bit setting		3		LSB	2
ADC_ERR_2V2				2		LSB	2
ADC_ERR_2V6				1		LSB	2
ADC_ERR_3V0				1		LSB	2
ADC_ERR_3V4				1		LSB	2

Table 38 Analog-to-Digital Converter (ADC) specifications

8.12 Timer specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{\text{TIMER0/1/2,16M}}$	Timer @16 MHz run current	24 bit		258		μA	1
		16 bit		178		μA	1
$t_{\text{TIMER,START}}$	Time from START task is given until timer start counting			0.25		μs	1

Table 39 Timer specifications

8.13 RTC

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{RTC}	Timer (LFCLK source)		0.2		μA	1

Table 40 RTC

8.14 Temperature sensor

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{TEMP}	Run current for Temperature sensor		185		μA	1
t_{TEMP}	Time required for temperature measurement		35		μs	1
T_{RANGE}	Temperature sensor range	-25		75	$^{\circ}\text{C}$	N/A
T_{ACC}	Temperature sensor accuracy	-4		+4	$^{\circ}\text{C}$	N/A
T_{RES}	Temperature sensor resolution		0.25		$^{\circ}\text{C}$	1

Table 41 Temperature sensor

8.15 Random Number Generator (RNG) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{RNG}	Run current @ 16 MHz			300		μA	1
$t_{\text{RNG,RAW}}$	Run time per byte in RAW mode	Uniform distribution of 0 and 1 is not guaranteed		167		μs	1
$t_{\text{RNG,UNI}}$	Run time per byte in Uniform mode	Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed		677		μs	1

Table 42 Random Number Generator (RNG) specifications

8.16 ECB/CCM/AAR specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{CRYPTO}	Run current for Crypto in all modes		400		μA	1
t_{CRYPTO}	Run time per 16 byte block in all modes		8.5		μs	1

Table 43 ECB/CCM/AAR specifications

8.17 Watch Dog Timer specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{WDT}	Run current for watch dog timer		1		μA	1
t_{WDT}	Time out interval, watch dog timer	30 μs		36 hrs		1

Table 44 Watch Dog Timer specifications

8.18 Quadrature Decoder specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{QDEC}				250		μA	1
t_{SAMPLE}	Time between sampling signals from quadrature decoder		128		16384	μs	N/A
t_{LED}	Time from LED is turned on to signals are sampled	Only valid for optical sensors	0		511	μs	N/A

Table 45 Quadrature Decoder specifications

8.19 NVMC specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$t_{ERASEALL}$	Erase flash memory			21		ms	1
$t_{PAGEERASE}$	Erase page in flash memory			21		ms	1
t_{WRITE}^1	Write one word to flash memory			22	43	μs	1

1. Nominal value applies when writing 32 words or more. Maximum value applies when writing a single word.

Note: The CPU will be halted for the duration of NVMC operations.

Table 46 NVMC specifications

8.20 General purpose I/O (GPIO) specification

Symbol	Parameter (condition)	Note	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		0.7 VDD		VDD	V
V_{IL}	Input low voltage		VSS		0.3 VDD	V
V_{OH}	Output high voltage (std. drive, 0.5 mA)		VDD-0.3		VDD	V
V_{OH}	Output high voltage (high-drive, 5 mA)	1	VDD-0.3		VDD	V
V_{OL}	Output low voltage (std. drive, 0.5 mA)		VSS		0.3	V
V_{OL}	Output low voltage (high-drive, 5 mA)		VSS		0.3	V
R_{PU}	Pull-up resistance		11	13	16	k Ω
R_{PD}	Pull-down resistance		11	13	16	k Ω

1. Maximum number of pins with 5 mA high drive is 3.

Table 47 General purpose I/O (GPIO) specification

9 Mechanical specifications

9.1 QFN48 package

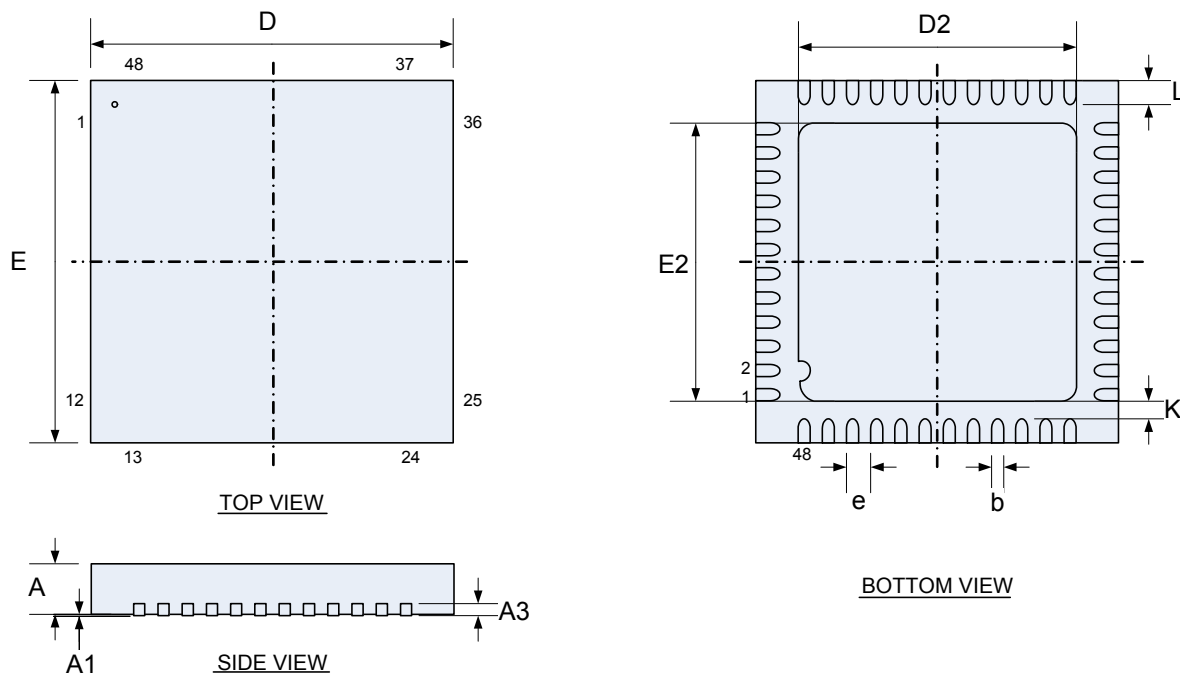


Figure 11 QFN48 6x6 mm package

Package	A	A1	A3	b	D, E	D2, E2	e	K	L	
QFN48 (6 x 6)	0.80	0.00		0.15		4.50		0.20	0.35	Min.
	0.85	0.02	0.2	0.20	6.0	4.60	0.4		0.40	Nom.
	0.90	0.05		0.25		4.70			0.45	Max.

Table 48 QFN48 dimensions in millimeters

9.2 WLCSP package

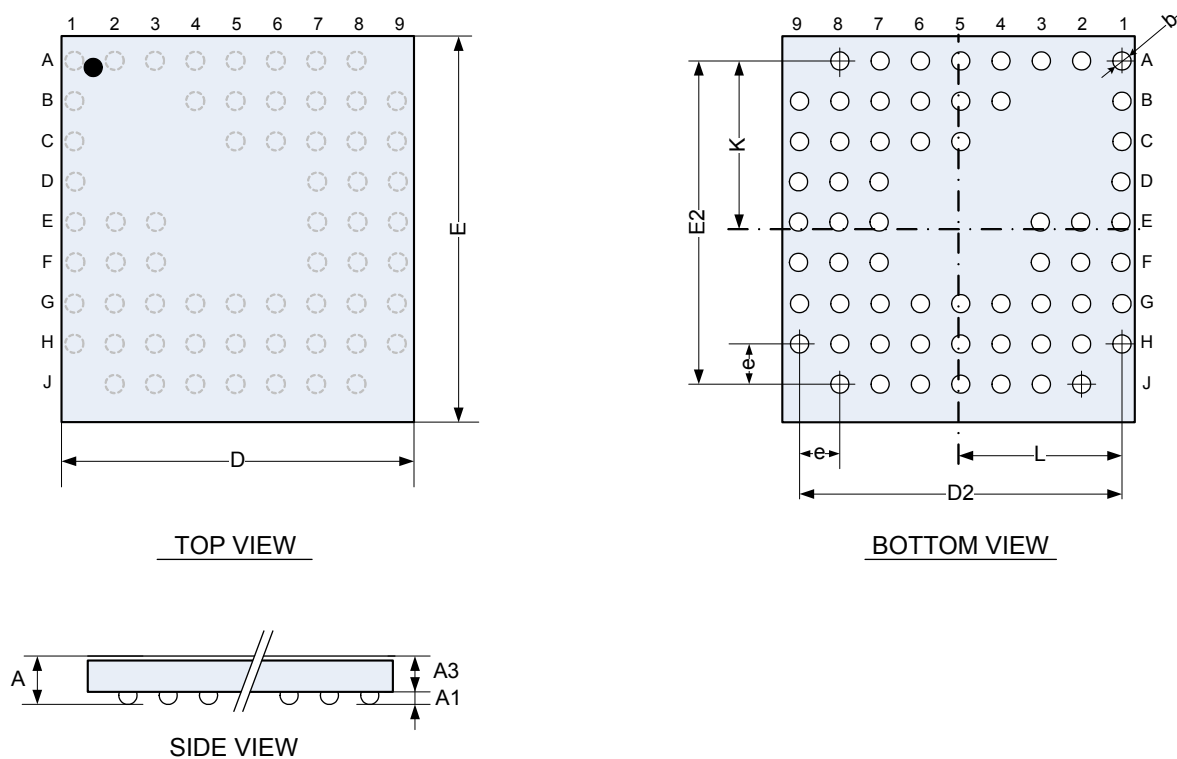


Figure 12 WLCSP package

Package	A	A1	A3	b	D	E	D2	E2	e	K	L	Min. Nom. Max.
WLCSP		0.12	0.31	0.16	3.45	3.78						
	0.50	0.15	0.33	0.20	3.50	3.83	3.20	3.20	0.4	1.66	1.61	
	0.55	0.18	0.35	0.24	3.55	3.88						

Table 49 WLCSP package dimensions in millimeters

10 Ordering information

10.1 Package marking

N	5	1	8	2	2
<P	P>	<V	V>	<H>	<P>
<Y	Y>	<W	W>	<L	L>

Table 50 Package marking

10.2 Order code

n	R	F	5	1	8	2	2	-	<P	P>	<V	V>	-	<C	C>
---	---	---	---	---	---	---	---	---	----	----	----	----	---	----	----

Table 51 Order code

10.3 Abbreviations

Abbreviation	Definition and Implemented Codes
N51/nRF51	nRF51 series product
822	Part code
<PP>	Package code
<VV>	Variant code
<H><P>	Build code H - Hardware version code P - Production version code (production site, etc.)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 52 Abbreviations

10.4 Code ranges and values

<PP>	Packet	Size (mm)	Pin/Ball Count	Pitch (mm)
QF	QFN	6 x 6	48	0.4
CE	WLCSP	3.50 x 3.83	62	0.4

Table 53 Package codes

<VV>	Flash (kB)	RAM (kB)	DC/DC Bond-out
AA	256	16	YES
AB	128	16	YES

Table 54 Variant codes

<H>	Description
[A..Z]	Hardware version/revision identifier (incremental)

Table 55 Hardware version codes

<P>	Description
[0..9]	Production device identifier (incremental)
[A..T]	Engineering device identifier (incremental)

Table 56 Production version codes

<YY>	Description
[12..99]	Production year: 2012 to 2099

Table 57 Year codes

<WW>	Description
[1..52]	Week of production

Table 58 Week codes

<LL>	Description
[AA..ZZ]	Wafer production lot identifier

Table 59 Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel
T	Tray

Table 60 Container codes

10.5 Product options

10.5.1 nRF ICs

Order code	MOQ ¹
nRF51822-QFAA-R7 nRF51822-QFAB-R7	1000
nRF51822-QFAA-R nRF51822-QFAB-R nRF51822-CEAA-R	3000
nRF51822-QFAA-T nRF51822-QFAB-T	490

1. Minimum Order Quantity

Table 61 Order code

10.5.2 Development tools

Order code	Description
nRF51822-DK ¹	nRF51822 Development Kit ²
nRF51822-EK ¹	nRF51822 Evaluation Kit
nRF6700	nRFgo Starter Kit

1. Uses the nRF51822-QFAA version of the chip
2. Requires nRF6700 nRFgo Starter Kit

Table 62 Development tools

11 Reference circuitry

For the following reference layouts, C_{pcb} , between X1 and XC1/XC2, is estimated to 0.5 pF each.

The exposed center pad of the QFN48 package must be connected to supply ground for proper device operation.

11.1 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality. A qualified RF-layout for the IC and its surrounding components, including matching networks, can be downloaded from www.nordicsemi.com.

A PCB with a minimum of two layers including a ground plane is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pins **ANT1**, **ANT2**, **VDD_PA**, and the antenna) to reduce the stray capacitances that influence RF performance.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have Via holes as close as possible to the VSS pads. A minimum of one Via hole should be used for each VSS pin.

Full-swing digital data or control signals should not be routed close to the crystal or the power supply lines. Capacitive loading of full-swing digital output lines should be minimized in order to avoid radio interference.

Documentation for the QFN48 package reference circuit, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from the nRF51822 product page on www.nordicsemi.com.

nRF51822 QFN48 schematic with internal LDO regulator

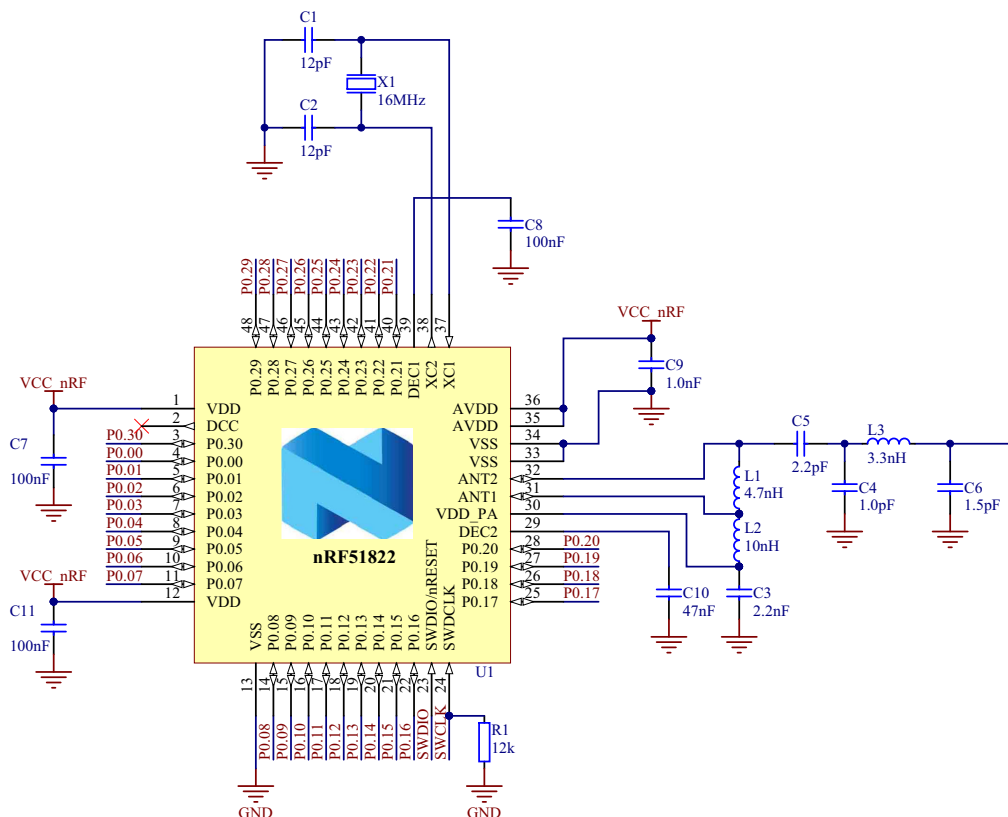


Figure 13 *nRF51822 QFN48 with internal LDO regulator*

11.2.1.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, $\pm 2\%$	0402
C3	2.2 nF	Capacitor, X7R, $\pm 10\%$	0402
C4	1.0 pF	Capacitor, NP0, ± 0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ± 0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ± 0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C9	1.0 nF	Capacitor, X7R, $\pm 10\%$	0402
C10	47 nF	Capacitor, X7R, $\pm 10\%$	0402
L1	4.7 nH	High frequency chip inductor $\pm 5\%$	0402
L2	10 nH	High frequency chip inductor $\pm 5\%$	0402
L3	3.3 nH	High frequency chip inductor $\pm 5\%$	0402
R1	12 k Ω	Resistor, $\pm 5\%$, 0.063 W	0402
U1	nRF51822-QFAA nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ± 40 ppm	2.5 x 2.0 mm

Table 63 nRF51822 QFN48 with internal LDO regulator

11.2.2 nRF51822 QFN48 schematic with 1.8 V low voltage mode

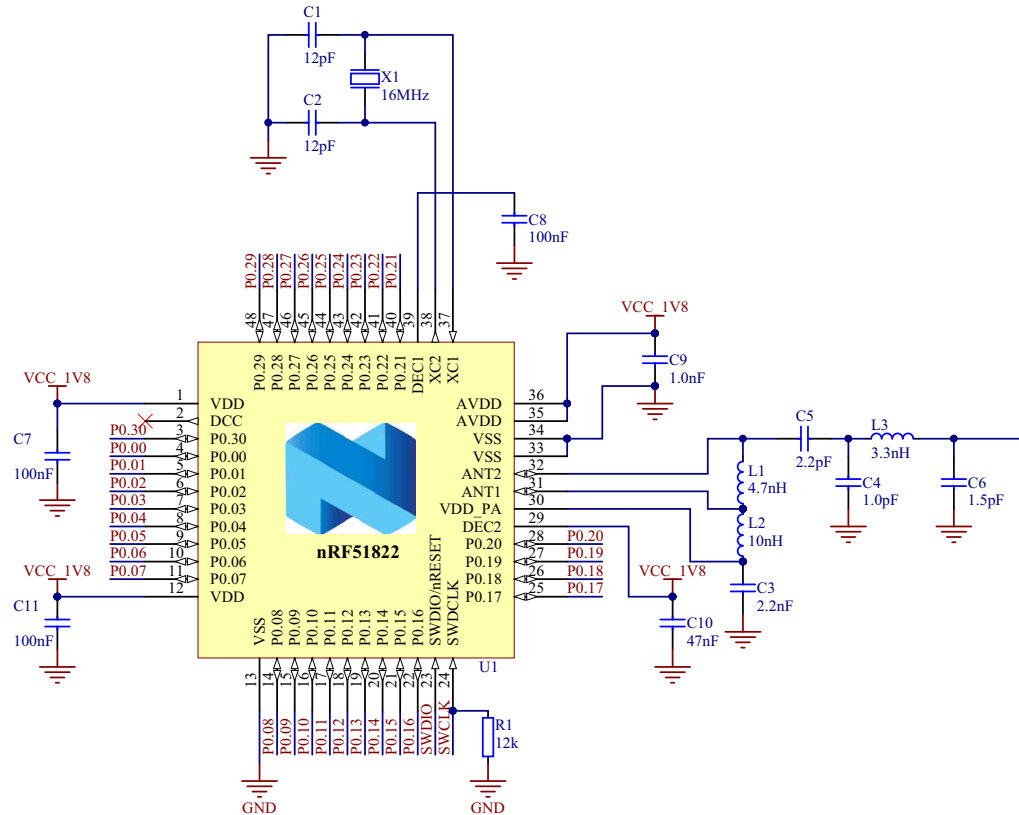


Figure 14 nRF51822 QFN48 with 1.8 V low voltage mode

11.2.2.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, $\pm 2\%$	0402
C3	2.2 nF	Capacitor, X7R, $\pm 10\%$	0402
C4	1.0 pF	Capacitor, NP0, ± 0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ± 0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ± 0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C9	1.0 nF	Capacitor, X7R, $\pm 10\%$	0402
C10	47 nF	Capacitor, X7R, $\pm 10\%$	0402
L1	4.7 nH	High frequency chip inductor $\pm 5\%$	0402
L2	10 nH	High frequency chip inductor $\pm 5\%$	0402
L3	3.3 nH	High frequency chip inductor $\pm 5\%$	0402
R1	12 k Ω	Resistor, $\pm 5\%$, 0.063 W	0402
U1	nRF51822-QFAA nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ± 40 ppm	2.5 x 2.0 mm

Table 64 nRF51822 QFN48 with 1.8 V low voltage mode

11.2.3 nRF51822 QFN48 schematic with internal DC/DC converter

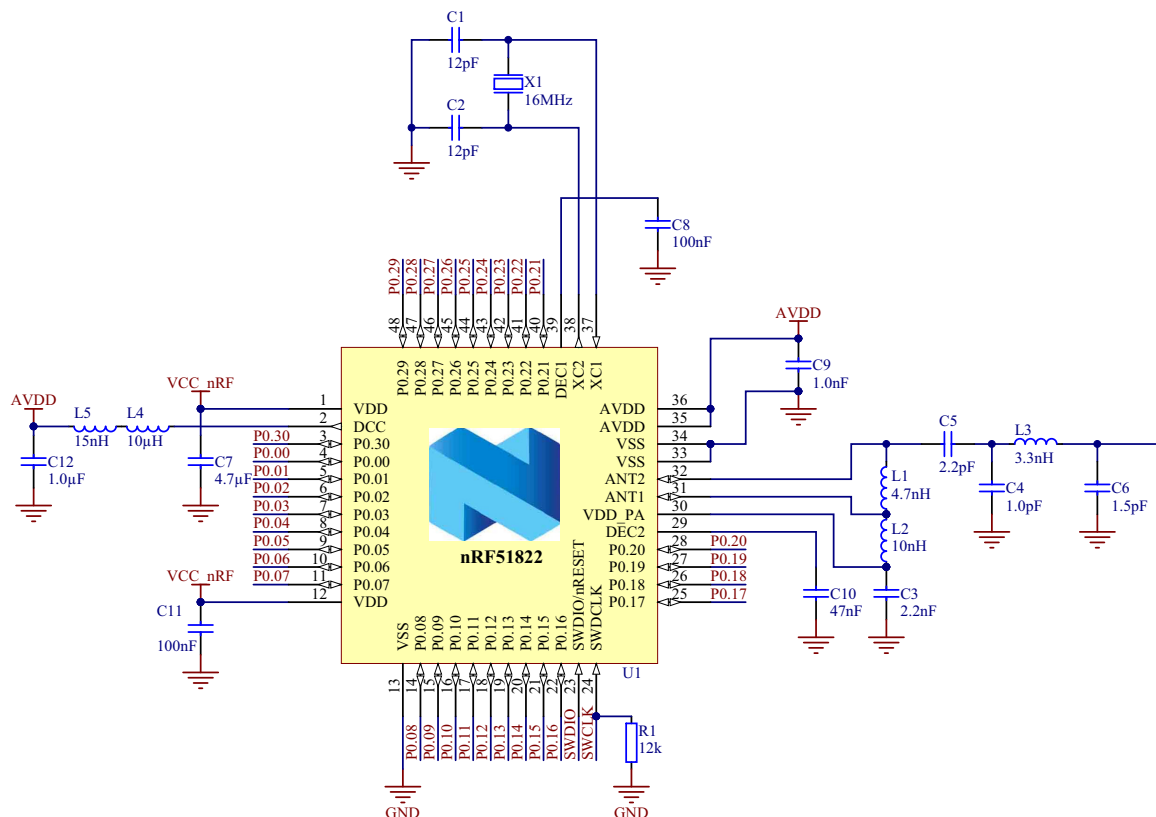


Figure 15 nRF51822 QFN48 with DC/DC converter

11.2.3.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, $\pm 2\%$	0402
C3	2.2 nF	Capacitor, X7R, $\pm 10\%$	0402
C4	1.0 pF	Capacitor, NP0, ± 0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ± 0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ± 0.1 pF	0402
C7	4.7 μ F	Capacitor, X5R, $\pm 10\%$	0603
C8, C11	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C9	1.0 nF	Capacitor, X7R, $\pm 10\%$	0402
C10	47 nF	Capacitor, X7R, $\pm 10\%$	0402
C12	1.0 μ F	Capacitor, X7R, $\pm 10\%$	0603
L1	4.7 nH	High frequency chip inductor $\pm 5\%$	0402
L2	10 nH	High frequency chip inductor $\pm 5\%$	0402
L3	3.3 nH	High frequency chip inductor $\pm 5\%$	0402
L4	10 μ H	Chip inductor, $I_{DC,min} = 50$ mA, $\pm 20\%$	0603
L5	15 nH	High frequency chip inductor $\pm 10\%$	0402
R1	12 k Ω	Resistor, $\pm 5\%$, 0.063 W	0402
U1	nRF51822-QFAA nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ± 40 ppm	2.5 x 2.0 mm

Table 65 nRF51822 QFN48 with DC/DC converter

Documentation for the WLCSP package reference circuit, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from the nRF51822 product page on www.nordicsemi.com.

[illegible]

Figure 16 *nRF51822 WLCSP with internal LDO regulator*

11.3.1.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-NRF02D3
C1, C2	12 pF	Capacitor, NP0, $\pm 2\%$	0402
C3	2.2 nF	Capacitor, X7R, $\pm 10\%$	0402
C7, C8, C11	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C9	1.0 nF	Capacitor, X7R, $\pm 10\%$	0402
C10	47 nF	Capacitor, X7R, $\pm 10\%$	0402
R1	12 k Ω	Resistor, $\pm 5\%$, 0.063 W	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ± 40 ppm	2.5 x 2.0 mm

Table 66 nRF51822 WLCSP with internal LDO regulator

11.3.2 nRF51822 WLCSP schematic with 1.8 V low voltage mode

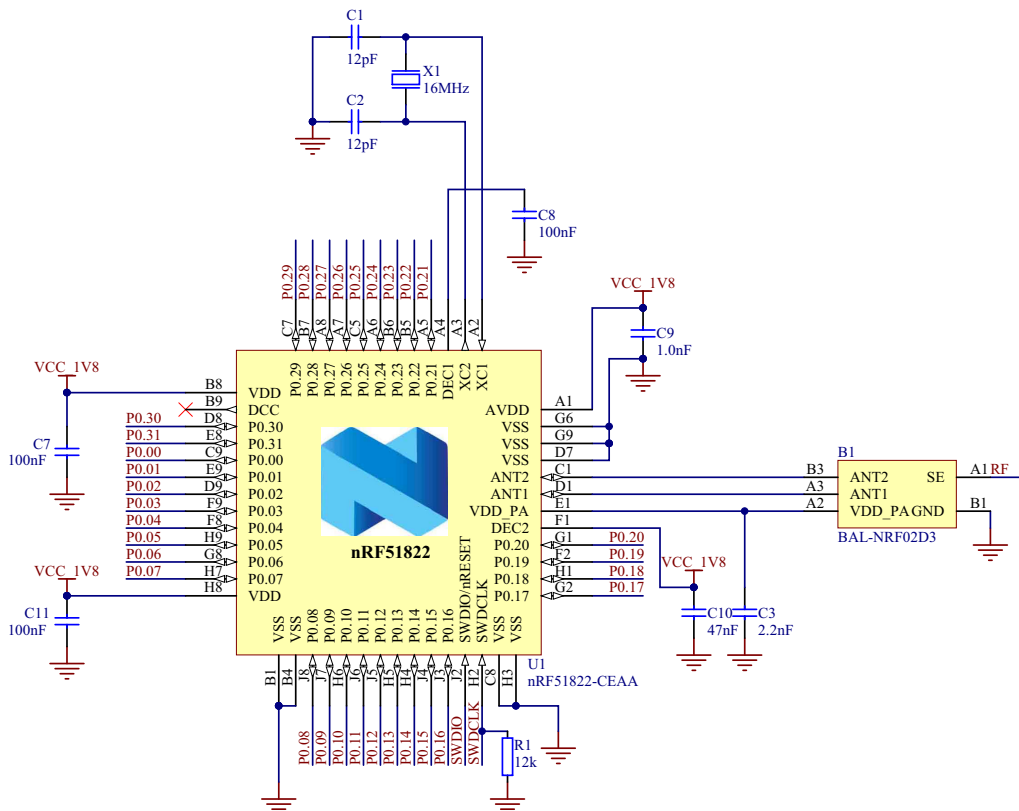


Figure 17 nRF51822 WLCSP with 1.8 V low voltage mode

11.3.2.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-NRF02D3
C1, C2	12 pF	Capacitor, NP0, $\pm 2\%$	0402
C3	2.2 nF	Capacitor, X7R, $\pm 10\%$	0402
C7, C8, C11	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C9	1.0 nF	Capacitor, X7R, $\pm 10\%$	0402
C10	47 nF	Capacitor, X7R, $\pm 10\%$	0402
R1	12 k Ω	Resistor, $\pm 5\%$, 0.063 W	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ± 40 ppm	2.5 x 2.0 mm

Table 67 nRF51822 WLCSP with 1.8 V low voltage mode

11.3.3 nRF51822 WLCSP schematic with internal DC/DC converter

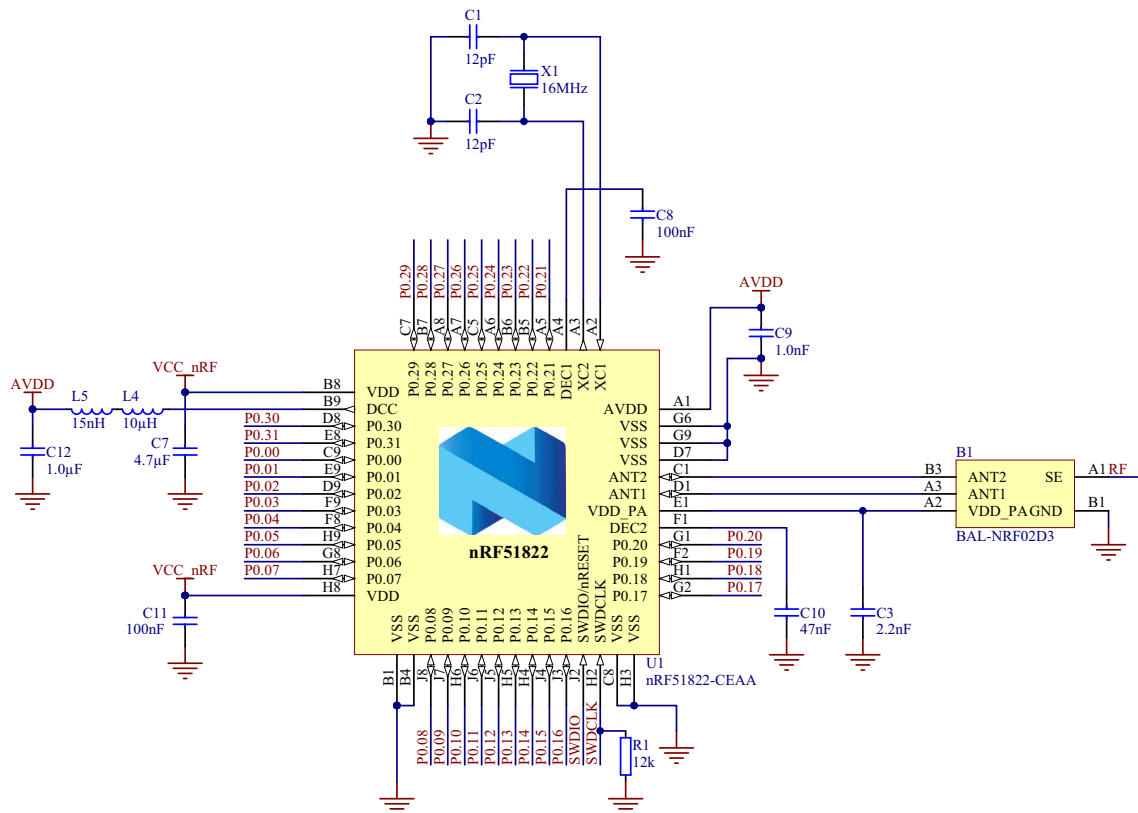


Figure 18 *nRF51822 WLCSP with DC/DC converter*

11.3.3.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-NRF02D3
C1, C2	12 pF	Capacitor, NP0, $\pm 2\%$	0402
C3	2.2 nF	Capacitor, X7R, $\pm 10\%$	0402
C7	4.7 μ F	Capacitor, X5R, $\pm 10\%$	0603
C8, C11	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C9	1.0 nF	Capacitor, X7R, $\pm 10\%$	0402
C10	47 nF	Capacitor, X7R, $\pm 10\%$	0402
C12	1.0 μ F	Capacitor, X7R, $\pm 10\%$	0603
L4	10 μ H	Chip inductor, $I_{DC,min} = 50$ mA, $\pm 20\%$	0603
L5	15 nH	High frequency chip inductor $\pm 10\%$	0402
R1	12 k Ω	Resistor, $\pm 5\%$, 0.063 W	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ± 40 ppm	2.5 x 2.0 mm

Table 68 nRF51822 WLCSP with DC/DC converter

12 Glossary

Term	Description
EOC	Extreme Operating Conditions
GFSK	Gaussian Frequency-Shift Keying
GPIO	General Purpose Input Output
ISM	Industrial Scientific Medical
MOQ	Minimum Order Quantity
NOC	Nominal Operating Conditions
NVMC	Non-Volatile Memory Controller
QDEC	Quadrature Decoder
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Radio Signal Strength Indicator
SPI	Serial Peripheral Interface
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver Transmitter
WLCSP	Wafer Level Chip Scale Packet

Table 69 Glossary