DATA SHEET

MFRC522
Contactless Reader IC

Product Specification
Revision 3.0
CONFIDENTIAL INFORMATION

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Philips
Semiconductors

PHILIPS

CONTENTS

1 GENERAL INFORMATION

1.1 Scope

This document describes the functionality of the contactless reader/writer MFRC522. It includes the functional and electrical specifications.

1.2 General Description

The MFRC522 is a highly integrated reader/writer for contactless communication at 13.56 MHz. The MFRC522 reader supports ISO 14443A / MIFARE® mode.

The MFRC522's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO 14443A / MIFARE® cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO 14443A / MIFARE® compatible cards and transponders. The digital part handles the complete ISO 14443A framing and error detection (Parity & CRC). The MFRC522 supports MIFARE® Classic (e.g. MIFARE® Standard) products. The MFRC522 supports contactless communication using MIFARE® higher transfer speeds up to 424kbit/s in both directions.

Various host interfaces are implemented:

- SPI interface
- serial UART (similar to RS232 with voltage levels according pad voltage supply)
- I2C interface.

1.3 Features

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers to connect an antenna with minimum number of external components
- Supports ISO 14443A / MIFARE®
- typical operating distance in reader/writer mode for communication to a ISO 14443A / MIFARE® up to 50 mm depending on the antenna size and tuning
- Supports MIFARE® Classic encryption in reader/writer mode
- Supports ISO 14443A higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Support of the MFIN / MFOUT
- Additional power supply to directly supply the smart card IC connected via MFIN / MFOUT
- Supported host interfaces
  - SPI interface up to 10 Mbit/s
  - I2C interface up to 400kbit/s in Fast Mode, up to 3400kbit/s in High Speed Mode
  - serial UART in different transfer speeds up to 1228.8 kbit/s, framing according to the RS232 interface with voltage levels according pad voltage supply
- Comfortable 64 byte send and receive FIFO-buffer
- Flexible interrupt modes
- Hard reset with low power function
- Power down mode per software
- Programmable timer
- Internal oscillator to connect 27.12 MHz quartz
- 3.3 V power supply

- CRC Co-processor
- free programable I/O pins
- internal self test

1.4 Simplified MFRC522 Block Diagram

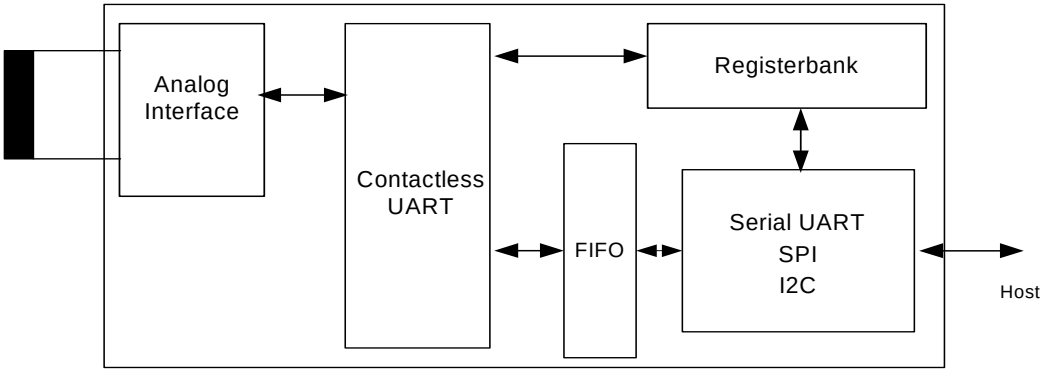

Fig.1 Simplified MFRC522 block diagram

The analog interface handles the modulation and demodulation of the analog signals.

The contactless UART handles the protocol requirements for the communication schemes in co-operation with the host. The comfortable FIFO buffer allows a fast and convenient data transfer from the host to the contactless UART and vice versa.

Various host interfaces are implemented to fulfil different customer requirements.

2 ORDERING INFORMATION

The MFRC522 can be ordered in following packages.

Table 1 Ordering Information

ORDERING CODE	TYPE DESCRIPTION	PACKAGE	VERSION	REMARKS
935280547151	MFRC52201HN1/TRAYB (delivered in 1 Tray)	HVQFN32	SOT617-1	- see Package Outline in Section 21. - see Packing Information in Section 4.1
935280547157	MFRC52201HN1/TRAYBM (delivered in 5 Tray)	HVQFN32	SOT617-1	- see Package Outline in Section 21. - see Packing Information in Section 4.2

Detailed package information can be found on Philips Internet:
http://www.semiconductors.philips.com/package/SOT617-1.html

3 HANDLING INFORMATION

Moisture Sensitivity Level (MSL) Evaluation has been performed according to SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C). MSL for this package is level 1 which means 260°C convection reflow temperature.

Dry pack is not required.

Unlimited out of pack Floor Life at maximum ambient 30°C/85%RH.

4 PACKING INFORMATION

4.1 1 Tray

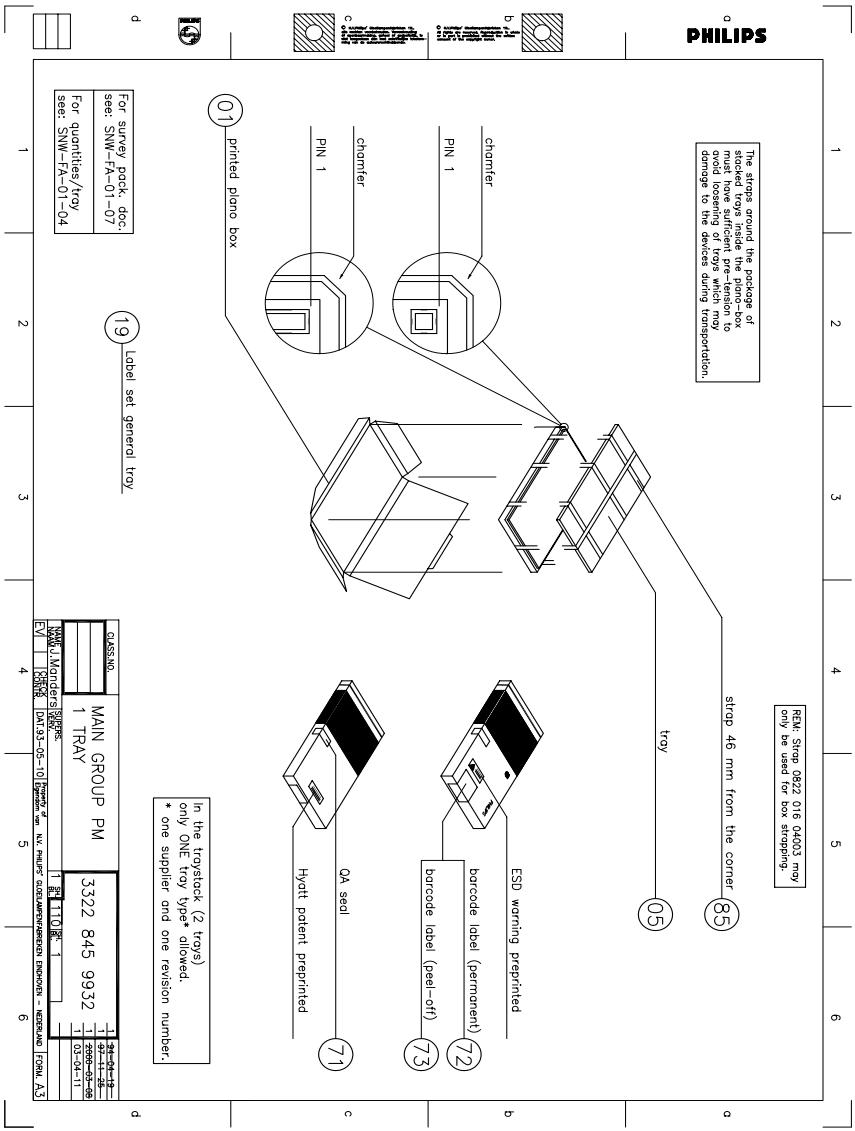

Fig.1 Packing Information 1 Tray

4.2 5 Tray

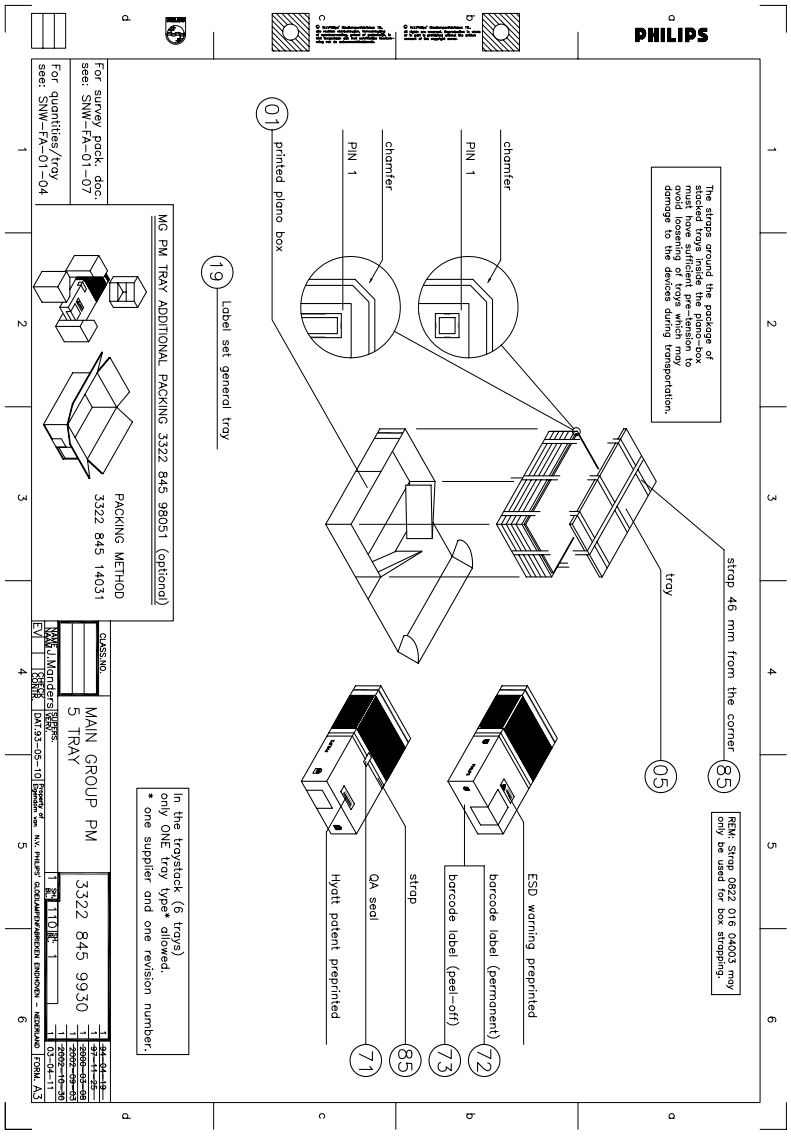

Fig.1 Packing Information 5 Tray

5 PINNING INFORMATION

5.1 Packages

The MFRC522 can be delivered in following packages:

Table 2 Package Information

PACKAGE	FUNCTIONAL REMARKS
HVQFN32	supports I²C, SPI and RS232 interface

5.2 Pin Description

Table 3 Pin Description

Note: Pin Types: I...Input; O...Output; PWR...Power

SYMBOL	HVQFN32	TYPE	DESCRIPTION
OSCIN	21	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (fosc = 27.12 MHz).
IRQ	23	O	**Interrupt Request:** output to signal an interrupt event
MFIN	7	I	**Mifare Signal Input**
MFOUT	8	O	**Mifare Signal Output**
TX1	11	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
TVDD	12	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
TX2	13	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
TVSS	10, 14	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
DVSS	4	PWR	**Digital Ground**
D1	25	I/O	
D2	26	I/O	
D3	27	I/O	
D4	28	I/O	**Data Pins for different interfaces (test port, I²IC, SPI, UART)**
D5	29	I/O	
D6	30	I/O	
D7	31	I/O	
SDA	24	I	**Serial Data Line**
EA	32	I	**External Address:** This Pin is used for coding I²C Address
I2C	1	I	**I²C enable**
DVDD	3	PWR	**Digital Power Supply**
AVDD	15	PWR	**Analog Power Supply**
AUX1	19	O	**Auxiliary Outputs:** These pins are used for testing.
AUX2	20	O	
AVSS	18	PWR	**Analog Ground**
RX	17	I	**Receiver Input:** Pin for the received RF signal.

SYMBOL	HVQFN32	TYPE	DESCRIPTION
VMID	16	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
NRSTPD	6	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world.With a positive edge on this pin the internal reset phase starts.
OSCOUT	22	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
SVDD	9	PWR	**MFIN / MFOUT Pad Power Supply:** provides power to for the MFIN / MFOUT pads
PVDD	2	PWR	**Pad power supply**
PVSS	5	PWR	**Pad Power supply ground**

The pin functionality for the interfaces is explained in chapter 9.

6 BLOCK DIAGRAM

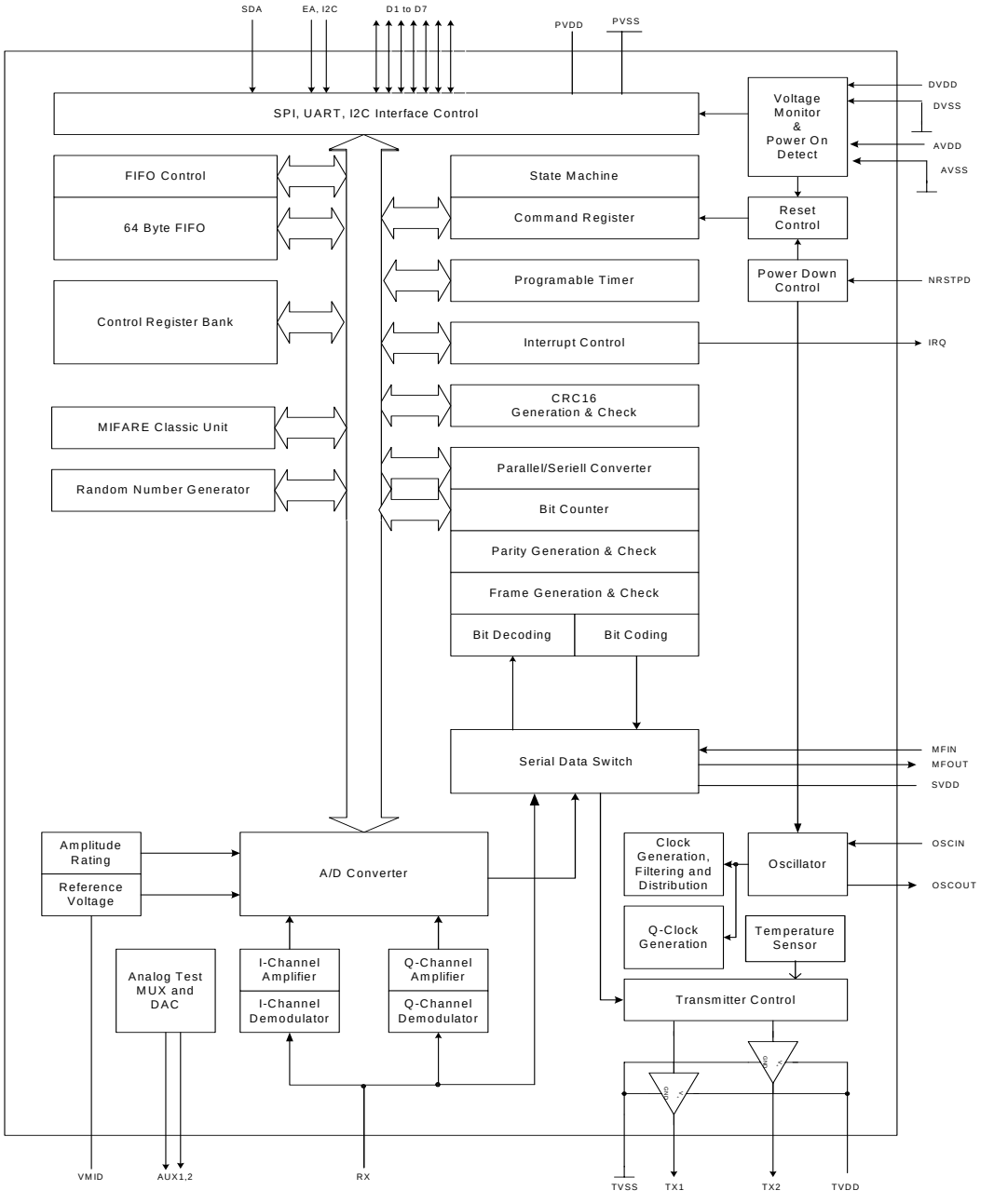

Fig.2 MFRC522 Block Diagram.

7 MFRC522 REGISTER SET

7.1 MFRC522 Registers Overview

Table 4 MFRC522 Register Overview

ADDR (HEX)	REGISTER NAME	FUNCTION
PAGE 0: COMMAND AND STATUS		
0	RFU	Reserved for future use
1	CommandReg	Starts and stops the command execution
2	ComlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
3	DivlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
4	ComIrqReg	Contains Interrupt Request bits
5	DivIrqReg	Contains Interrupt Request bits
6	ErrorReg	Error bits showing the error status of the last command executed
7	Status1Reg	Contains status bits for communication
8	Status2Reg	Contains status bits of the receiver and transmitter
9	FIFODataReg	In- and output of 64 byte FIFO buffer
A	FIFOLevelReg	Indicates the number of bytes stored in the FIFO
B	WaterLevelReg	Defines the level for FIFO under- and overflow warning
C	ControlReg	Contains miscellaneous Control Register
D	BitFramingReg	Adjustments for bit oriented frames
E	CollReg	Bit position of the first bit collision detected on the RF-interface
F	RFU	Reserved for future use
PAGE 1: COMMAND		
0	RFU	Reserved for future use
1	ModeReg	Defines general modes for transmitting and receiving
2	TxModeReg	Defines the transmission data rate during transmission
3	RxModeReg	Defines the transmission data rate during receiving
4	TxControlReg	Controls the logical behaviour of the antenna driver pins TX1 and TX2
5	TxASKReg	Controls the setting of the TX modulation
6	TxSelReg	Selects the internal sources for the antenna driver
7	RxSelReg	Selects internal receiver settings
8	RxThresholdReg	Selects thresholds for the bit decoder
9	DemodReg	Defines demodulator settings
A	RFU	Reserved for future use
B	RFU	Reserved for future use
C	MfTxReg	Controls some MIFARE® communication transmit parameters
D	MfRxReg	Controls some MIFARE® communication receive parameters
E	RFU	Reserved for future use
F	SerialSpeedReg	Selects the speed of the serial UART interface
PAGE 2: CFG		
0	RFU	Reserved for future use

ADDR (HEX)	REGISTER NAME	FUNCTION
1	CRCResultReg	Shows the actual MSB and LSB values of the CRC calculation
2		
3	RFU	Reserved for future use
4	ModWidthReg	Controls the setting of the ModWidth
5	RFU	Reserved fur future use
6	RFCfgReg	Configures the receiver gain
7	GsNReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation
8	CWGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation
9	ModGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation
A	TModeReg TPrescalerReg	Defines settings for the internal timer
B		
C	TReloadReg	Describes the 16 bit long timer reload value
D		
E	TCounterValueReg	Shows the 16 bit long actual timer value
F		
PAGE 3: TEST		
0	RFU	Reserved for future use
1	TestSel1Reg	General test signal configuration
2	TestSel2Reg	General test signal configuration and PRBS control
3	TestPinEnReg	Enables pin output driver on D1-D7 (Note: For serial interfaces only)
4	TestPin ValueReg	Defines the values for D1 - D7 when it is used as I/O bus
5	TestBusReg	Shows the status of the internal test bus
6	AutoTestReg	Controls the digital self test
7	VersionReg	Shows the version
8	AnalogTestReg	Controls the pins AUX1 and AUX2
9	TestDAC1Reg	Defines the test value for the TestDAC1
A	TestDAC2Reg	Defines the test value for the TestDAC2
B	TestADCReg	Show the actual value of ADC I and Q
C-F	RFT	Reserved for production tests

7.1.1 Register Bit Behaviour

Bits for different registers behave differently, depending on their functions. In principle bits with same behaviour are grouped in common registers.

Table 5 Behaviour of Register Bits and its Designation

ABBREVIATION	BEHAVIOUR	DESCRIPTION
r/w	read and write	These bits can be written and read by the μ-Controller. Since they are used only for control means, there content is not influenced by internal state machines, e.g. the ComlEnReg-Register may be written and read by the μ-Controller. It will also be read by internal state machines, but never changed by them.
dy	dynamic	These bits can be written and read by the μ-Controller. Nevertheless, they may also be written automatically by internal state machines, e.g. the *Command-Register* changes its value automatically after the execution of the actual command.
r	read only	These registers hold bits, which value is determined by internal states only, e.g. the *CRCReady* bits can not be written from external but shows internal states.
w	write only	Reading these registers returns always ZERO.
RFU	-	These registers are reserved for future use and shall not be changed.
RFT	-	These registers are reserved for production tests and shall not be changed.

7.2 Register Description

7.2.1 PAGE 0: COMMAND AND STATUS

7.2.1.1 RFU Register

Functionality is RFU

Table 6 RFUReg

RFUReg	**Address 0x00**							**Reset value 00000000 (0x00)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFU							

Table 7 Description of RFUReg bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFU

7.2.1.2 CommandReg

Starts and stops the command execution.

Table 8 CommandReg

CommandReg	**Address 0x01**	**Reset value 00100000 (0x20)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00		RcvOff	Power Down	Command			
Access Rights	RFU		r/w	dy	dy			

Table 9 Description of CommandReg bits

BIT	SYMBOL	FUNCTION
7-6	00	RFU.
5	RcvOff	Set to 1, the analog part of the receiver is switched off.
4	PowerDown	Set to 1, the Soft PowerDown Mode is entered. Set to 0, the MFRC522 starts the wake up procedure. During this procedure this bit still shows a 1. A 0 indicates that the MFRC522 is ready for operation. See chapter 15.2. Note: The bit Power Down cannot be set, when the command SoftReset is has been activated.
3-0	Command	Activates a command according to the Command Code. Reading this register shows, which command is actually executed. See chapter 17.3.

7.2.1.3 CommIEnReg

Controls bits to enable and disable the passing of interrupt requests.

Table 10 CommIEnReg

CommIEnReg **Address 0x02** **Reset value 10000000 (0x80)**

Bit	7	6	5	4	3	2	1	0
Symbol	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 11 Description of CommIEnReg bits

BIT	SYMBOL	FUNCTION
7	IRqInv	Set to 1, the signal on pin IRQ is inverted with respect to bit *IRq* in the register *Status1Reg*. Set to 0, the signal on pin IRQ is equal to bit *IRq*. In combination with bit *IRqPushPull* in register *DivIEnReg*, the default value of 1 ensures, that the output level on pin IRQ is tristate.
6	TxIEn	Allows the transmitter interrupt request (indicated by bit *TxIRq*) to be propagated to pin IRQ.
5	RxIEn	Allows the receiver interrupt request (indicated by bit *RxIRq*) to be propagated to pin IRQ.
4	IdleIEn	Allows the idle interrupt request (indicated by bit *IdleIRq*) to be propagated to pin IRQ.
3	HiAlertIEn	Allows the high alert interrupt request (indicated by bit *HiAlertIRq*) to be propagated to pin IRQ.
2	LoAlertIEn	Allows the low alert interrupt request (indicated by bit LoAlertIRq) to be propagated to pin IRQ.
1	ErrIEn	Allows the error interrupt request (indicated by bit ErrIRq) to be propagated to pin IRQ.
0	TimerIEn	Allows the timer interrupt request (indicated by bit TimerIRq) to be propagated to pin IRQ.

7.2.1.4 DivIEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 12 DivIEnReg

DivIEnReg **Address 0x03** **Reset value: 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	IRQPushPull	00		MfinActIEn	0	CRCIEn	00	
Access Rights	r/w	RFU		r/w	RFU	r/w	RFU	

Table 13 Description of DivIEnReg bits

BIT	SYMBOL	FUNCTION
7	IRQPushPull	Set to 1, the pin IRQ works as standard CMOS output pad. Set to 0, the pin IRQ works as open drain output pad.
6-5	00	RFU.
4	MfinActIEn	Allows the MFIN active interrupt request to be propagated to pin IRQ.
3	0	RFU
2	CRCIEn	Allows the CRC interrupt request (indicated by bit *CRCIRq*) to be propagated to pin IRQ.
1-0	00	RFU

7.2.1.5 CommIRqReg

Contains Interrupt Request bits.

Table 14 CommIRqReg

CommIRqReg **Address 0x04** **Reset value 00010100 (0x14)**

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access Rights	w	dy	dy	dy	dy	dy	dy	dy

Table 15 Description of CommIRQReg bits

BIT	SYMBOL	FUNCTION
7	Set1	Set to 1, Set1 defines that the marked bits in the register *CommIRqReg* are set. Set to 0, Set1 defines, that the marked bits in the register *CommIRqReg* are cleared.
6	TxIRq	Set to 1, immediately after the last bit of the transmitted data was sent out.
5	RxIRq	Set to 1, when the receiver detects the end of a valid data stream. If the bit *RxNoErr* in register *RxModeReg* is set to 1, Bit *RxIRq* is only set to 1 when data bytes are available in the FIFO.
4	IdleIRq	Set to 1, when a command terminates by itself e.g. when the *CommandReg* changes its value from any command to the Idle Command. If an unknown command is started, the *CommandReg* changes its content to the idle state and the bit *IdleIRq* is set. Starting the Idle Command by the µ-Controller does not set bit *IdleIRq*.
3	HiAlertIRq	Set to 1, when bit *HiAlert* in register *Status1Reg* is set. In opposition to *HiAlert*, *HiAlertIRq* stores this event and can only be reset as indicated by bit *Set1*.
2	LoAlertIRq	Set to 1, when bit *LoAlert* in register *Status1Reg* is set. In opposition to *LoAlert*, *LoAlertIRq* stores this event and can only be reset as indicated by bit *Set1*.
1	ErrIRq	Set to 1, if any error bit in the Error Register is set
0	TimerIRq	Set to 1, when the timer decrements the TimerValue Register to zero.

Note

1. All bits in the register *CommIRqReg* shall be cleared by software.

7.2.1.6 DivIRqReg

Contains Interrupt Request bits

Table 16 DivIRqReg

DivIRqReg	**Address 0x05**						**Reset value 000x0000 (0xX0)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Set2	00		MfinActIRq	0	CRCIRq	00	
Access Rights	w	RFU		dy	RFU	dy	RFU	

Table 17 Description of DivIRqReg bits

BIT	SYMBOL	FUNCTION
7	Set2	Set to 1, *Set2* defines that the marked bits in the register *DivIRqReg* are set. Set to 0, *Set2* defines, that the marked bits in the register *DivIRqReg* are cleared
6-5	00	RFU
4	MfinActIRq	Set to 1, when MFIN is active. This interrupt is set when either a rising or falling signal edge is detected.
3	0	RFU
2	CRCIRq	Set to 1, when the CRC command is active and all data is processed.
1-0	00	RFU

Note

1. All bits in the register *DivIRqReg* shall be cleared by software.

7.2.1.7 ErrorReg

Error bit register showing the error status of the last command executed.

Table 18 ErrorReg

ErrorReg **Address 0x06** **Reset value 0x000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	0	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access Rights	r	r	RFU	r	r	r	r	r

Table 19 Description of ErrorReg bits

BIT	SYMBOL	FUNCTION
7	WrErr	Set to 1, when data is written into the FIFO by the host during the MFAuthent command or if data is written into the FIFO by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface.
6	TempErr	Set to 1, if the internal temperature sensor detects overheating. In this case, the antenna drivers are switched off automatically.
5	0	RFU
4	BufferOvfl	Set to 1, if the host or a MFRC522's internal state machine (e.g. receiver) tries to write data into the FIFO buffer although the FIFO buffer is already full.
3	CollErr	Set to 1, if a bit-collision is detected. It is cleared automatically at receiver start-up phase. This bit is only valid during the bit wise anticollsion at 106kbit/s. During communication schemes at 212 and 424kbit/s this bit is always set to ZERO.
2	CRCErr	Set to 1, if bit *RxCRCEn* in register *RxModeReg* is set and the CRC calculation fails. It is cleared to 0 automatically at receiver start-up phase.
1	ParityErr	Set to 1, if the parity check has failed. It is cleared automatically at receiver start-up phase. Only valid for ISO 14443A / MIFARE® communication at 106 kbit/s.
0	ProtocolErr	Set to 1, if one out of the following cases occur: a.) Set to 1 if the SOF is incorrect. It is cleared automatically at receiver start-up phase. The bit is only valid for 106kbit/s. b.) During the MFAuthent Command, bit *ProtocolErr* is set to 1, if the number of bytes received in one data stream is incorrect.

Note

1. Command execution will clear all error bits except for bit *TempErr*. A setting by software is impossible.

7.2.1.8 Status1Reg

Contains status bits of the CRC, Interrupt and FIFO buffer.

Table 20 Status1Reg

Status1Reg **Address 0x07** **Reset value 00100001 (0x21)**

Bit	7	6	5	4	3	2	1	0
Symbol	0	CRCOk	CRCReady	IRq	TRunning	0	HiAlert	LoAlert
Access Rights	RFU	r	r	r	r	RFU	r	r

Table 21 Description of Status1Reg bits

BIT	SYMBOL	FUNCTION
7	0	RFU
6	CRCOk	Set to 1, if the CRC Result is zero. For data transmission and reception the bit *CRCOk* is undefined (use *CRCErr* in register *ErrorReg*). *CRCOk* indicates the status of the CRC coprocessor, during calculation the value changes to ZERO, when the calculation is done correctly, the value changes to ONE.
5	CRCReady	Set to 1, when the CRC calculation has finished. This bit is only valid for the CRC coprocessor calculation using the command CalcCRC.
4	IRq	This bit shows, if any interrupt source requests attention (with respect to the setting of the interrupt enable bits, see register *CommIEnReg* and *DivIEnReg*).
3	TRunning	Set to 1, if the MFRC522's timer unit is running, e.g. the timer will decrement the *TCounterValReg* with the next timer clock. Note: In the gated mode the bit TRunning is set to 1, when the timer is enabled by the register bits. This bit is not influenced by the gated signal.
2	0	RFU
1	HiAlert	Set to 1, when the number of bytes stored in the FIFO buffer fulfils the following equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ Example: FIFOLength=60, WaterLevel=4 → HiAlert =1 FIFOLength=59, WaterLevel=4 → HiAlert =0
0	LoAlert	Set to 1, when the number of bytes stored in the FIFO buffer fulfils the following equation: $LoAlert = FIFOLength \leq WaterLevel$ Example: FIFOLength=4, WaterLevel=4 → LoAlert =1 FIFOLength=5, WaterLevel=4 → LoAlert =0

7.2.1.9 Status2Reg

Contains status bits of the receiver, transmitter and data mode detector.

Table 22 Status2Reg

Status2Reg **Address 0x08** **Reset value 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	TempSens Off	I2C ForceHS	00		MFCrypto1 On	Modem State		
Access Rights	r/w	r/w	RFU		dy	r		

Table 23 Description of Status2Reg bits

BIT	SYMBOL	FUNCTION
7	TempSensOff	Set to 1, this bit clears the temperature error, if the temperature is below the alarm limit of 125°C.
6	I2CForceHS	I2C input filter settings. Set to 1, the I2C input filter is set to the high speed mode independent of the I2C protocol. Set to 0, the I2C input filter is set to the used I2C protocol.
5-4	00	RFU.
3	MFCrypto1On	This bit indicates that the MIFARE® Crypto1 unit is switched on and therefore all data communication with the card is encrypted. This bit can only be set to 1 by a successful execution of the MFAuthent Command. This bit is only valid in reader/writer mode for MIFARE® Standard cards. This bit can be cleared by software.
2- 0	ModemState	*ModemState* shows the state of the transmitter and receiver state machines. **Status Description** 000 IDLE 001 Wait for bit *StartSend* set in register *BitFramingReg* 010 TxWait: Wait until RF field is present, if the bit *TxWaitRF* is set to 1. The wait time for *TxWait* is defined by the *TxWaitReg* register. 011 Transmitting 100 RxWait: Wait until RF field is present, if the bit *RxWaitRF* is set to 1. The wait time for *RxWait* is defined by the *RxWaitReg* register. 101 Wait for data 110 Receiving

7.2.1.10 FIFODataReg

In- and output of 64 byte FIFO buffer.

Table 24 FIFODataReg

FIFODataReg	**Address 0x09**	**Reset value xxxxxxxx (0xXX)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FIFOData							
Access Rights	dy							

Table 25 Description of FIFODataReg bits

BIT	SYMBOL	FUNCTION
7-0	FIFOData	Data input and output port for the internal 64 byte FIFO buffer. The FIFO buffer acts as parallel in / parallel out converter for all serial data stream in- and outputs.

7.2.1.11 FIFOLevelReg

Indicates the number of bytes stored in the FIFO.

Table 26 FIFOLevelReg

FIFOLevelReg	**Address 0x0A**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FlushBuffer	FIFOLevel						
Access Rights	w	r						

Table 27 Description of FIFOLevelReg bits

BIT	SYMBOL	FUNCTION
7	FlushBuffer	Set to 1, this bit clears the internal FIFO-buffer's read- and write-pointer and the bit *BufferOvfl i*n the register *ErrReg* immediately. Reading this bit will always return 0.
6-0	FIFOLevel	Indicates the number of bytes stored in the FIFO buffer. Writing to the *FIFODataReg* increments, reading decrements the *FIFOLevel.*

7.2.1.12 WaterLevelReg

Defines the level for FIFO under- and overflow warning.

Table 28 WaterLevelReg

WaterLevelReg **Address 0x0B** **Reset value 00001000 (0x08)**

Bit	7	6	5	4	3	2	1	0
Symbol	00		WaterLevel					
Access Rights	RFU		r/w					

Table 29 Description of WaterLevelReg bits

BIT	SYMBOL	FUNCTION
7-6	00	RFU.
5-0	WaterLevel	This register defines a warning level to indicate a FIFO-buffer over- or underflow: The bit *HiAlert* in *Status1Reg* is set to 1, if the remaining number of bytes in the FIFO-buffer space is equal or less than the defined number of *WaterLevel* bytes. The bit *LoAlert* in *Status1Reg* is set to 1, if equal or less than *WaterLevel* bytes are in the FIFO. Note: For the calculation of HiAlert and LoAlert see clause in section 7.2.1.8.

7.2.1.13 ControlReg

Miscellaneous control bits.

Table 30 ControlReg

ControlReg **Address 0x0C** **Reset value 00010000 (0x10)**

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow	010			RxLastBits		
Access Rights	w	w	RFU			r		

Table 31 Description of ControlReg bits

BIT	SYMBOL	FUNCTION
7	TStopNow	Set to 1, the timer stops immediately. Reading this bit will always return 0.
6	TStartNow	Set to 1, starts the timer immediately. Reading this bit will always return 0.
5-3	010	RFU
2-0	RxLastBits	Shows the number of valid bits in the last received byte. If zero, the whole byte is valid.

7.2.1.14 BitFramingReg

Adjustments for bit oriented frames.

Table 32 BitFramingReg

BitFramingReg **Address 0x0D** **Reset value 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend	RxAlign			0	TxLastBits		
Access Rights	w	dy			RFU	dy		

Table 33 Description of BitFraming Register bits

BIT	SYMBOL	FUNCTION
7	StartSend	Set to 1, the transmission of data starts. This bit is only valid in combination with the Transceive command.
6-4	RxAlign	Used for reception of bit oriented frames: *RxAlign* defines the bit position for the first bit received to be stored in the FIFO. Further received bits are stored in the following bit positions. Example: *RxAlign* = 0: the LSB of the received bit is stored at bit 0, the second received bit is stored at bit position 1. RxAlign = 1: the LSB of the received bit is stored at bit 1, the second received bit is stored at bit position 2. RxAlign = 7: the LSB of the received bit is stored at bit 7, the second received bit is stored in the following byte at bit position 0. This bit shall only be used for bit wise anticollision at 106kbit/s. In all other modes it shall be set to ZERO.
3	0	RFU
2-0	TxLastBits	Used for transmission of bit oriented frames: *TxLastBits* defines the number of bits of the last byte that shall be transmitted. A 000 indicates that all bits of the last byte shall be transmitted.

7.2.1.15 CollReg

Defines the first bit collision detected on the RF interface.

Table 34 CollReg

CollReg	**Address 0x0E**							**Reset value 101XXXXX (0xXX)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Values AfterColl	0	CollPos NotValid	CollPos				
Access Rights	r/w	RFU	r	r				

Table 35 Description of CollReg Register bits

BIT	SYMBOL	FUNCTION
7	ValuesAfterColl	If this bit is set to 0, all receiving bits will be cleared after a collision. This bit shall only be used during bit wise anticollision at 106 kbit/s, otherwise it shall be set to 1.
6	0	RFU.
5	CollPosNotValid	Set to 1, if no Collision is detected or the Position of the Collision is out of the range of bits *CollPos*.
4-0	CollPos	These bits show the bit position of the first detected collision in a received frame, only data bits are interpreted Example: 0x00 indicates a bit collision in the start bit 0x01 indicates a bit collision in the 1st bit 0x08 indicates a bit collision in the 8th bit These bits shall only be interpreted if bit *CollPosNotValid* is set to 0.

7.2.1.16 RFU Register

Function is RFU

Table 36 RFUReg

RFUReg	**Address 0x0F**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFU							

Table 37 Description of RFUReg bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFU

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7.2.2.1 RFU Register

Functionality is RFU

Table 38 RFUReg

RFUReg	**Address 0x10**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFU							

Table 39 Description of RFUReg bits

BIT	**SYMBOL**	**FUNCTION**
7-0	00000000	RFU

7.2.2.2 ModeReg

Defines general mode settings for transmitting and receiving.

Table 40 ModeReg

ModeReg **Address 0x11** **Reset value 00111111 (0x3F)**

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	0	TxWaitRF	1	PolMfin	1	CRCPreset	
Access Rights	r/w	RFU	r/w	RFU	r/w	RFU	r/w	r/w

Table 41 Description of ModeReg bits

BIT	SYMBOL	FUNCTION
7-6	MSBFirst	Set to 1, the CRC co-processor calculates the CRC with MSB first and the *CRCResultMSB* and the *CRCResultLSB* in the *CRCResultReg* register are bit reversed. Note: During RF communication this bit is ignored.
6	0	RFU
5	TxWaitRF	Set to 1 the transmitter can only be started, if an RF field is generated.
4	1	RFU
3	PolMfin	PolMfin defines the polarity of the MFIN pin. Set to 1, the polarity of MFIN pin is active high. Set to 0 the polarity of MFIN pin is active low. Note: The internal envelope signal is coded active low. Note: Changing this bit will generate a MfinActIRq event.
2	1	RFU
1-0	CRCPreset	Defines the preset value for the CRC co-processor for the command CalCRC. Note: During any communication, the preset values is selected automatically according to the definition in the bits RxMode and TxMode. **Status** **Description** 00 0000 01 6363 10 A671 11 FFFF

7.2.2.3 TxModeReg

Defines the data rate during transmission.

Table 42 TxModeReg

TxModeReg	**Address 0x12**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TxCRCEn	TxSpeed			InvMod	000		
Access Rights	r/w	dy			r/w	RFU		

Table 43 Description of TxModeReg bits

BIT	SYMBOL	FUNCTION
7	TxCRCEn	Set to 1, this bit enables the CRC generation during data transmission. Note: This bit shall only set to 0 at 106kbit/s.
6-4	TxSpeed	Defines the bit rate while data transmission. The MFRC522's handles transfer speeds up to 424kbit/s. **Status** **Description** 000 106 kbit/s 001 212 kbit/s 010 424 kbit/s 011 (848 kbit/s) 100 RFU 101 RFU 110 RFU 111
3	InvMod	Set to 1, the modulation for transmitting data is inverted.
2-0	000	RFU

7.2.2.4 RxModeReg

Defines the data rate during reception.

Table 44 RxModeReg

RxModeReg **Address 0x13** **Reset value 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	RxCRCEn	RxSpeed			RxNoErr	RxMultiple	00	
Access Rights	r/w	dy			r/w	r/w	RFU	

Table 45 Description of RxModReg bits

BIT	SYMBOL	FUNCTION
7	RXCRCEn	Set to 1, this bit enables the CRC calculation during reception. Note: This bit shall only be set to 0 at 106kbit/s.
6-4	RxSpeed	Defines the bit rate while data receiving. The MFRC522's handles transfer speeds up to 424kbit/s. **Status** **Description** 000 106 kbit/s 001 212 kbit/s 010 424 kbit/s 011 (848 kbit/s) 100 RFU 101 RFU 110 RFU 111 RFU
3	RxNoErr	f set to 1, a not valid received data stream (less than 4 bits received) will be ignored. The receiver will remain active.
2	RxMultiple	Set to 0, the receiver is deactivated after receiving a data frame. Set to 1, it is possible to receive more than one data frame. This bit is only valid for data rates above 106 kbit/s to handle the Polling command. Having set this bit, the receive and transceive commands will not terminate automatically. In this case the multiple receiving can only be deactivated by writing any command (except the Receive command) to the CommandReg register or by clearing the bit by the host. If set to 1, at the end of a received data stream an error byte is added to the FIFO. The error byte is a copy of the *ErrorReg* register.
1-0	00	RFU

7.2.2.5 TxControlReg

Controls the logical behaviour of the antenna driver pins Tx1 and Tx2.

Table 46 TxControlReg

TxControlReg **Address 0x14** **Reset value 10000000 (0x80)**

Bit	7	6	5	4	3	2	1	0
Symbol	InvTX2RF On	InvTX1RF On	InvTX2RF Off	InvTX1RF Off	Tx2CW	0	Tx2RFEn	Tx1RFEn
Access Rights	r/w	r/w	r/w	r/w	r/w	RFU	r/w	r/w

Table 47 Description of TxControlReg bits

BIT	SYMBOL	FUNCTION
7	InvTX2RFOn	Set to 1, the output signal at pin TX2 will be inverted, if the driver TX2 is enabled.
6	InvTX1RFOn	Set to 1, the output signal at pin TX1 will be inverted, if the driver TX1 is enabled.
5	InvTX2RFOff	Set to 1, the output signal at pin TX2 will be inverted, if the driver TX2 is disabled.
4	InvTx1RFOff	Set to 1, the output signal at pin TX1 will be inverted, if the driver TX1 is disabled.
3	Tx2CW	Set to 1, the output signal on pin TX2 will deliver continuously the un-modulated 13.56 MHz energy carrier. Set to 0, *Tx2CW* is enabled to modulate the 13.56 MHz energy carrier.
2	0	RFU
1	Tx2RFEn	Set to 1, the output signal on pin TX2 will deliver the 13.56 MHz energy carrier modulated by the transmission data.
0	Tx1RFEn	Set to 1, the output signal on pin TX1 will deliver the 13.56 MHz energy carrier modulated by the transmission data.

7.2.2.6 TxASKReg

Controls the setting of the TX modulation

Table 48 TxASKReg

TxASKReg	**Address 0x15**							**Reset value 00000000 (0x00)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	0	Force100 ASK	000000					
Access Rights	RFU	r/w	RFU					

Table 49 Description of TxASKReg bits

BIT	SYMBOL	FUNCTION
7	0	RFU
6	Force100ASK	Set to 1, *Force100ASK* forces a 100% ASK modulation independent of the setting in register *ModGsPReg*.
5-0	000000	RFU

7.2.2.7 TxSelReg

Selects the internal sources for the analog part.

Table 50 TxSelReg

TxSelReg **Address 0x16** **Reset value 00010000 (0x10)**

Bit	7	6	5	4	3	2	1	0
Symbol	00		DriverSel		MfOutSel			
Access Rights	RFU		r/w		r/w			

Table 51 Description of TxSelReg bits

BIT	SYMBOL	FUNCTION	
7-6	00	RFU	
5-4	DriverSel	Selects the input of driver Tx1 and Tx2.	
		Value	**Description**
		00	Tristate Note: In soft power down the drivers are only in tristate mode if DriverSel is set to tristate mode.
		01	Modulation signal (envelope) from the internal coder, Miller Pulse Coded
		10	Modulation signal (envelope) from MFIN
		11	HIGH Note: The HIGH level depends on the setting of InvTx1RFOn/InvTX1RFOff and InvTx2RFOn/InvTx2RFOff.
3-0	MfOutSel	Selects the input for the MFOUT Pin.	
		Value	**Description**
		0000	Tristate
		0001	Low
		0010	High
		0011	Test bus signal as defined bit TestBusBitSel in register TestSel1Reg.
		0100	Modulation signal (envelope) from the internal coder, Miller Puls Coded
		0101	Serial data stream to be transmitted, data stream before Miller Coder
		0110	RFU
		0111	Serial data stream received, data stream after Manchester Decoder
		1000-1111	RFU

7.2.2.8 RxSelReg

Selects internal receiver settings.

Table 52 RxSelReg

RxSelReg	**Address 0x17**	**Reset value 10000100 (0x84)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	UartSel		RxWait					
Access Rights	r/w		r/w					

Table 53 Description of RxSelReg bits

BIT	SYMBOL	FUNCTION
7-6	UartSel	Selects the input of the contactless UART **Value** **Description** 00 Constant Low 01 Manchester with sub-carrier from MFIN pin 10 Modulation signal from the internal analog part, default 11 NRZ coding without sub-carrier from MFIN pin. Only valid for transfer speeds above 106 kbit/s.
5-0	RxWait	After data transmission, the activation of the receiver is delayed for *RxWait* bit-clocks. During this 'frame guard time' any signal at pin Rx is ignored. This parameter is ignored by the receive command. All other commands (e.g. Transceive, MFAuthent) use this parameter. The counter starts immediately after the external RF field is switched on.

7.2.2.9 RxThresholdReg

Selects thresholds for the bit decoder.

Table 54 RxThresholdReg

RxThresholdReg	**Address 0x18**	**Reset value 10000100 (0x84)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	MinLevel				0	CollLevel		
Access Rights	r/w				RFU	r/w		

Table 55 Description of RxThresholdReg bits

BIT	SYMBOL	FUNCTION
7-4	MinLevel	Defines the minimum signal strength at the decoder input that shall be accepted.If the signal strength is below this level, it is not evaluated.
3	0	RFU.
2-0	CollLevel	Defines the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester-coded signal to generate a bit-collision relatively to the amplitude of the stronger half-bit.

7.2.2.10 DemodReg

Defines demodulator settings.

Table 56 DemodReg

DemodReg **Address 0x19** **Reset value 01001101 (0x4D)**

	7	6	5	4	3	2	1	0
	AddIQ		FixIQ	0	TauRcv		TauSync	
Access Rights	r/w		r/w	RFU	r/w		r/w	

Table 57 Description of DemodReg bits

BIT	SYMBOL	FUNCTION
7-6	AddIQ	Defines the use of I and Q channel during reception Note: *FixIQ* bit has to be set to 0 to enable the following settings. **Value** **Description** 00 Select the stronger channel 01 Select the stronger and freeze the selected during communication 10 RFU 11 RFU
5	FixIQ	If set to 1 and the bits of *AddIQ* are set to X0, the reception is fixed to I channel. If set to 1 and the bits of *AddIQ* are set to X1, the reception is fixed to Q channel.
4	0	RFU
3-2	TauRcv	Changes the time constant of the internal PLL during data reception. Note: If set to 00, the PLL is frozen during data reception.
1-0	TauSync	Changes the time constant of the internal PLL during burst

7.2.2.11 RFU Register

Function is RFU

Table 58 RFUReg

RFUReg	**Address 0x1A**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFU							

Table 59 Description of RFUReg bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFU

7.2.2.12 RFUReg

Function is RFU

Table 60 RFUReg

RFUReg	**Address 0x1B**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFU							

Table 61 Description of RFUReg bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFU.

7.2.2.13 MfTxReg

Controls some MIFARE® communication transmit parameters

Table 62 MfTxReg

MfTxReg	**Address 0x1C**						**Reset value 01100010 (0x62)**	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	011000						TxWait	
Access Rights	RFU						r/w	

Table 63 Description of MfTxReg bits

BIT	SYMBOL	FUNCTION
7-2	011000	RFU
1-0	TxWait	These bits define the additional response time. Per default 7 bits are added to the value of the register bit.

7.2.2.14 MfRxReg

Table 64 MfRxReg

MfRxReg	**Address 0x1D**							**Reset value 00000000 (0x00)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	000			Parity Disable	0000			
Access Rights	RFU			r/w	RFU			

Table 65 Description of MfRxReg bits

BIT	SYMBOL	FUNCTION
7-5	000	RFU
4	ParityDisable	If this bit is set to 1, the generation of the Parity bit for transmission and the Partity-Check for receiving is switched off. The received Parity bit is handled like a data bit.
3-0	0000	RFU

7.2.2.15 RFUReg

Table 66 RFUReg

RFUReg	**Address 0x1E**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFU							

Table 67 Description of RFUReg bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFU.

7.2.2.16 SerialSpeedReg

Selects the speed of the serial UART interface.

Table 68 SerialSpeedReg

SerialSpeedReg	**Address 0x1F**						**Reset value 11101011 (0xEB)**	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BR_T0			BR_T1				
Access Rights	r/w			r/w				

Table 69 Description of SerialSpeedReg bits

BIT	SYMBOL	FUNCTION
7-5	BR_T0	Factor BR_T0 to adjust the transfer speed, for description see chapter 9.3.2.
4 -0	BR_T1	Factor BR_T1 to adjust the transfer speed, for description see chapter 9.3.2.

7.2.3 PAGE 2: CONFIGURATION

7.2.3.1 RFUReg

Function is RFU.

Table 70 RFUReg

RFUReg	**Address 0x20**							**Reset value 00000000 (0x00)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFU							

Table 71 Description of RFU bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFU

7.2.3.2 CRCResultReg

Shows the actual MSB and LSB values of the CRC calculation.
Note: This CRC is split into two 8bit register.

Table 72 CRCResultReg

CRCResultReg	**Address 0x21**	**Reset value 11111111(0xFF)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CRCResultMSB							
Access Rights	r							

Table 73 Description of higher CRCResultReg bits

BIT	SYMBOL	FUNCTION
7-0	CRCResultMSB	This register shows the actual value of the most significant byte of the CRCResult register. It is valid only if bit *CRCReady* in register *Status1Reg* is set to 1.

Table 74 CRCResultReg

CRCResultReg	**Address 0x22**	**Reset value 11111111(0xFF)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CRCResultLSB							
Access Rights	r							

Table 75 Description of lower CRCResultReg bits

BIT	SYMBOL	FUNCTION
7-0	CRCResultLSB	This register shows the actual value of the least significant byte of the CRCResult register. It is valid only if bit *CRCReady* in register *Status1Reg* is set to 1.

7.2.3.3 RFUReg

Table 76 RFUReg

RFU Reg	**Address 0x23**	**Reset value 10001000 (0x88)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	10001000							
Access Rights	RFU							

Table 77 Description of RFUReg bits

BIT	SYMBOL	FUNCTION
7-0	10001000	RFU.

7.2.3.4 ModWidthReg

Controls the setting of the modulation width.

Table 78 ModWidthReg

ModWidthReg	**Address 0x24**	**Reset value 00100110 (0x26)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ModWidth							
Access Rights	r/w							

Table 79 Description of ModWidthReg bits

BIT	SYMBOL	FUNCTION
7-0	ModWidth	These bits define the width of the Miller modulation as multiples of the carrier frequency (*ModWidth +1*/ fc). The maximum value is half the bit period.

7.2.3.5 RFUReg

Function is RFU.

Table 80 RFUReg

RFUReg	**Address 0x25**	**Reset value 10000111(0x87)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	10000111							
Access Rights	RFU							

Table 81 Description of RFUReg bits

BIT	SYMBOL	FUNCTION
7-0	10000111	RFU

7.2.3.6 RFCfgReg

Configures the receiver gain.

Table 82 RFCfgReg

RFCfgReg	**Address 0x26**							**Reset value 01001000 (0x48)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	0	RxGain			1000			
Access Rights	RFU	r/w			RFU			

Table 83 Description of RFCfgReg bits

BIT	SYMBOL	FUNCTION
7	0	RFU
6-4	RxGain	This register defines the receivers signal voltage gain factor: **Value** **Description** 000 18dB 001 23dB 010 18dB 011 23dB 100 33dB 101 38dB 110 43dB 111 48dB
3-0	1000	RFU

7.2.3.7 GsNReg

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when the driver is switched on.

Table 84 GsNReg

GsNReg	**Address 0x27**							**Reset value 10001000 (0x88)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CWGsN				ModGsN			
Access Rights	r/w				r/w			

Table 85 Description of GsNReg bits

BIT	SYMBOL	FUNCTION
7-4	CWGsN	The value of this register defines the conductance of the output N-driver during times of no modulation. This may be used to regulate the output power and subsequently current consumption and operating distance. Note: The conductance value is binary weighted. Note: During soft power down mode the highest bit is forced to 1. Note: This value is only used if the driver TX1 or TX2 are switched on.
3-0	ModGsN	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. Note: During soft power down mode the highest bit is forced to 1. Note: This value is only used if the driver TX1 or Tx2 are switched on.

7.2.3.8 CWGsPReg

Defines the conductance of the P-driver during times of no modulation.

Table 86 CWGsPReg

ModGsCfgReg **Address 0x28** **Reset value 00100000 (0x20)**

Bit	7	6	5	4	3	2	1	0
Symbol	0		CWGsP					
Access Rights	RFU		r/w					

Table 87 Description of CWGsPReg bits

BIT	SYMBOL	FUNCTION
7-6	00	RFU.
5-0	CWGsP	The value of this register defines the conductance of the output P-driver. This may be used to regulate the output power and subsequently current consumption and operating distance. Note: The conductance value is binary weighted. Note: During soft power down mode the highest bit is forced to 1.

7.2.3.9 ModGsPReg

Defines the driver P-output conductance during modulation.

Table 88 ModGsPReg

ModGsPReg	**Address 0x29**	**Reset value 00100000 (0x20)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00		ModGsP					
Access Rights	RFU		r/w					

Table 89 Description of ModGsPReg bits

BIT	SYMBOL	FUNCTION
7-6	00	RFU.
5-0	ModGsP	The value of this register defines the conductance of the output P-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. Note: During soft power down mode the highest bit is forced to 1. Note: If *Force100ASK* bit is set to one, the value of *ModGsP* has no effect.

7.2.3.10 TModeReg, TPrescalerReg

Defines settings for the internal timer.
Note: The prescaler value is split into two 8bit registers.

Table 90 TModeReg

TModeReg	**Address 0x2A**				**Reset value 00000000 (0x00)**			
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TAuto	TGated		TAuto Restart	TPrescaler_Hi			
Access Rights	r/w	r/w		r/w	r/w			

Table 91 Description of TModeReg bits

BIT	SYMBOL	FUNCTION
7	TAuto	Set to 1, the timer starts automatically at the end of the transmission in all communication modes at all speeds. The timer stops immediately after receiving the first data bit if the bit *RxMultiple* in the register *RxModeReg* is not set. If *RxMultiple* is set to 1, the timer never stops. In this case the timer can be stopped by setting the bit *TStopNow* in register *ControlReg* to 1. Set to 0 indicates, that the timer is not influenced by the protocol.
6-5	TGated	The internal timer is running in gated mode. Note: In the gated mode, the bit *TRunning* is 1 when the timer is enabled by the register bits. This bit does not influence the gated signal.
		Value / **Description** 00 / Non gated mode 01 / Gated by MFIN 10 / Gated by AUX1 11 / Gated by A3
4	TAutoRestart	Set to 1, the timer automatically restart its count-down from *TReloadValue*, instead of counting down to zero. Set to 0 the timer decrements to ZERO and the bit *TimerIRq* is set to 1.
3-0	TPrescaler_Hi	Defines higher 4 bits for TPrescaler. The following formula is used to calculate f_{Timer} : f_{Timer} = 6.78 MHz / TPreScaler. For detailed description see chapter 12.

Table 92 TPrescalerReg

TPrescalerReg **Address 0x2B** **Reset value 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	TPrescaler_Lo							
Access Rights	r/w							

Table 93 Description of TPrescalerReg bits

BIT	SYMBOL	FUNCTION
7 to 0	TPrescaler_Lo	Defines the lower 8 bits for TPrescaler. The following formula is used to calculate f_{Timer} : f_{Timer} = 6.78 MHz / TPreScaler. For detailed description see chapter 12.

7.2.3.11 TReloadReg

Describes the 16 bit long timer reload value.
Note: The Reload value is split into two 8bit registers.

Table 94 TReloadReg (Higher bits)

TReloadReg **Address 0x2C** **Reset value 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Hi							
Access Rights	r/w							

Table 95 Description of the higher TReloadReg bits

BIT	SYMBOL	FUNCTION
7-0	TReloadVal_Hi	Defines the higher 8 bits for the TReloadReg. With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

Table 96 TReloadReg (Lower bits)

TReloadReg **Address 0x2D** **Reset value 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Lo							
Access Rights	r/w							

Table 97 Description of lower TReloadReg bits

BIT	SYMBOL	FUNCTION
7-0	TReloadVal_Lo	Defines the lower 8 bits for the TReloadReg. With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

7.2.3.12 TCounterValReg

Contains the current value of the timer.
Note: The Counter value is split into two 8bit registers.

Table 98 TCounterValReg (Higher bits)

TCounterValReg **Address 0x2E** **Reset value xxxxxxxx (0xXX)**

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Hi							
Access Rights	r							

Table 99 Description of the higher TCounterValReg bits

BIT	SYMBOL	FUNCTION
7-0	TCounterVal_Hi	Current value of the timer, higher 8 bits.

Table 100 TCounterValReg (Lower bits)

TCounterValReg **Address 0x2F** **Reset value xxxxxxxx (0xXX)**

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Lo							
Access Rights	r							

Table 101 Description of lower TCounterValReg bits

BIT	SYMBOL	FUNCTION
7-0	TCounterVal_Lo	Current value of the timer, lower 8 bits.

7.2.4 PAGE 3: TEST

7.2.4.1 RFUReg

Function is RFU.

Table 102 RFUReg

RFUReg	**Address 0x30**							**Reset value 00000000 (0x00)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFU							

Table 103 Description of RFUReg bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFU

7.2.4.2 TestSel1Reg

General test signal configuration.

Table 104 TestSel1Reg

TestSel1Reg	**Address 0x31**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000					TstBusBitSel		
Access Rights	RFU					r/w		

Table 105 Description of TestSel1Reg bits

BIT	SYMBOL	FUNCTION
7-3	00000	RFU
2-0	TstBusBitSel	Select the TestBus bit from the testbus to be propagated to MFOUT.

7.2.4.3 TestSel2Reg

General test signal configuration and PRBS control

Table 106 TestSel2Reg

TestSel2Reg **Address 0x32** **Reset value 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	TstBusFlip	PRBS9	PRBS15	TestBusSel				
Access Rights	r/w	r/w	r/w	r/w				

Table 107 Description of TestSel2Reg bits

BIT	SYMBOL	FUNCTION
7	TstBusFlip	If set to 1, the test bus is mapped to the parallel port by the following order: TstBusBit4,TstBusBit3, TstBusBit2,TstBusBit6,TstsBusBit5, TstBusBit0. See chapter 18.
6	PRBS9	Starts and enables the PRBS9 sequence according ITU-TO150. Note: All relevant registers to transmit data have to be configured before entering PRBS9 mode. Note: The data transmission of the defined sequence is started by the send command.
5	PRBS15	Starts and enables the PRBS15 sequence according ITU-TO150. Note: All relevant registers to transmit data have to be configured before entering PRBS15 mode. Note: The data transmission of the defined sequence is started by the send command.
4-0	TestBusSel	Selects the testbus. See chapter 18.

7.2.4.4 TestPinEnReg

Enables the pin output driver on the test bus.

Table 108 TestPinEnReg

TestPinEnReg	**Address 0x33**	**Reset value 10000000 (0x80)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RS232 LinEn	TestPinEn						0
Access Rights	r/w	r/w						RFU

Table 109 Description of TestPinEnReg bits

BIT	SYMBOL	FUNCTION
7	RS232LinEn	Set to 0, the lines MX and DTRQ for the serial UART are disabled.
6-1	TestPinEn	Enables the pin output driver on D1 - D7. Example: Setting bit 1 to 1 enables D1. Setting bit 5 to 1 enables D5 Note: If the SPI interface is used only D1 to D4 can be used. Note: If the serial UART interface is used and RS232LineEn is set to 1 only D1 to D4 can be used.
0	0	RFU

7.2.4.5 TestPinValueReg

Defines the values for the test port when it is used as I/O.

Table 110 TestPinValueReg

TestPinValueReg **Address 0x34** **Reset value 00000000 (0x00)**

Bit	7	6	5	4	3	2	1	0
Symbol	UseIO	TestPinValue						0
Access Rights	r/w	r/w						RFU

Table 111 Description of TestPinValueReg bits

BIT	SYMBOL	FUNCTION
7	UseIO	Set to 1, this bit enables the I/O functionality for the test port if one of the serial interfaces is used. The input / ouput behaviour is defined by TestPinEn in register TestPinEnReg. The value for the output behaviour is defined in the bits TestPinVal.
6-1	TestPinValue	Defines the value of the test port, when it is used as I/O. Each output has to be enabled by the *TestPinEn* bits in register *TestPinEnReg.* Note: Reading the register indicates the actual status of the pins D6 - D1, if UseIO is set to 1. If UseIO is set to 0, the value of the register TestPinValueReg is read back.
0	0	RFU

7.2.4.6 TestBusReg

Shows the status of the internal testbus.

Table 112 TestBusReg

TestBusReg	**Address 0x35**	**Reset value xxxxxxxx (0xXX)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TestBus							
Access Rights	r							

Table 113 Description of TestBusReg bits

BIT	SYMBOL	FUNCTION
7-0	TestBus	Shows the status of the internal test bus. The test bus is selected by the register *TestSel2Reg*. See chapter 18.

7.2.4.7 AutoTestReg

Controls the digital selftest.

Table 114 AutoTestReg

AutoTestReg	**Address 0x36**	**Reset value 01000000 (0x40)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	0	AmpRcv	00		SelfTest			
Access Rights	RFT	r/w	RFT		r/w			

Table 115 Description of AutoTestReg bits

BIT	SYMBOL	FUNCTION
7-4	0	RFT
6	AmpRcv	If set to 1, the internal signal processing in the receiver chain is performed non-linear. This increases the operating distance in communication modes at 106 kbit/s. Note: Due to the non linearity the effect of the bits *MinLevel* and *CollLevel* in the register *RxThreshholdReg* are as well non linear.
5-4	00	RFT
3-0	SelfTest	Enables the digital self test. The selftest can be started by the selftest command in the command register. The selftest is enabled by 1001. Note: For default operation the selftest has to be disabled by 0000.

7.2.4.8 VersionReg

Shows the version.

Table 116 VersionReg

VersionReg	**Address 0x37**	**Reset value xxxxxxxx (0xXX)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Version							
Access Rights	r							

Table 117 Description of VersionReg bits

BIT	SYMBOL	FUNCTION
7-0	Version	indicates current version Note: The current version for MF RC 522 is 0x90.

7.2.4.9 AnalogTestReg

Controls the pins AUX1 and AUX2

Table 118 AnalogTestReg

AnalogTestReg	**Address 0x38**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AnalogSelAux1				AnalogSelAux2			
Access Rights	r/w				r/w			

Table 119 Description of AnalogSelAux bits

BIT	SYMBOL	FUNCTION	
7-4 3-0	AnalogSelAux1 AnalogSelAux2	Controls the AUX pin. Note: All test signals are described in Chapter 18.	
		Value	**Description**
		0000	Tristate
		0001	Output of TestDAC1 (AUX1), output of TESTDAC2 (AUX2) Note: Current output. The use of 1kOHM pulldown resistor on AUX is recommended.
		0010	Testsignal Corr1 Note: Current output. The use of 1kOHM pulldown resistor on AUX is recommended.
		0011	RFU
		0100	Testsignal MinLevel Note: Current output. The use of 1kOHM pulldown resistor on AUX is recommended.
		0101	Testsignal ADC channel I Note: Current output. The use of 1kOHM pulldown resistor on AUX is recommended.
		0110	Testsignal ADC channel Q Note: Current output. The use of 1kOHM pulldown resistor on AUX is recommended.
		0111	RFU
		1000	Testsignal for production test Note: Current output. The use of 1kOHM pulldown resistor on AUX is recommended.
		1001	RFU
		1010	HIGH
		1011	LOW
		1100	TxActive At 106 kbit /s: HIGH during Startbit, Databit, Parity and CRC. At 212 and 424 kbit: High during Data and CRC.
		1101	RxActive At 106 kbit/s: High during Databit, Parity and CRC At 212 and 424 kbit/s: High during Data and CRC.
		1110	Subcarrier detected 106 kbit/s: not applicable 212 and 424 kbit/s: High during last part of Data and CRC
		1111	Test bus bit as defined by the TstBusBitSel in register TestSel1Reg.

7.2.4.10 TestDAC1Reg

Defines the test value for TestDAC1.

Table 120 TestDAC1Reg

TestDAC1Reg	**Address 0x39**							**Reset value 00xxxxxx (0xXX)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	0	0	TestDAC1					
Access Rights	RFT	RFU	r/w					

Table 121 Description of TestDAC1Reg bits

BIT	SYMBOL	FUNCTION
7	0	RFT
6	0	RFU
5-0	TestDAC1	Defines the test value for TestDAC1. The output of the DAC1 can be switched to AUX1 by setting AnalogSelAux1 to 0001 in register AnalogTestReg.

7.2.4.11 TestDAC2Reg

Defines the test value for TestDAC2.

Table 122 TestDAC2Reg

TestDAC2Reg	**Address 0x3A**	**Reset value 00xxxxx (0xXX)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00		TestDAC2					
Access Rights	RFU		r/w					

Table 123 Description of TestDAC2Reg bits

BIT	SYMBOL	FUNCTION
7-6	00	RFU.
5-0	TestDAC2	Defines the test value for TestDAC2. The output of the DAC2 can be switched to AUX2 by setting AnalogSelAux2 to 0001 in register AnalogTestReg.

7.2.4.12 TestADCReg

Shows the actual value of ADC I and Q channel.

Table 124 TestADCReg

TestADCReg	**Address 0x3B**							**Reset value xxxxxxxx (0xXX)**
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ADC_I				ADC_Q			
Access Rights	r				r			

Table 125 Description of TestADCReg bits

BIT	SYMBOL	FUNCTION
7-4	ADC_I	Shows the actual value of ADC I channel.
3-0	ADC_Q	Shows the actual value of ADC Q channel.

7.2.4.13 RFTReg

Table 126 RFTReg

RFTReg	**Address 0x3C**	**Reset value 11111111 (0xFF)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	11111111							
Access Rights	RFT							

Table 127 Description of RFTReg bits

BIT	SYMBOL	FUNCTION
7-0	111111111	RFT

Table 128 RFTReg

RFTReg	**Address 0x3D**	**Reset value 00000000 (0x00)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFT							

Table 129 Description of RFTReg bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFT

Table 130 RFTReg

RFTReg	**Address 0x3E**	**Reset value 00000011 (0x03)**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000011							
Access Rights	RFT							

Table 131 Description of RFTReg bits

BIT	SYMBOL	FUNCTION
7-0	00000011	RFT

Table 132 RFTReg

RFTReg	**Address 0x3F**						**Reset value 00000000 (0x00)**	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	00000000							
Access Rights	RFT							

Table 133 Description of RFTReg bits

BIT	SYMBOL	FUNCTION
7-0	00000000	RFT

8 MFRC522 FUNCTIONALITY

MFRC522 transmission module supports the Reader/Writer mode for ISO 14443A / MIFARE® with different transfer speeds and modulation schemes.

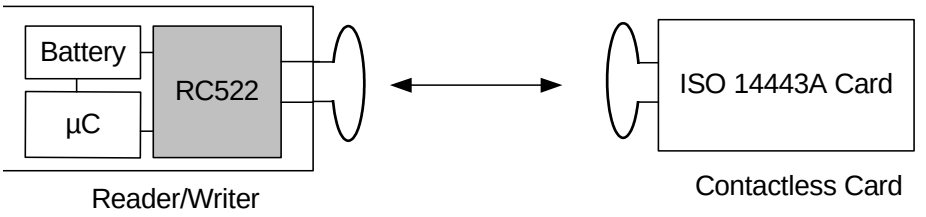


Fig.3 MFRC522 Reader/Writer mode

The ISO 14443A / MIFARE® reader/writer mode is the general reader/writer to card communication scheme according to the ISO 14443A / MIFARE® specification.The following diagram describes the communication on a physical level, the communication overview in Table 134 describes the physical parameters.

- Communication diagram for ISO 14443A / MIFARE® reader/ writer functionality

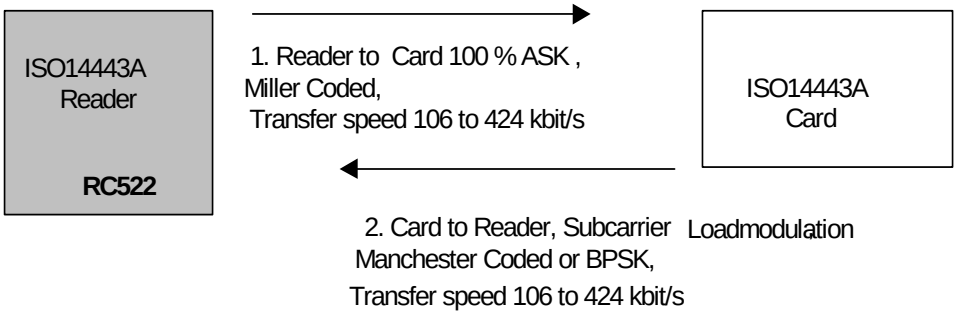


Fig.4 ISO 14443A / MIFARE® reader/writer mode communication diagram.

- Communication overview for ISO 14443A / MIFARE® reader/writer functionality

Table 134 Communication overview for ISO 14443A / MIFARE® Reader /Writer

COMMUNICATION DIRECTION		ISO 14443A / MIFARE®	MIFARE® HIGHER TRANSFER SPEEDS	
	transfer speed	**106kbit/s**	**212 kbit/s**	**424kbit/s**
Reader → Card (send data from the MFRC522 to a card)	Modulation on reader side	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
	Bitlength	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
Card → Reader (receive data from a card)	Modulation on card side	Subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	Subcarrier frequency	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16
	bit coding	Manchester coding	BPSK	BPSK

The contactless UART of MFRC522 and a dedicated external host are required to handle the complete MIFARE® / ISO 14443A / MIFARE® protocol.

- Data Coding and framing according to ISO 14443A / MIFARE®

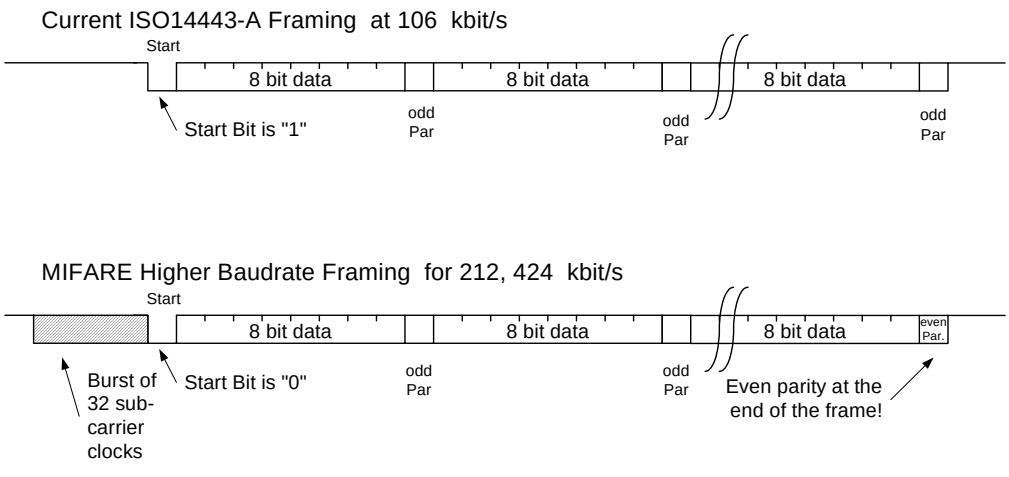


Fig.5 Data Coding and framing according to ISO 14443A.

The internal CRC coprocessor calculates the CRC value according to the definitions given in the ISO 14443A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off by bit *ParityDisable* in register *0x1D ManualRCVReg*.

9 DIGITAL INTERFACES

9.1 Automatic µ-Controller Interface Type Detection

The MFRC522 supports direct interfacing of various host as the SPI, I2C and serial UART interface type. The MFRC522 resets its interface and checks the current host interface type automatically having performed a Power-On or Hard Reset. The MFRC522 identifies the host interface by the means of the logic levels on the control pins after the Reset Phase. This is done by a combination of fixed pin connections.The following table shows the different configurations:

Table 135 Connection Scheme for detecting the different Interface Types

MFRC522	SERIAL INTERFACE TYPES		
Pin	**UART**	**SPI**	**I2C**
SDA	RX	NSS	SDA
I2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	–	–	ADR_2
D3	–	–	ADR_3
D2	–	–	ADR_4
D1	–	–	ADR_5

Note: Overview on the pin behaviour

Pin behaviour	Input	Output	In/Out

9.2 SPI Compatible interface

A serial peripheral interface (SPI compatible) is supported to enable high speed communication to the host. The SPI Interface can handle data speed of up to 10 Mbit/s. In the communication with a host MFRC522 acts as a slave receiving data from the external host for register settings and to send and receive data relevant for the communication on the RF interface.

9.2.1 GENERAL

An interface compatible to an SPI interface enables a high-speed serial communication between the MFRC522 and a µ–Controller for the communication. The implemented SPI compatible interface is according to a standard SPI interface.

For timing specification refer to chapter 18.13.

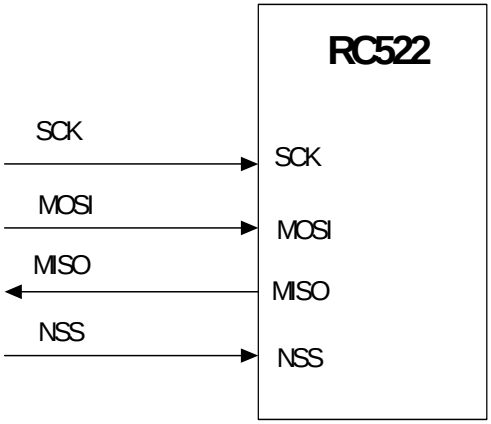


Fig.6 Connection to host with SPI

The MFRC522 acts as a slave during SPI communication. The SPI clock SCK has to be generated by the master. Data communication from the master to the slave uses the Line MOSI. Line MISO is used to send data back from the MFRC522 to the master.
On both lines (MOSI, MISO) each data byte is sent by MSB first. Data on MOSI line should be stable on rising edge of the clock line and can be changed on the falling edge. The same is valid for the MISO line. Data is provided by the MFRC522 on the falling edge and is stable during the rising edge.

9.2.2 READ DATA:

To read out data using the SPI compatible interface the following byte order has to be used. It is possible to read out up to n-data bytes.

The first sent byte defines both, the mode itself and the address byte.

Table 136 Byte Order for MOSI and MISO

	byte 0	**byte 1**	**byte 2**	**……..**	**byte n**	**byte n+1**
MOSI	adr 0	adr 1	adr 2	……..	adr n	00
MISO	X	data 0	data 1	……..	data n-1	data n

Note: The most significant bit (MSB) has to be send first.

9.2.3 WRITE DATA:

To write data to the MFRC522 using the SPI interface the following byte order has to be used. It is possible to write up to n-data bytes by only sending one's the address byte.

The first send byte defines both, the mode itself and the address byte.

Note: The most significant bit (MSB) has to be send first.

Table 137 Byte Order for MOSI and MISO

	byte 0	**byte 1**	**byte 2**	**……..**	**byte n**	**byte n+1**
MOSI	adr	data 0	data 1	……..	data n-1	data n
MISO	X	X	X	……..	X	X

9.2.4 ADDRESS BYTE:

The address byte has to fulfil the following format. The MSB bit of the first byte defines the used mode. To read data from the MFRC522 the MSB bit has to be set to 1. To write data to the MFRC522 the MSB bit has to be set to 0. The bits 6-1 define the address and the LSB shall be set to 0.

Table 138 Address byte format

Address (MOSI)	**bit 7, MSB**	**bit 6 - bit 1**	**bit 0**
byte 0	1 (read) 0 (write)	address	RFU (0)

9.3 UART Interface

9.3.1 CONNECTION TO A HOST

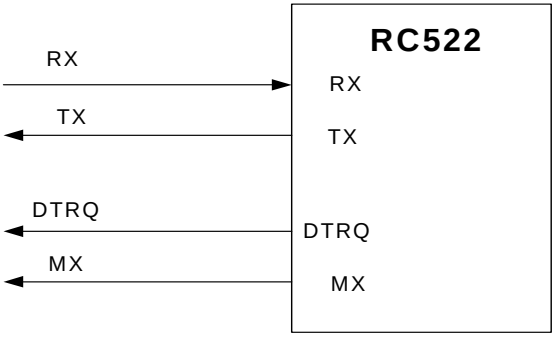


Fig.7 Connection to host with UART.

Note: DTRQ and MX can be disabled by clearing the bit RS232LineEn in register TestPinEnReg.

9.3.2 SELECTION OF THE TRANSFER SPEEDS

The internal UART interface is compatible to an RS232 serial interface.

Table 140 describes examples for different transfer speeds and relevant register settings.

The resulting transfer speed error is less than 1.5% for all described transfer speeds.
The default transfer speed is 9.6 kbit/s.
To change the transfer speed, the host controller has to write the value for a new transfer speed to the register SerialSpeedReg. The bits BR_T0 and BR_T1 in *SerialSpeedReg* define the factors to set the transfer speed.

Table 139 describes the settings of BR_T0 and BR_T1.

Table 139 Settings of BR_T0 and BR_T1

BR_T0	0	1	2	3	4	5	6	7
factor BR_T0	1	1	2	4	8	16	32	64
range BR_T1	1-32	33-64	33-64	33-64	33-64	33-64	33-64	33-64

Table 140 Selectable transfer speeds

TRANSFER SPEED [BIT/S]	***SerialSpeedReg***		**TRANSFER SPEED ACCURACY**
	dez	**hex**	
7.2k	250	FA	-0,25%
9.6k	235	EB	0,32%
14.4k	218	DA	-0,25%
19.2k	203	CB	0,32%
38.4k	171	AB	0,32%
57.6k	154	9A	-0,25%
115.2k	122	7A	-0,25%
128k	116	74	-0,06%
230.4k	90	5A	-0,25%
460.8k	58	3A	-0,25%
921.6k	28	1C	1,45%
1228.8k	21	15	0,32%

The selectable transfer speeds as shown in table 140 are calculated according to the following formulas:

if *BR_T0*=0: transfer speed = 27,12 MHz /(BR_T1+1)

if *BR_T0*>0 transfer speed = 27,12 MHz / (BR_T1 +33) / 2^(BR_T0 - 1)

Note: transfer speeds above 1228.8k are not supported.

9.3.3 FRAMING:

Table 141 UART Framing

	LENGTH	VALUE
Start bit	1 bit	0
Data bits	8 bits	Data
Stop bit	1 bit	1

For data and address bytes the LSB bit has to be sent first.

Note: No parity bit is used during transmission.

Read data:

To read out data using the UART interface the flow described below has to be used. The first send byte defines both the mode itself and the address.

Table 142 Byte Order to Read Data

	byte 0	byte 1
RX	adr	
TX		data 0

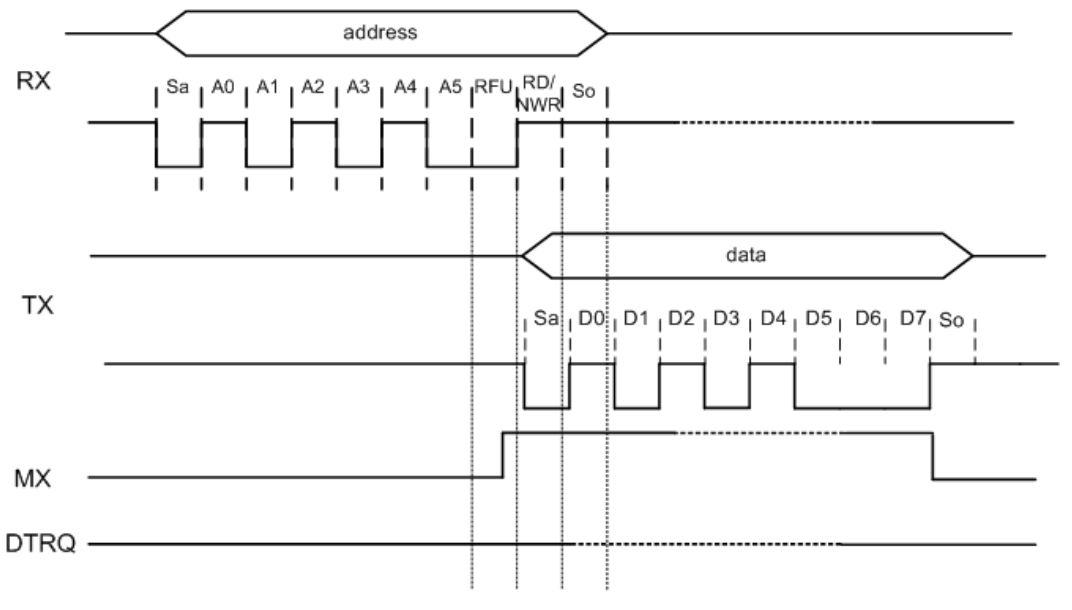


Fig.8 Schematic Diagram to Read Data

Write data:

To write data to the MFRC522 using the UART interface the following structure has to be used.

The first send byte defines both, the mode itself and the address.

Table 143 Byte order to Write Data

	byte 0	byte 1
RX	adr 0	data 0
TX		adr 0

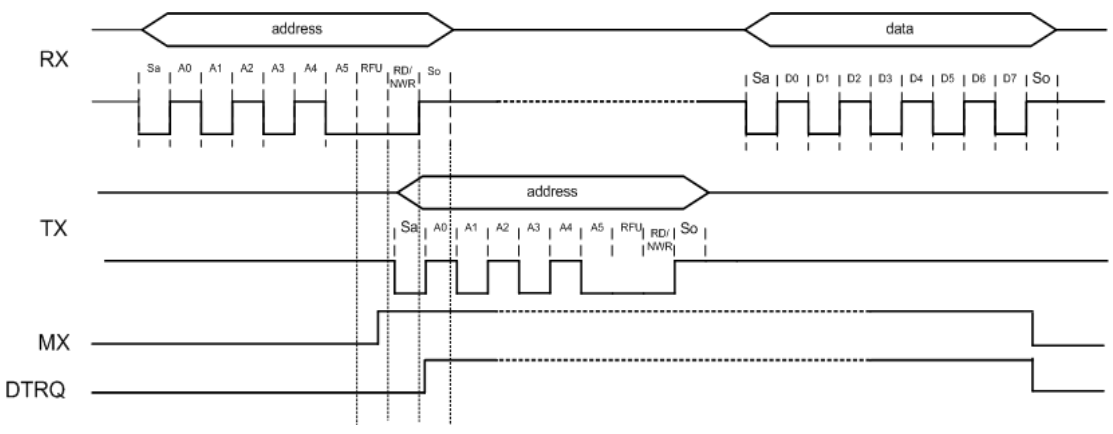


Fig.10 Schematic Diagram to Write Data.

Note: The data byte can be send directly after the address byte on the RX line.

Address byte:

The address byte has to fulfil the following format. The MSB of the first byte defines the used mode. To read data from the MFRC522 the MSB has to be set to 1. To write data to the MFRC522 the MSB has to be set to 0. The bit 6 is RFU and the bits 5-1 define the address.

Table 144 Address byte

Address	bit 7, MSB	bit 6	bit 5- bit 0
byte 0	1 (read), 0 (write)	RFU	address

9.4 I²C Bus Interface

An Inter IC (I^2C) bus interface is supported to enable a low cost, low pin count serial bus interface to the host.
The implemented I^2C interface is implemented according the Philips Semiconductors I^2C interface specification, rev. 2.1,January 2000. The implemented interface can only act in slave mode. Therefore no clock generation and access arbitration is implemented in the MFRC522.

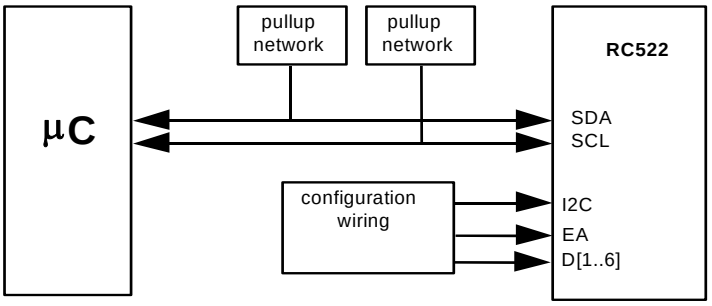


Fig.11 I²C interface.

9.4.1 GENERAL

The implemented interface is conforming to the I²C-bus specification version 2.1, January 2000. The MFRC522 can act as a slave receiver or slave transmitter in standard mode, fast mode and high speed mode.

SDA is a bi-directional line, connected to a positive supply voltage via a current-source or a pull-up resistor. Both lines, SDA and SCL are set to HIGH level if no data is transmitted. The MFRC522 has a tri-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kbit/s in standard-mode up to 400 kbit/s in the fast-mode or up to 3.4Mbit/s in the high speed mode.
If the I²C interface is selected, a spike suppression according to the I²C interface specification on SCL and SDA is activated.

For timing requirements refer to chapter 18.14.

9.4.2 DATA VALIDITY

The data on the SDA line shall be stable during the HIGH period of the clock. The HIGH or LOW state of the data line shall only change when the clock signal on the SCL line is LOW.

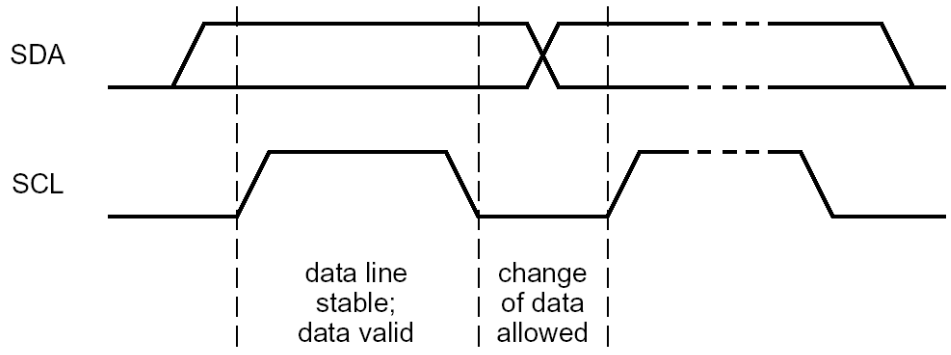


Fig.12 bit transfer on the I^2C-bus.

9.4.3 START AND STOP CONDITIONS

To handle the data transfer on the I^2C-bus, unique START (S) and STOP (P) conditions are defined.

A START condition is defined with a HIGH to LOW transition on the SDA line while SCL is HIGH.

A STOP condition is defined with a LOW to HIGH transition on the SDA line while SCL is HIGH.

The master always generates the START and STOP conditions. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical. Therefore, the S symbol will be used as a generic term to represent both the START and repeated START (Sr) conditions.

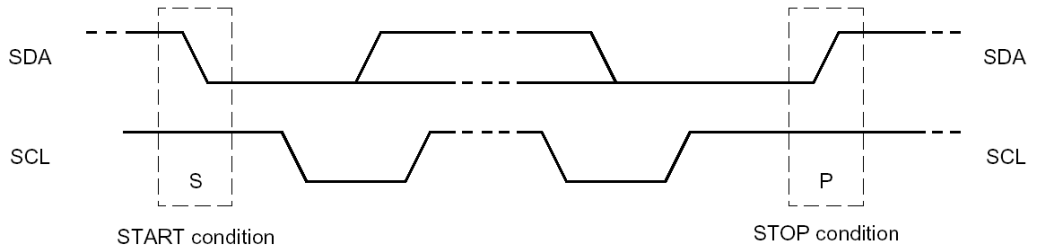


Fig.13 START and STOP conditions.

9.4.4 BYTE FORMAT

Each byte has to be followed by an acknowledge bit. Data is transferred with the MSB first, see figure 16. The number of transmitted bytes during one data transfer is unrestricted but shall fulfil the read/ write cycle format.

9.4.5 ACKNOWLEDGE

An acknowledge at the end of one data byte is mandatory. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver shall pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer, or a repeated START (Sr) condition to start a new transfer.

A master-receiver shall indicate the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter shall release the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

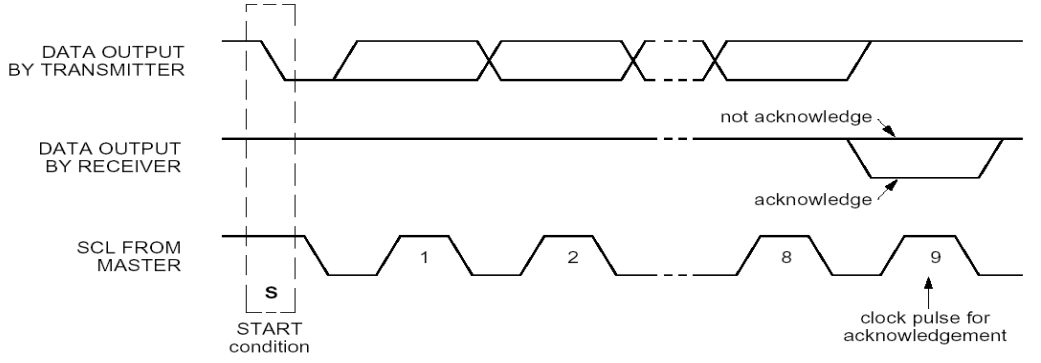


Fig.14 Acknowledge on the I^2C- bus.

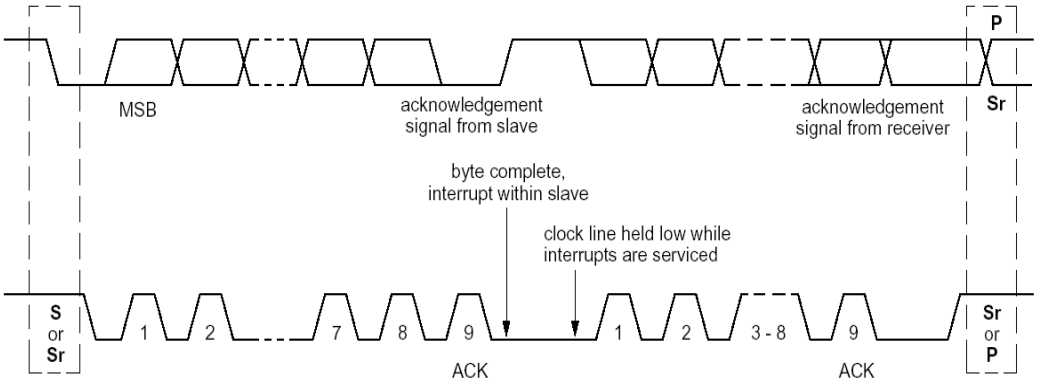


Fig.15 Data transfer on the I²C-bus.

9.4.6 7-BIT ADDRESSING

During the I²C-bus addressing procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

As an exception several address numbers are reserved. During device configuration, the designer has to ensure, that no collision with these reserved addresses is possible. Check the corresponding I²C specification for a complete list of reserved addresses.

The I²C address specification is dependent on the definition of the EA Pin. Immediately after releasing the reset pin or after power on reset, the device defines the I2C address according EA pin.

If EA Pin is set to LOW than for all MFRC522 devices the upper 4 bits of the device bus address are reserved by Philips and set to 0101(bin). The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the Slave Address can freely configured by the customer in order to prevent collisions with other I²C devices.

If EA Pin is set to HIGH than ADR_0 - ADR_5 can be completely specified at the external pins according to Table 135. ADR_6 is always set to 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I²C address pins could be used for test signal output.

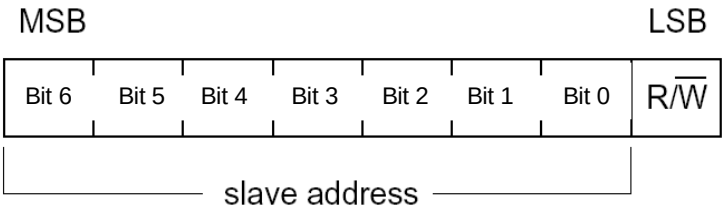


Fig.16 First byte following the START procedure.

9.4.7 Register Write Access

To write data from the host controller via I^2C to a specific register of the MFRC522 the following frame format shall be used.

The first byte of a frame indicates the device address according to the I^2C rules. The second byte indicates the register address followed by up to n-data bytes. In one frame all n-data bytes are written to the same register address. This enables for example a fast FIFO access.

The read/write bit shall be set to 0.

9.4.8 Register Read Access

To read out data from a specific register address of the MFRC522 by the host controller the following procedure shall be used:

First a write access to the specific register address has to be performed as indicated in the following frame.

The first byte of a frame indicates the device address according to the I^2C rules. The second byte indicates the register address. No data bytes are added.

The read/write bit shall be 0.

Having performed this write access, the read access can start. The host has to send the device address of the MFRC522. As an answer to this, the MFRC522 responds with the content of this register. In one frame up to n-data bytes could be read from the same register address. This enables for example a fast FIFO access or register polling.

The read/write bit shall be set to 1.

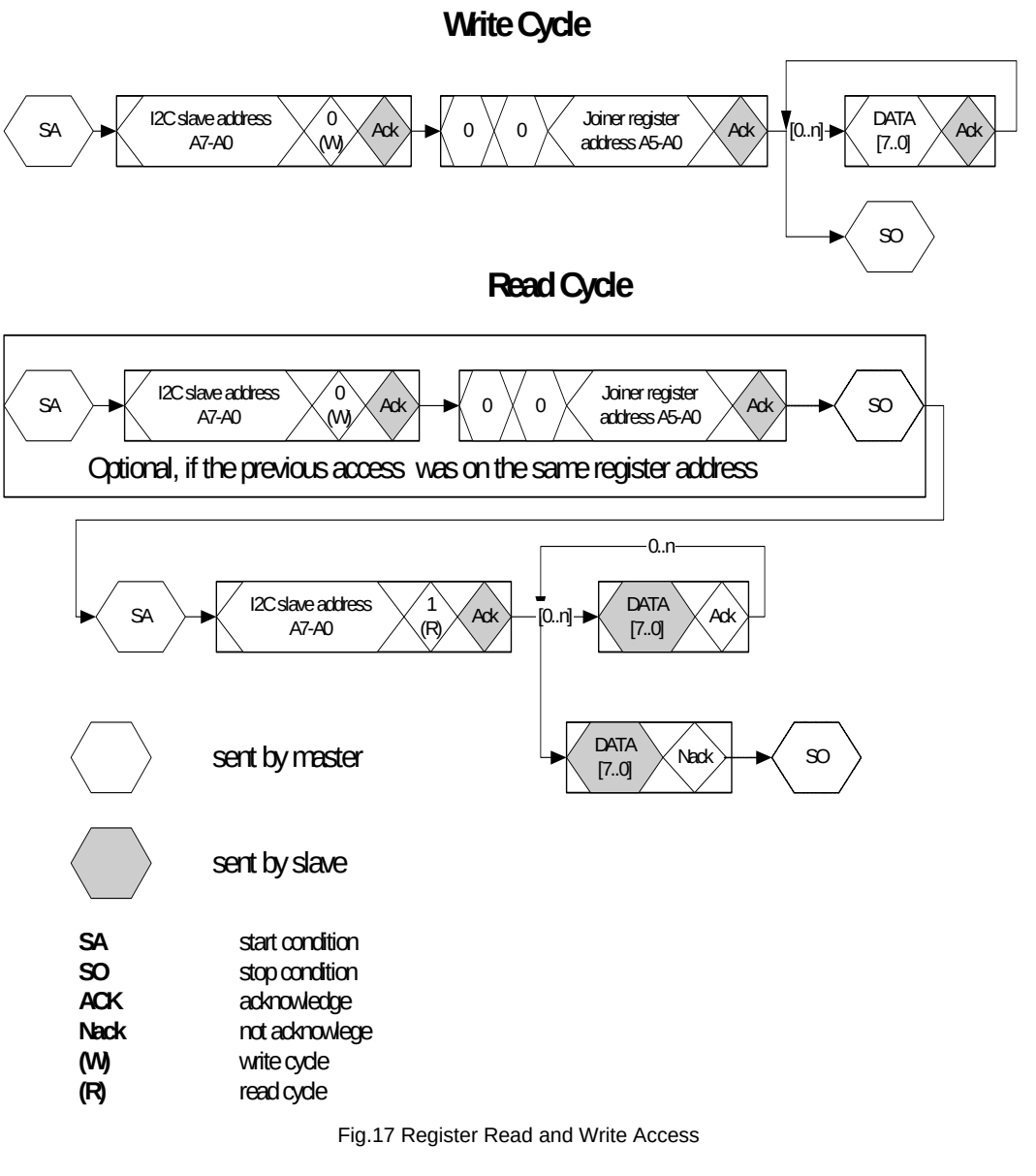


Fig.17 Register Read and Write Access

9.4.9 Hs-Mode

In High-speed mode (Hs-mode) the device can transfer information at data rates of up to 3.4 Mbit/s, it remains fully downward compatible with Fast- or Standard-mode (F/S-mode) for bi-directional communication in a mixed-speed bus system.

9.4.10 HIgh Speed Transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to the regular I2C-bus behaviour.

- The inputs of the device in Hs-mode incorporates spike suppression and a Schmitt-trigger at the SDA and SCL inputs with different timing constants compared to F/S mode.
- ·The output buffers of the device in Hs-mode incorporates slope control of the falling edges of the SDA and SCL signals with different falling time compared to F/S mode.

9.4.11 Serial Data transfer Format in HS mode

Serial data transfer format in Hs-mode meets the Standard-mode I2C-bus specification. Hs-mode can only commence after the following conditions (all of which are in F/S-mode):

1. START condition (S)

2. 8-bit master code (00001XXX)

3. Not-acknowledge bit (A)

The active master then sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address, and receives an acknowledge bit (A) from the selected MFRC522.

Data transfer continues in Hs-mode after the next repeated START (Sr), and only switches back to F/S-mode after a STOP condition (P). To reduce the overhead of the master code, it's possible that a master links a number of Hs-mode transfers, separated by repeated START conditions (Sr).

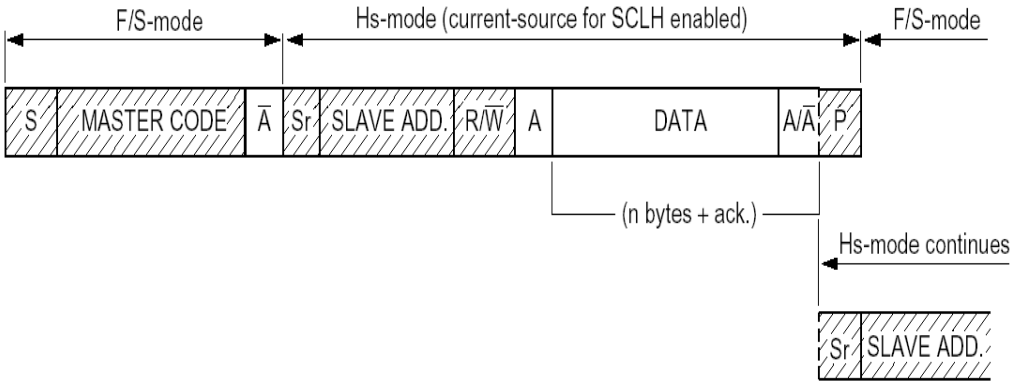


Fig.18 I2C HS mode protocol switch

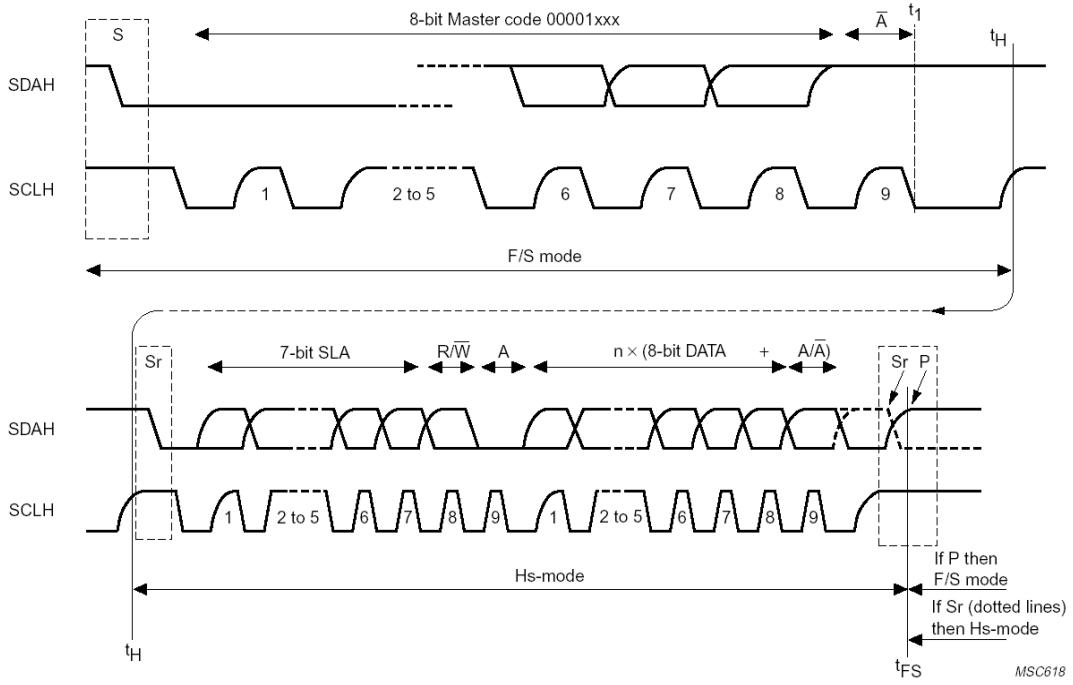


Fig.19 I2C HS Mode protocol frame

9.4.12 Switching from F/S to HS mode and Vice Versa

After reset and initialization, the MFRC522 is in Fast-mode (which is in effect F/S-mode as Fast-mode is downward compatible to Standard-mode). The connected MFRC522 recognises the "S 00001XXX A" sequence and switches its internal circuitry from the Fast-mode setting to the Hs-mode setting.

Following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in Hs-mode.

2. Adapt the slope control of the SDA output stages.

For system configurations, where no other I2C devices are involved in the communication, have an additional possibility to switch to HS-mode. By setting the bit *I2CForceHS* in register *Status2Reg* to 1, the HS mode is entered. Setting this bit to 1 changes the HS-mode permanent meaning that sending the master code is no longer necessary. This is not according the specification and should only be used when no other devices are connected on the bus. Spikes on the I2C lines shall be avoided because of the reduced spike suppression.

9.4.13 MFRC522 AT LOWER SPEED MODES

MFRC522 is fully downwards compatible, and can be connected to an F/S-mode I2C-bus system. As no master code will be transmitted in such a configuration, the device stays in F/S-mode and communicates at F/S-mode speeds.

10 ANALOG INTERFACE AND CONTACTLESS UART

10.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 424 kbit/s. An external circuit can to be connected to the communication interface pins MFIN / MFOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication schemes in co-operation with the host. The protocol handling itself generates bit- and byte-oriented framing and handles error detection like Parity and CRC according to the different contactless communication schemes.

Note: The size and the tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

10.2 TX Driver

The signal delivered on pin TX1 and pin TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly, using a few passive components for matching and filtering, see chapter 19. The signal on TX1 and TX2 can be configured by the register *TxControlReg,* see chapter 7.2.2.5.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured by the registers *CWGsPReg* and *ModGsPReg*. The impedance of the n-driver can be configured by the register *GsNReg*. Furthermore, the modulation index depends on the antenna design and tuning.

The register *TxModeReg* and *TxAutoSelReg* control the data rate and framing during the transmission and the setting of the antenna driver to support the different requirements at the different modes and transfer speeds.

Table 145 Settings for TX1

TX1RFEN	FORCE 100ASK	INVTX1 RFON	INVTX1 RFOFF	ENVE LOPE	TX1	GSPMOS	GSNMOS	REMARKS
0	x	x	x	x	x	x	x	not specified if RF is switched off
1	0	0	x	0	RF	pMod	nMod	100% ASK: TX1 pulled to 0, independent of InvTx1RFOff
				1	RF	pCW	nCW	
	0	1	x	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	x	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

Table 146 Settings for TX2

TX2 RFEN	FORCE 100 ASK	TX2CW	INVTX2R FON	INVTX2R FOFF	ENVE LOPE	TX2	GSPMOS	GSNMOS	REMARKS
0	x	x	x	x	x	x	x	x	not specified if RF is switched off
1	0	0	0	x	0	RF	pMod	nMod	
					1	RF	pCW	nCW	
			1	x	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	x	X	RF	pCW	nCW	Gs always CW for TX2CW
			1	x	X	RF_n	pCW	nCW	
	1	0	0	x	0	0	pMod	nMod	100%ASK:Tx2 pulled to 0 (independent of InvTx2RFOn/INVTX2RFOff)
					1	RF	pCW	nCW	
			1	x	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	x	X	RF	pCW	nCW	
			1	x	X	RF_n	pCW	nCW	

Note:

The following abbreviations are used
RF: 13. 56 MHz clock derived from 27.12 MHz Quartz divided by 2
RF_n: inverted 13.56 MHz clock
gspmos: Conductance, configuration of the PMOS array
gsnmos: Conductance, configuration of the NMOS array
pCW: PMOS conductance value for continuous wave defined by *CWGsP* register
pMod: PMOS conductance value for modulation defined by *ModGsP* register
nCW: NMOS conductance value for continuous wave defined by *CWGsN* register
nMod: NMOS conductance value for modulation defined by *ModGsN* register

Note: If only 1 driver is switched on, the values for *ModGsN, ModGsP* and *CWGsN, CWGsP* are used for both drivers.

10.3 Serial Data Switch

Two main blocks are implemented in the MFRC522. A digital circuitry, comprising state machines, coder and decoder logic and an analog circuitry with the modulator and antenna drivers, receiver and amplification circuitry. For example, the interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins MFIN and MFOUT.

This topology supports, that the analog part of the MFRC522 may be connected to the digital part of another device.

The serial signal switch is controlled by the register *TxSelReg* and *RxSelReg*.

The following figure shows the serial data switch for TX1 and TX2.

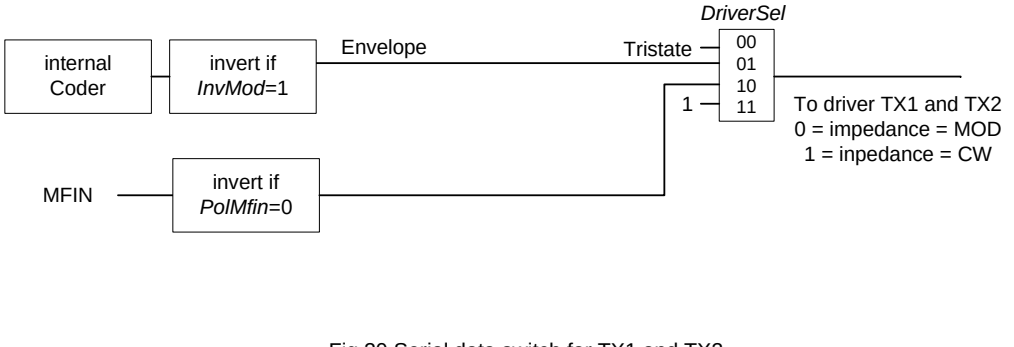


Fig.20 Serial data switch for TX1 and TX2.

10.4 MFIN / MFOUT interface support

The MFRC522 is basically divided into digital circuitry and analog circuitry. The digital circuitry contains state machines, coder and decoder logic and so on and the analog circuitry contains the modulator and antenna drivers, receiver and amplification circuitry. The interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins MFIN and MFOUT (see Figure 21). The configuration is done by bits *SigOutSel*, *DriverSel* and *UARTSel* of registers *TxSelReg* and *RxSelReg*.

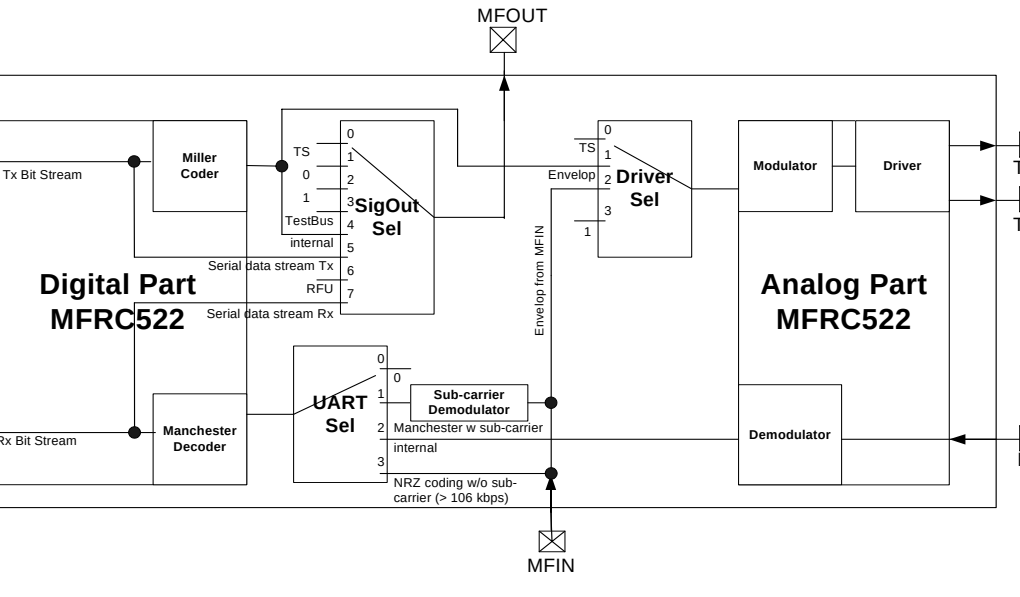


Fig.21 Overview MFIN / MFOUT Signal Routing

This topology supports, that some parts of the analog part of the MFRC522 may be connected to the digital part of another device.

The switch *SigOutSel* in register *TxSelReg* can be used to measure MIFARE® and ISO14443 related signals. This is especially important during the design In phase or for test purposes to check the transmitted and received data.

However, the most important use of MFIN / MFOUT pins is the active antenna concept. An external active antenna circuit can be connected to the digital circuit of the MFRC522. *SigOutSel* has to be configured in that way that the signal of the internal Miller Coder is send to MFOUT pin (*SigOutSel* = 4). *UARTSel* has to be configured to receive Manchester signal with sub-carrier from MFIN pin (*UARTSel* = 1).

It is possible, to connect a 'passive antenna' to pins TX1, TX2 and RX (via the appropriate filter and matching circuit) and at the same time an Active Antenna to the pins MFOUT and MFIN. In this configuration, two RF-parts may be driven (one after another) by one host processor.

Note: The MFRC522 has an extra supply pin (SVDD and PVSS as Ground line) for the MFIN and MFOUT pads.

10.5 CRC-Coprocessor

Only the CRC Preset Value of the CRC co-processor can be configured. The CRC preset value could be either 0x0000, 0x6363, 0xA671 or 0xFFFF depending on the bits CRCPreset in register *ModeReg*.

Table 147 CRC-Coprocessor Parameters

PARAMETER	VALUE
CRC Register Length	16 Bit CRC
CRC Algorithm	Algorithm according ISO 14443A and CCITT
CRC Preset Value	0000, 6363,A671 or FFFF depending on the CRCPresetReg register settings

The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$.

The register *CRCResultReg* indicates the result of the CRC calculation. This register is split into two 8-bit registers indicating the higher and lower byte.

The bit MSBFirst in the register ModeReg indicates that data will be loaded with MSB first.

11 FIFO BUFFER

11.1 Overview

An 64*8 bit FIFO buffer is implemented in the MFRC522. It buffers the input and output data stream between the host and the internal state machine of the MFRC522. Thus, it is possible to handle data streams with lengths of up to 64 bytes without taking timing constraints into account.

11.2 Accessing the FIFO Buffer

The FIFO-buffer input and output data bus is connected to the register *FIFODataReg*. Writing to this register stores one byte in the FIFO-buffer and increments the internal FIFO-buffer write-pointer. Reading from this register shows the FIFO-buffer contents stored at the FIFO-buffer read-pointer and decrements the FIFO-buffer read-pointer. The distance between the write- and read-pointer can be obtained by reading the register *FIFOLevelReg*.

When the µ-Controller starts a command, the MFRC522 may, while the command is in progress, access the FIFO-buffer according to that command. Physically only one FIFO-buffer is implemented, which can be used in input- and output direction. Therefore the µ-Controller has to take care, not to access the FIFO-buffer in an unintended way.

11.3 Controlling the FIFO-Buffer

Besides writing to and reading from the FIFO-buffer, the FIFO-buffer pointers might be reset by setting the bit *FlushBuffer* in the register *FIFOLevelReg* to 1. Consequently, the *FIFOLevel* bits are set to 0, the bit *BufferOvfl* in the register *ErrorReg* is cleared, the actually stored bytes are not accessible any more and the FIFO-buffer can be filled with another 64 bytes again.

11.4 Status Information about the FIFO-Buffer

The host may obtain the following data about the FIFO-buffers status:

- Number of bytes already stored in the FIFO-buffer: *FIFOLevel* in register *FIFOLevelReg*
- Warning, that the FIFO-buffer is almost full: *HiAlert* in register *Status1Reg*
- Warning, that the FIFO-buffer is almost empty: *LoAlert* in register *Status1Reg*
- Indication, that bytes were written to the FIFO-buffer although it was already full: *BufferOvfl* in register *ErrorReg*. *BufferOvfl* can be cleared only by setting bit *FlushBuffer* in the register *FIFOLevelReg*.

The MFRC522 can generate an interrupt signal

- If *LoAlertIEn* in register *CommIEnReg* is set to 1 it will activate Pin IRQ when *LoAlert* in the register *Status1Reg* changes to 1.
- If *HiAlertIEN* in register *CommIEnReg* is set to 1 it will activate Pin IRQ when *HiAlert* in the register *Status1Reg* changes to 1.

The bit *HiAlert* is set to 1 if maximum *WaterLevel* bytes (as set in register *WaterLevelReg)* or less can be stored in the FIFO-buffer. It is generated according to the following equation:

$$HiAlert = (64 - FIFOLength) \leq WaterLevel$$

The bit *LoAlert* is set to 1 if *WaterLevel* bytes (as set in register *WaterLevelReg*) or less are actually stored in the FIFO-buffer. It is generated according to the following equation:

$$LoAlert = FIFOLength \leq WaterLevel$$

12 TIMER UNIT

A timer unit is implemented in the MFRC522. The external host may use this timer to manage timing relevant tasks. The timer unit may be used in one of the following configurations:

- Timeout-counter
- Watch-dog counter
- Stop watch
- Programmable one-shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events which will be explained in the following, but the timer itself does not influence any internal event (e.g. A timeout during data reception does not influence the reception process automatically). Furthermore, several timer related bits are set and these bits can be used to generate an interrupt.

The timer has a input clock of 6,78 MHz (derived from the 27.12 MHz quartz). The timer consists of 2 stages: 1 prescaler and 1 counter.

The prescaler is a 12 bit counter. The reload value for TPrescaler can be defined between 0 and 4095 in register *TModeReg* and *TPrescalerReg*.

The reload value for the counter is defined by 16 bits in a range of 0 to 65535 in the register *TReloadReg.*

The current value of the timer is indicated by the register TCounterValReg.

If the counter reaches 0 an interrupt will be generated automatically indicated by setting the *TimerIRq* bit in the register *CommonIRqReg*. If enabled, this event can be indicated on the IRQ line. The *TimerIRq* bit can be set and reset by the host. Depending on the configuration the timer will stop at 0 or restart with the value from register *TReloadReg*.

The status of the timer is indicated by bit *TRunning* in register *Status1Reg*.

The timer can be manually started by *TStartNow* in register *ControlReg* or manually stopped by *TStopNow* in register *ControlReg*.

Furthermore the timer can be activated automatically by setting the bit *TAuto* in the register *TModeReg* to fulfil dedicated protocol requirements automatically.

The time delay of a timer stage is the reload value +1.

Maximum time:TPrescaler = 4095, TReloadVal = 65535

=> 4096*65536 / 6,78 MHz = 39,59s

Example:

To indicate 100us it is required to count 678 clock cycles. This means the value for TPrescaler has to be set to TPrescaler =677.The timer has now an input clock of 100us. The timer can count up to 65535 time slots of each 100us.

13 INTERRUPT REQUEST SYSTEM

The MFRC522 indicates certain events by setting bit *IRq* in the register *Status1Reg* and additionally if activated by pin IRQ. The signal on pin IRQ may be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

The following table shows the available interrupt bits, the corresponding source and the condition for its activation.
The interrupt bit *TimerIRq* in register *CommIRqReg* indicates an interrupt set by the timer unit. The setting is done when the timer decrements from 1 down to 0.
The TxIRq bit in register *CommIRqReg* indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit sets the interrupt bit automatically.
The CRC coprocessor sets the bit *CRCIRq* in the register *DivIRqReg* after having processed all data from the FIFO buffer. This is indicated by the bit CRCReady = 1.

The bit *RxIRq* in register *CommIRqReg* indicates an interrupt when the end of the received data is detected.

The bit *IdleIRq* in register *CommIRqReg* is set if a command finishes and the content of the command register changes to idle.

The bit *HiAlertIRq* in register *CommIRqReg* is set to 1 if the *HiAlert* bit is set to 1, that means the FIFO buffer has reached the level indicated by the bit *WaterLevel*.

The bit *LoAlertIRq* in register *CommIRqReg* is set to 1 if the *LoAlert* bit is set to 1, that means the FIFO buffer has reached the level indicated by the bit *WaterLevel.*

The bit ErrIRq in register *CommIRqReg* indicates an error detected by the contactless UART during sending or receiving. This is indicated by any bit set to 1 in register *ErrorReg*.

Table 148 Interrupt Sources

INTERRUPT FLAG	INTERRUPT SOURCE	IS SET AUTOMATICALLY, WHEN
TimerIRq	Timer Unit	the timer counts from 1 to 0
TxIRq	Transmitter	a transmitted data stream ends
CRCIRq	CRC-Coprocessor	all data from the FIFO buffer has been processed
RxIRq	Receiver	a received data stream ends
IdleIRq	Command Register	a command execution finishes
HiAlertIRq	FIFO-buffer	the FIFO-buffer is getting full
HiAlertIRq	FIFO-buffer	the FIFO-buffer is getting empty
ErrIRq	contactless UART	an error is detected

14 OSCILLATOR CIRCUITRY

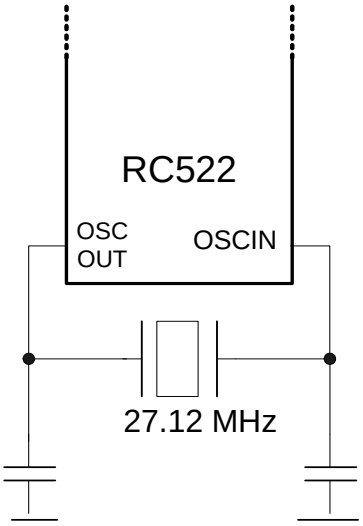


Fig.22 Quartz Connection.

The clock applied to the MFRC522 acts as time basis for the coder and decoder of the synchronous system. Therefore stability of the clock frequency is an important factor for proper performance. To obtain highest performance, clock jitter has to be as small as possible. This is best achieved by using the internal oscillator buffer with the recommended circuitry. If an external clock source is used, the clock signal has to be applied to pin OSCIN. In this case special care for clock duty cycle and clock jitter is needed and the clock quality has to be verified.

15 POWER REDUCTION MODES

15.1 Hard Power Down

A Hard Power Down is enabled with LOW level on pin NRSTPD. This turns off all internal current sinks as well as the oscillator. All digital input buffers are separated from the input pads and clamped internally (except pin NRSTPD itself). The output pins are frozen at a certain value.

15.2 Soft Power Down

The Soft Power Down-mode is entered immediately after setting the bit *PowerDown* in the register *CommandReg* to 1. All internal current sinks are switched off (including the oscillator buffer).

In opposition to the Hard Power Down-mode, the digital input-buffers are not separated by the input pads and keep their functionality. The digital output pins do not change their state.

During Soft Power Down, all registers values, the FIFO's content and the configuration itself will keep its content during.

After setting bit *PowerDown* in the register *CommandReg* to 0 it takes 1024 clocks until the Soft Power Down mode is left as indicated by the PowerDown bit itself. Setting it to 0 does not immediately clear it. It is cleared automatically by the MFRC522 when the Soft Power Down-Mode is left.

Note: If the internal oscillator is used, you have to take into account that it is supplied by AVDD and it will take a certain time t_{osc} until the oscillator is stable and the clock cycles can be detected by the internal logic.

Note: If the serial UART interface is used the soft power down mode is reset by sending the value 55 (hex) to the MFRC522. For further access to the registers the oscillator must be stable. The first read or write access must be to address 0.

For the serial UART it is recommended to send the value 55(hex) first and perform read accesses to address 0 till the MFRC522 answers to the last read command with the register content of address 0. This indicates that the MFRC522 is active for further operation.

15.3 Transmitter Power Down

The Transmitter Power Down mode switches off the internal antenna drivers to turn off the RF field by setting either *TX1RfEn* or *TX2RfEn* in the register *TXControlReg* to 0.

16 RESET AND OSCILLATOR START UP TIME

16.1 Reset Timing Requirements

The reset signal is filtered by a hysteresis circuit and a spike filter (rejects signals shorter than 10ns) before it enters the digital circuit. In order to perform a reset, the signal has to be low for at least 100ns.

16.2 Oscillator Start up time

Having set the MFRC522 in a power down mode or supplying the IC with XVDD the following figure describes the startup timing for the oscillator.

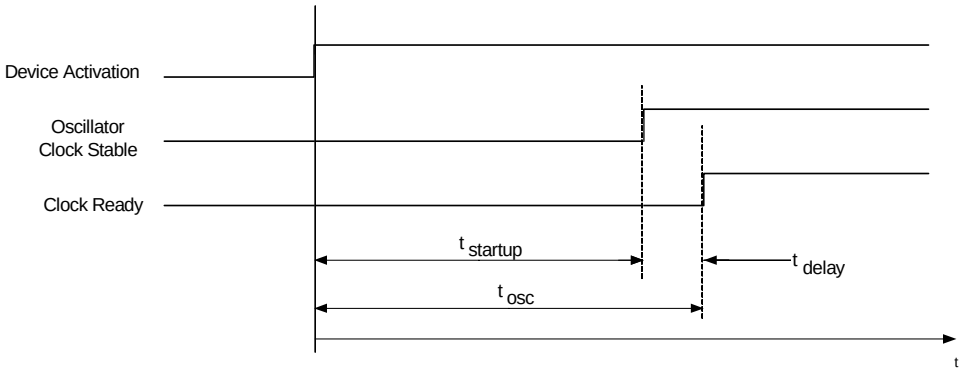


Fig.23 Oscilator Start Up time.

The time $t_{startup}$ defines the start-up time of crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal itself.

The t_{delay} defines the internal delay time of the MFRC522 when the clock signal is stable before the MFRC522 can be addressed. The delay time is calculated as follows: $t_{delay}[\mu s] = 1024/27.12 = 37.76\ \mu s$.

The time t_{osc} is defined as the sum of the time t_{delay} and $t_{startup}$.

17 MFRC522 COMMAND SET

17.1 General Description

The MFRC522 behaviour is determined by a state machine capable to perform a certain set of commands. By writing the according command to the Command-Register the command is executed.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

17.2 General Behaviour

- Each command, that needs a data stream (or data byte stream) as input will immediately process the data it finds in the FIFO buffer. An exception to this rule is the Transceive command. Using this command the transmission is started with the StartSend bit in the *BitFramingReg* register.
- Each command that needs a certain number of arguments will start processing only when it has received the correct number of arguments via the FIFO buffer.
- The FIFO buffer is not cleared automatically at command start. Therefore, it is also possible to write the command arguments and/or the data bytes into the FIFO buffer and start the command afterwards.
- Each command may be interrupted by the host by writing a new command code into the Command-Register e.g.: the Idle-Command.

17.3 MFRC522 Commands Overview

Table 149 Command overview

COMMAND	COMMAND CODE	ACTION
Idle	0000	No action; cancels current command execution.
Mem	0001	Stores 25 byte into the internal buffer
Generate RandomID	0010	Generates a 10 byte random ID number
CalcCRC	0011	Activates the CRC-Coprocessor or perform selftest.
Transmit	0100	Transmits data from the FIFO buffer.
NoCmd Change	0111	No command change. This command can be used to modify different bits in the command register without touching the command. E.G. Power down.
Receive	1000	Activates the receiver circuitry.
Transceive	1100	Transmits data from FIFO buffer to the antenna and activates automatically the receiver after transmission.
RFU	1101	Reserved for further use
MFAuthent	1110	performs the MIFARE® standard authentication as a reader
Soft Reset	1111	resets the MFRC522

17.4 MFRC522 Command Description

17.4.1 IDLE COMMAND

The MFRC522is in idle mode. This command is also used to terminate the actual command.

17.4.2 Mem Command

Transfers 25 byte from the FIFO to the internal buffer.

To read out the 25 byte from the internal buffer, the command Mem with an empty FIFO buffer has to be started. In this case the 25 bytes are transferred from the internal buffer to the FIFO.

During a hard power down (reset pin) the 25 byte in the internal buffer remains unchanged but will be lost when supply power is removed from MFRC522.

This command terminates automatically when finished and the active command is idle.

17.4.3 Generate RandomID Command

This command generates a 10 byte random number stored in the internal buffer and overwrites the 10 bytes of the internal 25 byte buffer. This command terminates automatically when finished and the MFRC522 returns to idle.

17.4.4 CalcCRC Command

The content of the FIFO is transferred to the CRC-coprocessor and a CRC calculation is started. The result of this calculation is stored in the *CRCResultReg* register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped, when the FIFO gets empty during the data stream. The next byte written to the FIFO is added to the calculation.

The pre-set value of the CRC is controlled by the *CRCPreset* bits of the *ModeReg* register *and the value is loaded* to the CRC-coprocessor when the command is started.

This command has to be terminated by writing any command to the Command-register e.g. the command Idle.
If the *SelfTes*t bits in the *AutoTestReg* register are set correctly, the MFRC522 is in self test mode and starting the CalcCRC command performs a digital selftest. The result of the selftest is written to the FIFO.

17.4.5 Transmit Command

The content of the FIFO is transmitted immediately after starting the command. Before transmitting the FIFO content all relevant registers have to be set to transmit data.

This command terminates automatically when the FIFO gets empty it can be terminated by another command written to the command register.

17.4.6 NoCmdChange Command

This command does not influence any ongoing command in the CommandReg register. It can be used to manipulate any bit except the command bits in the CommandReg register, e.g. the bits RcvOff or PowerDown.

17.4.7 Receive Command

The MFRC522 activates the receiver path and waits for any data stream to be received. The correct settings have to be chosen before starting this command.

This command terminates automatically when the received data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected framing and speed.

Note: If the bit *RxMultiple* in the *RxModeReg* register is set to 1 the Receive command does not terminate automatically. It has to be terminated by activating any other command in the *CommandReg* register.

17.4.8 TRANSCEIVE COMMAND

This circular command repeats transmitting data from the FIFO and receiving data from the RF field continuously. The first action is transmitting and after a transmission the command is changed to receive a data stream.

Each transmission process has to be started with setting the bit *StartSend* in the register *BitFramingReg* to 1. This command has to be cleared by software by writing any command to the Command-register e.g. the command idle.

Note: If the bit *RxMultiple* in register *RxModeReg* is set to 1, this command will never leave the receiving state, because the receiving will not be cancelled automatically.

17.4.9 MFAUTHENT COMMAND

This command handles the Mifare® authentication to enable a secure communication to any Mifare® classic card. The following data shall be written to the FIFO before the command can be activated:

- Authentication command code (0x60, 0x61)
- Block address.
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes shall be written to the FIFO.

Note: When the MFAuthent command is active, any FIFO access is blocked. Anyhow if there is an access to the FIFO, the bit *WrErr* in the *ErrorReg* register is set.

This command terminates automatically when the Mifare® card is authenticated and the bit *MFCrypto1On* in the *Status2Reg* register is set to 1.

This command does not terminate automatically when the card does not answer, therefore the timer should be initialized to automatic mode. In this case, beside the bit *IdleIrq* the bit *TimerIrq* can be used as termination criteria. During authentication processing the bit *RxIrq* and bit *TxIrq* are blocked. The *Crypto1On* bit is only valid after termination of the authent command (either after processing the protocol or after writing IDLE to the command register).

In case there is an error during Authentication the bit *ProtocolErr* in the *ErrorReg* register is set to 1 and the bit *Crypto1On* in register *Status2Reg* is set to 0.

17.4.10 SoftReset Command

This command performs a reset to the device. The configuration data of the internal buffer remains unchanged.

All registers are set to the reset values. This command terminates automatically when finished.

Note: The *SerialSpeedReg* register is reset and therefore the serial data rate is set to 9.6kbps.

18 TEST SIGNALS

18.1 Sefttest

The MFRC522 has the capability to perform a selftest. To start the digital selftest the following procedure has to be performed:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 0x00 and perform the Config Command.
3. Enable the Selftest by writing the value 0x09 to register *AutoTestReg*.
4. Write 0x00 to the FIFO.
5. Start the Selftest with the CalcCRC Command.
6. The Selftest will be performed.
7. When the Selftest is finished, the FIFO is contains the following bytes:

Correct answer for register *VersionReg* equal to 0x90:

```
0x00, 0x87, 0x98, 0x0f, 0x49, 0xff, 0x07, 0x19
0xbf, 0x22, 0x30, 0x49, 0x59, 0x63, 0xad, 0xca
0x7f, 0xe3, 0x4e, 0x03, 0x5c, 0x4e, 0x49, 0x50
0x47, 0x9a, 0x37, 0x61, 0xe7, 0xe2, 0xc6, 0x2e
0x75, 0x5a, 0xed, 0x04, 0x3d, 0x02, 0x4b, 0x78
0x32, 0xff, 0x58, 0x3b, 0x7c, 0xe9, 0x00, 0x94
0xb4, 0x4a, 0x59, 0x5b, 0xfd, 0xc9, 0x29, 0xdf
0x35, 0x96, 0x98, 0x9e, 0x4f, 0x30, 0x32, 0x8d
```

18.2 Test bus

The test bus is implemented for production test purpose. The following configuration can be used to improve the design of a system using the MFRC522. The test bus allows to route internal signals to the digital interface. The test bus signals are selected by accessing *TestBusSel* in register *TestSel2Reg*.

Table 150 TestSel2Reg set to 0x07

PINS	D6	D5	D4	D3	D2	D1	D0
Test signal	sdata	scoll	svalid	sover	RCV_reset	RFU	Envelop

Table 151 Test signals description

TEST SIGNAL	DESCRIPTION
sdata	shows the actual received data stream.
scoll	shows if in the actual bit a collision has been detected (106 kbit/s only)
svalid	shows if sdata and scoll are valid
sover	shows that the receiver has detected a stop condition.
RCV_reset	shows if the receiver is reset
Envelope	shows if the receiver is reset

Table 152 TestSel2Reg set to 0x0D

PINS	D6	D5	D4	D3	D2	D1	D0
Test signal	clkstable	clk27/8	RFU	RFU	clk27	RFU	RFU

Table 153 Test signals description

TEST SIGNAL	DESCRIPTION
clkstable	shows if the oscillator delivers a stable signal.
clk27/8	shows the output signal of the oscillator divided by 8
clk27	shows the output signal of the oscillator

18.3 Test signals at pin AUX

With the MFRC522, the user may select internal signals to measure them at pin AUX. These measurements can be helpful during the design-in phase to optimise the design or for test purpose.

Table 154 shows an overview of the signal that can be switched to pin AUX1 or AUX2 by setting *SelAux1 or SelAux2* in the register *AnalogTestReg.*

Please also refer to register *AnalogSelAux*.

Note: The DAC has a current output, it is recommended to use a 1kOhm pull down resistance at pins *AUX1/AUX2*.

Table 154 Test signals description

SELAUX	DESCRIPTION FOR AUX1 / AUX2
0000	Tristate
0001	DAC: register TestDAC 1/2
0010	DAC: test signal corr1
0011	RFU
0100	DAC: test signal MinLevel
0101	DAC: ADC_I
0110	DAC: ADC_Q
0111	RFU
1000	RFT
1001	RFU
1010	High
1011	Low
1100	TxActive
1101	RxActive
1110	Subcarrier detected
1111	TstBusBit

18.3.1 Example: Output TestDAC 1 on AUX1 and TestDAC 2 on AUX2

Register *AnalogTestReg* is set to 0x11. The output of *AUX1* corresponds to the *TestDAC 1* and the output of *AUX2* to the *TestDAC 2*. The value of *TestDAC 1* and *TestDAC 2* is controlled by register *TestDAC1Reg* and *TestDAC2Reg*.

Figure 24 shows *TestDAC1Reg* programmed with a slope from 0x00...0x3F. *TestDAC2Reg* has been programmed with a rectangular signal with values of 0x00 and 0x3F.

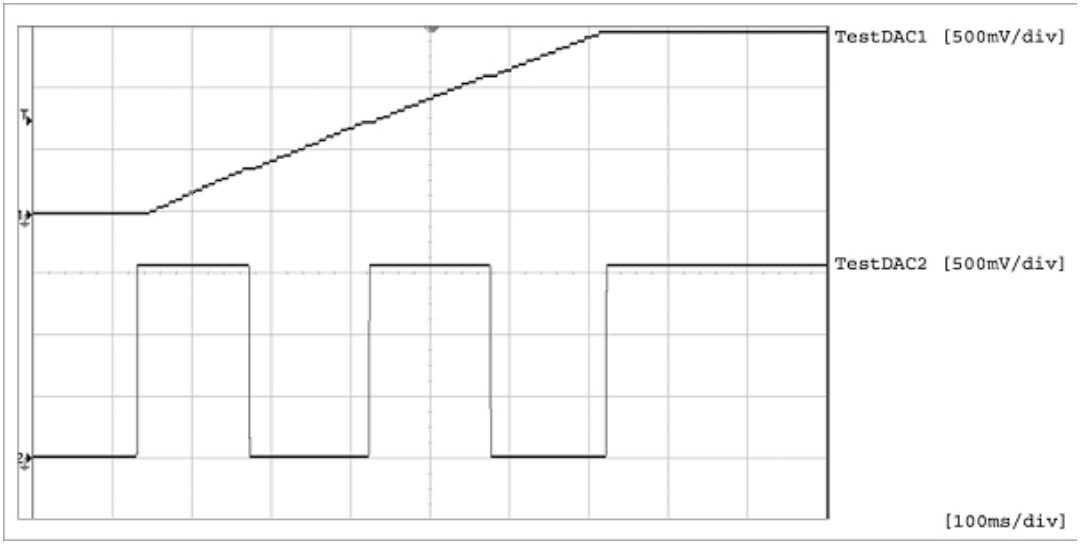


Fig.24 Output *TestDAC 1* on *AUX1* and *TestDAC 2* on *AUX2*

18.3.2 Example: Output Testsignal Corr1 on AUX1 and MinLevel on AUX2

The following figure 25 shows the test signal *Corr 1* and the test signal *MinLevel*. The *AnalogTestReg* is set to 0x24. The output of *AUX1* corresponds to the *Corr1* signal and *AUX2* to the *MinLevel*.

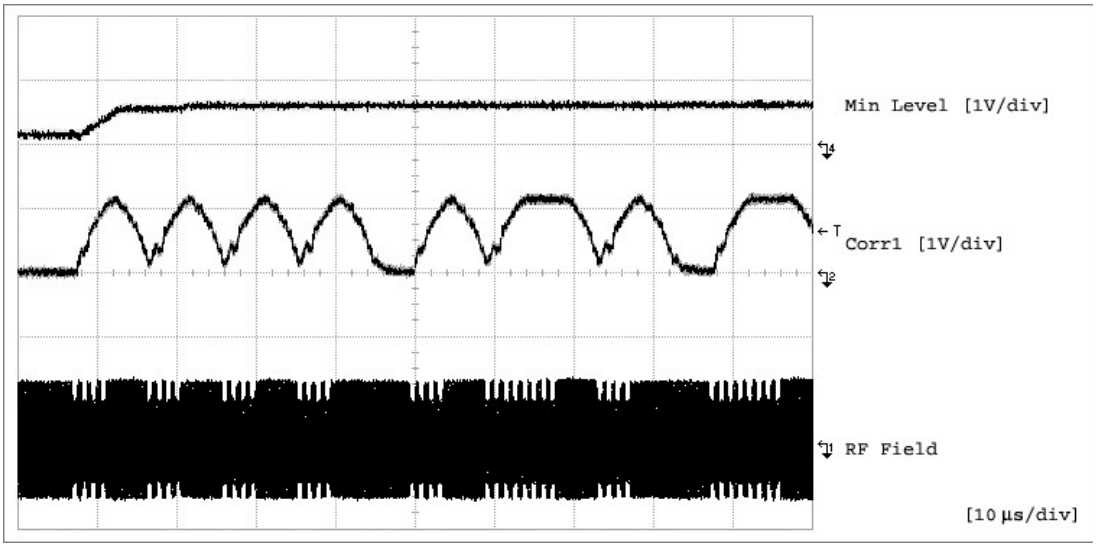


Fig.25 Output Testsignal *Corr1* on *AUX1* and *MinLevel* on *AUX2*.

18.3.3 Example: Output ADC channel I on AUX 1 and ADC channel Q on AUX 2

Figure 26 shows the *ADC_I* and *ADC_Q* channel behaviour. The *AnalogTestReg* is set to 0x56.

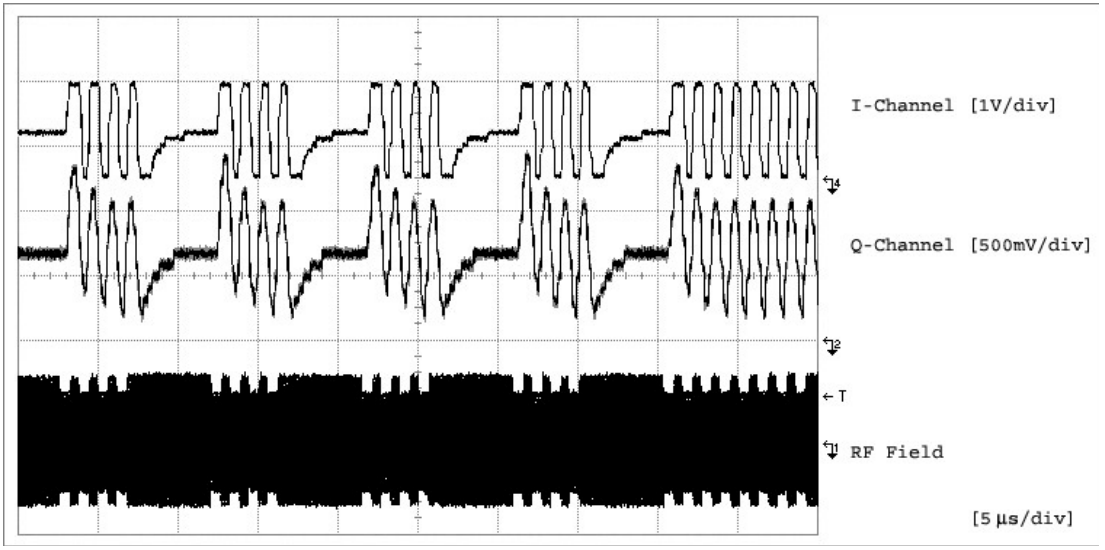


Fig.26 Output ADC channel I on AUX 1 and ADC channel Q on AUX 2.

18.3.4 Example: Output RxActive on AUX 1 and TxActive on AUX 2

The following figure 27 shows the *RXActive* and *TXActive* signal in accordance to the RF communication. The *AnalogTestReg* was set to 0xCD.

Note:
At 106 kbit/s, *RxActive* is HIGH during databits, parity and CRC reception. Startbits are not included.
At 106 kbit/s, *TxActive* is HIGH during startbits, databits, parity and CRC transmission.
At 212 and 424 kbit/s, *RxActive* is HIGH during datbits and CRC reseption. Startbits are not included.
At 212 and 424 kbit/s, *TxActive* is HIGH during databits and CRC transmission.

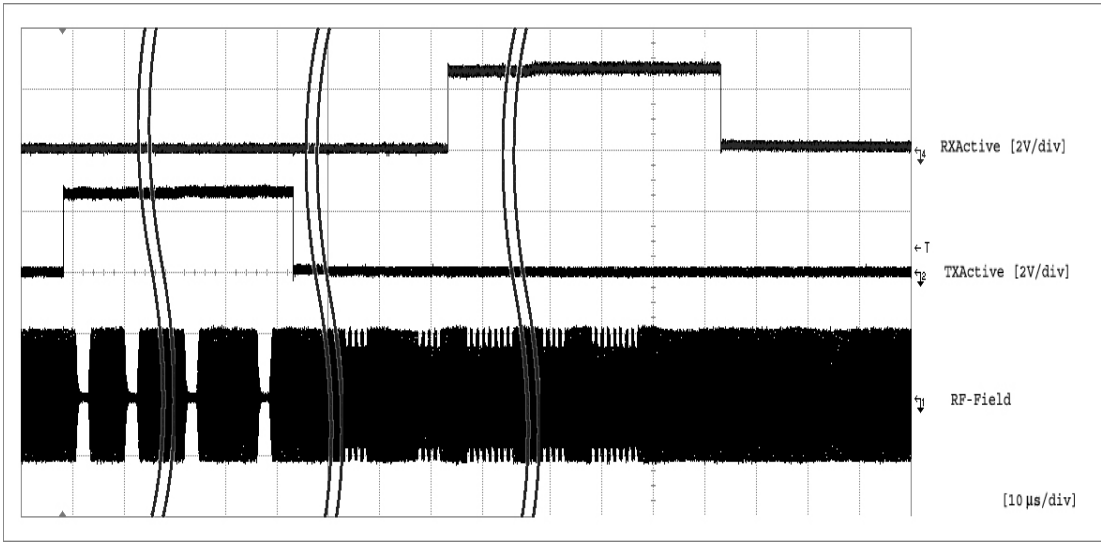


Fig.27 Output RxActive on AUX 1 and TxActive on AUX 2.

18.3.5 Example: Output Rx data stream on AUX 1 and AUX 2

The following figure 28 shows the actual received data stream. *TestSel2Reg* is set to 0x07 to enable certain digital test data on D0-D6 (see chapter 18.2).
The register *TestSel1Reg* is set to 0x06 (D6 = sdata) and *AnalogTestReg* is set to 0xFF to output the received data stream to pin *AUX1* and *AUX2*.

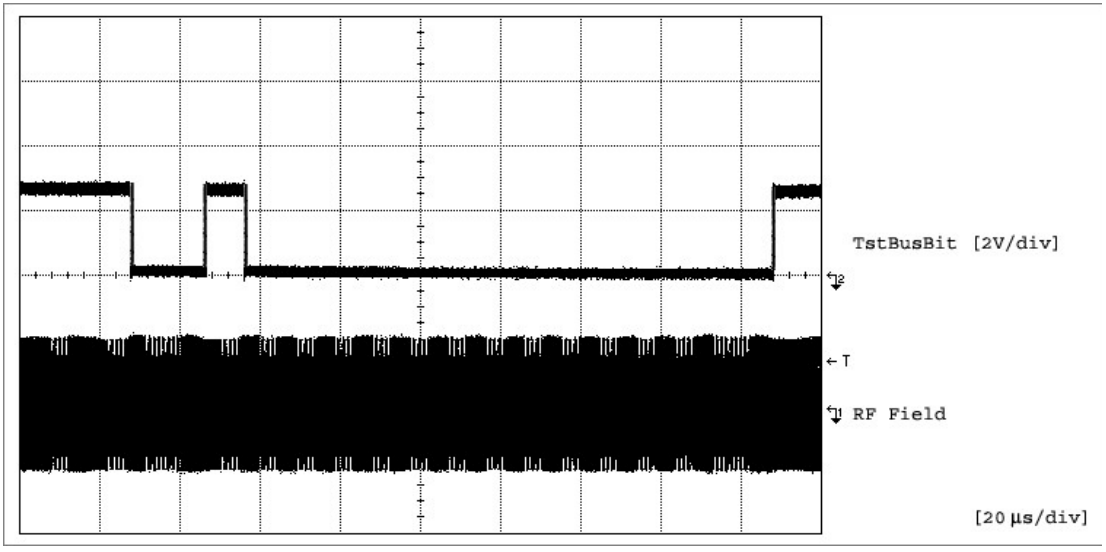


Fig.28 Output Rx data stream on AUX 1 and AUX 2.

18.4 PRBS (Pseudo-Random Binary Sequence)

Enables the PRBS9 or PRBS15 sequence according to ITU-TO150. To start the transmission of the defined data stream the command send has to be activated. The preamble / Sync byte /start bit / parity bit are generated automatically depending on the selected mode.

Note: All relevant register to transmit data have to be configured before entering PRBS mode according ITU-TO150.

19 TYPICAL APPLICATION

The figure below shows a typical circuit diagram, using a directly matched antenna connection to the MFRC522:

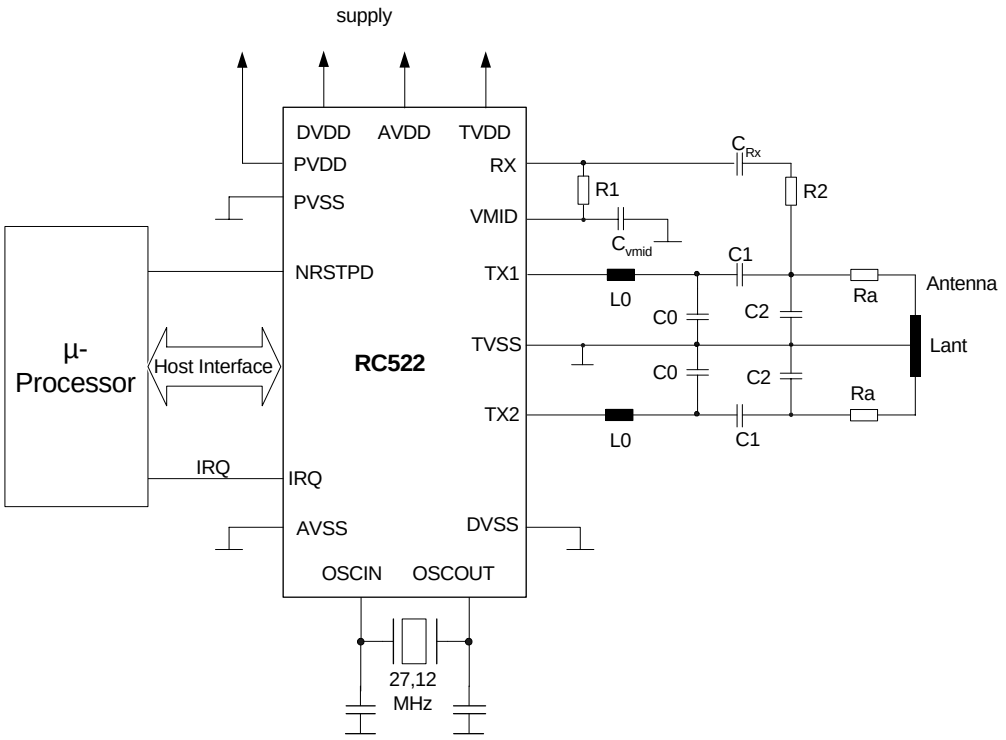


Fig.29 Typical Circuit Diagram

The antenna tuning and RF part matching is described in the application note "*MFRC522 Reader IC Family Directly Matched Antenna Design".*

20 ELECTRICAL CHARACTERISTICS

20.1 Absolute Maximum Ratings

Table 155 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
AVDD, DVDD, PVDD, TVDD SVDD	Supply Voltages	-0.5	4.0	V

20.2 Limiting Values

Table 156 Limiting values

SYMBOL	PARAMETER	MIN	MAX	UNIT
P_{tot}	Total power dissipation		200	mW
T_j	Junction temperature		100	°C

20.3 ESD Characteristics

Table 157 ESD Characteristics

SYMBOL	PARAMETER	CONDITION	SPECIFICATION	VALUE
ESDH	ESD Susceptibility (Human Body model)	1500 Ohm, 100pF	JESD22-A114-B	2000V
ESDM	ESD Susceptibility (Machine model)	0.75 µH, 200 pF	JESD22-A114-A	200V

20.4 Thermal Characteristics

Table 158 Thermal Characteristics

SYMBOL	PARAMETER	CONDITIONS	PACKAGE	VALUE	UNIT
R_{thj-a}	Thermal resistance from junction to ambient	In still air with exposed pad soldered on a 4 layer Jedec PCB	HVQFN32	40	k/W

20.5 Operating Condition Range

Table 159 Operating Condition Range

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	HVQFN32	-30		+85	°C
AVDD, DVDD, TVDD	Supply Voltages	AVSS=DVSS=PVSS=TVSS=0V, PVDD<=AVDD=DVDD=TVDD	2.5	3.3	3.6	V
PVDD	Supply Voltage	AVSS=DVSS=PVSS=TVSS=0V, PVDD<=AVDD=DVDD=TVDD	1.6	1.8	3.6	V

Note

1. Supply voltages below 3 V reduces the performance (e.g. the achievable operating distance).
2. AVDD, DVDD and TVDD shall always be on the same voltage level.
3. PVDD shall always be on the same or lower voltage level than DVDD.

20.6 Input Pin Characteristics

20.6.1 Input Pin characteristics for pins EA, I2C and NRESET

Table 160 Input Pin characteristics for pins EA, I2C and NRESET

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 PVDD	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 PVDD	V

20.6.2 Input Pin characteristics for pin MFIN

Table 161 Input Pin characteristics for pin MFIN

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 SVDD	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 SVDD	V

20.6.3 Input / Output Pin characteristics for pins D1, D2, D3, D4, D5, D6 and D7

Table 162 Input / Output Pin characteristics for pins D1, D2, D3, D4, D5, D6 and D7

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 PVDD	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 PVDD	V
V_{OH}	Output voltage HIGH	PVDD=3V, Io=4mA	PVDD -400mV	-	PVDD	V
V_{OL}	Output voltage LOW	PVDD=3V, Io=4mA	PVSS	-	PVSS +400mV	V
I_{OL}	Output current drive LOW	PVDD=3V	-	-	4	mA
I_{OH}	Output current drive HIGH	PVDD=3V	-	-	4	mA

20.6.4 Output Pin characteristics for pin SDA

Table 163 Output Pin characteristics for pin SDA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 PVDD	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 PVDD	V
V_{OL}	Output voltage LOW	PVDD=3V, Io=3mA	-	-	PVSS +400mV	V
I_{OL}	Output current drive LOW	PVDD=3V	-	-	4	mA

20.6.5 Output Pin characteristics for Pin MFOUT

Table 164 Output Pin characteristics for Pin MFOUT

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage HIGH	SVDD=3V, Io=4mA	SVDD +400mV	-	SVDD	V
V_{OL}	Output voltage LOW	SVDD=3V, Io=4mA	SVSS	-	PVSS +400mV	V
I_{OL}	Output current drive LOW	SVDD=3V	-	-	4	mA
I_{OH}	Output current drive HIGH	SVDD=3V	-	-	4	mA

20.6.6 Output Pin characteristics for Pin IRQ

Table 165 Output Pin characteristics for Pin IRQ

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage HIGH	PVDD=3V, Io=4mA	PVDD -400mV	-	PVDD	V
V_{OL}	Output voltage LOW	PVDD=3V, Io=4mA	PVSS	-	PVSS +400mV	V
I_{OL}	Output current drive LOW	PVDD=3V	-	-	4	mA
I_{OH}	Output current drive HIGH	PVDD=3V	-	-	4	mA

20.6.7 Input Pin characteristics for Pin Rx

Table 166 Input Pin characteristics for Pin Rx

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN,RX}$	Input voltage Range		-1	-	AVDD +1V	V
$C_{IN,RX}$	RX Input capacitance	AVDD = 3V, Receiver active, V_{RX} = 1Vpp, 1.5 V_{DC} offset	-	10	-	pF
$R_{IN,RX}$	RX Input Series resistance	AVDD = 3V, Receiver active, V_{RX} = 1Vpp, 1.5 V_{DC} offset	-	350	-	Ohm

Note: The voltage on RX in clamped by internal diodes to AVSS and AVDD.

20.6.8 Input Pin characteristics for Pin OSCIN

Table 167 Input Pin characteristics for Pin OSCIN for external clock

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 AVDD	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 AVDD	V
C_{OSCIN}	Input capacitance	AVDD=2.8V, V_{DC}=0.65V, V_{AC}=1Vpp	-	2	-	pF

20.6.9 Output Pin characteristics for Pins AUX1 and AUX2

Table 168 Output Pin characteristics for Pins AUX1 and AUX2

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage HIGH	DVDD=3V, Io=4mA	DVDD -400mV	-	DVDD	V
V_{OL}	Output voltage LOW	DVDD=3V, Io=4mA	DVSS	-	DVSS +400mV	V
I_{OL}	Output current drive LOW	DVDD=3V	-	-	4	mA
I_{OH}	Output current drive HIGH	DVDD=3V	-	-	4	mA

20.6.10 Output Pin characteristics for Pins TX1 and TX2

Table 169 Output Pin characteristics for Pins TX1 and TX2

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH,C32,3V}$	Output voltage HIGH	TVDD=3V and I_{TX} =32mA, CWGsP=3F(hex)	TVDD-150 mV	-	-	mV
$V_{OH,C80,3V}$	Output voltage HIGH	TVDD= 3V and I_{TX} = 80mA, CWGsP=3F(hex)	TVDD-400 mV	-	-	mV
$V_{OH,C32,2V5}$	Output voltage HIGH	TVDD=2.5V and I_{TX} =32mA, CWGsP=3F(hex)	TVDD-240 mV	-	-	mV
$V_{OH,C80,2V5}$	Output voltage HIGH	TVDD=2.5V and I_{TX} =80 mA, CWGsP=3F(hex)	TVDD-640 mV	-	-	mV
$V_{OLC32,3V}$	Output voltage LOW	TVDD=3V and I_{TX} =32mA, CWGsN=F(hex)	-	-	150	mV
$V_{OL,C80,3V}$	Output voltage LOW	TVDD= 3V and I_{TX} = 80mA, CWGsN=F(hex)	-	-	400	mV
$V_{OL,C32,2V5}$	Output voltage LOW	TVDD=2.5V and I_{TX} =32mA, CWGsN=F(hex)	-	-	240	mV
$V_{OL,C80,2V5}$	Output voltage LOW	TVDD=2.5V and I_{TX} =80 mA, CWGsN=F(hex)	-	-	640	mV

20.7 Current Consumption

Table 170 Current Consumption

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{HPD}[4]	Hard Power down Current	AVDD=DVDD=TVDD=PVDD= =3V, NRESET= LOW	-	-	5	µA
I_{SPD}[4]	Soft Power down Current	AVDD=DVDD=TVDD=PVDD= 3V	-	-	10	µA
I_{DVDD}	Digital Supply Current	DVDD=3V	-	6,5	9	mA
I_{AVDD}	Analog Supply Current	AVDD=3V, bit *RCVOff*=0	-	7	10	mA
$I_{AVDD,RCVOFF}$	Analog Supply Current, receiver switched off	AVDD=3V, bit *RCVOff*=1	-	3	5	mA
I_{PVDD}[2]	Pad Supply Current		-	-	40	mA
I_{TVDD}[1,3]	Transmitter Supply Current	Continuous Wave	-	60[5]	100	mA
I_{SVDD}[6]	MFIN / MFOUT Pad Supply Current		-	-	4	mA

Note:

1. I_{TVDD} depends on TVDD and the external circuitry connected to Tx1 and Tx2.
2. I_{PVDD} depends on the overall load at the digital pins.
3. During operation with a typical circuitry the overall current is below 100 mA.
4. I_{SPD} and I_{HPD} are the total currents over all supplies.
5. Typical value using a complementary driver configuration and an antenna matched to 40 Ohm between TX1 and TX2 at 13.56 MHz.
6. ISVDD depends on the load at the MFOUT pin.

20.8 RX Input Voltage Range

Table 171 RX Input Voltage Range

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RX,MinIV,Man}$	Minimum Input voltage, Manchester Coded	AVDD = 3V, 212 and 424 kbit/s	-	100	-	mVpp
$V_{RX,MaxIV,Man}$	Maximum Input voltage, Manchester Coded	AVDD = 3V, 212 and 424 kbit/s	-	4	-	Vpp

Figure 30 outlines the voltage definitions.

20.9 RX Input Sensitivity

Table 172 RX Input Sensitivity

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RXMod,Man}$[1]	Minimum modulation voltage	AVDD = 3V, RxGain= 7	-	5	-	mV

Note 1: The minimum modulation voltage is valid for all modulation schemes.

Figure 30 outlines the voltage definitions.

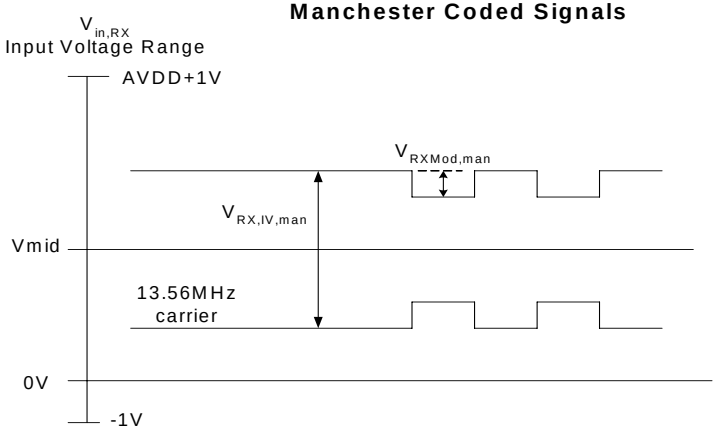


Fig.30 RX Input Voltage Range,

20.10 Clock Frequency

Table 173 Clock Frequency

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
f_{OSCIN}	Clock Frequency	-	27.12	-	MHz
d_{FEC}	Duty Cycle of Clock Frequency	40	50	60	%
t_{jitter}	Jitter of Clock Edges	-	-	10	ps, RMS

20.11 XTAL Oscillator

Table 174 XTAL Oscillator

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$V_{OH,OSCOUT}$	Output Voltage High XTAL2	-	1.1	-	V
$V_{OL,OSCOUT}$	Output Voltage Low XTAL2	-	0.2	-	V
$C_{IN,OSCOUT}$	Input capacitance OSCOUT	-	2	-	pF
$C_{IN,OSCIN}$	Input capacitance OSCIN	-	2	-	pF

20.12 Typical 27.12 MHz Crystal Requirements

Table 175 XTAL Oscillator

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
f_{XTAL}	XTAL Frequency Range	-	27.12	-	MHz
ESR	XTAL Equivalent Series resistance	-	-	100	Ohm
C_L	XTAL Load capacitance	-	10	-	pF
P_{XTAL}	XTAL Drive Level	-	50	100	µW

20.13 Timing for the SPI compatible interface

Table 176 Timing Specification for SPI

SYMBOL	PARAMETER	MIN.	MAX	UNIT
t_{SCKL}	SCK low pulse width	50	-	ns
t_{SCKH}	SCK high pulse width	50	-	ns
t_{SHDX}	SCK high to data changes	25	-	ns
t_{DXSH}	data changes to SCK high	25	-	ns
t_{SLDX}	SCK low to data changes	-	25	ns
t_{SLNH}	SCK low to NSS high	0	-	ns

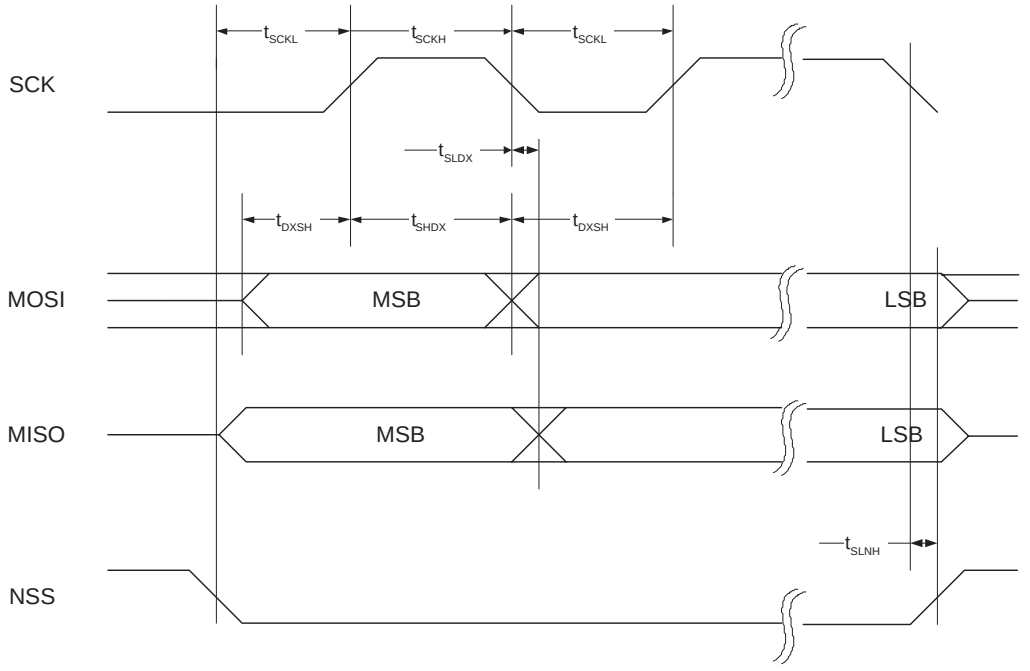


Fig.31 Timing Diagram for SPI.

Note: The signal NSS has to be low to be able to send several bytes in one data stream.

To send more than one data stream NSS has to be set to HIGH level in between the data streams.

20.14 I²C Timing

Table 177 Overview I²C Timing in fast mode

SYMBOL	PARAMETER	FAST – MODE		HIGH SPEED– MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0	400	0	3400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	600	–	160	–	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	600	–	160	–	ns
$t_{SU;STO}$	Set-up time for STOP condition	600	–	160	–	ns
t_{LOW}	LOW period of the SCL clock	1300	–	160	–	ns
t_{HIGH}	HIGH period of the SCL clock	600	–	60	–	ns
$t_{HD;DAT}$	Data hold time	0	900	0	70	ns
$t_{SU;DAT}$	Data set-up time	100	–	10	–	ns
t_{rscl}	Rise time SCL signals	20	300	10	40	ns
t_{fsc}l	Fall time SCL signals	20	300	10	40	ns
t_{rsda}	Rise time of both SDA and SCL signals	20	300	10	80	ns
t_{fsda}	Fall time of both SDA and SCL signals	20	300	10	80	ns
t_{BUF}	Bus free time between a STOP and START condition	1.3	–	1.3	–	µs

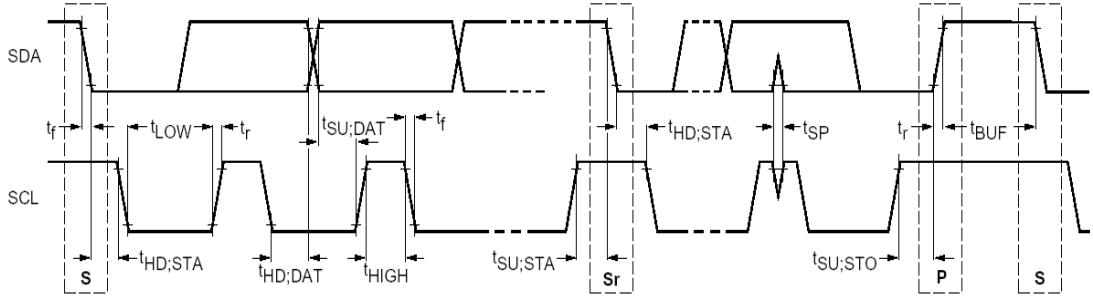
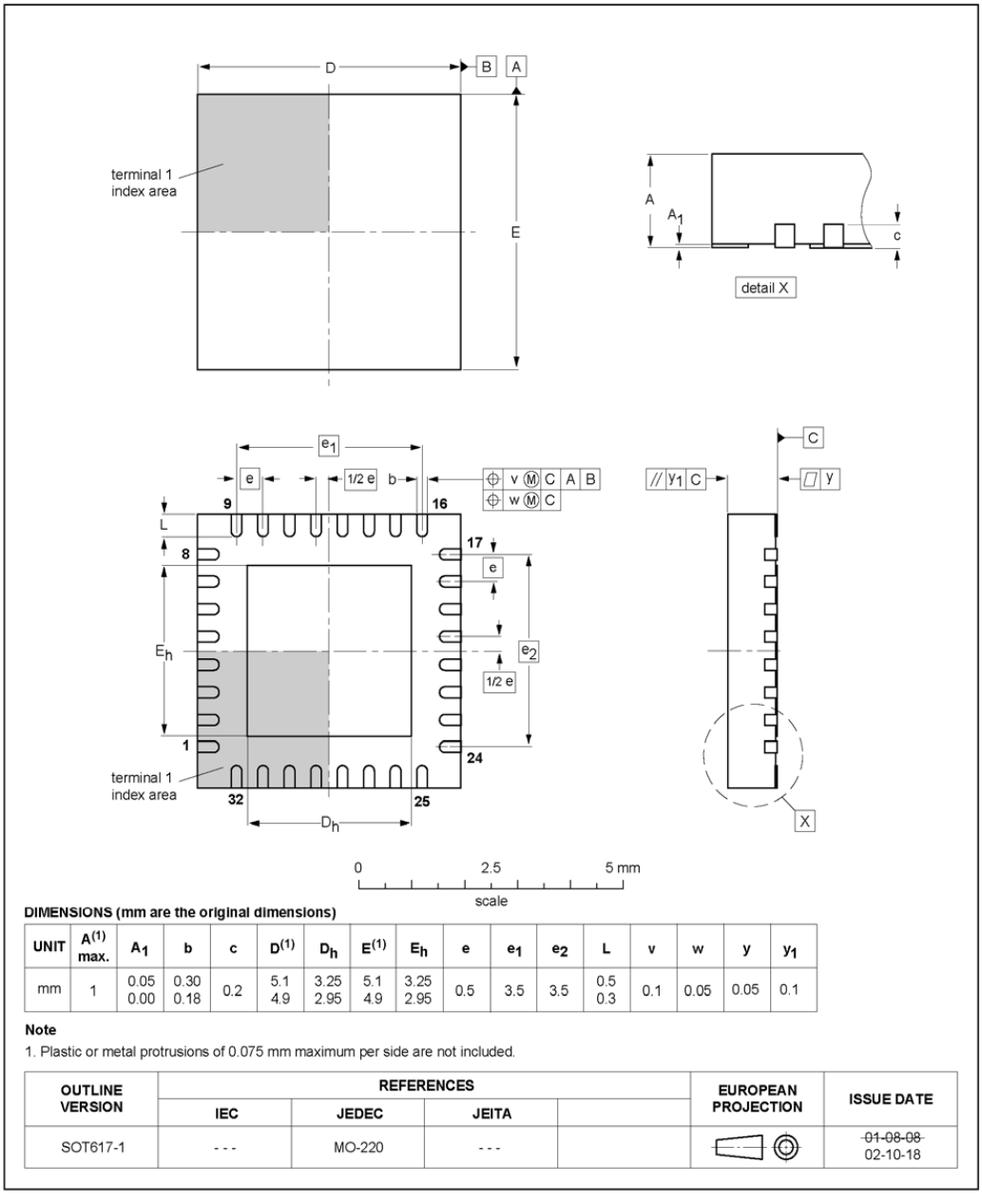


Fig.32 Timing for F/S-mode devices on the I²C-bus.

21 PACKAGE OUTLINES

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

22 TERMS AND ABBREVIATIONS

Table 178 Term and Abbreviations

DESIGNATION	DESCRIPTION
ASK	Amplitude Shift keying
PCD	Proximity Coupling Device. Definition for a Card Reader/ Writer according to the ISO 14443 specification.
PICC	Proximity Cards. Definition for a contactless Smart Card according to the ISO 14443 specification.
PCD → PICC	Communication flow between a PCD and a PICC according to the ISO 14443A / MIFARE®.
PICC→ PCD	Communication flow between a PICC and a PCD according to the ISO 14443A / MIFARE®.
Initiator	Generates RF field @ 13.56 MHz and starts the NFCIP-1 communication.
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin) / (Vmax + Vmin).
Loadmodulation Index	The load modulation index is defined as the card's voltage ratio (Vmax - Vmin) / (Vmax + Vmin) measured at the card's coil.
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).

23 DEFINITIONS

Table 179 Definitions

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Electrical Characteristics	
Category "typical"	Values given for "typical" electrical characteristics of the devices represent average operation properties and are not tested during mass production.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

24 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

25 REVISION HISTORY

Table 180 Versions up to Revision 0.2

REVISION	DATE	CPCN	PAGE	DESCRIPTION
0.2	August 2004			first external draft version
0.3	October 2004			changes in register description
0.4	November 2004			temporary remove type ordering information changes in register description adaptation figure 22
1.0	July 2005			Document status changed to objective specification changes in various register descriptions SVDD Pin (chapter 5.2) ParityDisable bit (chapter 7.2.2.14) add MFIN / MFOUT description (chapter 10.4) various spelling corrections
2.0	July 2005			Document status chacnged to preliminary specification add package web-link (chapter 5.1) add ordering information (chapter 2)
2.1	September 2005			TxSelReg - bit DriverSel - combination 10
3.0	December 2005			Document status changed to product specification Change Ordering Information Chapter 2 Add Handling Information Chapter 3 Add Packing Information Chapter 4 Add Test Signal Examples in Chapter 18.3

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