# 2021 Digital IC Design

# Homework 2: Booth Algorithm

## 1. Introduction:

Booth algorithm is a multiplication operation that multiplies two numbers in two's complement notation. The detail algorithm is described as below:

(1) Assume that the multiplicand *m* is x-bit and multiplier *r* is y-bit.
Initialize a register *P* for the final result, and the length is x+y+1 bits.
The initial value of *P* is 0(x bits)_*r*(y bits)_0(1 bit).

(2) The rightmost 2 bits used for the selection of different executions.

| Rightmost 2 bits | Execution |
|---|---|
| 00 | No execution |
| 01 | Add *m* to the left part of *P* |
| 10 | Subtract *m* from the left part of *P* |
| 11 | No execution |

* Overflow condition can be ignored during the execution.

(3) **Arithmetically** shift 1 bit on *P*.

(4) Repeat the step (2) and (3) for y times.

(5) The final answer is obtained by dropping the LSB from *P*.

## 2. Design Specifications:

### 2.1 Block Overview

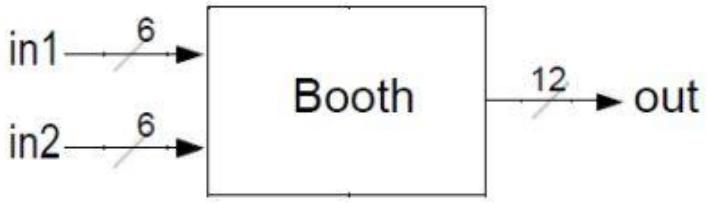


Fig. 1. The block overview.

### 2.2 I/O Interface

| Signal Name | I/O | width | Description |
|---|---|---|---|
| *in1* | I | 6 | Multiplicand |
| *in2* | I | 6 | Multiplier |
| *out* | O | 12 | Product |

### 2.3 File Description

| File Name | Description |
|---|---|
| booth.v | The top module of the design. |
| booth_tb.v | The testbench file. The content in this file is **not allowed** to be modified. |

## 3. Scoring:

### 3.1 Functional Simulation **[60%]**

All of the result should be generated correctly, and you will get the following message in ModelSim simulation.

```
#        4004 data is correct
#        4005 data is correct
#        4006 data is correct
#        4007 data is correct
#        4008 data is correct
#        4009 data is correct
#        4010 data is correct
#        4011 data is correct
#        4012 data is correct
#        4013 data is correct
#        4014 data is correct
#        4015 data is correct
#        4016 data is correct
#        4017 data is correct
#        4018 data is correct
#        4019 data is correct
#        4020 data is correct
#        4021 data is correct
#        4022 data is correct
#        4023 data is correct
#        4024 data is correct
#        4025 data is correct
#        4026 data is correct
#        4027 data is correct
#        4028 data is correct
#        4029 data is correct
#        4030 data is correct
#        4031 data is correct
#        4032 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
```

Fig. 2. Functional simulation result.

### 3.2 Gate-Level Simulation **[30%]**

#### 3.2.1 Synthesis

Your code should be synthesizable. After it is synthesized in Quartus, a file named *booth.vo* will be obtained.

#### 3.2.2 Simulation

All of the result should be generated correctly using booth.vo, and you will get the following message in ModelSim simulation.

```
#        4024 data is correct
#        4025 data is correct
#        4026 data is correct
#        4027 data is correct
#        4028 data is correct
#        4029 data is correct
#        4030 data is correct
#        4031 data is correct
#        4032 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
```

Fig. 3. Gate-level simulation result.

Device：**Cyclone II EP2C70F896C8**

### 3.3 Performance **[10%]**

The performance is scored by the clock width your design can operate in gate-level simulation. The score will be decided by your ranking in all received homework. (The smaller the better)

## 4. Submission:

### 4.1 Submitted files

You should classify your files into three directories and compress them to .zip format. The naming rule is HW2_studentID_name.zip. If your file is not named according to the naming rule, you will lose five points.

| | RTL category |
|---|---|
| *.v | All of your Verilog RTL code |
| | Gate-Level category |
| *.vo | Gate-Level netlist generated by Quartus |
| *.sdo | Gate-Level netlist generated by Quartus |
| | Documentary category |
| *.pdf | The report file of your design (in pdf). |

### 4.2 Report file

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible, and the flow summary result is necessary in the report.

| Flow Summary | |
|---|---|
| Flow Status | Successful - Sat Mar 27 18:40:05 2021 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web |
| Revision Name | booth |
| Top-level Entity Name | booth |
| Family | Cyclone II |
| Device | EP2C70F896C8 |
| Timing Models | Final |
| Total logic elements | 132 / 68,416 ( < 1 % ) |
| Total combinational functions | 132 / 68,416 ( < 1 % ) |
| Dedicated logic registers | 0 / 68,416 ( 0 % ) |
| Total registers | 0 |
| Total pins | 24 / 622 ( 4 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 1,152,000 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 0 / 300 ( 0 % ) |
| Total PLLs | 0 / 4 ( 0 % ) |

Fig. 4. The flow summary.

## 4.3 Note

Please submit your .zip file to folder HW2 in moodle.

Deadline: 2021/4/19 23:55

If you have any problem, please contact TA by email.

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