VLSI System Design (Graduate Level)

Fall 2023

HOMEWORK IV

REPORT

Must do self-checking before submission:

Compress all files described in the problem into one tar

All SystemVerilog files can be compiled under SoC Lab environment

All port declarations comply with I/O port specifications

Organize files according to File Hierarchy Requirement

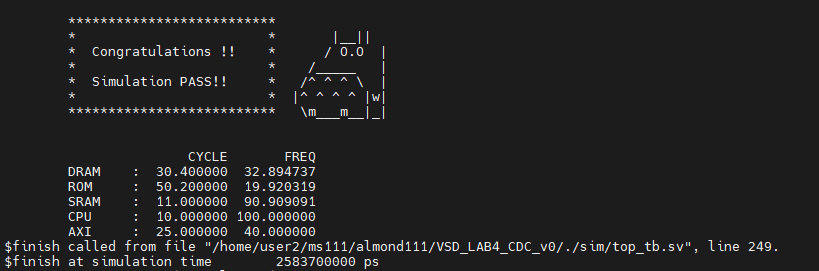
No waveform files in deliverables

Student name: \_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_

Student ID: \_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_

|  |  |  |  |
| --- | --- | --- | --- |
| Performance & Area | | | |
|  | rtl | syn | pr |
| Prog0 time |  | 2583700000 |  |
| Prog1 time |  |  |  |
| Prog2 time |  |  |  |
| Prog3 time |  |  |  |
| Area(um^2)  In APR |  | | |
| CPU cycle | 10ns | | |

Refer to the figure to fill in the simulation time !!



// Initiate your report from this point.