VLSI System Design (Graduate Level)

Fall 2023

HOMEWORK IV

REPORT

Must do self-checking before submission:

Compress all files described in the problem into one tar

All SystemVerilog files can be compiled under SoC Lab environment

All port declarations comply with I/O port specifications

Organize files according to File Hierarchy Requirement

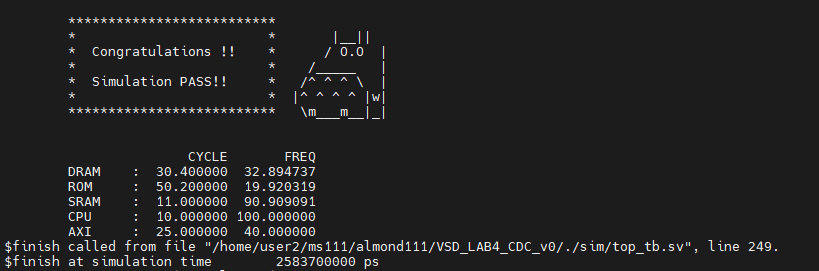
No waveform files in deliverables

Student name: \_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_

Student ID: \_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_

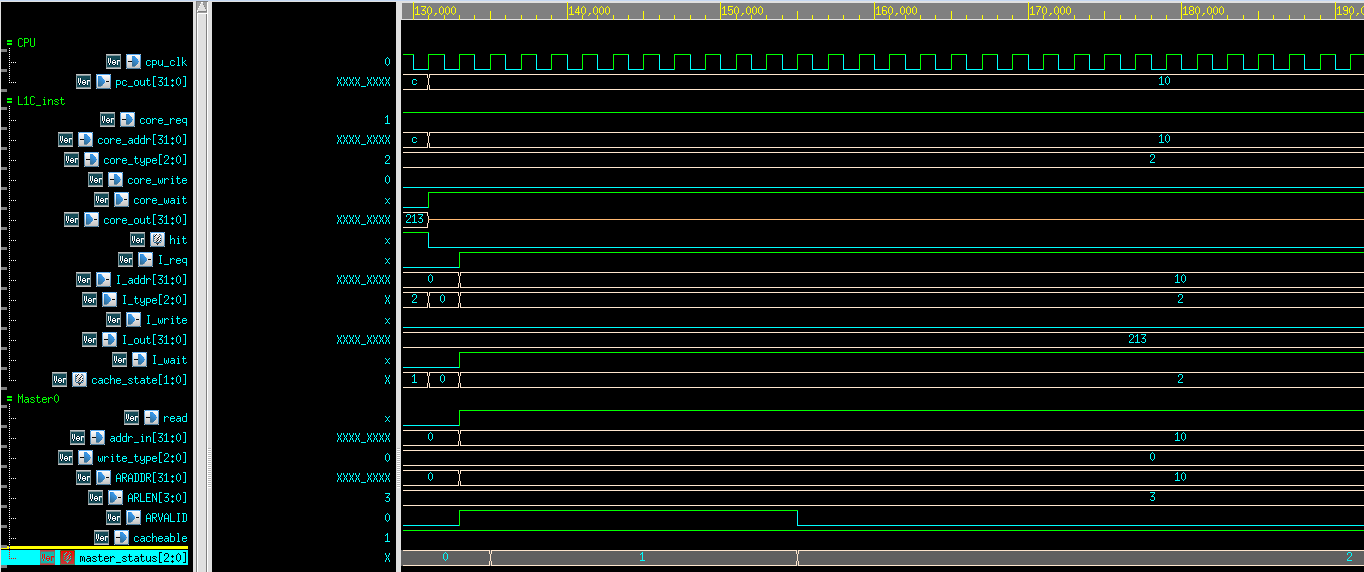
|  |  |  |  |
| --- | --- | --- | --- |
| Performance & Area | | | |
|  | rtl | syn | pr |
| Prog0 time |  | 2583700000 |  |
| Prog1 time |  |  |  |
| Prog2 time |  |  |  |
| Prog3 time |  |  |  |
| Area(um^2)  In APR |  | | |
| CPU cycle | 10ns | | |

Refer to the figure to fill in the simulation time !!

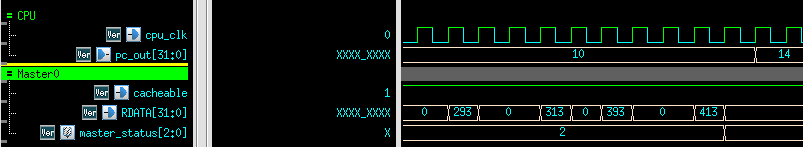


// Initiate your report from this point.

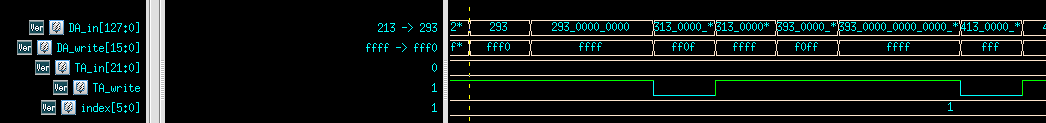
1. Cache read miss:



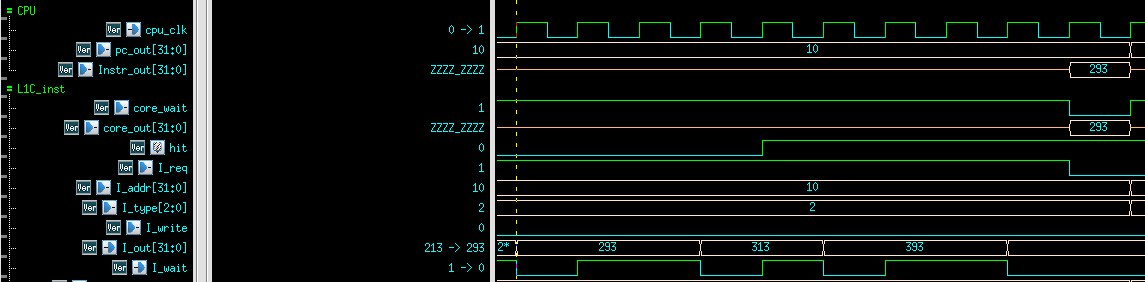
在pc\_out為10時,CPU對L1C\_inst發出core\_req請求指令,core\_wait設為1直到正確資料回傳給CPU , core\_write為0因為此時為請求instruction指令並且core\_addr為10,所以是去ROM讀取指令,可以看到此時hit為0代表L1C\_inst中並沒有暫存這個指令,所以cache\_state = 2轉為read\_miss狀態,設定送往master0的資料來透過AXI讀取ROM,此時將read設為1因為是要讀取資料,將ARADDR設為10來讀取ROM,ARLEN設為3因為一個block有4個word需要讀出連續4筆資料傳回cache,ARVALID設為1開始透過AXI存取資料,cacheable一直設為1因為master0只會讀取ROM或IM並不會讀取sensor\_wrapper , master\_status = 2為讀取資料狀態



Master0等待4筆資料(293,313,393,413)回傳後將資料傳給cache存進Data\_array以及Tag\_array

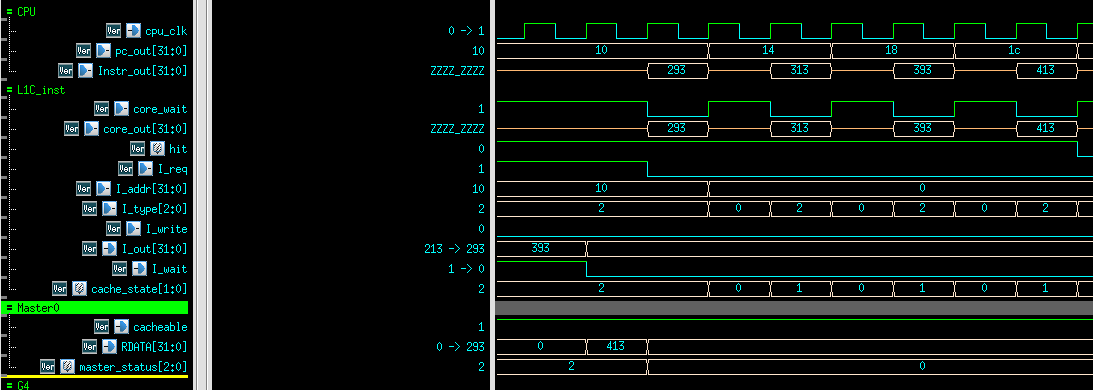


依照DA\_in及DA\_write將四筆資料存入Data\_array後,



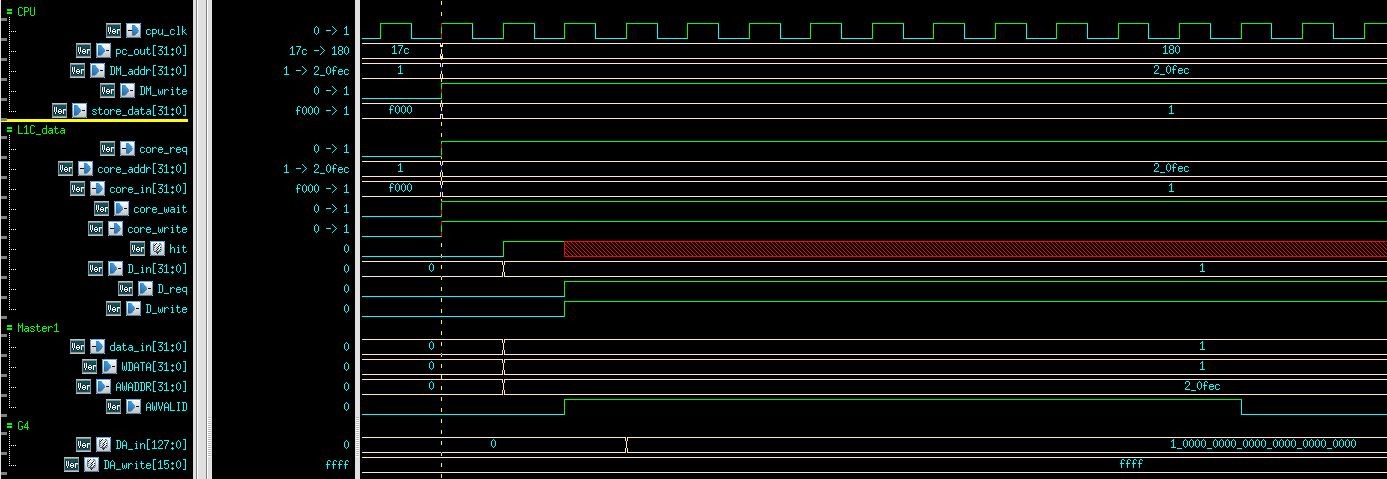
最後透過core\_out將指令傳給CPU中的IF-stage。

1. Cache read hit

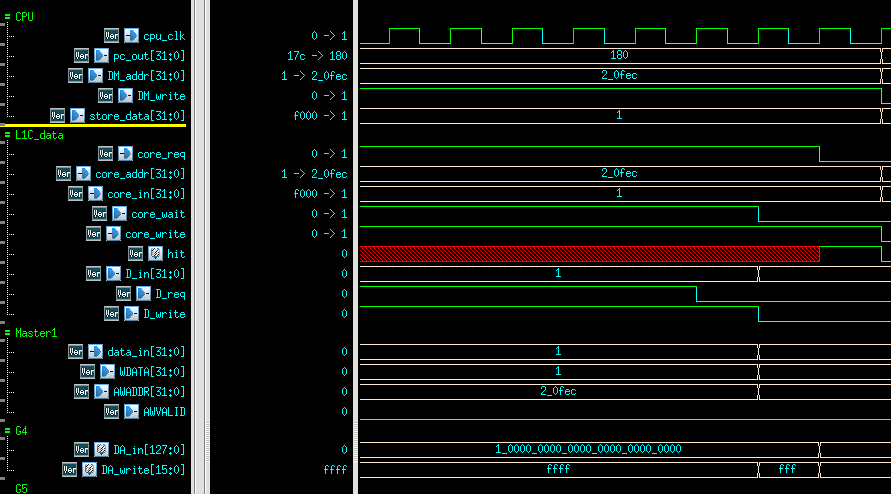


在經過pc\_out為10 的指令後,因為指令是連續讀取的,所以後面的三個指令都已經暫存在L1C\_cache中,所以可以看到後面三個指令hit都為1代表資料在cache中,不需要透過master0去讀取memory中的指令,所以會將I\_req設為0表示不需要去存取memory,可以看到core\_out直接將暫存的指令輸出給CPU中的IF-stage。

1. Cache write (write through)



當pc\_out為180時,MEM-stage要對DM\_addr為20fec寫入資料store\_data為1,所以CPU會發出core\_req並將core\_addr設為20fec , core\_in為要寫入的資料設為1,因為現在為hit所以必須對master1下指令去寫入AWADDR為20fec, WDATA為1



因為是hit所以cache中也有資料所以必須更新Data\_array中的資料。