

Why do we need this?

Physics: the fister a bus is the shorter it must be.

Physics: the fister a bus is the shorter it must be.

(why memory is always close to CPU)

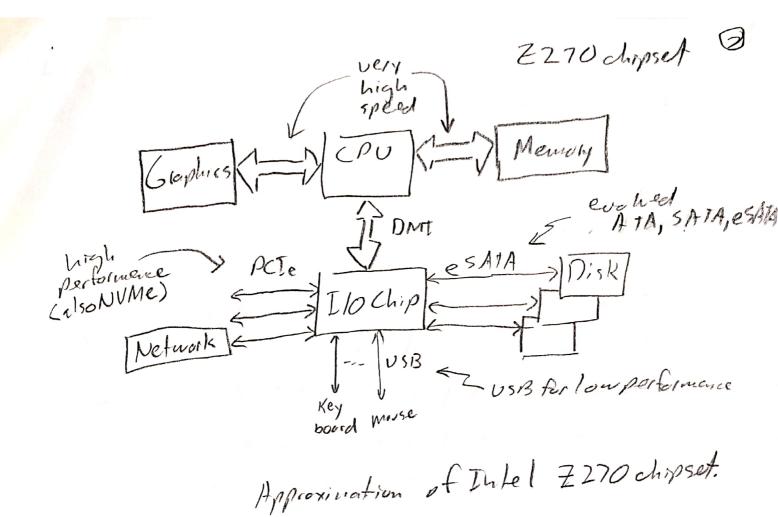
(why memory is always close to CPU)

costs: higher clocks, harder to week around, cross

coupling tems effects goup as switching

spends merease, Harder to engineer.

High performence, less of, closer low performance, more of for the away



- High performence up hop
- CPU comments to Ilochip was Intel proprietory
 DMI (Direct Media Interface) bus.
- Note single chip handles all the bus pictucals

1) - has hordware interface - allows the system software to control it.

- consists of interface + protocal for hypical meraction

D) internal structure - control of the device,

simple-lor afew HW chops to implement functionality

complex- a simple CRU, memory other device chips

ex. Modern RAID controllers have thousands

of times of firmware.

Interface Registers Status Command Data

Interface Registers Status Command Data

Microcontraller (CPU)

Memory (DRAM or SRAM or Both)

other HIW chips

Status-whats going on command-tell it what to do Data - data that goes ma out

OS controls device by reading/writing)

while (Status == busy) & pollong! (1)

i // wait until not

withe Data to Data reg

withe a command to Command reg.

(starts the device & executes the command)

while (status = 2 busy) & pollong

; Il wait until device done al regrest.

Polling - could waste lots of CPU Limewasting on slow device, How to avoid?

Solve - Interrupts

os issues request tor mark

pts the calling process to sleep

switch to other process

when device finishes work

device raises H/W interrupt

CPU jumps to OS at ISR (interrupt Sorvice)

Exertine

ISR finishes request & maybe rands data & 3

Emaybe error code &

and walses the process waiting for ID

scerlap

p-pollris

(5)

above piecess I ions, issues request to read from disk, process I polls waiting for data

Interrates

1111111222221111111

os ruis 2 while waiting her disk to service I's request when disk read is done, device interrupts CPU, I reanablemed by OS, runs again

Interrupts are not always the best solution!

if device performs it's task quickly

Hen 1st poll finds It done.

Better to poll (few clock eyeles) verses

13e Her to poll (few clock eyeles) verses context suitches x ISR (100,000 cycles)

So interrupts make sense for slow devices

If you don't know speed maybe use
hybrid, pull for a bit then switch to interrupts

I were neteringt problem

- arises in networks luge stream of mounty packets, each generaling interrupt - possible for system to only process interrupts (livelock)
- way he better to.
 swork abit } know there garny to be

 poll Sajob(s) don't better

 w/ context switch overhead.

- or coaksce

if device needs to gen an interrupt

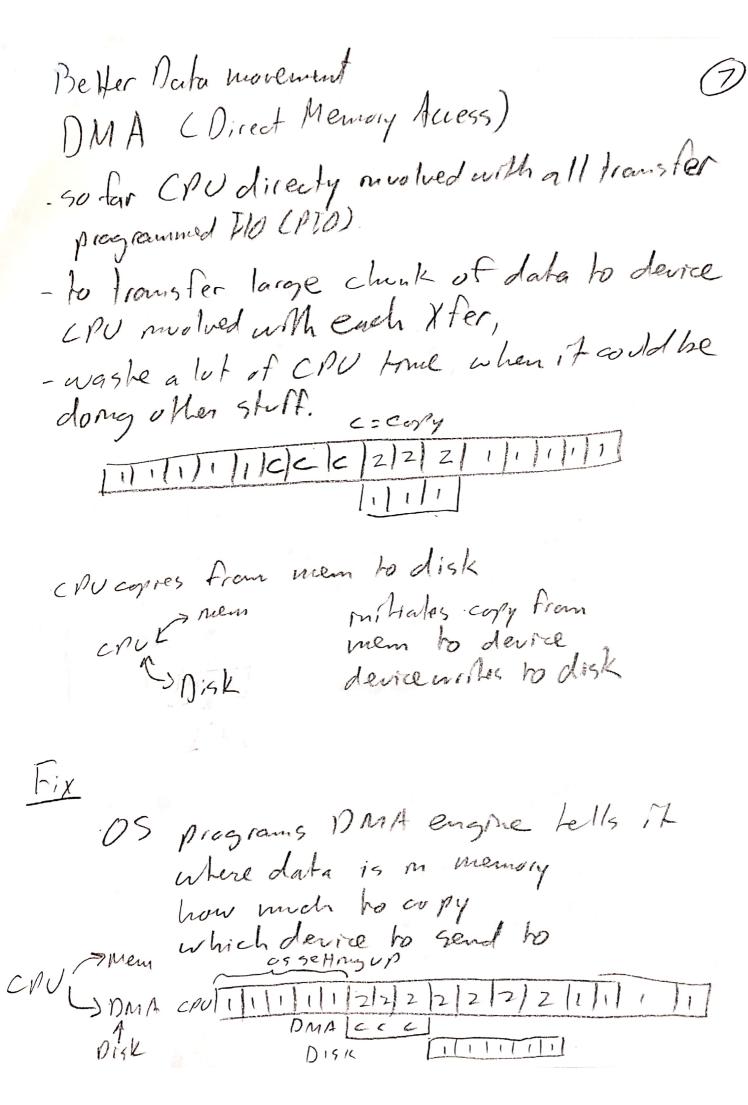
wastabit rese if more tasks complete

then generate one interrupt for all.

(miltiple -> single) lowers int piecessing

overhead.

Chome to service interrupt)



copying handled by DMA controller. (8) How dolo 05 communicate with Devrce? 2 ways O Explicit Ilo mélluctions (8) Mem Mapped Flo - How makes device registers available as if they were men locations. - Looccess register, 05 issues a load (read) or skie (write) command at the device address, Him rates add 2 Devz

Frally

- How to FA devices, leach having unique characteristics)

request to device not incom.

- ex frengstem - would like it bo work on SCSI, IDE, VKeycham disks. like filesystem to be oblivious to details Of particular Allerystem

Abstraction general APT Coppn, read, write close etc...) device driver, implements all for a particular bit of hardware OS sees only generic API, just rendo Jurites Vendois supply device direct for their It/W Consequene - lots of devices, lots of drivers - sometimes written by ametuers, run as Kernel can cause system eragh - all must be available on system ever though you only use a few -40 most OSa consists of mostly on sed device drivers, [Immx 70% of US ande is device drivers)