

Embench tester

Embench meeting, 2020-10-19 Karol Gugala, kgugala@antmicro.com





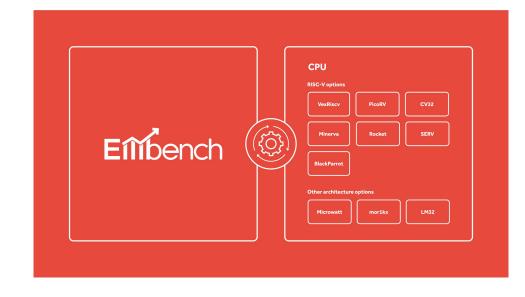
MOTIVATION

- Test as many open source soft-core CPUs as possible
- CI for tracking the changes
- Compare different CPUs (architectures and implementations)



EMBENCH TESTER OVERVIEW

- Open source github.com/antmicro/embench-tester
- CPUs under test are instantiated within LiteX sim SoC
- All the tests are run in Cl in Verilator simulation
- All the tests are run from simulated RAM
- Results are collected in csv tables
- The system can automatically generate and deploy gh-pages website presenting the results



FPGA

SoC infrastructure and memory

Bus Arbiter Clock control

Timer

Wishbone Bridge

ILA

Debug

Flash

DDR

I/O interfaces

UART

I2C

GPIO

SPI

USB

PCle

125

Video

GbE

SATA

SDIO

CPU

RISC-V options

VexRiscv

PicoRV

CV32

Minerva

Rocket

SERV

BlackParrot

 ${\bf Other\, architecture\, options}$

Microwatt

mor1kx

LM32



RESULTS

- · Generated in CI
- Collected in the tables and presented on gh-pages website
- antmicro.github.io/embench-tester/
- · Presents relative and absolute results
- Summarizes test platform

Absolute tests results: [ms]

	Absolute tests results. [ms]							
	vexriscv	picorv32	minerva	cv32e40p	serv	lm32	mor1kx	microwatt
aha-mont64	5468	29142	60117	12746	1201669	8438	7823	3369
crc32	5403	26656	49102	14464	367018	5928	5575	11027
cubic	14673	47643	61400	22527	3302039	19999	14613	7353
edn	4671	39668	18544	13601	4294967	5348	6436	18789
huffbench	4008	14785	29594	12406	162626	4190	4602	9115
matmult-int	4938	30685	15123	13647	2151027	6716	6450	22964
minver	8742	30971	47172	15284	4294967	12529	11331	10567
nbody	5232	19982	32245	9488	2448259	10833	8217	4273
nettle-aes	6885	23857	66303	14501	338046	6965	5975	9567
nettle-sha256	7848	27021	82610	15810	252651	9851	11822	7212
nsichneu	13018	13194	21905	12107	157985	11022	11125	21131
picojpeg	5858	25445	41957	15033	267163	6235	5516	12211
qrduino	3986	17601	47899	10906	303785	4117	4535	7547
sglib-combined	4486	14238	21994	11367	247771	5281	5172	9414
sire	4044	14147	20873	10689	152571	4689	4269	8210
st	7176	31470	49641	15002	3535898	19865	14092	4783
statemate	4859	12340	20259	11289	127387	5297	7202	10306
ud	7460	27969	30747	15494	572278	11597	7922	15551
wikisort	2755	11015	13911	6547	1095370	5772	4455	4926



FUTURE WORK

- Thorough review
- Automatic extraction of the CPUs configuration
- 64 bit CPUs support
- Setup more automatic system (e.g. dependabot for bumping the tools)
- Automatic tests on FPGA
- Work with authors of specific cores to introduce obvious improvements to implementations where results don't match expectations
- Add more CPUs



THANK YOU FOR YOUR ATTENTION!