CHAIR OF COMPUTER ARCHITECTURE AND PARALLEL SYSTEMS

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Dynamic Binary Translation for RISC–V code on x86–64

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1 Introduction

The aim of this project is to create a system capable of executing code compiled for the RISC-V instruction set architecture on an x86-64 system.

RISC-V is an open ISA first conceptualised in 2010 with the initial goals of research and education in mind. Its development took the lessons learned in terms of backwards compatibility and future-proofing from other widespread ISAs like Intel x86 into account, and aims to provide an open interface for the architecture, rather than strict implementation details. This grants a large freedom to the implementors and greatly increases the flexibility and ease of working with the architecture [1, S. 1f].

1.1 Problem description

As there is as yet no real hardware available for the RISC-V ISA, developers must rely on emulation in order to test their software.

We aim to provide such an emulator, allowing the execution of such RISC-V code on an x86-64 machine by means of dynamic binary translation.

Continued here (compare ISAs and note challenges)...

2 Approach

3 Implementation Details

4 Results and Performance

5 Summary

References

[1] Editors Andrew Waterman and Krste Asanović. *The RISC-V Instruction Set Manual, Volume I: User Level ISA, Document Version 20191213*. RISC-V Foundation, December 2019.