### With solar cell maximum power point tracking function

### **5A** multi-type battery charging management integrated circuit

#### **CN3722**

Overview:	Features:
CN3722 (Note 1) is a PWM step-down mode charging management integrated	ÿ Wide input voltage range: 7.5V to 28V ÿ Solar battery
circuit that can be powered by solar cells, and has the function of maximum	maximum power point tracking ÿ For single or multi-cell
power point tracking of solar cells. CN3722 is very suitable for charge	lithium battery or lithium iron phosphate
management of single or multi-cell lithium battery or lithium iron phosphate	battery for complete charge management
battery. It has the advantages of small package shape, few peripheral	ÿ Constant voltage charging voltage is set by an external resistor
components and simple use.	divider
CN3722 has constant current and constant voltage charging mode, which is	network ÿ Charging current up to
very suitable for charging lithium battery or lithium iron phosphate battery. In	5A ÿ PWM switching frequency: 300KHz ÿ Constant
constant voltage charging mode, the constant voltage charging voltage is set	current charging current is set by an external resistor ÿ Trickle
by an external resistor divider network; in constant current charging mode,	charging for deeply discharged batteries ÿ Battery temperature
the charging current is set	monitoring function ÿ Charging status ÿ
by an external resistor. For deeply discharged batteries, when the battery	Soft-start function $\ddot{y}$ Battery terminal overvoltage protection $\ddot{y}$
voltage is lower than 66.7% of the set constant voltage charging voltage,	Working environment
CN3722 will trickle charge the battery with 15% of the set constant current	temperature: -40ÿ to +85ÿ ÿ 16-pin
charging current. In the constant voltage charging stage, the charging current	TSSOP package ÿ The product is lead-free, halogen-free, and meet
gradually decreases, and when the charging current decreases to $9.5\%\ \text{of}$	RoHS
the set constant current charging current, it enters the charging end state.	
When the input power fails or the input voltage is lower than	Pin arrangement:
the battery voltage, CN3722 automatically enters the low-power	riii anangenieni.
sleep mode. Other functions include input low voltage latch, battery	
temperature monitoring, battery terminal overvoltage protection and charging status in	ndication, etc. VG 1 16 DRV
The CN3722 is available in a 16-pin TSSOP package.	PGND 2 15 VCC
application:	GND 3 14 ONE
application.	CHRG 4 13 CSP
ÿ Charging with solar cells ÿ Notebook	DONE 5 CN3722 12 NC
computers ÿ Backup battery	TEMP 6 11 COM3
applications ÿ Portable industrial	MPPT 7 10 FB
and medical instruments ÿ Power tools ÿ	
Standalone battery	COM1 8 9 COM2
chargers	

Note 1: Patent protection has been applied for

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Typical application circuit:

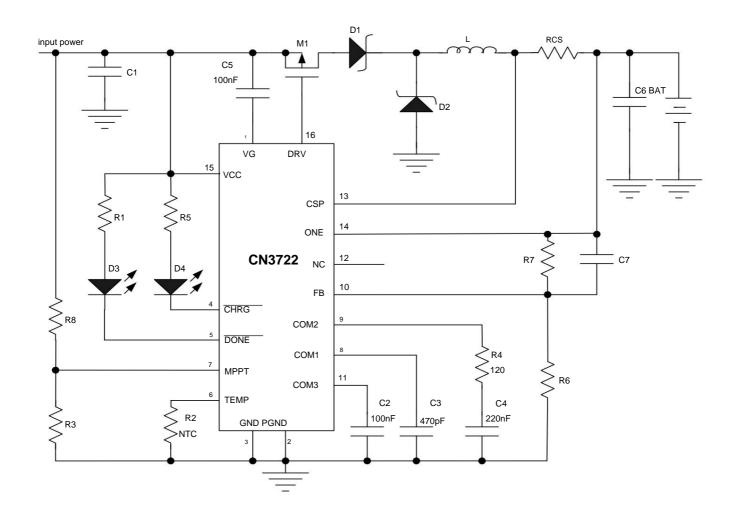


Figure 1 Typical application circuit

#### Ordering Information:

model	Working	Constant voltage charging voltage
CN3722 temperature -40°C to +85°C		External Resistor Divider Network Setup

#### Pin description:

Description of pin no	ımber and name	
1	VG	Internal Voltage Modulator Output. Provides power to the internal drive circuitry. at the VG pin and
		Connect a 100nF capacitor between VCC pins.
2	PGND power grou	and Control of the Co
3	GND analog gro	und
4	CHRG Open-drain	output. In trickle charge state, constant current charge state and constant voltage charge state
4		state, the internal transistor pulls this pin low; otherwise, this pin is in a high-impedance state.
5	DONE Open-drair	output. In the end-of-charge state, an internal transistor pulls this pin low
		level; otherwise, this pin is in a high-impedance state.
6	TEMP	Battery Temperature Monitoring Input. Connect a negative temperature coefficient
O	T E IVII	thermistor.
		Solar cell maximum power point tracking terminal. During normal operation, the voltage on this pin is regulated
7	MPPT	Controlled to 1.04V (25ÿ), the temperature coefficient is -0.4%/ÿ, in line with the maximum solar cell
,		The temperature coefficient of the power point voltage. This pin needs to be connected to a resistor divider network to detect the sun
		battery voltage.
8	COM1 Loop comp	ensation input terminal 1. Connect a 470pF capacitor from this pin to ground.
9	COM2	Loop Compensation Input 2. Connect a 120ÿ resistor in series from this pin to ground
J	COME	resistor and a 220nF capacitor.
10	FB Battery volt	age feedback terminal. External resistor divider network to detect battery voltage.
11	COM3 Loop comp	ensation input 3. Connect a 100nF capacitor from this pin to ground.
12	NC is not conne	ected
13	CSP	Charge Current Sense Positive Input. This pin and the BAT pin measure the charging current detection voltage
15		Resist the voltage at both ends of RCS, and feed this voltage signal back to the chip for current modulation.
14	ONE	Charge Current Sense Negative Input. This pin and the CSP pin measure the charge current sense voltage
1.7	ONE	Resist the voltage at both ends of RCS, and feed this voltage signal back to the chip for current modulation.
15	VCC	External power input terminal. VCC is also the power supply for internal circuits. Between this pin and ground
.5	.55	A filter capacitor is required.
16	DRV drives the (	ate of the off-chip P-channel MOS field effect transistor.

#### Limit parameter

VCC, CHRG, DONE to GND Voltage – 0.3V to 30V VG, DRV to VCC Voltage 8V CSP, BAT to GND
The voltage ofÿ0.3V to 28V The voltage of COM3 to
GND
0.3V to VCOM3+0.3V Storage temperatureÿ65ÿ150ÿ
Working environment temperature40ÿ85ÿ
Soldering temperature (10 seconds)260ÿ

Exceeding the limit parameters listed above may cause permanent damage to the device, \* The above given are only limit ranges, under such limit conditions the technical indicators of the device will not be guaranteed, and the reliability of the device will be affected under such conditions for a long time.

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Electrical Characteristics:

(VCC=15V, TA=-40ÿ to 85ÿ, unless otherwise noted)

(VCC=15V, TA=-40ÿ to 85ÿ, unle	ess otherwise no	otea)				i	
Parameter test conditions	symbol				Min Typical Max Unit		
Input Voltage Range	VCC			7.5		28 V	
Low Voltage Latch Threshold	VLOOK			4.2	6	7.3 V	
Chip Working Current	IVCC	VBAT ÿVREG		1.2	1.7	2.2 m	A
Feedback	VFB FB pin	voltage, constant voltage	e charging mode 2.392 2.	116		2.44 V	
Voltage FB Pin Bias Current	IFB	VFBÿ2.4V			50	300 nA	
Current Detection	VCS	VBATÿ66.7%×VRE	G VBAT	190	200	210	mV
Voltage (VCSPÿVBAT)	VC3	ÿ66.7%×VREG		15	27	42	IIIV
Flows into BAT Pin Current	DIFFERE	NT VBATÿ12V		5	10	15 u <i>A</i>	`
Trickle Charge Threshold	VPRE FB ہ	in voltage rises			66.7%		
Recharge Threshold	VRE FB p	in voltage drops			95.8%		VREG
Overvoltage	Vov Batte	y terminal voltage ris	es	1.06	1.08	1.1	(Note 2)
Threshold Overvoltage Release Threshold	Vclr batter	y terminal voltage dro	р	0.98	1	1.02	
MPPT pin	-						
MPPT pin modulation voltage VMF	PT in maximur	n power point tracking	g state 1.0 VMPPT		1.04	1.08 V	
temperature coefficient TCMPPT in	n maximum pov	ver point tracking state	e		ÿ0.4%		ÿÿ
MPPT pin bias current IMPPT TEN	<b>IP</b> pin			ÿ100	0	100 n/	\
Pull-Up Current	lup			42	55	68 uA	
Comparator High-Side Threshold	Vthh TEMF	P pin voltage rises		1.57	1.61	1.65 V	
Comparator Low-Side Threshold		pin voltage drops		0.145 0.	175 0.205 V		
CHRG pin							
CHRG pin pull-down current ICHR	G VCHRG=1V.	charging mode CHR	G pin	7	12	18 m.	Ą
leakage current		RG=25V, end of char				1 u	A
pin DONE pin			<u> </u>				
pull-down current IDONE VDONE=	1V. end of cha	rge mode 7 DONE pir	n leakage current		12	18 m.	Ą
		NE=25V, charge mod				1 u	A
	1 12.12.73		.e eeeate			<u> </u>	
	dark			240	300	360 kH	 Z
Frequency Maximum	Dmax			-	94		%
Duty Cycle Sleep Mode							,,,
Duty Cycle Sleep Wode			VBAT=8V	0.06	0.1	0.14	
Sleep Mode Threshold	VOLD V	00 fallin		0.00	0.14	0.14	IN
(measure VCCÿVBAT)	VSLP V(	CC falling	VBAT=12V	0.1	0.14	0.18	114
			VBAT=18V VBAT=8V	0.16	0.23	0.28	
Sleep Mode Release Threshold	VOI 55 175	D miletin m	-	0.20	0.32	0.59	IN
(measure VCCÿVBAT)	VSLPR VC	o rising,	VBAT=12V				IIN
DDV :			VBAT=18V	0.38	0.47	0.58	
DRV pin						<u> </u>	
VDRV high level	VH IDRVÿ	ÿ10mA			60		mV
(VCCÿVDRV) Electrical							

parameter	symbol	Test Conditions	Min Typio	cal Max Unit		
VDRV low level	VL IDRVÿ0m	Δ	5	6.5	8 V	
(VCCÿVDRV) rise time	VE IDICTYON					
fall time Note 2:	tr	Cloadÿ2nF, 10% to 90%	30	40	65	ns
VREG is the	tf	Cloadÿ2nF, 90% to 10%	30	40	65	ns

modulation voltage of BAT pin in constant voltage charging mode

A detailed description:

CN3722 is a PWM step-down mode charging management integrated circuit that can be powered by solar cells, with the maximum power of solar cells

Point tracking function. CN3722 has a constant current and constant voltage charging mode, which is very suitable for charging management of single-cell or multi-cell lithium batteries or lithium iron phosphate batteries

The constant current charging current is set by the current detection resistor RCS connected between the CSP pin and the BAT pin. In the constant voltage charging mode, the constant voltage charging woltage is set by an external resistor-divider network.

When the VCC pin voltage meets the following three conditions at the same time:

- (1) The VCC pin voltage is greater than the low-voltage latch threshold
- (2) The VCC pin voltage is greater than the battery voltage
- (3) The VCC pin voltage is not less than the set maximum power point voltage

The charger is working normally, charging the battery. If the battery voltage is lower than 66.7% of the set constant voltage charging voltage, the charger will automatically enter trickle

In current charging mode, the charging current is 15% of the set constant charging current. When the battery voltage is greater than the set constant voltage charging voltage

66.7%, the charger enters the constant current charging mode, and the charging current is set by the internal 200mV reference voltage and an external resistor RCS, that is, charging

The electric current is 200mV/RCS. When the battery voltage continues to rise close to the constant voltage charging voltage, the charger enters the constant voltage charging mode, and the charging current gradually

When the charging current decreases to 9.5% of the set constant current charging current, it enters the charging end state, and the charging current is zero at this time.

CN3722 has two status indication pins, namely the charging status indication pin and the charging through distribution pin. In trickle charge state.

DONE

State, constant current charging state and constant voltage charging state, the internal transfeld by the open-drain output pin is turned on, and the output is low level; the other the internal transistor of the open-drain output pin is turned on, and the output is low level; the open-drain output pin is turned on, and the output is low level; the open-drain transistor of the open-drain output pin is turned off, and the output is in a high-impedance state; the transistor inside the other open-drain pin is turned on, output low level to indicate the charging end status.

At the end of charging, if the input power is disconnected and then reconnected, a new charging cycle will start; if the battery voltage drops

When it reaches the recharging threshold (95.8% of the constant voltage charging voltage), it will automatically start a new charging cycle.

CN3722 uses the constant voltage method to track the maximum power point of the solar cell, and the maximum power point voltage is divided by two resistors and then sent to MPPT pin, in the maximum power point tracking state, the MPPT pin voltage is modulated at 1.04V, and the MPPT pin modulation voltage has a -0.4% ÿ

The temperature coefficient is very consistent with the temperature coefficient of the maximum power point voltage of the solar cell.

When the input voltage fails, CN3722 automatically enters the sleep mode, and the internal circuit is turned off, which can reduce the current consumption of the battery.

Extend standby time.

In order to monitor the battery temperature, a 10kÿ negative temperature coefficient thermistor needs to be connected between the TEMP pin and the GND pin. like

If the battery temperature is outside the normal range, the charging process will be suspended until the battery temperature returns to the normal temperature range.

There is also an overvoltage comparator inside CN3722. When the BAT pin voltage rises due to load changes or sudden removal of the battery, etc.,

If the BAT pin voltage rises to 1.08 times of the constant voltage charging voltage, the overvoltage comparator will act and turn off the off-chip P-channel MOS field effect crystal tube, the charger is temporarily stopped until the BAT pin voltage returns to below the constant voltage charging voltage. In some cases, such as when the battery is not connected Connected to the charger, or the battery is suddenly disconnected, the voltage of the BAT pin may reach the overvoltage protection threshold. This is normal.

The schematic diagram of charging current and charging voltage is shown in Figure 2.

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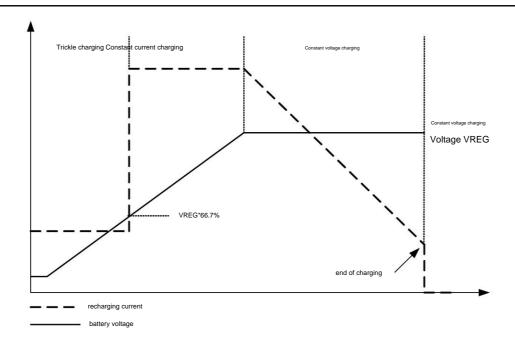


Figure 2 Schematic diagram of the charging process

application information

Under voltage lockout (UVLO) The low

voltage latch circuit inside the chip monitors the input voltage. When the input voltage is lower than 6V (typical value), the internal circuit is shut down, and the charger does not

Constant voltage charging voltage setting

As shown in Figure 1, the voltage at the battery terminal is fed back to the FB pin through a resistor divider network composed of resistors R6 and R7.

voltage determines the state of charge. When the voltage of the FB pin is close to 2.416V, the charger enters the constant voltage charging state. In the constant voltage charging state, the charging

The current gradually decreases and the battery voltage remains constant.

Considering the bias current flowing into the FB pin, the voltage corresponding to the battery terminal in the constant voltage charging state is:

VBATÿ2.416x(1ÿR7ÿR6)ÿIBxR7

Among them, IB is the bias current of the FB pin, and its typical value is 50nA

It can be seen from the above formula that the bias current of the FB pin causes an error in the voltage division result of the resistor voltage divider network, and the error value is IBxR7. Suppose R7= 500Kÿ, then the error value is about 25 millivolts. Therefore, when designing the resistor divider network, the above errors should be taken into account.

The adjustable constant voltage charging voltage should be less than 25V.

Since resistors R6 and R7 will consume a certain amount of current from the battery, when selecting the resistance value of R6 and R7, it should be based on the allowable current consumption.

Select the value of R6 + R7, and then calculate the values of R6 and R7 respectively according to the above formula.

Solar Cell Maximum Power Point Tracking

CN3722 uses constant voltage method to track the maximum power point of solar cells. In the volt-ampere characteristic curve of the solar cell, when the ambient temperature is constant

, under different sunlight intensities, the output voltage corresponding to the point of maximum output power is basically the same, that is, as long as the solar cell's

The output terminal voltage is a constant voltage, which can ensure that the solar cell can output the maximum power when the light intensity is different under this temperature. But when

When the ambient temperature changes, the voltage corresponding to the maximum power point of the solar cell changes with the temperature roughly according to the temperature coefficient of -0.4%/ÿ. When the ambient temperature is 25°C, the voltage of the MPPT pin at the maximum power point tracking end of the CN3722 solar cell is modulated at 1.04V, and its temperature depends on

 $The value is -0.4\%/\bar{y}, and the voltage divider network composed of two off-chip resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the maximum solar cell resistors (R3 and R8 in Figure 1) can realize the resistors (R3 and R8 in Figure 1) can realize the resistors (R3 and R8 in Figure 1) can realize the realize the realized (R3 and R8 in Figure 1) can realize the realized (R3 and R8 in Figure 1) can realize the realized (R3 and R8 in Figure 1) can realize the realized (R3 and R8 in Figure 1) can realize the realized (R3 and R8 in Figure 1) can realize the realized (R3 and R8 in Figure 1) can realize the realized (R3 and R8 in Figure 1) can realize the realized (R3 and R8 in Figure 1) can reali$ 

Power points are tracked. This maximum power point tracking method is very suitable for situations where the temperature difference between the four seasons is relatively large or the daily temperature difference is relatively large. At 25°C, the maximum power point voltage of the solar cell is determined by the following formula:

VMPPTÿ1.04×(1ÿR8ÿR3)

Powering the CN3722 with an adapter and a solar cell Both an

adapter and a solar cell can be used to power the CN3722, because the adapter usually has a relatively large current output capability and can charge the battery quickly. In this case, the charging current of CN3722 can be set according to the output current capability of the adapter. When the solar battery is used for power supply, even if the output power of the solar battery is small, CN3722 can automatically track the maximum power point of the solar battery and set the charging current current adjusted to the maximum power point. It should be noted that the output voltage of the adapter should be greater than the set maximum power point voltage of the solar battery, otherwise the adapter cannot charge the battery normally. Trickle charging is

in the charging

state, if the battery voltage is lower than 66.7% of the set constant-voltage charging voltage, the charger enters the trickle charging mode, and the charging current is 15% of the set constant-current charging current. Charging current

setting The constant

current charging current is determined by the following formula:

$$ICH = \frac{200mV}{RCS}$$

in:

ICH is the constant charge current

RCS is the charging current detection resistor connected between the CSP pin and the BAT pin. The

charging ends

in the constant voltage charging state, and the charging current gradually decreases. When the charging current decreases to 9.5% of the set constant current charging current, CN3722 enters the charging end state, at this time, the DRV pin outputs a high level, and the charging

After automatic recharging, if the input power and the battery are still connected to the charger, the battery voltage will gradually drop due to battery self-discharge or load. When the battery voltage drops to 95.8% of the set constant voltage charging voltage, A new charge cycle will start, which will keep the battery above 90% full. Battery Temperature Monitoring In order to monitor the

temperature of the

battery, a thermistor with a negative temperature coefficient close to the battery is required. When the battery temperature exceeds the acceptable range, charging will be temporarily stopped until the battery temperature returns to the normal range. A thermistor with a

negative temperature coefficient should be connected between the TEMP pin and ground. Inside the chip, the TEMP pin is connected to the input terminals of two comparators, and its low voltage threshold is 175 millivolts, corresponding to the upper limit temperature point of the normal temperature range; the high voltage threshold is 1.6 volts, corresponding to the lower limit temperature point of the normal temperature range.

The pull-up current of the TEMP pin is 50uA, so the thermistor value of the negative temperature coefficient should be 10kÿ at 25°C, and its resistance value should be about 3.5kÿ at the upper limit temperature point (corresponding to about 50°C); at the lower limit temperature Its resistance value should be about 32kÿ (corresponding to about 0°C) at the point. Some NTC thermistors, such as TH11-3H103F, MF52 (10 kÿ), QWX-103 and NCP18XH103F03RB, etc., can be used with CN3722. The models of thermistors with negative temperature coefficients listed above are for reference only, and users can choose appropriate models according to specific needs. If the value

of the negative temperature coefficient thermistor at the upper limit temperature point and the lower limit temperature point is slightly larger than 3.5 kỹ and 32 kỹ, the user can move the normal operating temperature range down by connecting an ordinary resistor in parallel with the thermistor; otherwise, it can be A common resistor in series with the thermistor shifts the normal operating

temperature range up. If the battery temperature monitoring function is not used, just connect a 10Kÿ resistor between the TEMP pin and the ground, status indication

The CN3722 has two open-drain status indication outputs: pin and the pin is in high state, constant current charging state and constant voltage charging state, the pin is pulled to low level by the internal transistor, and the pin is in high impedance states. In the charging end state, the pin is DONE pulled down to low level by the internal transistor, and in other states, the pin states, the pin states.

When the battery is not connected to the charger, CN3722 will charge the output capacitor to the constant voltage charging voltage and enter the charging end state. Due to the discharge effect of the working current of the BAT pin on the output capacitor, the voltage of the BAT pin will slowly drop to recharge threshold, CN3722 enters charging again

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In this way, a sawtooth waveform is formed on the BAT pin, and a pulse signal is output at the same property indicate that no battery is installed.

When the status indication function is not used, connect the unused status indication pin to ground.

Table 1 lists the status of the charger corresponding to the two status indication ports. Here it is assumed that the red LED is connected to the pin and on the preduction of the charger corresponding to the two status indication ports.

DONE The pins are connected as shown in Figure 1.

CHRG Pin low	DONE Pin high-	status description
level (red LED on) high impedance	impedance state (green LED off) low	Charge
state (red LED off) pulse signal	level (green LED on) pulse signal	end of charging
		no battery connected
		four possible scenarios
		ÿ The VCC pin voltage is lower than the low-voltage lock
High impedance state (red LED off)	High impedance state (green LED off)	storage voltage, or
		ÿ The VCC pin voltage is lower than the BAT tube
		pin voltage
		ÿ The battery temperature is abnormal

#### Table 1 Description of status indication

Off-chip power tube driver

The DRV pin of CN3722 is used to drive the gate of the off-chip MOS field effect transistor. This pin can provide relatively large transient current to quickly connect

On and off off-chip MOS field effect transistor. Rise and fall times are typically 40nS when driving a 2nF load. Generally come

In other words, the equivalent capacitance of a MOS field effect transistor with an on-resistance of 50 milliohms is about 2nF.

There is a clamping circuit inside CN3722 to ensure that the low level of DRV pin is 8V (maximum value) lower than the voltage of VCC pin. For example, assuming VCC's

The voltage is 20V, then the low level of the DRV pin is a minimum of 12V. In this way, some low-voltage P-channel MOS field effect

Transistors can be used with CN3722, which improves the working efficiency of the charger.

loop compensation

In order to ensure the stability of the current modulation loop and the voltage modulation loop, the following loop compensation components are required:

- (1) Connect a 470pF capacitor from COM1 pin to ground
- (2) Connect a 120ÿ resistor and a 220nF ceramic capacitor in series from COM2 to ground
- (3) Connect a 100nF ceramic capacitor from COM3 to ground
- (4) The value of capacitor C7 in Figure 1 is roughly estimated according to the right formula: C7=8x(R6/R7) (pF) Battery connection check

CN3722 has no battery connection check function. When the battery is not connected to the charger, the CN3722 charges the output capacitor as a battery to a constant voltage

After charging the voltage, it enters the charging end state. Due to the discharge effect of the working current of the BAT pin on the output capacitor, the voltage of the BAT pin will be

Slowly drop to the recharge threshold, CN3722 enters the charging state again, the charger will cycle between the charging state and the charging end state, this

A sawtooth waveform is formed on the BAT pin, and a pulse signal is output at the time to indicate that no battery is installed. When the battery is connected to the BAT pin of the

When the external capacitor is 10 uF, the pulse frequency is about 4Hz.  $\label{eq:helpower}$ 

It is best not to connect the battery to the charger while the charger is running, otherwise the charger may sink a large current into the battery for a short time.

Input and Output Capacitance

The input capacitor acts as a filter for the input power supply and needs to absorb the ripple current generated on the input power supply, so the input capacitor must have sufficient

rated ripple current. In the worst case, the rated RMS ripple current of the input capacitor needs to be half of the charging current.

For the selection of the output capacitor, in order to reduce the ripple voltage at the output terminal and improve the transient characteristics, the series equivalent resistance (ESR) is mainly considered. Generally come In other words, an output capacitor of 10uF can meet the requirements.

Inductor selection

During normal operation, the transient inductor current varies periodically. During the conduction period of the P-channel MOS field effect transistor, the input voltage charges the inductor

Electricity, the inductor current increases; during the off period of the P-channel MOS field effect transistor, the inductor discharges to the battery, and the inductor current decreases. Inductor Ripple

Current increases with decreasing inductance value and increases with increasing input voltage. Larger inductor ripple current will result in larger ripple charge

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Electrical current and magnetic losses. So the ripple current of the inductor should be limited within a reasonable range.

The ripple current of the inductor can be estimated by the following equation

$$\triangle I_L = \frac{1}{(f)(L)} V_{BAT} (1 - \frac{V_{BAT}}{VCC})$$

in

f is the switching frequency, 300KHz

L is the inductance value

VBAT battery voltage

VCC is the input voltage

When selecting the inductance value, the inductor ripple current can be limited to ÿIL=0.4xICH, where ICH is the charging current. Please pay attention to the maximum inductor ripple current ÿIL appears at the maximum value of the input voltage and the minimum value of the inductance. Therefore, when the charging current is low, a larger inductance value should be selected.

For the selection of inductance value, please refer to Table 2:

recharging current	Input voltage	Inductance value
40	>20V	40uH
1A	<20V	30uH
2a	>20V	30uH
Zd	<20V	20uH
3A	>20V	20uH
	<20V	15uH
4A	>20V	15uH
4/\(\frac{4}{\tau}\)	<20V	10uH
5A	>20V	10uH
	<20V	8uH

Table 2 Selection of inductance value

#### MOSFET selection

The application circuit of CN3722 needs to use a P-channel MOS field effect transistor. When selecting the MOS field effect transistor, the conversion should be considered Efficiency, MOS field effect transistor power dissipation, and maximum temperature.

Inside the chip, the gate drive voltage is clamped at 5.8V (typical value), and a P-channel MOS field effect transistor with a low turn-on voltage can be used. Place It should be noted that the breakdown voltage BVDSS of the MOS field effect transistor is greater than the highest input voltage.

Factors to be considered when selecting a P-channel MOS field effect transistor include on-resistance Rds(on), total gate charge Qg, reverse conduction capacitance CRSS, input voltage and maximum charge current.

The maximum power dissipation of a MOS field effect transistor can be approximated by the following formula

$$Pd = \frac{VBAT}{VCC} \times Rds(on) \times ICH^2 \times (1+0.005dT)$$

in:

Pd is the power dissipation of the MOS field effect transistor

VBAT is the highest voltage of the battery

VCC is the minimum input voltage

Rds(on) is the on-resistance of the P-channel field effect transistor at room temperature (25°C)

ICH is the charging current

dT is the temperature difference between the actual temperature of the P-channel MOS field effect transistor and room temperature (25°C)

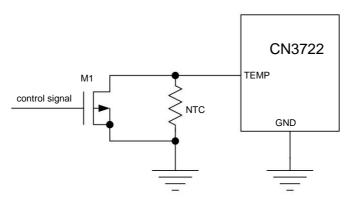
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In addition to the conduction loss described by the previous formula  $\hat{l}$  In addition to Rds(on), the MOS field effect transistor also has switching loss, and the switching loss increases with the increase of the input voltage. Generally speaking, when the input voltage is less than 20V, the conduction loss is greater than the switching loss, and the MOS field effect transistor with a relatively small conduction resistance should be given priority; when the input voltage is greater than 20V, the switching loss is greater than the conduction loss, and the reverse transistor should be given priority A MOS field effect transistor with a relatively small conduction capacitance CRSS. Generally, the value of CRSS is listed in the technical specifications of MOS field effect transistors. If the capacitance value is not clearly listed, it can be estimated by the formula CRSS = QGD/i/VDS. Many types of MOS field effect transistors, such as AO4459, STM9435 (or WT9435) and AO3407A,

can be used. The models of MOS field effect transistors listed above are for reference only, and users need to select suitable models according to specific requirements. Diode selection Diodes D1 and D2 in the typical application circuit Figure 1 are Schottky diodes. The current passing capability of these two diodes must be at least greater than the charging current; the withstand voltage of the diodes must be greater.

than the minimum input voltage requirement. When the charging current is relatively large, the diode will have relatively large power consumption, so full consideration should be given to the heat dissipation of the diode. The selection principle of diodes D1 and D2 is sufficient. If the current passing capacity or withstand voltage of the selected diodes is far beyond the required value, since such diodes have high junction capacitance, it will increase the switching loss of the charger. Reduce

efficiency. Use the TEMP pin to realize the charging prohibition function Use the TEMP pin to realize the charging prohibition function, as shown in Figure 3:



Note: M1 is an N-channel field effect transistor

Figure 3 Use the TEMP pin to realize the charging prohibition function

When the control signal is at a high level, M1 is turned on, the TEMP pin is at a low level, and charging is prohibited; when the control signal

is at a low level, M1 is turned off, and the voltage of the TEMP pin is determined by the NTC resistance value, and the normal battery temperature monitoring. About battery current in sleep mode In the typical application circuit shown in Figure 1, when the

input voltage is powered off or the input voltage is lower than the battery voltage, CN3722 enters sleep mode. The current consumed by the battery in sleep mode includes: (1) The current flowing into the BAT pin and the CSP pin, about 10uA (VBAT=12V) (2) The current flowing

from the battery terminal to the input voltage terminal through the diode D1, which is determined by The leakage current of diode

D1 determines the

(3) The current flowing from the battery

This current charges the capacitor C1 at the input terminal, and the voltage at the input terminal will increase to a certain extent. In order to avoid misoperation, a resistor can be connected in parallel with capacitor C1 to release the leakage current of diode D1 through the resistor. The resistance value depends on the leakage current of diode D1. Generally, a resistance of about 20Ký can meet the requirements.

terminal to the ground (GND) through the diode D2. This current is determined by the leakage current of the diode D2. Considerations for PCB Design In order to ensure

and improve the conversion efficiency, the following should be considered when designing the PCB A few points: (1) In order to ensure the lowest possible electromagnetic

radiation, the leads of the two diodes, P-channel MOS field effect transistor, inductor and input filter capacitor should be as short as possible. The distance from the positive electrode of the input capacitor to the P-channel MOS field effect transistor should also be as short as possible. (2) The ground terminals of the loop compensation components on the COM1.

COM2 and COM3 pins should be connected to the analog ground (GND) of CN3722, so as to avoid

Avoid switching noise affecting the stability of the loop.

- (3) Since the maximum power point tracking voltage of CN3722 is related to the ambient temperature, in order to make CN3722 truly reflect the ambient temperature, when designing the PCB, CN3722 needs to keep a certain distance from some heating devices, such as off-chip MOF transistors, diodes, etc.
- (4) The ground terminal of the output capacitor and the ground terminal of the input capacitor must be connected to the same piece of copper and then returned to the ground terminal of the
- system. (5) The analog ground and the ground that flows through the large current (power ground) should return to the system ground alone.
- (6) The GND pin and PGND pin of CN3722 also have the function of heat dissipation, so the ground copper area should be as large as possible. This is especially important when the input voltage is relatively high or the gate capacitance of the off-chip P-channel MOS field effect transistor is relatively large. (7) Put the charging current detection
- resistor RCS close to the output end of the inductor, and its placement direction should ensure that the connection from the chip's CSP pin and BAT pin to RCS is relatively short. The connection between CSP pin and BAT pin and RCS should be on the same level, and the distance should be as small as possible. (8) In order to ensure the detection

accuracy of the charging current, the CSP pin and the BAT pin should be directly connected to the charging current detection resistor. As shown in Figure 4.

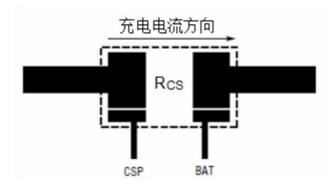
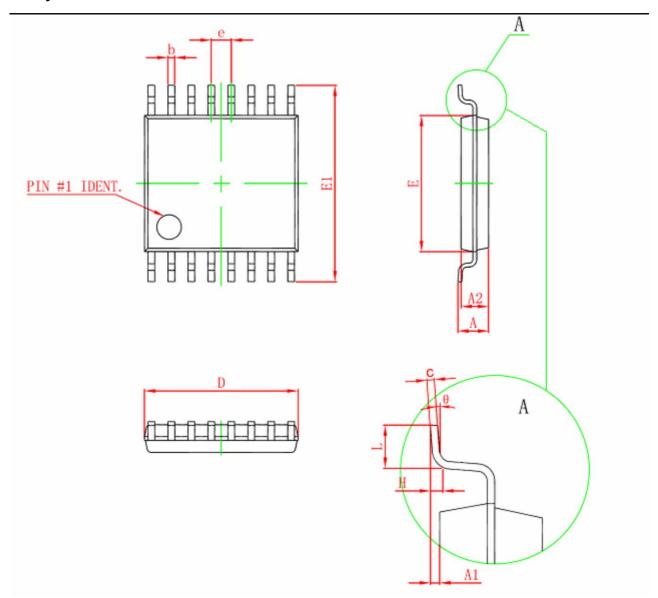


Figure 4 Detection of charging current

Package information



Symbol	Dimensions In Millimeters		Dimensions	In Inches	
Symbol	Min	Max	Min	Max	
D	4.900	5.100	0.193	0.201	
E	4. 300	4.500	0.169	0.177	
b	0.190	0.300	0.007	0.012	
С	0.090	0.200	0.004	0.008	
E1	6. 250	6.550	0.246	0.258	
A		1.100		0.043	
A2	0.800	1.000	0.031	0.039	
Al	0.020	0.150	0.001	0.006	
e	0.65 (BSC)		0. 026 (BSC)		
L	0.500	0.700	0.020	0. 028	
Н	0. 25	(TYP)	0. 01 (TYP)		
θ	1 °	7°	1°	7°	

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