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Layer Assignment for Maximizing The Reliability of 3D ICs

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ABSTRACT

In the design of a three-dimensional integrated circuit (3D IC), the task of layer assignment is to assign each functional unit to a layer that can accommodate it. In a 3D IC, through silicon vias (TSVs) are used to communicate signals between different layers. To improve the reliability of a 3D-IC, previous layer assignment works concentrate on minimizing the number of TSVs to reduce the risk of the defect occurred in the manufacturing process. However, the risk in the fabricating process of a TSV is also related to the length of this TSV. Based on this observation, in this paper, we propose an integer linear programming (ILP) approach to maximize the reliability of TSVs during the layer assignment stage. Compared with the previous work (that does not take the reliability of TSVs into account), experimental results show that our approach can greatly increase the reliability under the same number of TSVs .

INTRODUCTION

Three-dimensional (3D) integrated circuit (IC) [1-4] is a chip in which two or more layers of active electronic components are integrated vertically into a single circuit. Because of the reduction of wire length, the 3D IC technology can improve the circuit speed and reduce the power consumption. Thus, as the design size continues to increase, the design of 3D IC has become an important industry trend. Note that, in a 3D IC, through silicon vias (TSVs) are used to communicate signals between different layers. Since the defects may be introduced during the manufacturing of TSVs, the implementation of TSVs has a great impact on the reliability of a 3D IC.

To improve the reliability of a 3D IC, previous works [5-10] concentrate on the reduction of the number of TSVs to minimize the risk of the defects occurred in the manufacturing process. However, in fact, the risk of the defects during the manufacturing of a TSV is also related to the length of this TSV (i.e., the number of layers that this TSV passes through). For example, suppose that TSV T1 passes through two layers and TSV T2 passes through three layers. Then, the risk of the defects during manufacturing TSV T1 should be smaller than the risk of the defects during manufacturing TSV T2. In other words, the reliability of TSV T1 (for implementing TSV T1) should be larger than the reliability of TSV T2 (for implementing TSV T2). Thus, in addition to minimize the number of TSVs, the lengths of TSVs should also be taken into account for further improving the reliability of a 3D IC.

In the design of a 3D IC, the task of layer assignment [5-10] is to assign each functional unit to a layer that can accommodate this functional unit (under the constraint on the number of layers and the constraint on the footprint area). It is recognized that the layer assignment result has a great impact on the implementation of TSVs. Therefore, a lot of layer assignment algorithms have been devoted to the TSV count minimization problem for improving the reliability of a 3D IC. However, to the best of our knowledge, no attention has been paid to the lengths of TSVs. Since the lengths of TSVs also influence the reliability, there is a demand to consider the lengths of TSVs for further improving the reliability.

In fact, even two layer assignment results have the same number of TSVs, they still may have different reliabilities. Therefore, we are motivated to further improve the 3D IC reliability with the lengths of TSVs considered. In this paper, we propose an integer linear programming (ILP) approach to formally draw up this problem. Note that, different from previous works [5-10], our approach considers both the number of TSVs and the lengths of TSVs. Our objective is to maximize the reliability under the constraint on the number of layers, the constraint on the footprint area, and the constraint on the number of TSVs. Experimental results show that, in each test circuit, compared with the previous work [9], our approach can greatly enhance the reliability under the same design constraints.

The proposed ILP approach is based on the framework of the previous work [11], which attempts to minimize the temperature increase. Since our objective is different from the previous work [11], we make modifications to their ILP formulations for the new problem formulation (i.e., maximize the reliability under the constraint on the number of layers, the constraint on the footprint area, and the number of TSVs).

The main contributions of our work are elaborated below.
(1) Our approach considers both the number of TSVs and the lengths of TSVs. To our knowledge, our approach is the first work for maximizing the reliability with the lengths of TSVs considered.
(2) The proposed ILP approach guarantees solving this problem optimally. Benchmark data consistently show that, compared with the previous work [9], our approach can greatly improve the reliability under the same design constraints.

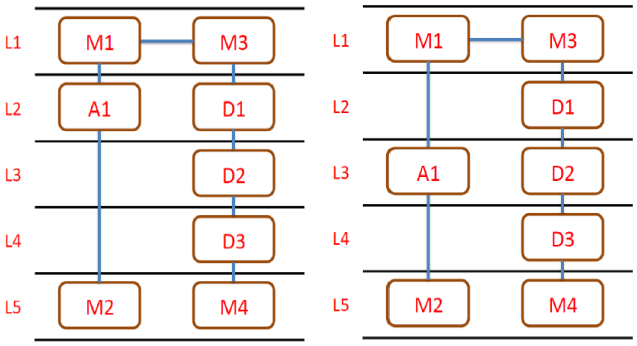
MOTIVATION

We use Figure 1 as an example to demonstrate the motivation. This 3D IC has 5 layers: L1, L2, L3, L4, and L5. This circuit has 8 functional units: one adder A1, four multipliers M1, M2, M3, and M4, and three dividers D1, D2, and D3. Table I gives the reliabilities of different TSV lengths. If a TSV passes through 2 layers, its reliability is 0.99; if a TSV passes through 3 layers, its reliability is 0.95; and so on. Note that the layer assignment shown in Figure 1(a) and the layer assignment shown in Figure 1(b) have the same number of TSVs. Based on Table I, we analyze the reliabilities of these two

layer assignments as below.

(1) *The layer assignment shown in Figure 1(a)*. In this layer assignment, five TSVs pass through 2 layers and one TSV passes through 4 layers. Therefore, the reliability is $0.80 \times 0.99 \times 0.99 \times 0.99 \times 0.99 \times 0.99 = 0.761$.

(2) *The layer assignment shown in Figure 1(b)*. In this layer assignment, four TSVs pass through 2 layers and two TSVs pass through 3 layers. Therefore, the reliability is $0.95 \times 0.95 \times 0.99 \times 0.99 \times 0.99 \times 0.99 = 0.867$.



(a) (b)

Figure 1: Motivational example.

Table I. The reliabilities of different TSV lengths.

#Layers	Reliability
2	0.99
3	0.95
4	0.80

In this example, we find that even if two 3D ICs have the same number of TSVs, they still may have different reliabilities. Therefore, we are motivated to further improve the 3D IC reliability with the lengths of TSVs considered. In this paper, we propose an integer linear programming (ILP) approach to formally draw up this problem. Note that, different from previous works [5-10], our approach considers both the number of TSVs and the lengths of TSVs.

THE PROPOSED APPROACH

In this part, we use ILP to formally draw up the problem of layer assignment for maximizing the reliability of 3D ICs. Under the constraint on the number of layers, the constraint on the footprint area, and the constraint on the number of TSVs, our objective is to maximize the reliability.

Note that our ILP approach is based on the framework of the previous work [11], which attempts to minimize the temperature increase. Since our objective is different from the previous work [11], here we make modifications to their ILP formulations for the new problem formulation (i.e., to maximize the reliability under the constraint on the number of layers, the constraint on the footprint area, and the number of TSVs).

Table II tabulates the definitions of the notations used in our ILP formulation.

Table II. The notations used in our ILP formulation.

Notation	Definition
$r_{k,l}$	A binary variable (i.e., 0-1 variable). If functional unit k is assigned to layer l, then $r_{k,l}=1$; otherwise, $r_{k,l}=0$.
R_{max}	An inetger constant that denotes the total number of functional units (resources).
D_l	A real-value constant that denotes the reliability of a TSV passes through l layers.
MINTSV	An integer variable that denotes the constraint on the number of TSVs.
L_{max}	An integer constant that denotes the total number of layers in the 3D IC.
A_{max}	An inetger constant that denotes the constraint on footprint area.
A_k	An inetger constant that denotes the area of functional unit k.
$High_{k1 \rightarrow k2}$	An integer variable. If the layer number of functional unit k1 is greater than the layer number of functional unit k2, then the value of $High_{k1 \rightarrow k2}$ is the layer number of functional unit k1; otherwise, the value of $High_{k1 \rightarrow k2}$ the layer number of functional unit k2.
$Low_{k1 \rightarrow k2}$	An integer variable. If the layer number of functional unit k1 is less than the layer number of functional unit k2, then the value of $Low_{k1 \rightarrow k}$ is the layer number of functional unit k1; otherwise, the value of $Low_{k1 \rightarrow k}$ the layer number of functional unit k2.
$V_{k1,k2}$	An integer variable that denotes the total number of TSVs (TSV count) between functional unit k1 and functional unit k2.
$R_{k1,k2,n}$	A binary variable (i.e, 0-1 variable). If the number of TSVs between functional unit k1 and functional unit k2 is n, then $R_{k1,k2,n}=1$; otherwise, $R_{k1,k2,n}=0$.

Next, we demonstrate the objective function and the constraints. Our objective is to maximize the reliability of a 3D IC. To formulate the objective function in a linear form, here we use the log function for the claculation of the reliability. For example, the reliability of the layer assignment shown in Figure 1(a) is estimated to be log(0.80)+log(0.99)+log(0.99)+ log(0.99)+log(0.99)+log(0.99), and the reliability of the objective function for the layer assignment shown in Figure 1(b) is estimated to be log(0.95)+log(0.95)+ log(0.99)+log(0.99)+log(0.99)+log(0.99).

Therefore, the objective function is:

$$\text{Maximize } \sum_{k=1}^{R_{MAX}}((\sum_{l=0}^{L_{MAX}} \log(D_l) \times (\sum_{l=0}^{L_{MAX}} R_{k1,k2,l}))$$

In addition to the objective function, we have 11 formulas (constraints) in our ILP approach. In the following, we describe these 11 formulas.

Each functional unit must be assigned to one and only one layer. Therefore, for each functional unit k, we have the following constraint:

$$\sum_{l=1}^{L_{MAX}} r_{k,l} = 1$$

The summation of the areas of all the functional units at the same layer must be less than or equal to the footprint area. Therefore, for each layer l, we have the following constraint:

$$\sum_{k=1}^{R_{MAX}} A_k \times r_{k,l} \leq A_{MAX}$$

According to the previous work [11], the layer number of functional unit k1 and the layer number of functional unit k2 should be greater than or equal to the value of integer variable $Low_{k1\rightarrow k2}$. Therefore, we have the following two constraints:

$$Low_{k1\rightarrow k2} \leq \sum_{l=1}^{L_{MAX}} l \times r_{k1,l}$$

$$Low_{k1\rightarrow k2} \leq \sum_{l=1}^{L_{MAX}} l \times r_{k2,l}$$

According to the previous work [11], the layer number of functional unit k1 and the layer number of functional unit k2 should be smaller than or equal to the value of integer variable $High_{k1\rightarrow k2}$. Therefore, we have the following two constraints:

$$\sum_{l=1}^{L_{MAX}} l \times r_{k1,l} \leq High_{k1\rightarrow k2}$$

$$\sum_{l=1}^{L_{MAX}} l \times r_{k2,l} \leq High_{k1\rightarrow k2}$$

According to the previous work [11], the summation of the layer number of functional unit k1 and the layer number of functional unit k2 should be equal to the summation of the amount of $Low_{k1\rightarrow k2}$ and the amount of $High_{k1\rightarrow k2}$. As a result, we have the following constraint:

$$\sum_{l=1}^{L_{MAX}} l \times (1 - r_{k1,l}) + \sum_{l=1}^{L_{MAX}} l \times (1 - r_{k2,l}) + Low_{k1\rightarrow k2} + High_{k1\rightarrow k2} = 2 \times \sum_{l=1}^{L_{MAX}} l$$

According to the previous work [11], the integer variable $High_{k1\rightarrow k2}$ subtract the integer variable $Low_{k1\rightarrow k2}$ should be equal to the number of TSVs between functional unit k1 and functional unit k2. Therefore, we have the following constraint:

$$High_{k1\rightarrow k2} - Low_{k1\rightarrow k2} = V_{k1,k2}$$

The TSV count must satisfy the constraint on the number of TSVs Therefore, we have the following constraint:

$$\sum_{i=0}^{R_{MAX}}(\sum_{j=0}^{R_{MAX}} V_{i,j}) \leq MINTSV$$

The summation of binary variable $r_{k1,l}$ and $r_{k2,l}$ must be less than or equal to the summation of binary variable $R_{k1,k2,l}$ and 1. Thus, we have the following constraint:

$$r_{k1,l} + r_{k2,l} \leq R_{k1,k2,l} + 1$$

Since the number of TSVs between functional unit k1 and functional unit k2 must be only one value, the summation of binary variable Rk1,k2,l must equal to 1. Therefore, we have the following constraint:

$$\sum_{l=0}^{L_{MAX}} R_{k1,k2,l} = 1$$

EXPERIMENTAL RESULTS

We use Extended LINGO Release 13.0 (running on AMD Athlon CPU) as the solver of our ILP formulation. In the experiment, we use five test circuits, including CKT1, CKT2, CKT3, CKT4, and CKT5, to test the effectiveness of our approach. Table III tabulates the characteristics of these test circuits. The column Resources gives 3-tuple (#add, #mul, #div), where #add, #mul#, and #div denote the numbers of adders, the number of multipliers, and the number of divisors, respectively. The column #vias denotes the constraint on the number of TSVs.

Our experimental results are tabulated in Table IV. To verify the effectiveness of our approach, we compare our results with those of work [9] (that does not take the reliability into account). Note that, our experiments are under the constraint of the same total number of TSVs obtained by the previous work [9], which attempts to minimize the total number of TSVs under the constraint on footprint area and the constraint on the number of layers. The column Imp% denotes the percentage of the increase in the reliability. In each test circuit, our approach can further improve the reliability. For example, in circuit CKT1, compared with the previous work [9], our approach can increase 17.56% reliability; in circuit CKT2, compared with the previous work [9], our approach can increase 3.17% reliability; and so on. With an analysis, we find what, even if the total number of TSVs of each circuit is minimized (i.e., under the constraint of the same total number of TSVs obtained by the previous work [9]), the reliability still can be increased.

Table III. Characteristics of test circuits.

Circuit	Resources	#vias
I1	(1,6,2)	7
I2	(3,6,2)	7
I3	(5,10,3)	8
I4	(8,13,5)	9
I5	(6,11,7)	11

Table IV. Experiment results.

Circuit	Reliability		
	[9]	Ours	Imp%
I1	0.768476	0.903441	17.56%
I2	0.875694	0.903441	3.17%
I3	0.894406	0.922745	3.17%
I4	0.858269	0.913517	6.44%
I5	0.867841	0.895338	3.17%

CONCLUSIONS

In this paper, we demonstrate that TSV length has a great impact on the reliability of 3D ICs. Thus, we propose a layer assignment method to maximize the reliability under the constraint on the footprint area, the constraint on the number of layers, and the constraint on the number of TSVs. Compared with the previous work (that does not take the TSV reliability into account), experimental results show that our approach can greatly increase the reliability under all the same design constraints.

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