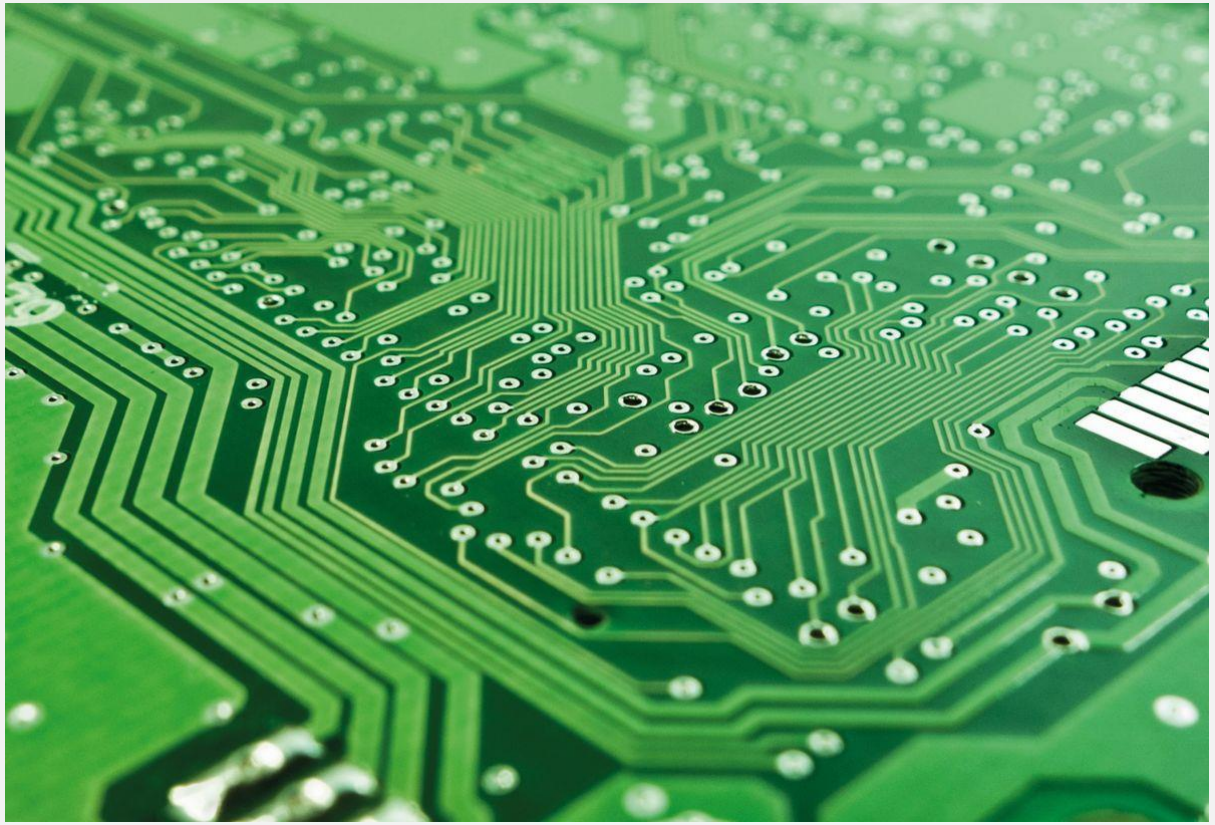
E7020e

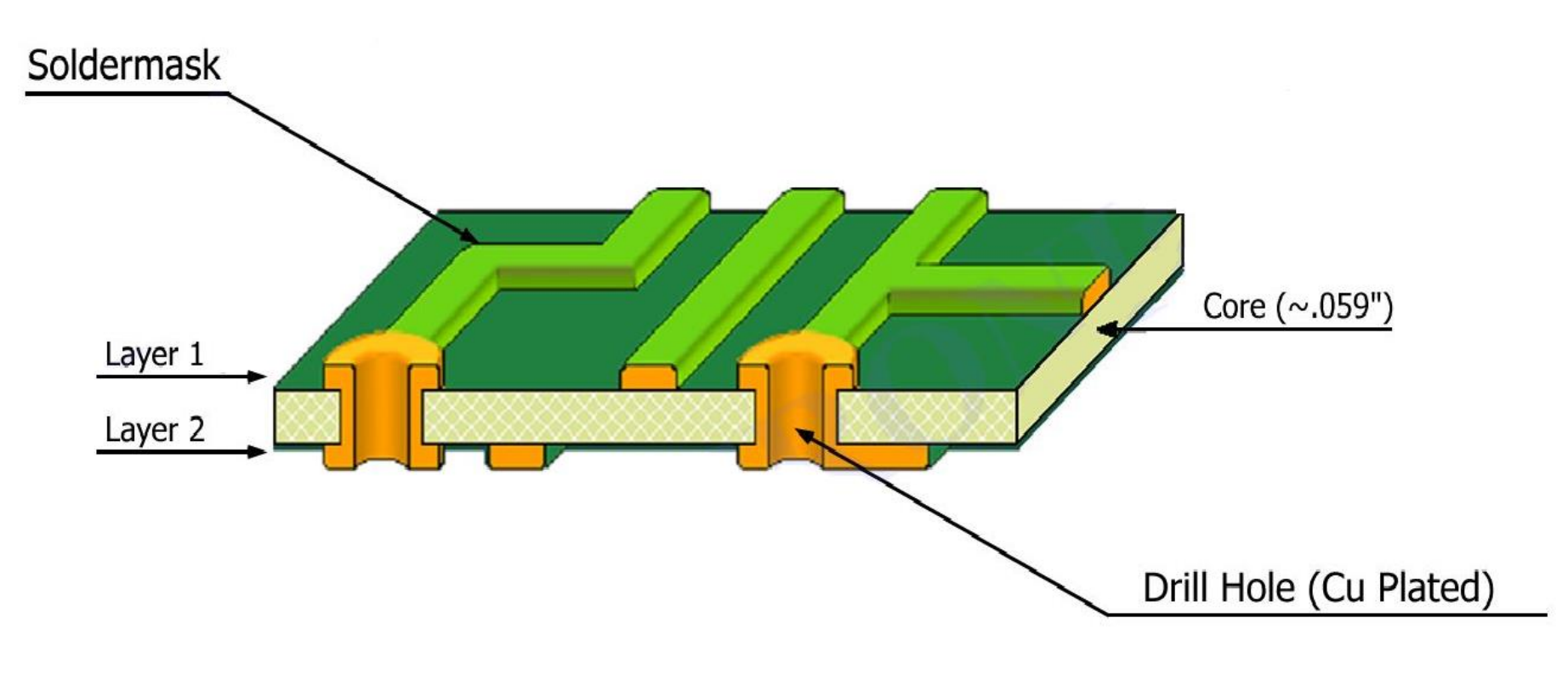
HARDWARE #3

PCB LAYOUT



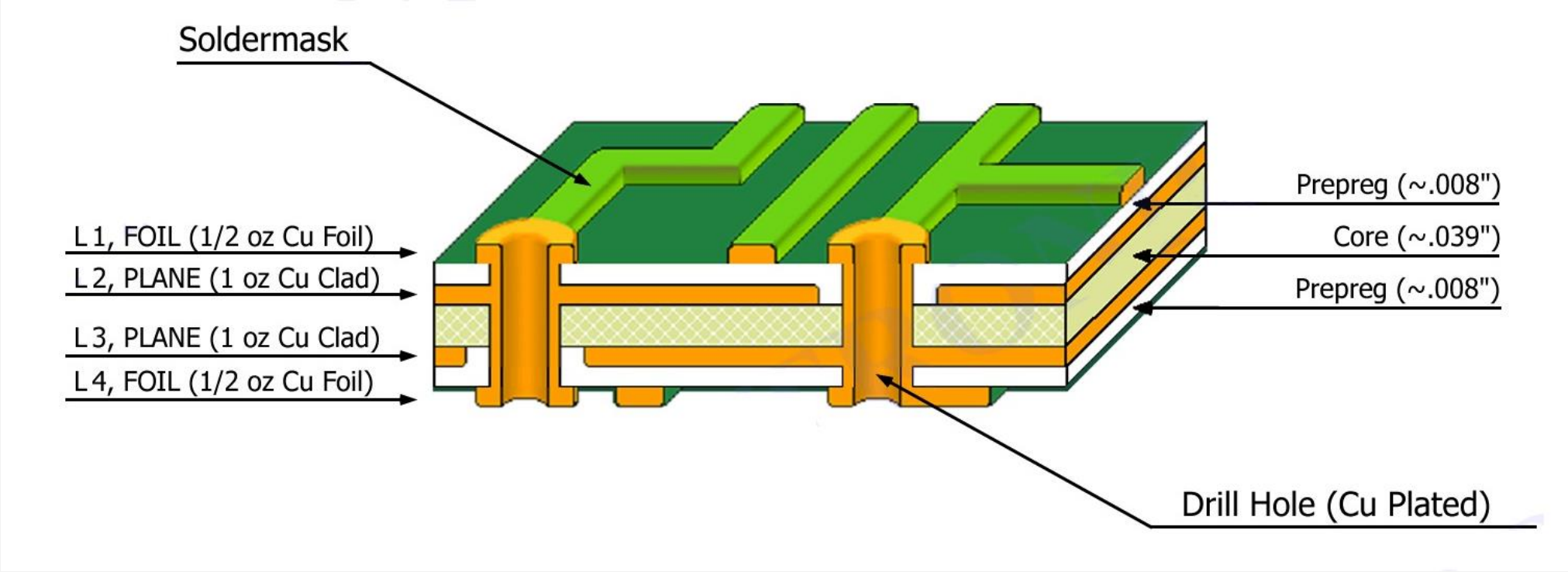
PCB PRINTED CIRCUIT BOARD

2-LAYER BOARD



PCB PRINTED CIRCUIT BOARD

4-LAYER BOARD

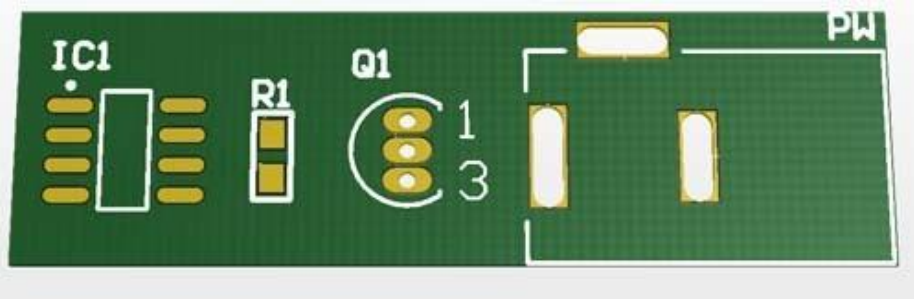


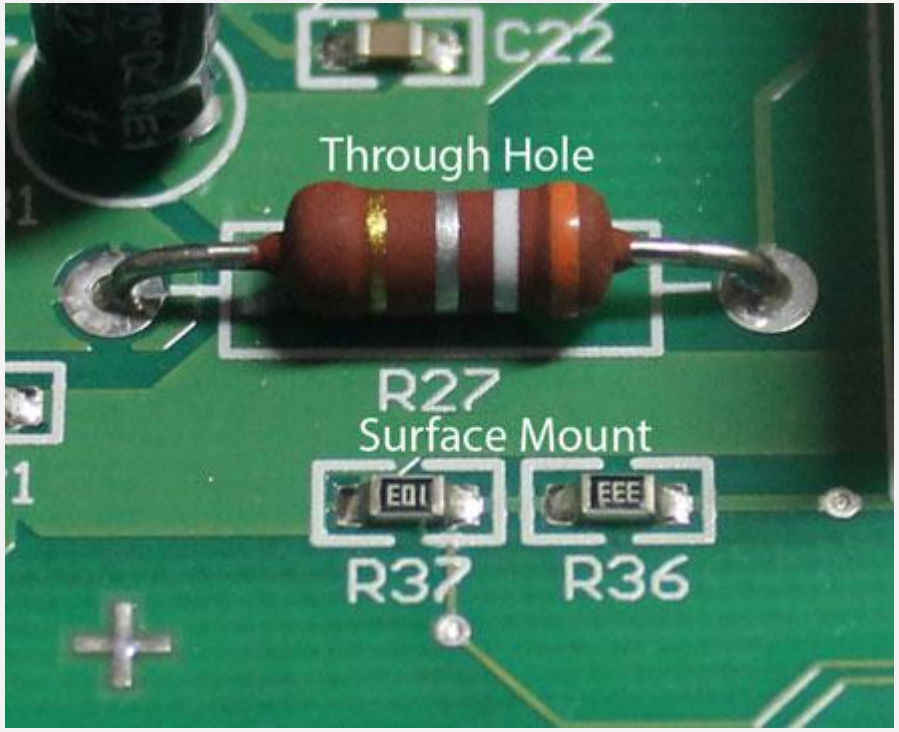
COMPONENT MOUNTING

THROUGH HOLE (TH)

SURFACE MOUNT (SMD)

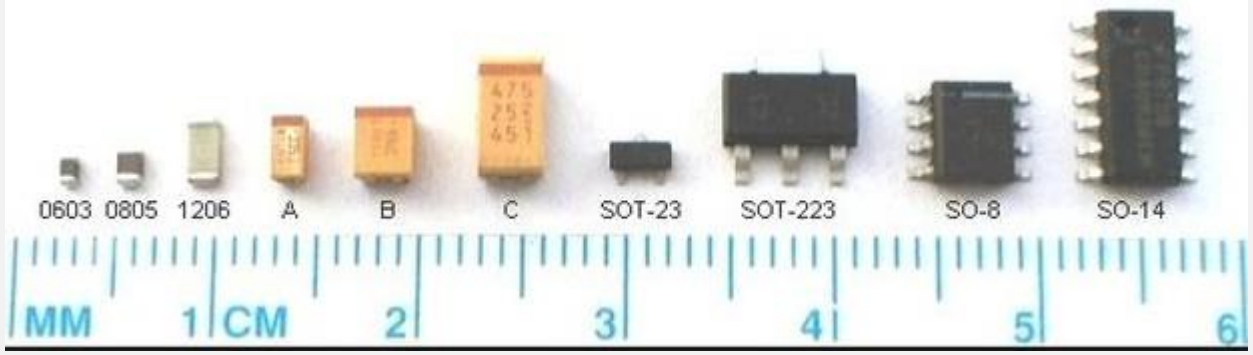
FOOTPRINT





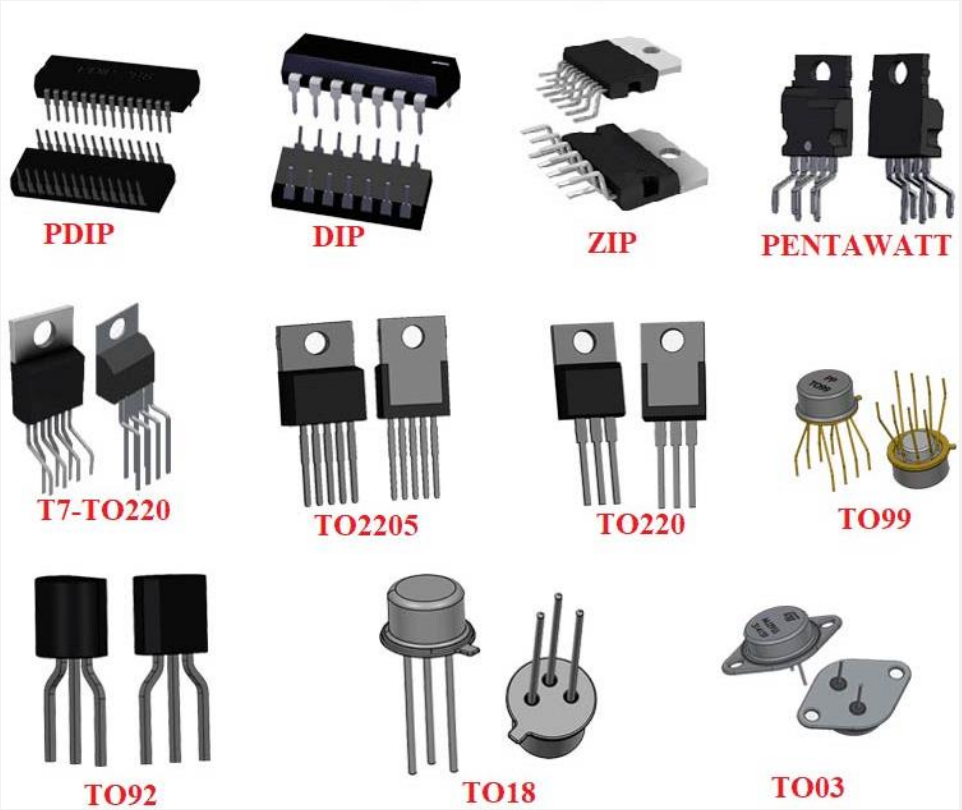
COMPONENT PACKAGES

SURFACE MOUNT



Size - design density
Assembly (hand? pick&place machine?)
Heat dissipation
Parasitics

THROUGH HOLE



SIGNALS

ELECTROMAGNETIC FIELDS

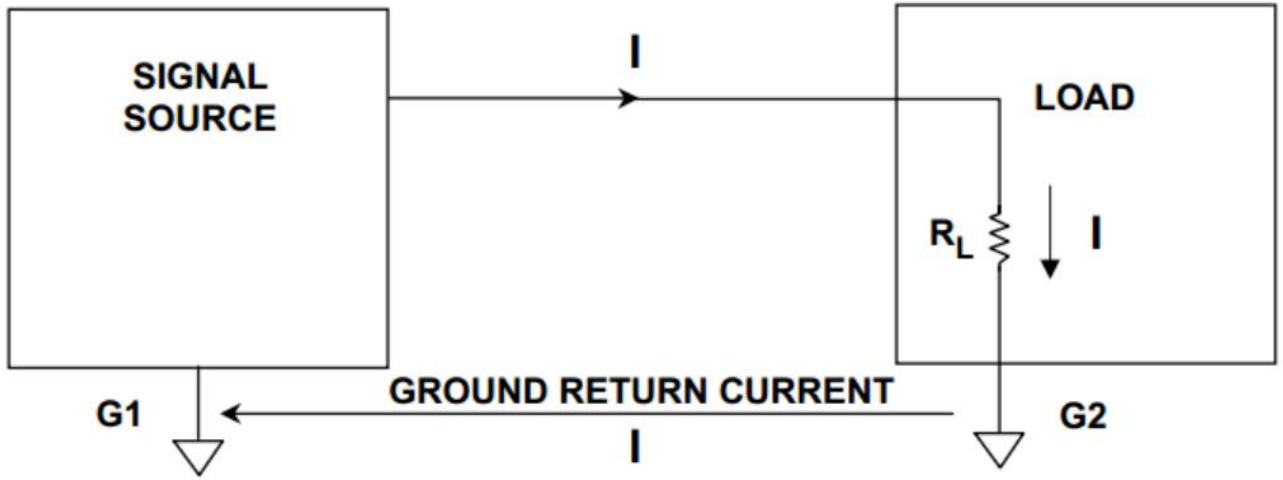
Travels IN THE PLASTIC between signal and return paths

→ Current flow in the copper traces (waveguides)
Voltage between signal and return paths

Propagates at speed of light of the dielectric material

~15cm/ns in FR4

SIGNALS

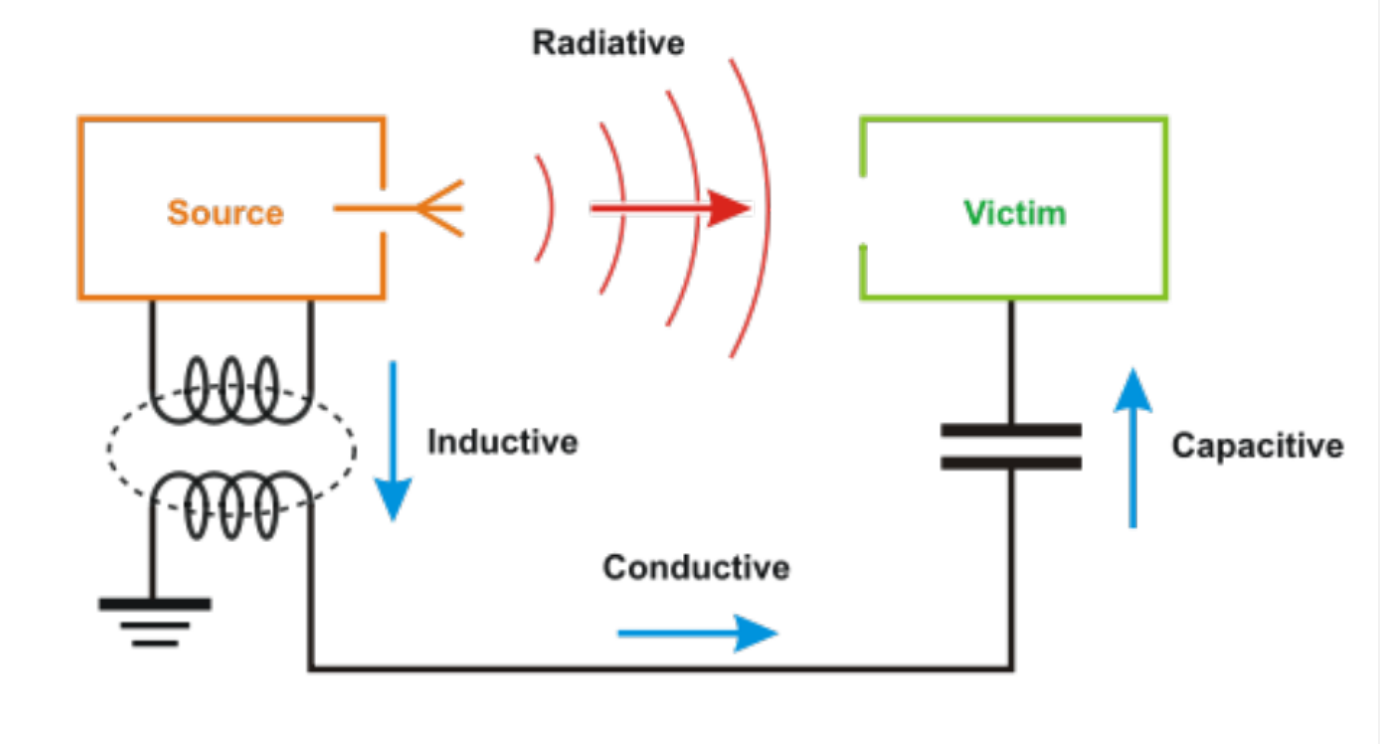


AT ANY POINT IN A CIRCUIT
THE ALGEBRAIC SUM OF THE CURRENTS IS ZERO
OR
WHAT GOES OUT MUST COME BACK
WHICH LEADS TO THE CONCLUSION THAT
ALL VOLTAGES ARE DIFFERENTIAL
(EVEN IF THEY'RE GROUNDED)

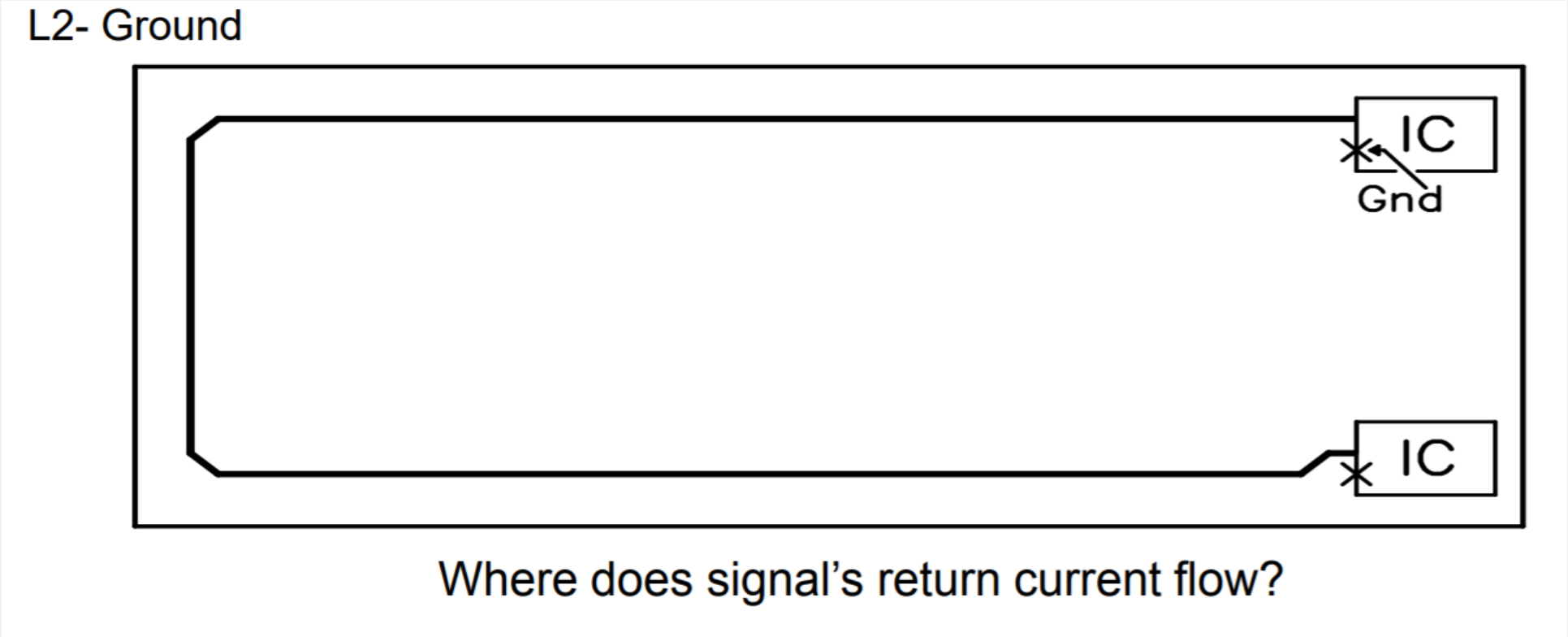
SIGNALS

Electromagnetic compatibility (EMC)

The physical layout will affect the system's emission and susceptibility



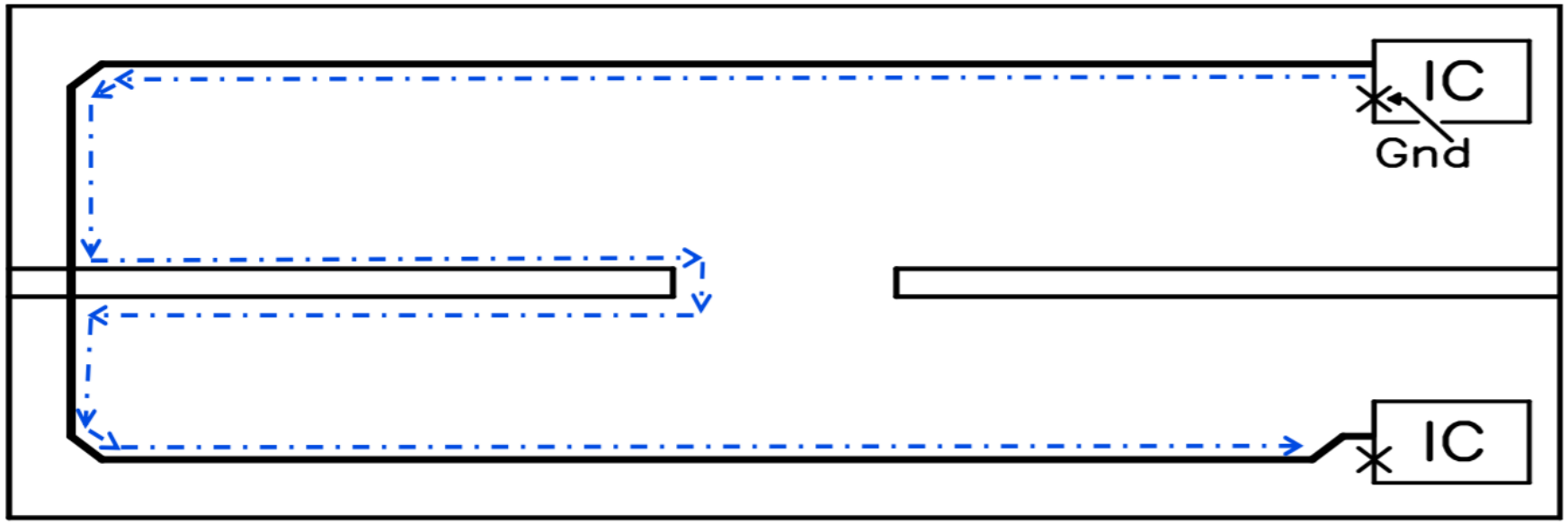
SIGNALS



SIGNALS

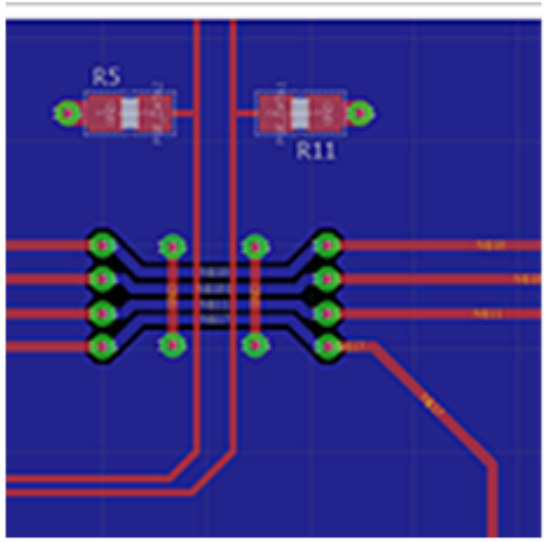
What happens if return plane is split?

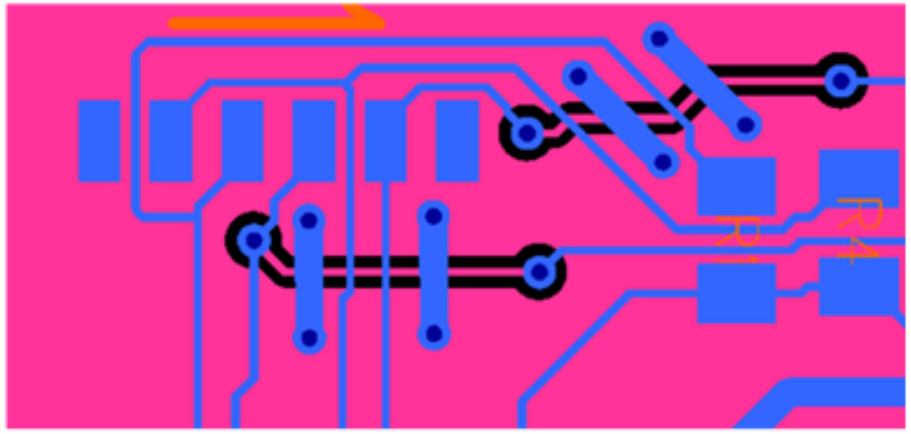
Now where does return current flow?



SIGNALS

If you must route across split – use return straps

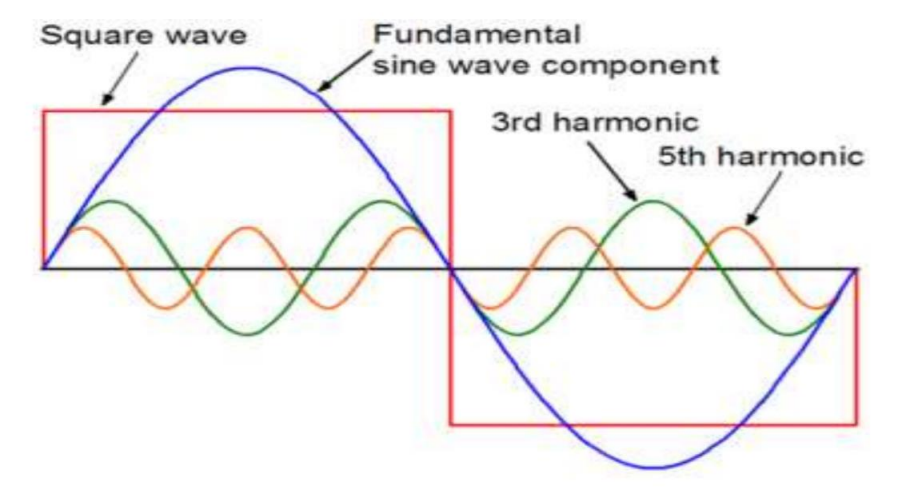


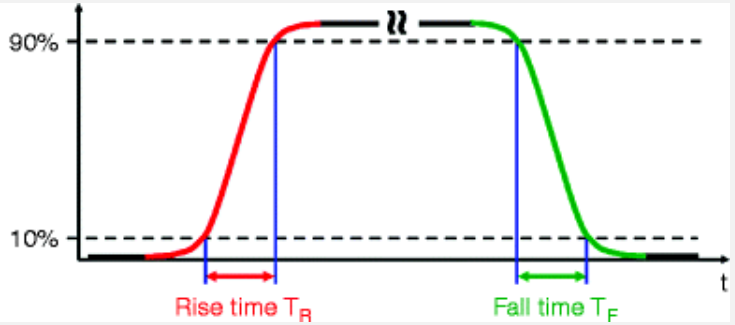


SIGNALS

SQUARE WAVE

Infinite number of sine waves (fundamental + harmonics)





High/low speed circuit is not determined by clock speed but by RISE and FALL times

SIGNALS

LUMPED CIRCUIT

Rise/fall times are LONG compared to propagation time

DISTRIBUTED CIRCUIT

Rise/fall times are SHORT compared to propagation time

→ Reflection

Requires controlled impedance transmission lines

SIGNALS

RISE TIME → MAX TRACE LENGTH

DEVICE TYPE	RISETIME	Max Line Length Outer (inch/mm)
Standard TTL	5.0 ns	9.23 / 235
Schottky TTL	3.0 ns	5.54 / 141
10K ECL	2.5 ns	4.62 / 117
ASTTL	1.9 ns	3.51 / 89
FTTL	1.2 ns	2.22 / 56
BICMOS	0.7 ns	1.29 / 33
10KH ECL	0.7 ns	1.29 / 33
100K ECL	0.5 ns	.923 / 23
GaAs	0.3 ns	.554 / 14

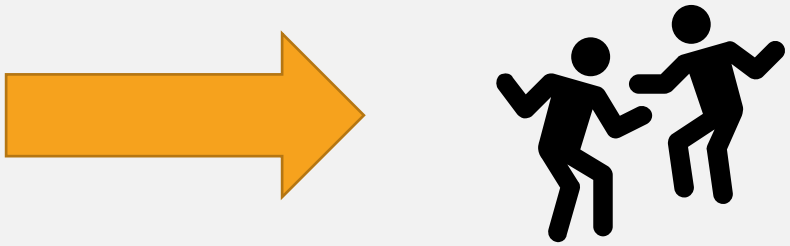
SIGNALS

Use slowest possible rise/fall times

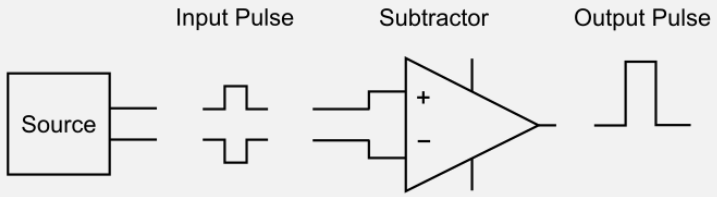
Limited by clock speed (< 15% of total period time)

Set GPIO speed in firmware (OSPEEDR register)

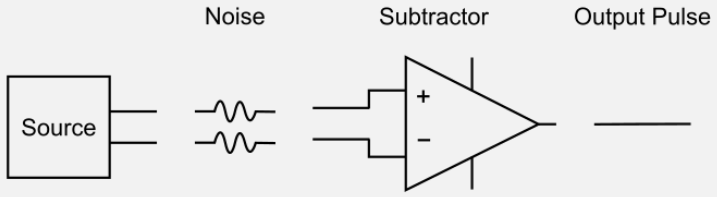
Limit drive current using series resistor at driver



DIFFERENTIAL PAIR



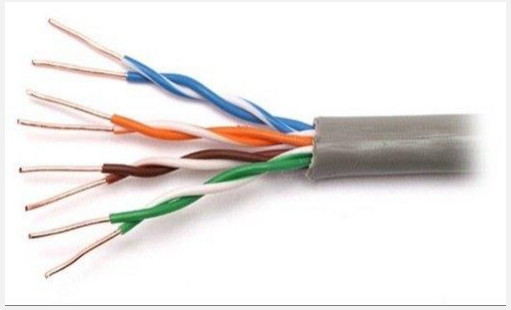
Equal but opposite signals

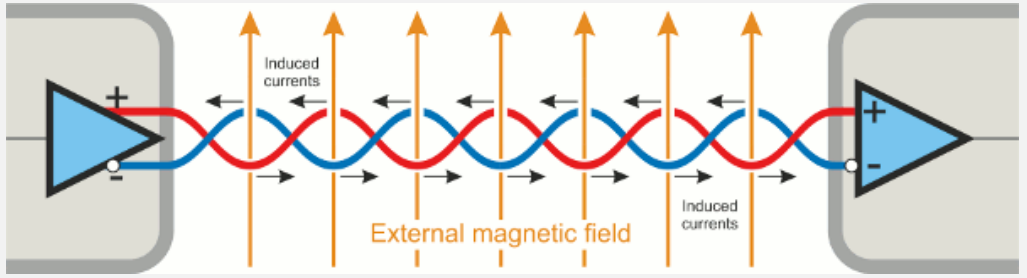


Receiver sees DIFFERENCE

Ignores GND-offsets between sender and receiver

Ignores common mode noise (twisted pair)

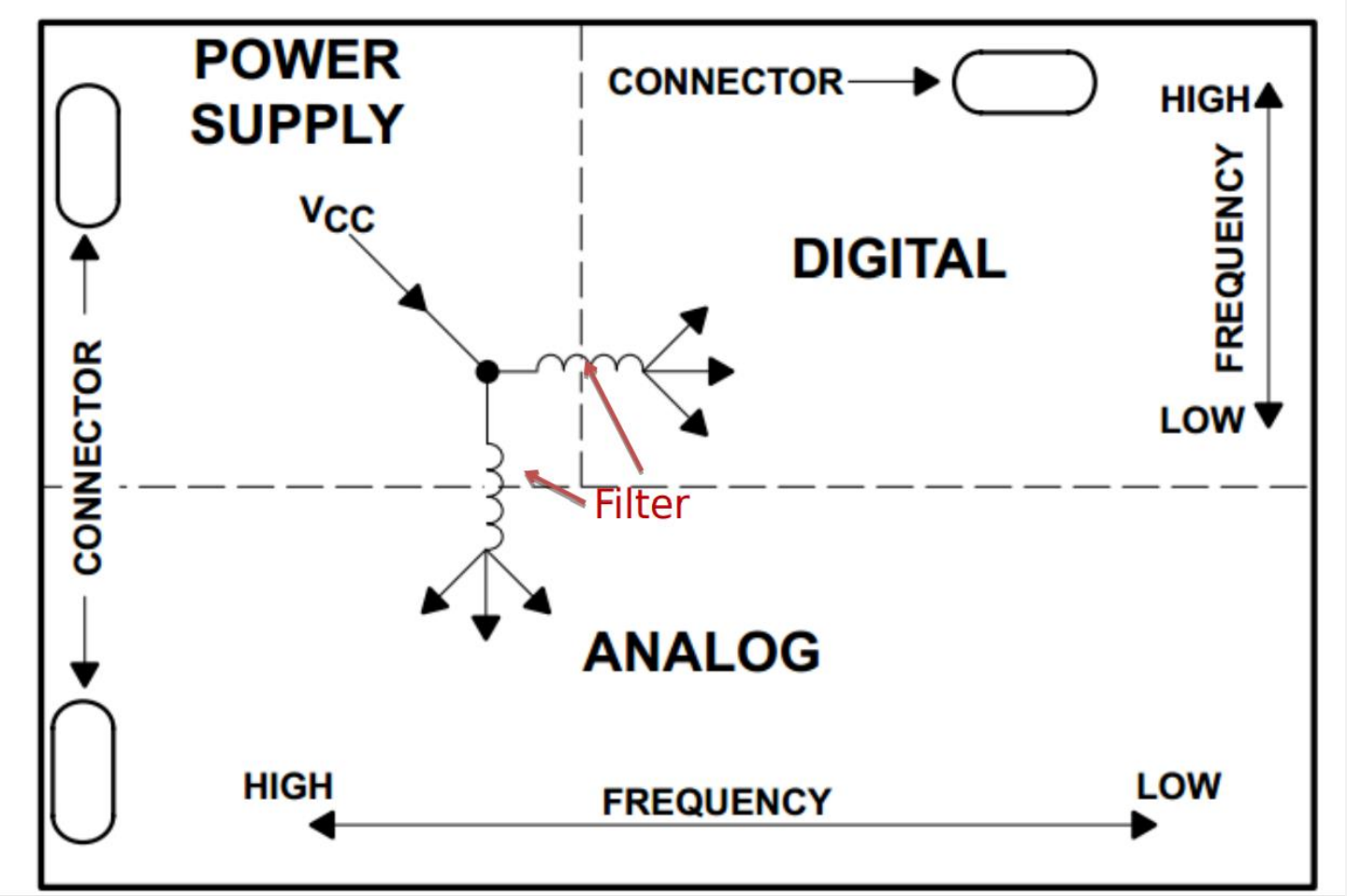




USB

GOOD LAYOUT HABITS

Partitioning your layout



GOOD LAYOUT HABITS

Put all components and route all signals / power on top layer

Use bottom layer for solid GND plane

Decoupling capacitors as close as possible to power pins

Place components for least congested routing

Space signal traces far apart

If you need to cross-under on the bottom layer, make it short

If you can’t make it short, add a return strap over it

LET’S KICAD