~~REGISTERS~~ Sequential Circuits : Introduction

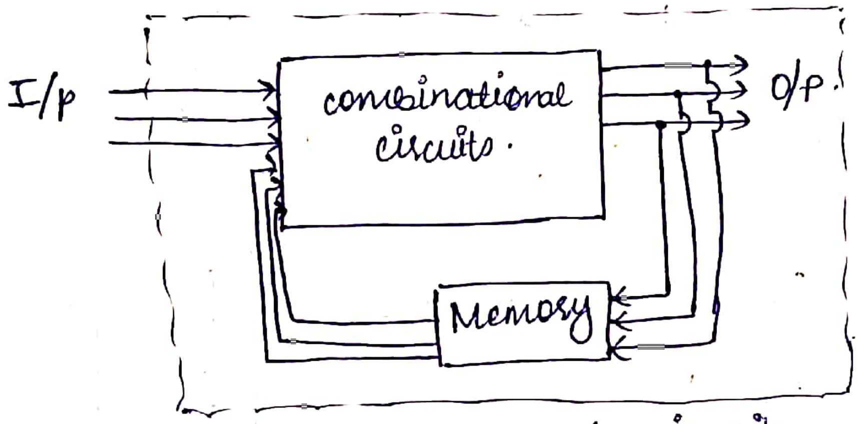
→ Sequential circuits are combinational circuits with memory.

→ In sequential circuits, the present o/p depends on the present i/p as well as previous output.

→ combinational circuits are those in which present O/p depend on present i/p.

- Adder
- Subtractor
- Multiplexer.
- Decoders
- Encoders.

→



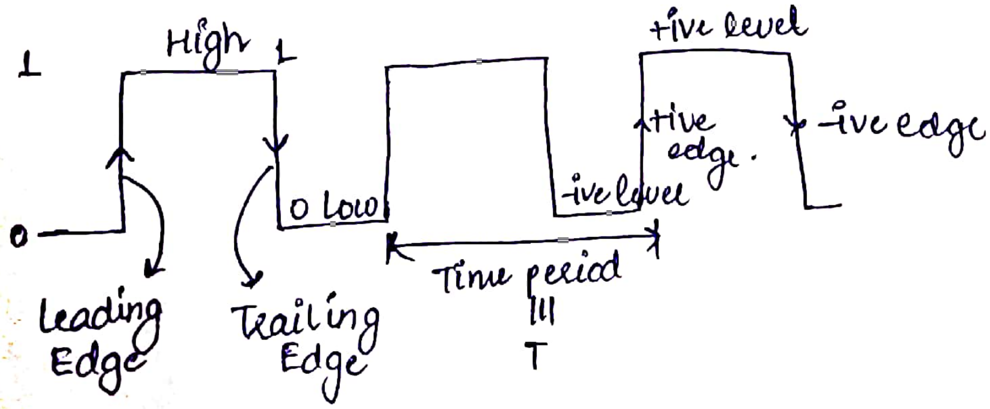
sequential circuit.

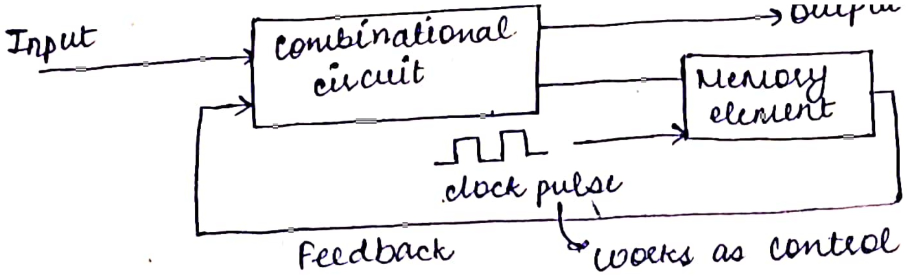
Clock & Triggering Methods

→ Clock signal is a timing signal.

→ used to provide sequence of the circuit.

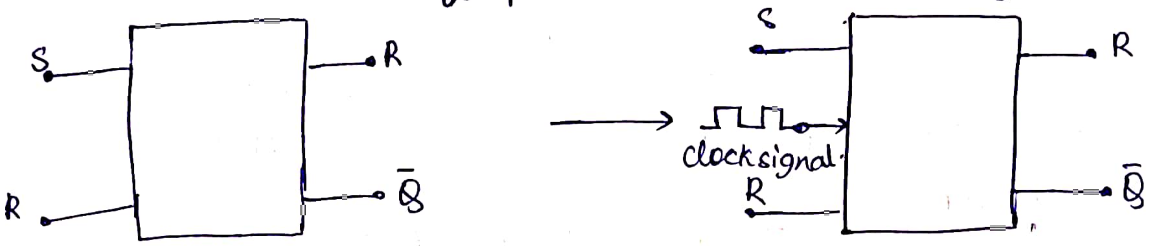
→ clock is a rectangular signal called clock pulse with duty cycle equal to 50%





works as control input for memory element

output varies if input is changed.



→ when nothing is applied to this circuit it behaves asynchronously and is called latch.

→ now this circuit becomes synchronous and is called SR Flip Flop.

→ output is shown when clock signal is in high state.

→ The clock signal decides if the change in input signal must be reflected in the output signal or not.

→ speed of the circuit can be varied by changing the frequency of clock signal.

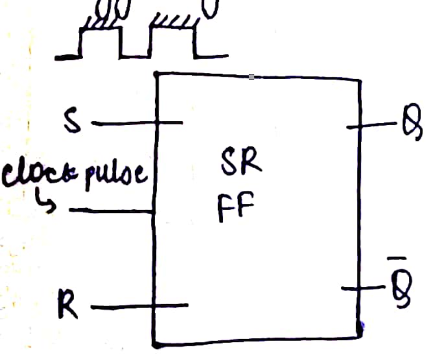
clock frequency $= \frac{1}{T}$

duty cycle $= \dfrac{\text{ratio of time for which pulse is high}}{\text{total time}}$.

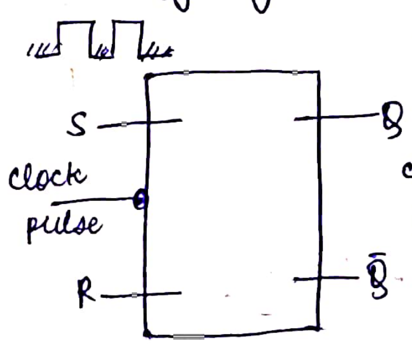
Triggering Methods

- Level Triggering
  - +ive level triggering
  - -ive level triggering
- Edge Triggering
  - +ive edge triggering
  - -ive Edge triggering

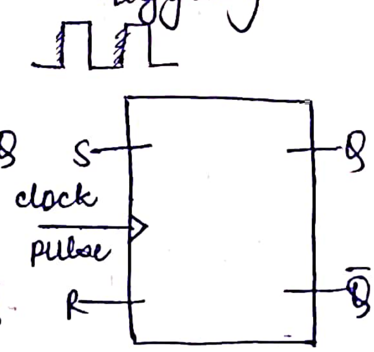
+ive level triggering



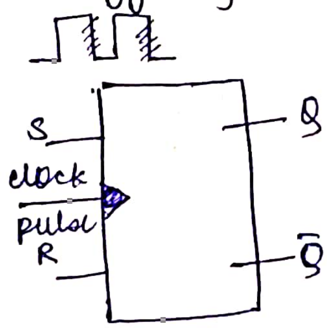
-ive level triggering



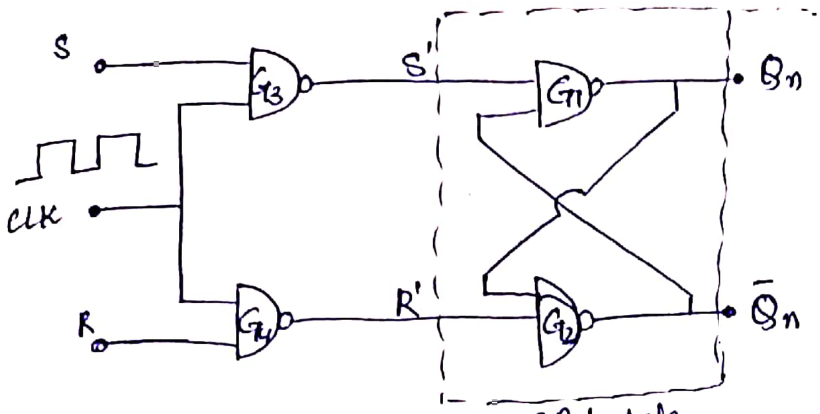
+ive edge triggering



-ive Edge triggering



NAND Gates used SR FLIP FLOP



SR latch.

$S' = \overline{S \cdot CLK}$

$= \bar{S} + \overline{CLK}$ — (1)

$R' = \overline{R \cdot CLK}$

$= \bar{R} + \overline{CLK}$ — (2)

when CLK=1

$S' = \bar{S}$

$R' = \bar{R}$

when CLK=0

$S' = \bar{S} + \bar{0} \Rightarrow S' = \bar{S} + 1 = 1$

$R' = \bar{R} + \bar{0} \Rightarrow R' = \bar{R} + 1 = 1$

Truth Table for SR FF

$X \equiv$ either 0 or 1

CLK	S	R	Q_n	$\bar{Q}_{n+1}$
0	X	X	Prev. state (Memory)	
1	0	0	Prev. state (Memory)	
Reset → 1	0	1	0	1
Set → 1	1	0	1	0
1	1	1	Invalid	

Q_{n+1}

Q_n

when CLK=1

(i) S=0 R=0
$S'=1$ $R'=1$

(ii) S=0 R=1
$S'=1$ $R'=0$

(iii) S=1 R=0
$S'=0$ $R'=1$

(iv) S=1 R=1
$S'=0$ $R'=0$

TRUTH Table of SR Latch

S	R	Q	$\bar{Q}$
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	Prev. state (Memory)	

Characteristic Equation of SR FF.

Present state $\equiv Q_n$

Next state $\equiv Q_{n+1}$

Q_n also acts as an input

Truth table of SRFF

CLK	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0 Reset
1	1	0	1 Set
1	1	1	Invalid

Char Table

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X invalid
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X invalid

Q_n \ S_nR_n ($\bar{S}_n\bar{R}_n$)	00	01	11	10
0	0 (0)	0 (1)	X (3)	1 (2)
1	1 (4)	0 (5)	X (7)	1 (6)

$$\boxed{Q_{n+1} = S_n + \bar{R}_n Q_n}$$

Excitation Table for SR FF

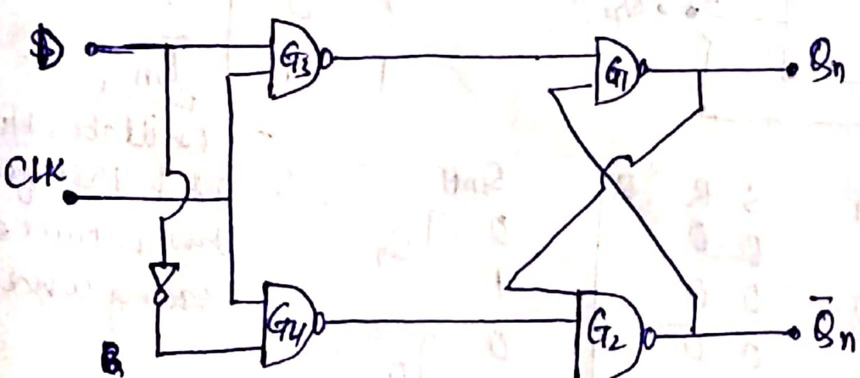
Char Table

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

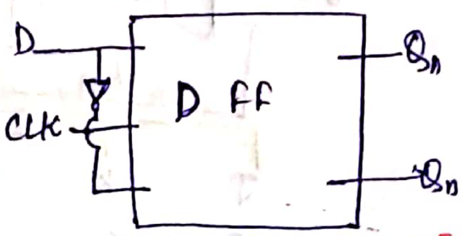
Outputs		Input	
Present state Q_n	Next state Q_{n+1}	S_n	R_n
0	0	0	0
		0	1
0	1	1	0
1	0	0	1
1	1	0	0
		1	0

Excitation table is used when output are given an we have to find the corresponding input.

D FLIP FLOP (used for data storage)



(S=0 , R=1 ⟶ 0 Reset
S=1 , R=0) ⟶ 1 set.



TRUTH TABLE OF D FF

CLK	D	Q_{n+1}
0	X	Q_n Memory
1	0	0 Reset
1	1	1 set

Characteristic Eqⁿ

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

char table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

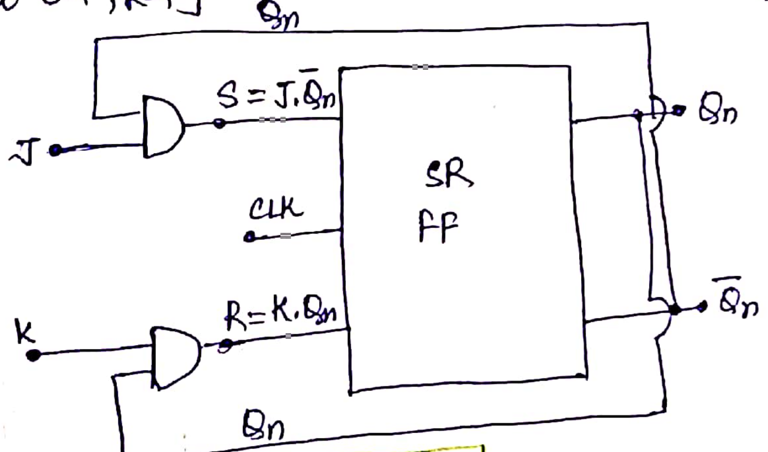
Char. Equation: $\boxed{Q_{n+1} = D}$

Excitation table

Present Q_n	Next Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

[just used for last input where S=1, R=1]

JK FLIP FLOP (we change the invalid state of SR FF into $\bar{Q}_n$ condition of Racing)



Truth Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

oscillates b/w 0 & 1 therefore this is called racing condition.

J	K	Q_n	$\bar{Q}_n$	S	R	Q_{n+1}	
0	0	0	1	0	0	0	Q_n
0	0	1	0	0	0	1	
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	
1	1	0	1	1	0	1	$\bar{Q}_n$
1	1	1	0	0	1	0	

Char Table

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$$\boxed{Q_{n+1} = \overline{Q_n}J + Q_n\overline{K}}$$

Excitation Table

Present state Q_n	Next Q_{n+1}	J	K
0	0	0 0	0 1
0	1	1 1	0 1
1	0	0 1	1 1
1	1	0 1	0 0

Excitation Table.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$J = Q_{n+1}$ $\quad K = \overline{Q_{n+1}}$

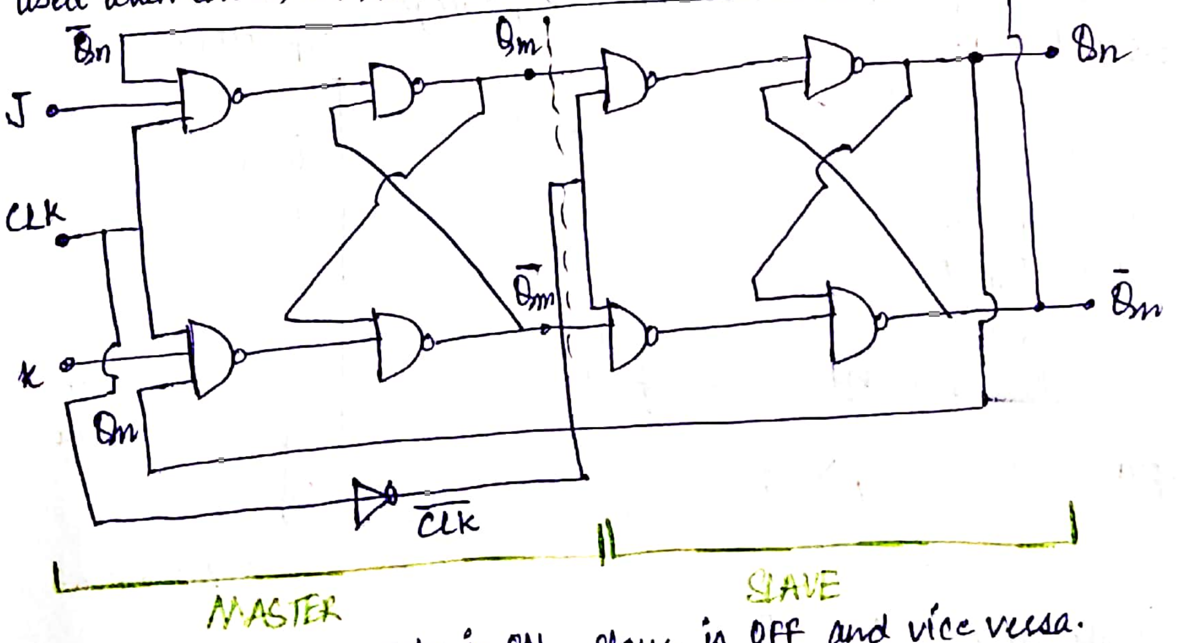
→ Race Around condition can be removed by

Impractical → 1. clock time < Propogation time.

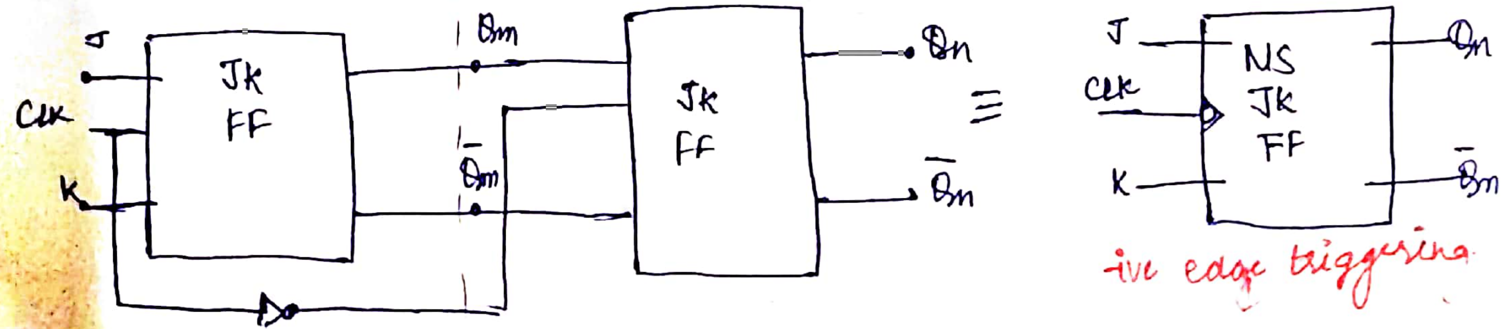
2. Edge triggering. (Master slave JK FF)

MASTER SLAVE JK FF (Toggling)

used when CLK=1, J=1, K=1

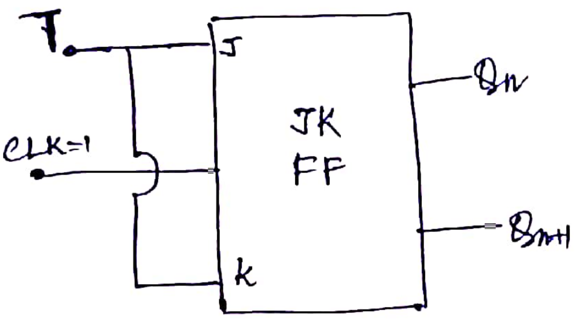


when master is ON slave is OFF and vice versa.



-ive edge triggering

T FLIPFLOP (when we have to do only toggling)



CLK	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$

$\boxed{J=K}$

Char Table

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE

CLK	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$\bar{Q}_n$

Excitation Table

Q	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

FLIP FLOP CONVERSION

1. Identify available & req. FF.
2. Make excitation table for Available FF.
3. Make char table for req. FF.
4. Write Boolean exp. for available FF using Kmap.
5. Draw circuit dia.

LVDT

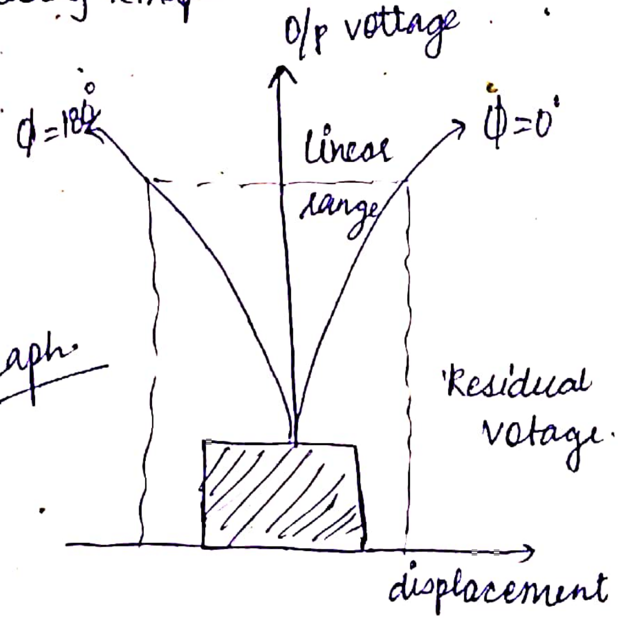
$E_0 = E_{S1} - E_{S2}$

when $E_{S1} = E_{S2}$

$E_0 = 0$

$\Rightarrow$ Null position

graph



LHS displacement $E_{S1} > E_{S2}$

$E_0 > 0$

RHS displacement $E_{S1} < E_{S2}$

$E_0 < 0$