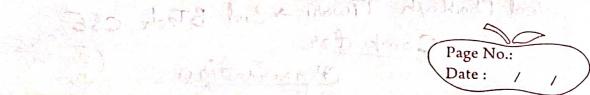
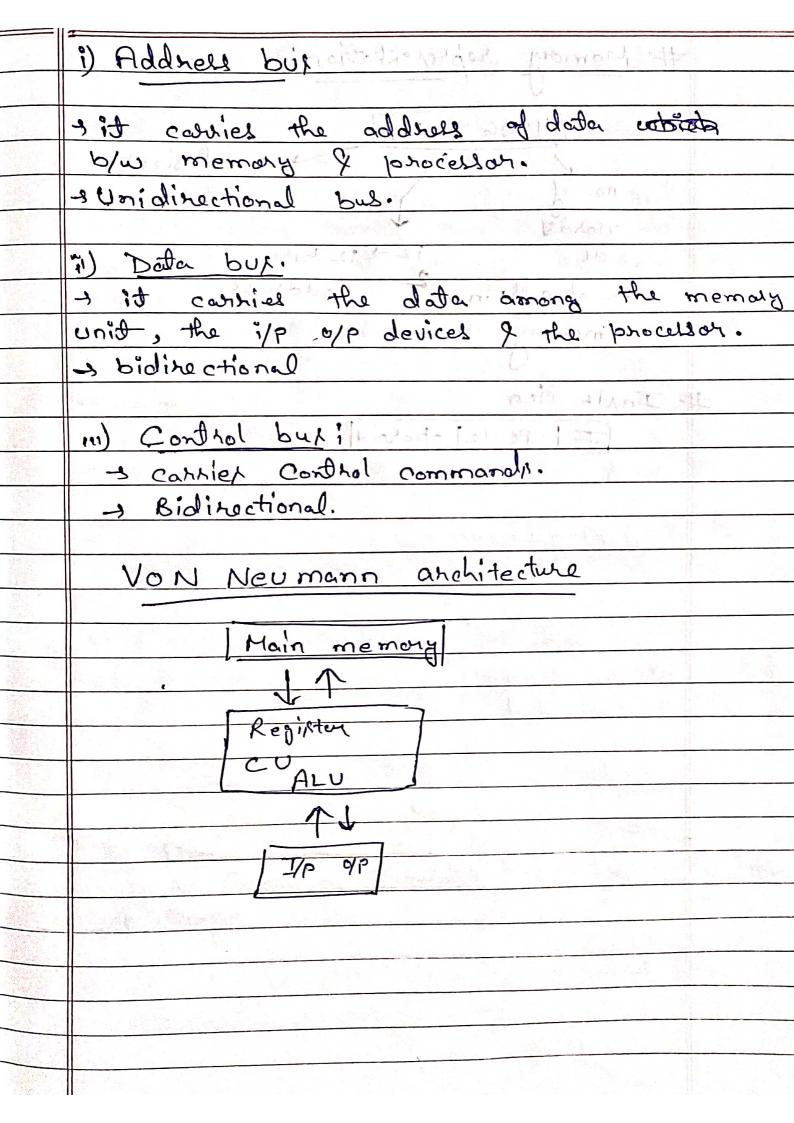
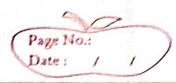
	Veol Prakash Tiwari - 2 2nd Brech CSE Comporter Page No.:
	Compositer
	Organization Page No.: Date: //
	The same that a state of the same of the s
	ALU-s withemetical & logic
	CU-> generales certhal & timing Signals.
	ALU-s axithemotic & logic CU-s generales certhal & diming Signals. registers:
2	ICPU (2017) 2017 Main memory
	SYSTEM BUS
N.	officiality and to propose while the
+1	men month bodatal of old boun test.
	Basic Terminology:
	0
	eus a control unit Randler all instruction
	or processor control system and generates
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	control and timing signals.
	It directs all i/p or 0/p flow, fetches the
7	data for instudion & controlling how data
	moves around the system 10 to 21 11 (11)
Mart	non noithwater trackers do mailtenation
	ALU:
	port of CPU that handles all the calculation
100	and ou prilliped is to spling resident in
	REGISTORS:
	the patient
	9) ACCUMULATOR:
	it stores result, of Calculations made by
	ALU. mand plan of rections
	Longeton report all the Antiquas
	plansin A CHO with all Advantagings
Mag	I what I was to
100	



i) PROGRAM COUNTER (PC)	
- it keep thack of the memory next instruction to be dealt a	location of
thesh ed ut noithurtani tren	with.
-> Pc then passes next address	s do
Memor address register (MAR)	
n) MAR:	
it stores memory location of	Inotheritani
that need to be jetched you	om memody
or stored memory.	157 25 113 1
0	
in) MURIO The How	
odstate notbuttani aft sarote ti	(Promo
memory or any deta that is	to be
transferred to and stored in m	emory.
Her service you'llocking a point dans	0
IN) IR OR CIRCLE	
(Instruction or Current instruc	Iron ougister)
	I DEATH
it stores the most recently de	etcheal
instruction while it is wainting	to be coded
	Ar transfer of
	Correspond
BUSES!	e all 1
Data ix thankmitted your or	re point of
I we comprise the couples	Ui o
comeding all the mayor	r internal
components to the CPU & mayor meant of butes.	remaly by
Meany Manes.	

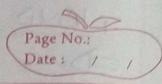




	CHARECTER CODES
	The Done of the State of the St
	BCD
	Les binay coded decimal
	-> when using binary numbers for higher
* 7.	decimal not, , it becomes long chain of
	Zero fone
	Is To a void this diff BCD codes are used
	to represent decimal not.
	-> 8421 BCD code it very common
	method to represent decimal no.
	-> other BCD codes ore 5421, 5311 etc.
	- in BCD code each decimal mo. if
	represented by 4 bit code.
	2Ethi Sunot
	(5) (539) in BCD (d) (AD)
	(011101100100)=(764)
	5 3 5 BCD
	(0101 0011 1001)
ACATON STATE OF THE STATE OF TH	Bc)
V	ASCIT
	1 13 American standard code for Information
	interchange
, and the second	
	-s it is character encoding standard dur
ing.	electronic communication.

Page No.: Date: / /

18. ₁₀	sid represent dent in computer, teleco
- Y.	Tele communication equipment and
	athor devices.
	Larrison District of
	ASS 97,3-122
- W	which when dending it provided ground in the
->	it uses 7 bit de represent a charecter.
	with the state of
1	was school and bib with blown on and
	EBCDIC won Romissis to 12 19 10 to 1
	Is entended binary code decimal interchange
	coder imple assisted of basis
1	->18 bit character encoding.
77	10000001 -5133 000000 11 -1
	al a strain in the hotastardas



	& SYSTEM BUS
-	But in a communication channel used we different model to provide communication
	www different model to provide communication
	ACOUNT MORE ACOR
->	The Bus used to provide communication blu
	CPU, memory & IIP OIP component is called
	SYSTEM BUS
	Michael
	phocussing pasters pastorage
	CPU momory
	1
	[I/P 0/P]
	Le enternal devivo
	Lyvery Blow.
0	1000
1	Advantage of System bus!
	TO THE PARTY OF TH
13	i) Shared transmission medica
1 / W	dikadvaritage;
	dikadvantage; i) only 1 thankmission at a time
	* Address line!
	towards memory & i/P 0/P
	towards memory & i/P 0/P
	3 Unidirectional



1	
=	& based on the no. of lines we can determine
	the corporatify of morning system.
4-3-1	on significant at lesso family property
7	eg. 8085 contains 16 address lines hence
	memory corporately in 216 on 64K
	8086 combains 20 address lines,
	money capacity is 220 de
	mannos & Wodpil lordans marcines
	* Data Lines in and onde election
411	s there lines are used to corry the binary
	Sequence b/w CPU and memory and IP 01P
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bidirectional
	1) TO 010 Whereld the
<u>ہ</u>	V
	the world length of processor
	& based word length we can détermine perjoin-
	-ance of a phocessor.
	1/2 0/2 1/2 1/2
	ey 8085 contains 8 data lines, So the
	word length of phocessor is 8 bist.
	8086 -> 16 data lines, So word length=16bits
	- Contain
	* CONTROL LINES!
	1 1 0 A 1 0 · 1 · 0 · A' ·
	-> used to carry Control Signal & timing
	Signal. 1860
	Signal. 100 de la contraction

	444			Date
(to a control of the	- A 1 5	0:000	indicates ty	per of operation
TA MAN	-3 Control	Signo	itorespect to 1	
<u> </u>	1	9:00-0	sed to Sy.	nchonile mamony
0100	-> timing	old you c	en obera	tion with
	A YP	0,7	alack.	Paracri U
	proces	X 64	CIOCK	
	Capil With	obo or	Lielan	8086
	-> When	there as	to Common	bul,
	11		Signal &	· ·
	address S	hace bl	w momery	1/201P, X
portes	processor	then	there is	the possibility
910	71 al ambig	wither to	(19) eyle	asmoulped.
	7 3170	d	Renai	to exillized
	I/P 0/P	hocollash	· 查得	
Quens	91- 367 54	carii d	A P. Da	as Lalas la
)×:	of Line (c)	a demande	Adding to the Marie of the Mari
missiony	enincolato man	Common	Common	Common
		bus	Control Signal	A - C. december - d -
	I/P 0/P	Х	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
-01	phocesson	otol a	a Auggan	7619 60
	10 8 11	to be work	to Alfred	note / U
	I Soloted To		V	
1121 = 11	11 10 00	Azzii	tob all too	y o d
	Memory	V	~	×
	pardoera		23117 1 115	X CONTR
And Angeles in Angeles and Angeles in Angeles in Angeles in Angeles in Angele	1/0			TO A
mink	- intoducing	'add': A'	oral bus in	Applica Str
	operation	the sings	nik a "	Ti who wire
	wed is	n shiah	nix configue	auton
		1.0	Joenformance	Computity.
			S. R. S.	

	Page No.: Date:
	2) isolate 1/P 0/P: MEMRD (Load)
	Different _ > Memory based (mem. write)
- T	Different -> Memory based (mem. write)
	continol Signal
	TORD (IN)
	5 TORD (IN) based SIONR (OUT)
->	8082, 8086 contains isolated I/o configuration