module division\_6(clk,rst,clk\_odd); //六分频器

input clk;

input rst;

output clk\_odd;

reg clk\_odd;

reg[3:0] count;

parameter N=6;

always @(posedge clk) //同步清零

if(!rst) //如果rst=0则全部清零

begin

count<=1'b0;

clk\_odd<=1'b0;

end

else if(N%2==0)

begin //如果小于N/2-1那么计数+1，clk\_odd保持

if(count<N/2-1)

begin

count<=count+1'b1;

end

else //其他情况则计数值清零，clk\_odd反转

begin //达到50%占空比的六分频器

count<=1'b0;

clk\_odd<=~ clk\_odd;

end

end

endmodule