`timescale 10ns/1ns

module fp\_tp;

reg clk,rst;

wire clk\_odd,clk\_even;

fp myfp(clk,rst,clk\_even,clk\_odd);

initial clk=0;

always

begin

#5 clk=1'b1; //每隔五clk翻转

#5 clk=1'b0;

end

initial

begin

rst=0;

#20 rst=1;

#800 $finish;

end

endmodule