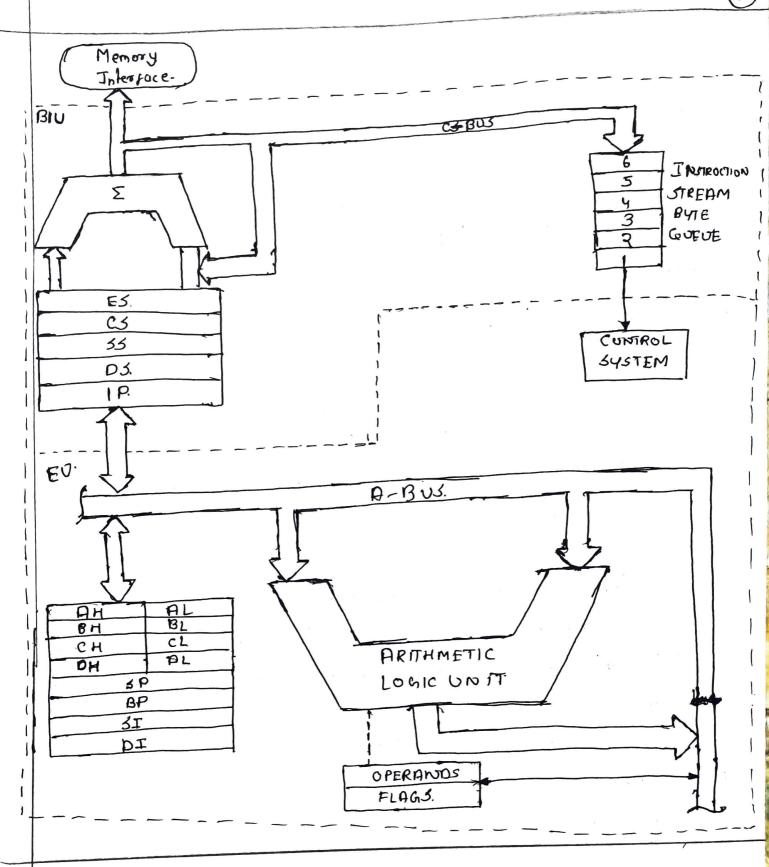
(1) D. Neha. SSIGNMENT-245319733015 CSE-A Draw and explain the pin diagram of 8086 mixoprocessor. And Pin diagram. and description of 8086: MAX. MIN MODE MODE 40 / Vcc (5P) VSS (GND) 39 D DD AD14 2, 37 DA 16 133. HDB 3 37 PAN/34. ADIZ. 4 36 PA18 155. ADII 35 A19.156. AD10. A D9. BHE137. 口8 BO8 93 [] MN/MX AD7 32 ] RD 10 AD6 31 ] RQ/610 11 HOLD A 05 0 12 D ROIGTI HLDA 29 D Lock 113 WR PD3 MIJO AD2. DT/R ADI DEN ADD DIE □ @30 ALE NMI 24 2051 INTA JNTR. 1 1 23 TEST CLK. 19 READY REJET **√**33(6ND)□20 The following pinfunction descriptions are for the microprocessor sort in minimum) maximum mode. Common pindes coiption: It consists of the following pins: > ADO-ADIS (I/O): Address Dala Bus ABIR/S6, ABIR/S5, AM/S4, A16/53 (0): Address & Takes 53/854 BHE / S 7(0): Bus High Enable / Status -> RDCO: READ -> TEST (I) INTR(I): Interupt Request

1)

->

>	NMI (I): Non-Maskable Intersupt	1.	
<b>→</b>	Reset (I)		
7	Ready CI)		
->	CLKCI): Clock	·	1
→	MN/MX CI): Maximum/Minimum		
	Min mode pin descriptions		
	The following & pin function descriptions are for the 8006 i	in minimum mode,	
	MN/MX=1,	- 4	
4	M/IO(a): Status line		
4	wr(a): write	1.0	
	INTA (0): Interrupt Acknowledge		
-	ALE (o): Address Lakh Enable.		
<del>)</del>	DT/R(W: Data Transmit/Receive		
<b>⊸</b>	DENCO): Dala Enable		
	HOLDSHLDA (IIO): Hold and Hold Acknowledge	s :	
	Max mode pin description:	, in a	
	To the second second		
	The following pin descriptions are for the for(18088 systems in MN/MX = 0	maximum mode:	_
		,,,	e,
7	52,51,50(0): Shehus Pins		
	650, G51 (0): Gueue Status		
-3	Lock(o)		
	RQ/GTO and Ra/GTI(IIO): Request/Grant		
₹}.	Explain the architecture of 8086 microprocessor with a jur	ochional block	
	diagram.	2,000	
JPJ.	The 8086 CPU is divided into two independent functional units:		
->	s. Interpace Unit (BIU)		
)	Erecution. Unit (EU).		
- 1			



3) What is pipelining an Ladvantuges of pipelining.

A). In 8086, he speed up the execution of program, the instructions petching and execution of instructions are overlapped each other. The technique is known as pipelining. In pipelining, when the nth instruction is executed, the n+1th execution is tetched and thus the processing speed is increased.

Advantages:

->	instruction throughout increases.		
->	increase in the number of pipeline shager increases the number of instructions,		
	executed simultaneously		
<b>→</b> )	Forter ALU can be designed when pipelining is used.		
-3	Pipelined CPU's works at ligher clock prequencies than the RAM.		
<b>→</b>	Pipeline increases the overall performance of the CPU.		
4)	List the features of 8086		
A)	Microps ocenor 8086 realises:		
-	It is a 16 bit microprocessor		
->	It has a 16 bit data bus, so it can sead data from as write data to memory and		
	ports either 16-bit or & bit atalime.		
<del>-)</del>	It has 20 bitaddress bus and can access upto 220 memory locations (IMR).		
	It consupport upto 64 K. I/O ports		
<b>-</b> >	It pourides With-bit registers.		
	It has multiplexed address and data bus ADO-ADIS, SAIG-AIQ.		
-)	It requires single phase clock with 33% duly cycle to provide internal timina		
٦,	Prefetches upto (instruction bykes from memory and queues themin order to		
	spère dup the processing.		
	sus 6 supports 2 modes of operation.		
	Maximum mode		
6)	Minimum. mode.		
5).	Explain memory segmentation. Whatave the registers used to access me mory		
9)	Memory segmentation is the process in which the main memory of the		
	computer is logically divided into different segments and each segment has its		
	cun bare address. It is basically used to enhance the speed of execution of the		
	computer system. , so that the processor is able to tetch and execute. The data.		
	from the memory easily and past.		

(2)
The index and regulars used to access memory are:
BP-Base Piler
BP-Base Pointer.
SP- Stuck Pointer
SI- Scurce Index.
DI-Destination index.
The pointers registers contain offset within the particular segments.
The pointer register IP. contains of set within the orderegment.
The pointer register BP contains offset within shell segment
The pointer registers p contains offset within shick segment
The index. registers are wed as general purpose registers as well as two uppoel
showing e in case of indexed, base indexed and relative base indexed
addressing modes.
The register SI is used hishare. the upset or source data in data segment.
The regular DI is used his hore the appel of destination in data or extrasegment
Theinder registers are particularly useful forstring manipulation.
Give the contents, of the slag. register after addition of given two binary number
0110 0101 1101 0001,0010 1000 1010
0110 0101 1101 000)
+ 0010 1001 0010 1010
10001110 1111 1011

CF=0. PF=0. PF=1 ZF=0. SF=0. OF=0.