1. It is known that $F1=\sum_{A,B,C,D}(0,2,5,6,9,12,13,15)$, $F2=\sum_{A,B,C,D}(0,2,3,6,9,10,13,15)$ $F3=\sum_{A,B,C,D}(3,5,10,12)$, and the correct one in the following logical relationship is (_____).

A) $F3=F1\oplus F2'$ B) $F3=F1\oplus F2$ C) $F3=F1\oplus F2^{D}$ D) $F2=F1^{D}$

2. A code converter circuit is shown in Figure 1-2. If the input X(X3X2X1X0) is a Excess-3 code, the output Y(Y3Y2Y1Y0) is (_____).

A) 2421 BCD code B) 5421 BCD code

C) 4221 BCD code D) 8421 BCD code

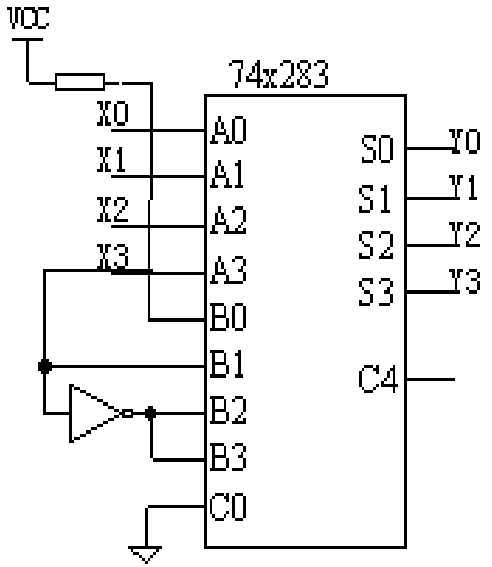


Figure 1-2

3. An 8-bit comparator has inputs P and Q, and its output $F_{P=Q}$ and $F_{P>Q}$ are both active low ($F_{P=Q}$=0 when P=Q, and $F_{P>Q}$=0 when P>Q). To generate an active-high $F_{P<Q}$ ($F_{P<Q}$=1 when P<Q), $F_{P=Q}$ and $F_{P>Q}$ can be connected to (_____).

A) AND B) OR C) NAND D) NOR

4. Which of the following statements about flip-flops is CORRECT? ( )

A) A T flip-flop can be built by using a J-K flip-flop with J=1 and K=d.

B) A JK flip-flop can be built by using a D flip-flop with $D=KQ'+J'Q$.

C) A D flip-flop can be built by using a J-K flip-flop with J=D and K=D.

D) All of the above are wrong.

5. To design a "11011010" serial sequence generator by shift registers, we need a (___)-bit shift register as least.

A) 3 B) 4 C) 5 D) 8

6. In a temperature measurement system, if the measured temperature range is -50°C ~ 120°C, the linear temperature converter output voltage range is 0 ~ 5V. If the A/D converter is required to recognize the amount of change of 0.1°C, an A/D converter of not less than (_____) bit should be used.

A) 8 B) 9 C) 10 D) 11

7. If the clock input is connected to a 10MHz digital signal, which of the following circuits can output a 1MHz signal with 50% duty cycle ? (　　)

A) a self-correcting 10-bit ring counter with a single circulating 1

B) a self-correcting 5-bit Johnson counter

C) a free-running decade counter (十进制计数器)

D) a 4-bit LFSR counter

8. The logic diagram contains a DAC and a 4-bit counter 74x163 is shown in Figure 1-8. When the input of the 3-bit DAC is 001, the output voltage is 1V, and when the input number is 111, the output voltage is 7V. The output (Vout) waveform of the circuit shown in Figure 1-8 is (　　).

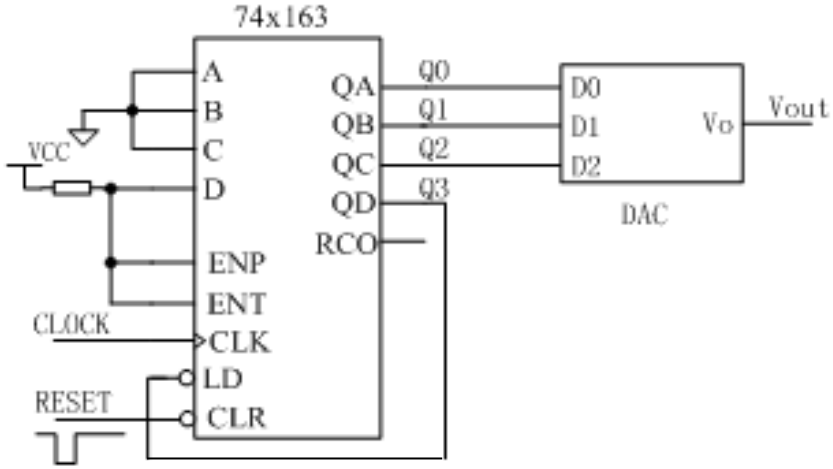


Figure 1-8

A.　　B.　　C.　　D.

9. Which state in Figure 1-9 is ambiguous? (_____)

A) state A　　B) state B　　C) state C　　D) state D

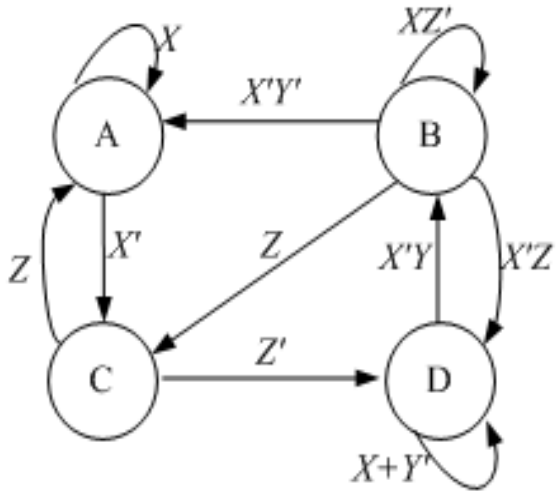


Figure 1-9

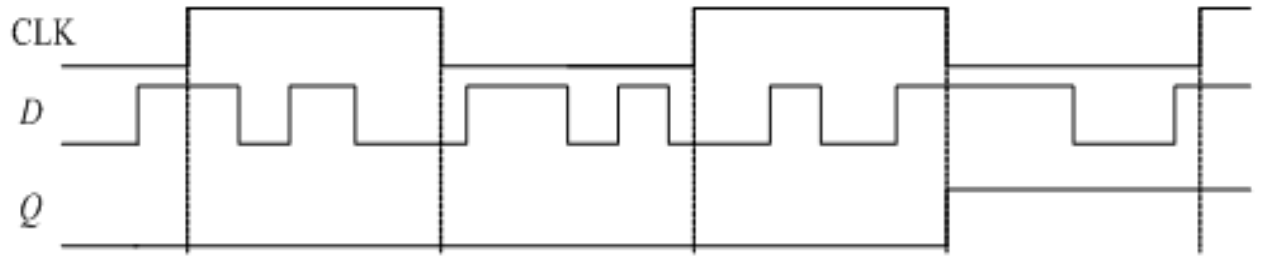


Figure 1-10

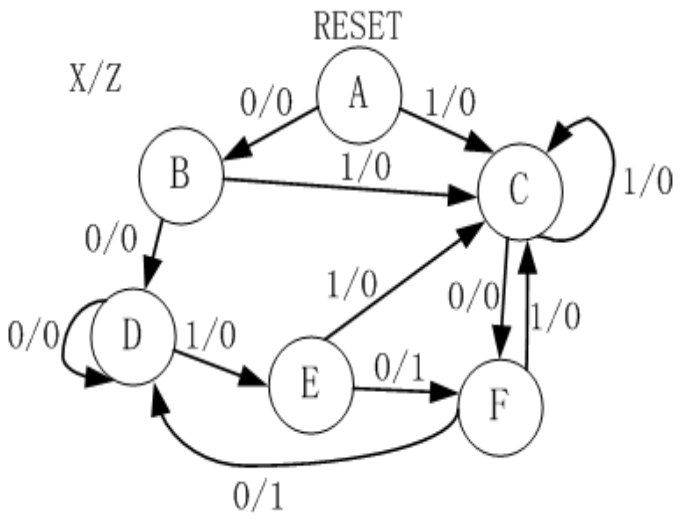
10. The input CLK, D, and the corresponding output Q on a storage element are shown in Figure 1-10, then the storage element is (_____).

A）Positive（正）-edge-triggers D flip-flop　　B）D latch with enable active low

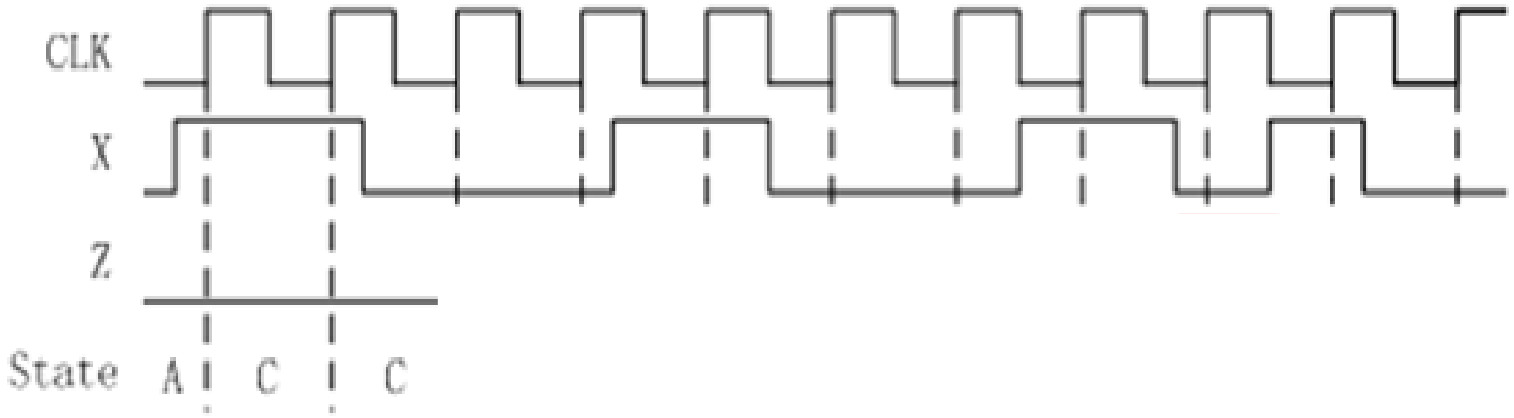
C）Negative（负）-edge-triggers D flip-flop　　D）D latch with enable active high

A Mealy sequential circuit (The state graph as Figure 2) which investigates(监测) an input sequence X and will produce an output of $Z = 1$ for some input sequences.

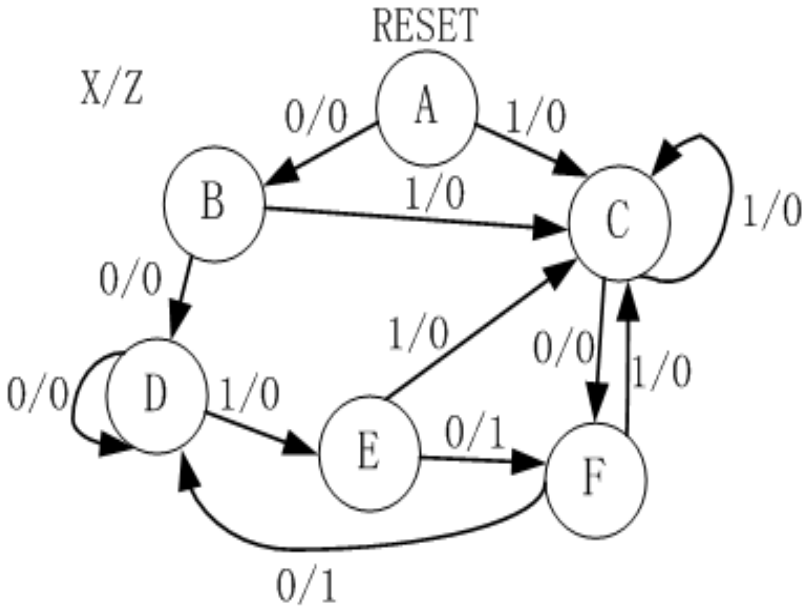
The circuit has a start state A.



1. Starting in the initial state A, determine the output sequence Z for the following input sequences X and write the next state. Assuming the transition time and propagation delay of all devices in the circuit are zero, complete the timing diagram below. (6')

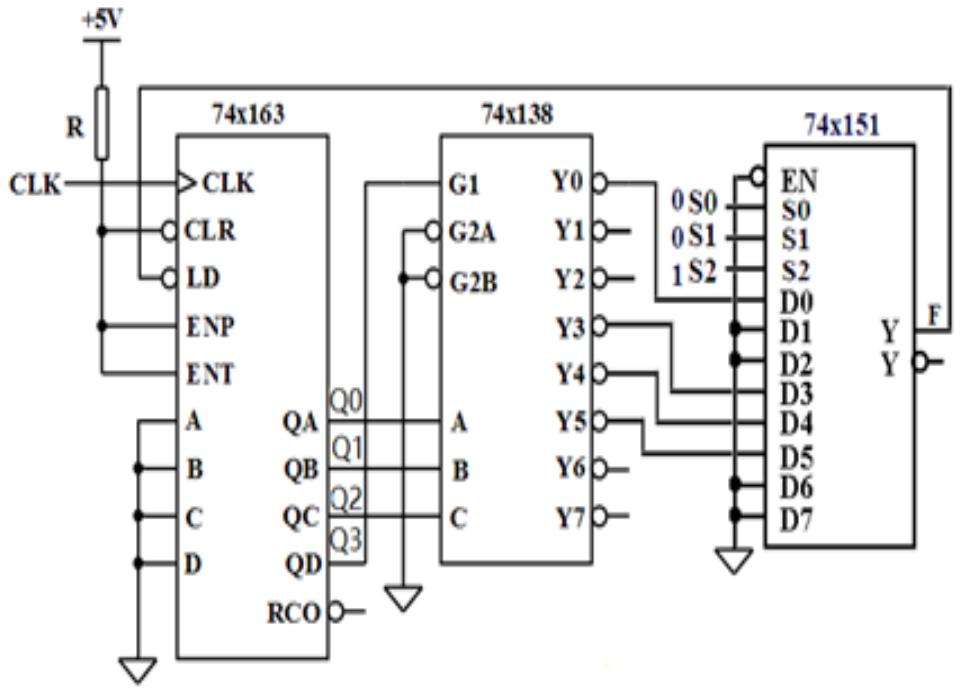


2. The Mealy sequential circuit (Figure 2) which investigates an input sequence X and will produce an output of Z = 1 for any input sequence ending in _____and _____. (4')

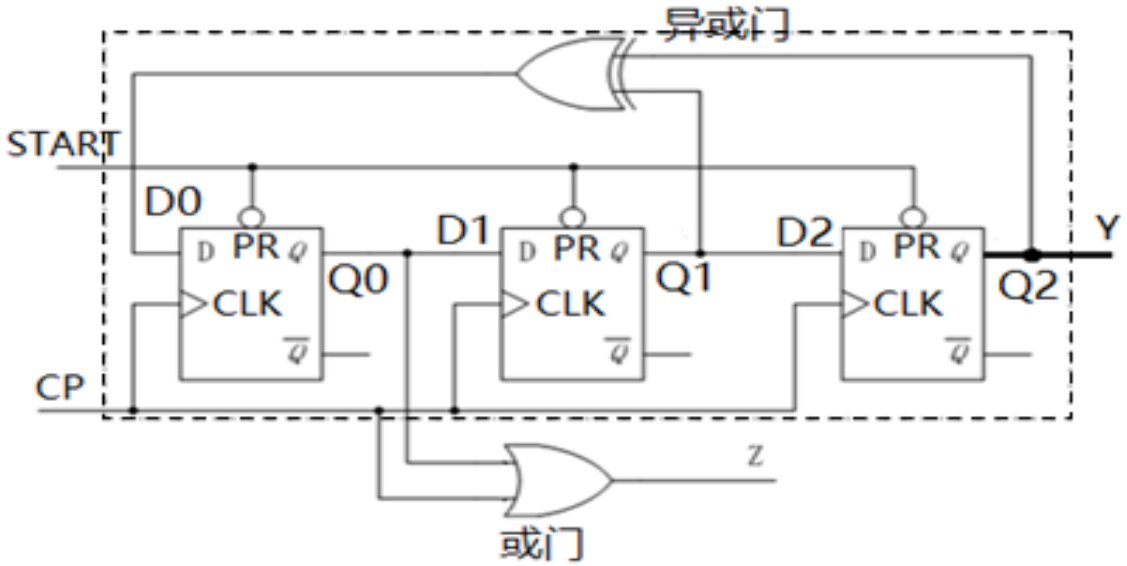


Analyze the circuit as shown in Figure 3, which contains a 74x163 4-bit binary counter, a 74x138 3-8 decoder and a 74x151 8-input,1-bit multiplexer. When control input S2S1S0=100 for 74x151 multiplexer,

1. Write out the logic expression of 74x151' output F(Q3,Q2,Q1,Q0). (3')
2. Write out the sequence of states for the 74x163 in the circuit. (5')
3. Describe the modulus(模) of the circuit. (2')



Analyze the circuit with two gates and three D flip-flops with an asynchronous（异步） set as shown in figure 4.



1) The circuit in the dashed box（虚线框） is a clock (_____) state machine? (1')

A. synchronous（同步） B. asynchronous（异步）

2) Write the excitation equations and the logic equations of Y and Z. (5')

excitation equations :

D0=Q1⊕Q2

D1=Q0

D2=Q1

logic equations of Y and Z:

Y=Q2

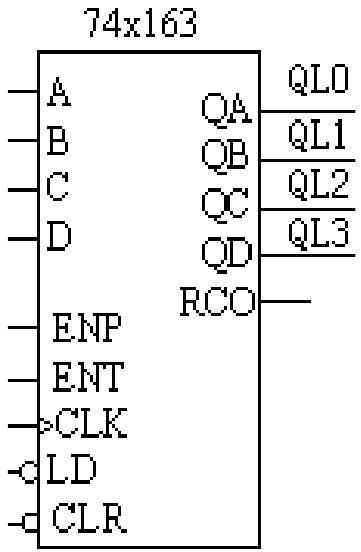
Z=Q0+CP

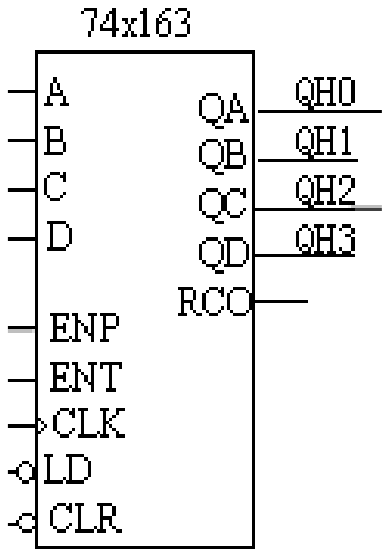
Design a synchronous circuit with one input X and one MOORE type output EDGE, which detects transitions（转换）on X. The machine tests its X input at each tick of the clock and asserts EDGE if the value of X at that tick is different from the value at the previous tick. Use state names A, B, C, and so on as needed. Please describe the state meaning and finish the minimal state/output table. (Hint: No more than 6 states are required.)

Solution: **The minimal state/output table**

State meaning	S	X		EDGE
		0	1	
初态	A			
	S*			

Using two 74x163 4-bit binary counter, design a modulo-60 counter circuit with the counting sequence 00, 01, ..., 59, 00, 01, ... The input to the circuit is the 1Hz clock signal CLOCK and the output is the 8421 BCD code. Please complete the circuit connection below using only some basic logic gates.





1. An 8×2 ROM can be used to realize two combinational logic functions F1 and F2 whereas F1=AB'+AC'+B'C' and F2=A'+BC. The connections to perform the logic function using an 8×2 ROM is presented in Figure 7-1. Please give the content in the ROM. (8')

A2	A1	A0	D1	D0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

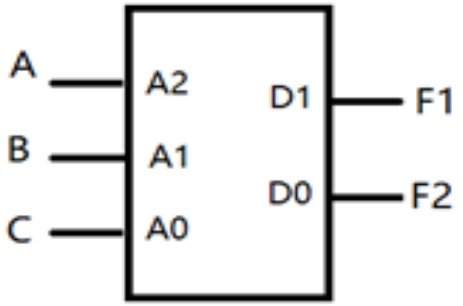


Figure 7-1

2. The ROM and 74x194 are connected, as shown in Figure 7-2.

1） Starting with state 000, write the sequence of states on Q2 Q1 Q0 for the next 8 clock ticks for the circuit. (4')

Q2 Q1 Q0： 000→ (　　)→(　　)→(　　)→(　　)→

(　　)→(　　)→(　　)→(　　)

2） Is the circuit shown in Figure 7-2 a self-correcting counter? (　　) (YES/NO) (1')

3） The periodic sequence generated on Y is (　　), (1')

and the periodic sequence generated on Z is (　　) (1')

A2	A1	A0	D1	D0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1