Lab4: Cachelab

CSE4009: System Programming

Woong Sul

Overview

- Fetch the handout from hconnect
- Place and extract the handout file
- Complete your assignment
- Push your final source files to hconnect

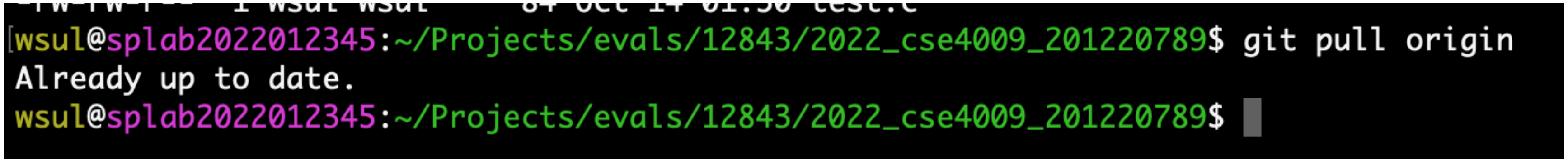
Goal

- Understanding the basic concepts of cache organization
- Understanding how cache memories affects the performance

1. Download the handout file

- Check the handout file assigned to you

  $ git pull origin



```
-rw-rw-r--  1 wsul wsul    84 Oct 14 01:30 test.c
[wsul@splab2022012345:~/Projects/evals/12843/2022_cse4009_201220789$ git pull origin
Already up to date.
wsul@splab2022012345:~/Projects/evals/12843/2022_cse4009_201220789$ 
```

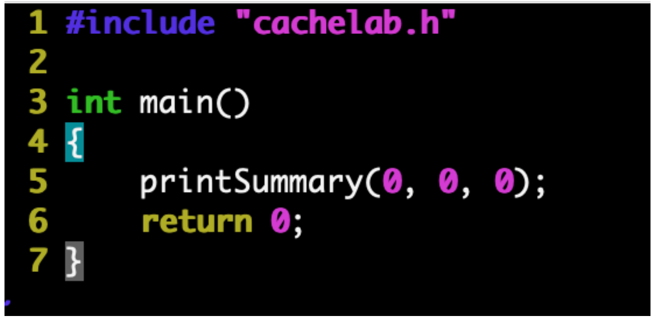
2. Extract handout

- Check your files (6 files)
  - README
  - Makefile
  - cachelab.c, cachelab.h: required files for your cache simulator
  - **csim.c:** your cache simulator (incomplete)
  - csim-ref: the reference binary for csim.c

    얘와 동일한 결과를 내게끔..
  - **trans.c:** your matrix transpose function (incomplete)
  - test-csim: Tests your cache simulator
  - test-trans: Tests your transpose function
  - tracegen.c: Helper program used by test-trans
  - Tra~~i~~ces: Trace files used by test-csim.c

3. Complete your cache simulator

- The main function is almost empty..
  - Fill the required stuffs that works properly as a cache simulator



```c
#include "cachelab.h"

int main()
{
    printSummary(0, 0, 0);
    return 0;
}
```

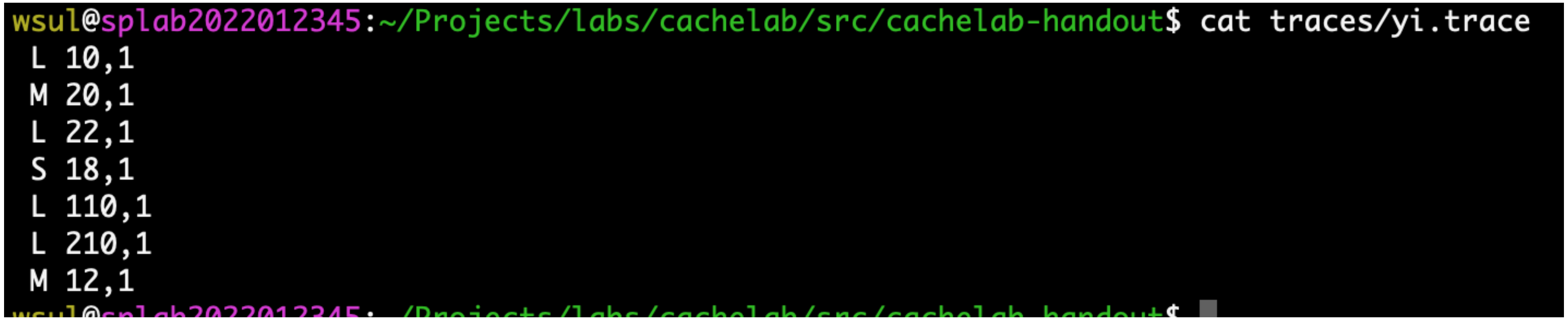
  - printSummary placed at cachelab.c
  - getopt() is very useful to passing parameters

-V

    - -v: memory trace info
    - -s: number of set
    - -E: associativity
    - -b: number of block bits (B=2^b is the block size)
    - -t <trace file>
    - test-trans.c and tracegen.c have examples for this function

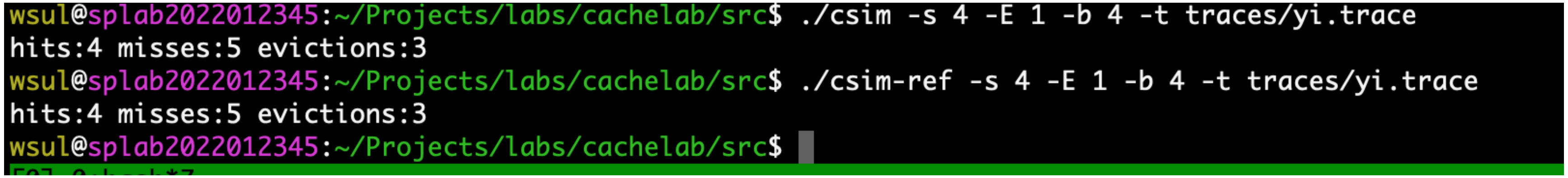
3. Complete your cache simulator (Cnt’d)

- Test your cache simulator
  - make csim
  - Trace files show operations, address, size
    - L: load, S: store, M: load and store, I: instruction (ignore)
    - Check the cachelab-handout.pdf (in LMS)



```
wsul@splab2022012345:~/Projects/labs/cachelab/src/cachelab-handout$ cat traces/yi.trace
 L 10,1
 M 20,1
 L 22,1
 S 18,1
 L 110,1
 L 210,1
 M 12,1
wsul@splab2022012345:~/Projects/labs/cachelab/src/cachelab-handout$
```

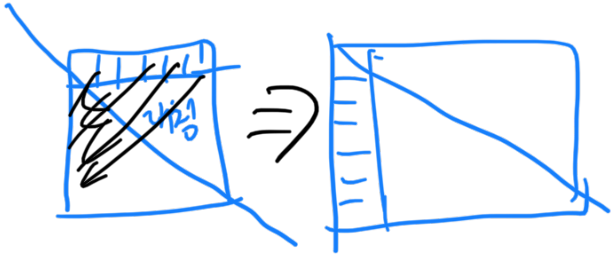
  - Compare the result from both csim and sim-ref

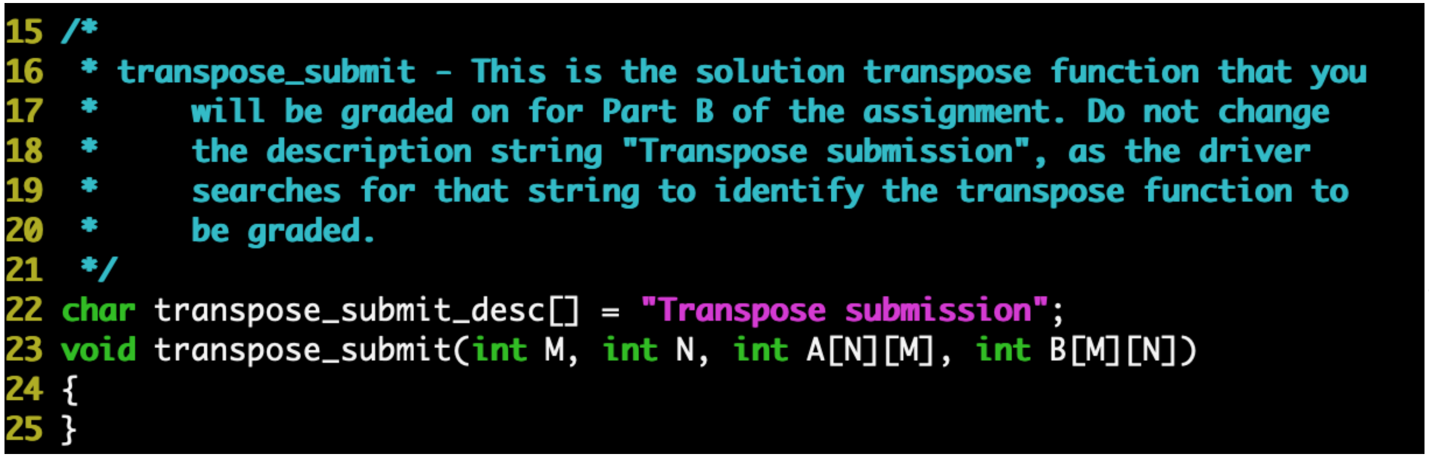


```
wsul@splab2022012345:~/Projects/labs/cachelab/src$ ./csim -s 4 -E 1 -b 4 -t traces/yi.trace
hits:4 misses:5 evictions:3
wsul@splab2022012345:~/Projects/labs/cachelab/src$ ./csim-ref -s 4 -E 1 -b 4 -t traces/yi.trace
hits:4 misses:5 evictions:3
wsul@splab2022012345:~/Projects/labs/cachelab/src$
[0] 0:bash*
```

4. Complete your transpose function

- You have an empty function
  - to minimize cache misses (given s = 5, E = 1, b = 5)
  - with up to 12 local int variables (not arrays)
  - without recursion





```
/*
 * transpose_submit - This is the solution transpose function that you
 *     will be graded on for Part B of the assignment. Do not change
 *     the description string "Transpose submission", as the driver
 *     searches for that string to identify the transpose function to
 *     be graded.
 */
char transpose_submit_desc[] = "Transpose submission";
void transpose_submit(int M, int N, int A[N][M], int B[M][N])
{
}
```

- make test-trans tracegen
  - You may need valgrind

    # sudo apt-get install valrind

5. Tests

- Cache simulator

```
linux> ./csim -s 1 -E 1 -b 1 -t traces/yi2.trace
linux> ./csim -s 2 -E 1 -b 4 -t traces/dave.trace
linux> ./csim -s 2 -E 2 -b 4 -t traces/trans.trace
linux> ./csim -s 5 -E 1 -b 4 -t traces/long.trace
```

결과가 ref와 같아야함.

- Transpose function

```
linux> make
linux> ./test-trans -M 32 -N 32
Step 1: Evaluating registered transpose funcs for correctness:
func 0 (Transpose submission): correctness: 1
func 1 (Simple row-wise scan transpose): correctness: 1
func 2 (column-wise scan transpose): correctness: 1
func 3 (using a zig-zag access pattern): correctness: 1
```

- Or…

```
linux> python3 ./driver.py
```

– 전체 테스트

6. Submission

- You are supposed to submit **csim.c** and **trans.c** file to hconnect

Good Luck!