



EE6094
CAD for VLSI Design




Compiler and Checker

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Outline


- ◆ Compiler
- ◆ Checker




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Compiler




- ◆ How to compile and execute your source code on workstation?
 - Step1: Use g++ command

```
[ ]@cad ~/PA1]$ g++ -std=c++11 test.cpp -o test
```



- Step2: Execute your output file

```
[ ]@cad ~/PA1]$ ./test  
Hello PA1!
```

./Your output file name




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Checker

- ◆ How to check the Verilog code dumped by your C++ code is correct?
 - We need to use testbench to check the result.



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Checker

◆ How to use the checker?

- Step1: Generate an executable file (ex. exe)
- Step2: Make sure you put your Verilog code, testbench code files, Makefile and executable file in the same folder

```
[ ]@cad ~/PA1]$ g++ -std=c++11 PA1.cpp -o exe
```

```
[ ]@cad ~/PA1]$ ls
c17.isc  c17_testbench.v  exe  PA1.cpp
```

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Checker

◆ How to use the checker?

- Step3: Key in the following commands


```
source /usr/cad/cadence/CIC/incisiv.cshrc
source /usr/cad/synopsys/CIC/verdi.cshrc
```

```
[ ]@cad ~/PA1]$ source /usr/cad/cadence/CIC/incisiv.cshrc
[ ]@cad ~/PA1]$ source /usr/cad/synopsys/CIC/verdi.cshrc
```
- Step4: Use your executable file to translate the ISCAS85 format to Verilog format.


```
[ ]@cad ~/PA1]$ ./exe c17.isc c17.v
[ ]@cad ~/PA1]$ ls
c17.isc  c17_testbench.v  c17.v  exe  PA1.cpp
```

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