Code - HW3

記憶體積體電路 Memory Circuit Design

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List. 1: Result 1 with overloading - WE, CSL, WL

```
1
     *** HW3 Basic Sense Amplifier Circuit Diagram - DRAM ***
     *** .protect
     .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
 3
 4
     .unprotect
 5
     ***
 6
 7
     .param VCC = 1
     .param VOVER = 'VCC + 0.5'
 8
 9
10
     .global VSS! VCC!
11
     VCC VCC! 0
                  dc VCC
12
     VSS VSS! 0
                    dc 0
13
14
     ***inverter
15
     ** Mos D G S B
     ** .ic 是初始偏壓值
16
17
     .subckt inv in out Wp = 1 Wn = 1
     Mp out in VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
18
     Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
19
20
     .ends
21
22
     .subckt buf in out
23
     xinv1 in 1 inv Wp = 20 Wn = 1
     xinv2 1 out inv Wp = 40 Wn = 1
24
25
     .ends
26
27
     * .IC v(C2)='VCC/2'
28
     * .IC v(BL) = 0
29
     * .IC v(BLB) = 0
30
     .IC V(SAN) = 0
31
     .IC V(SAP) = 0
32
33
     * VWL
                     VSS! pulse('VCC+0.4' 0 -0.5ns 0.05ns 0.05ns 2.5ns 10ns)
               INPUT VSS! pulse(0
34
     * VINPUT
                                      VCC -0.5ns 0.05ns 0.05ns 10ns 20ns)
     * VPRE
                     VSS! pulse(VCC
35
               PRE
                                         0 0.5ns 0.05ns 0.05ns 2.5ns 10ns)
     * VWE
               WE
36
                     VSS! pulse(VCC
                                         0 -0.5ns 0.05ns 0.05ns 5ns 10ns)
37
     * VEQ
               EQ
                     VSS! pulse(0
                                     VCC
                                            0.5ns 0.05ns 0.05ns 2ns 10ns)
38
     * VCSL
               CSL
                     VSS! pulse(VCC
                                      0 -0.5ns 0.05ns 0.05ns 4ns 10ns)
39
     * VHVCC
               HVCC VSS! dc VCC/2
40
41
```

```
VSS! pulse(0 'VCC+0.5' 0.5ns 0.05ns 0.05ns 8.5ns 10ns)
42
    VWL
            WL
           INPUT VSS! pulse(0
    VINPUT
                               VCC 0.5ns 0.05ns 0.05ns 13.5ns 25ns)
43
            PRE VSS! pulse(0 VCC -0.5ns 0.05ns 0.05ns 9.5ns 10ns)
44
    * VPRE
    VWE
            WE
                  VSS! pulse(0 'VCC+0.5' 0.5ns 0.05ns 0.05ns 3ns 14ns)
45
                  VSS! pulse(VCC 0 Ons 0.05ns 0.05ns 9ns 10ns)
46
    VEQ
47
    VCSL
            CSL
                  VSS! pulse(0 'VCC+0.5' 0.5ns 0.05ns 0.05ns 4ns 13ns)
    VHVCC
            HVCC VSS! dc VCC/2
48
49
    xinvinput INPUT INPUTB inv Wp = 0.2 Wn = 0.1
50
    * xinvinput1 INPUTB INPUT inv Wp = 0.2 Wn = 0.1
51
52
    * xinvout OUT
                      OUTB inv Wp = 0.2 Wn = 0.1
53
    * xinvout1
                OUTB
                        OUT inv Wp = 0.2 Wn = 0.1
                            inv Wp = 0.2 Wn = 0.1
54
    * xinvbit
                BL BLB
55
    * xinvbit1 BLB
                       BL
                            inv Wp = 0.2 Wn = 0.1
56
57
58
    xbuf INPUT
                  IN
                        buf
    xbufB INPUTB INB
59
                        buf
60
    *** Write Enable
61
62
    MNWE1
            IN
                  WE OUT
                            gnd nmos w = 10u l = 65n
63
    MNWE2
            INB
                  WE OUTB gnd nmos w = 10u l = 65n
64
65
66
    MNCSL1
             OUT
                   CSL
                         BL
                              gnd
                                  nmos w = 10u l = 65n
    MNCSL2
             OUTB CSL
67
                         BLB gnd
                                  nmos w = 10u l = 65n
68
    *** Voltage Equalization Circuit
69
70
           BL
                EQ BLB
    MNEQR
                           GND
                               nmos w = 6u 1 = 650n
    MNEQL1 BL
                 EQ HVCC GND
71
                               nmos w = 6u 1 = 650n
    MNEQL2 HVCC EQ BLB
                           GND
72
                                 nmos w = 6u 1 = 650n
73
    *** Sensing Circuit
74
            BL BLB SAN
                           GND
75
    MNSC1
                                nmos w = 5u l = 100n
76
    MNSC2
            SAN BL
                     BLB
                           GND
                                nmos w = 5u l = 100n
    MPSC1
            BL BLB SAP
                           VCC! pmos w = 10u l = 100n
77
    MPSC2 SAP BL
                     BLB
                           VCC! pmos w = 10u l = 100n
78
79
80
    * XSAN BL BLB inv Wp = 0.2 Wn = 0.1
81
82
    MNCT
                   WL
            BL
                         c1
                              GND
                                   nmos w = 5u l = 65n
    MNR
                   WL
                         BLB GND
83
            c2
                                   nmos w = 5u 1 = 65n
84
85
    CCT
            c1
                    gnd
                             1p
    CR
86
            c2
                    gnd
                             1p
87
88
    * MPRE1
              SAN
                      PRE
                              VCC!
                                     VCC!
                                             pmos w = 10u l = 65n
89
    * MPRE2
              SAP
                      PRE
                              VCC!
                                    VCC!
                                             pmos w = 10u l = 65n
90
    * .probe PWR_BLB = 'I(Mn5)'*'V(BLB)'
91
92
    * .probe PWR_BL = 'I(Mn6)'*'V(BL)'
93
    .tran
            1p
                   28ns
94
    * .MEAS TRAN AvgPower AVG(power) FROM=1pS TO=10ns
95
96
97
    .option post
98
    .end
```

List. 2: Result 2 with overloading - WL

```
*** HW3 Basic Sense Amplifier Circuit Diagram - DRAM ***
 1
 3
     .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
 4
     .unprotect
 5
     ***
 6
 7
     .param VCC = 1
     .param VOVER = 'VCC + 0.5'
 8
9
10
     .global VSS! VCC!
     VCC VCC! 0
                 dc VCC
11
    VSS VSS! 0
12
                   dc 0
13
     ***inverter
14
    ** Mos D G S B
15
     ** .ic 是初始偏壓值
16
17
     .subckt inv in out Wp = 1 Wn = 1
    Mp out in VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
18
19
    Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
20
     .ends
21
22
     .subckt buf in out
    xinv1 in 1 inv Wp = 20 Wn = 1
23
     xinv2 1 out inv Wp = 40 Wn = 1
24
25
     .ends
26
     * .IC v(C2)='VCC/2'
27
    * .IC v(BL) = 0
28
     * .IC v(BLB) = 0
30
    .IC V(SAN) = 0
     .IC V(SAP) = 0
31
32
33
                    VSS! pulse('VCC+0.4' 0 -0.5ns 0.05ns 0.05ns 2.5ns 10ns)
     * VWL
              WL
34
     * VINPUT INPUT VSS! pulse(0
                                      VCC -0.5ns 0.05ns 0.05ns 10ns 20ns)
              PRE
                                        0 0.5ns 0.05ns 0.05ns 2.5ns 10ns)
35
     * VPRE
                    VSS! pulse(VCC
36
    * VWE
              WE
                    VSS! pulse(VCC
                                         0 -0.5ns 0.05ns 0.05ns 5ns 10ns)
37
    * VEQ
                    VSS! pulse(0
                                            0.5ns 0.05ns 0.05ns 2ns 10ns)
              ΕQ
                                     VCC
38
    * VCSL
              CSL
                    VSS! pulse(VCC
                                     0 -0.5ns 0.05ns 0.05ns 4ns 10ns)
              HVCC VSS! dc VCC/2
    * VHVCC
39
40
41
42
    VWL
                  VSS! pulse(0 'VCC+0.5' 0.5ns 0.05ns 0.05ns 8.5ns 10ns)
             WL
    VINPUT
            INPUT VSS! pulse(0
                                   VCC 0.5ns 0.05ns 0.05ns 13.5ns 25ns)
43
     * VPRE
              PRE
                     VSS! pulse(0
                                   VCC -0.5ns 0.05ns 0.05ns 9.5ns 10ns)
44
                  VSS! pulse(0 'VCC' 0.5ns 0.05ns 0.05ns 3ns 14ns)
45
    VWE
             WE
                  VSS! pulse(VCC
                                   0 Ons 0.05ns 0.05ns 9ns 10ns)
46
     VEQ
47
     VCSL
                  VSS! pulse(0 'VCC' 0.5ns 0.05ns 0.05ns 4ns 13ns)
             CSL
48
     VHVCC
            HVCC VSS! dc VCC/2
49
50
    xinvinput INPUT INPUTB inv Wp = 0.2 Wn = 0.1
51
     * xinvinput1 INPUTB INPUT inv Wp = 0.2 Wn = 0.1
     * xinvout
                OUT
                      OUTB
                             inv Wp = 0.2 Wn = 0.1
                        OUT inv Wp = 0.2 Wn = 0.1
53
    * xinvout1
                OUTB
                             inv Wp = 0.2 Wn = 0.1
54
                    BLB
     * xinvbit
                BL
                             inv Wp = 0.2 Wn = 0.1
55
    * xinvbit1
                BLB
                       BL
56
57
```

```
58
    xbuf INPUT IN
                        buf
59
    xbufB INPUTB INB
                        buf
60
     *** Write Enable
61
                             gnd nmos w = 10u l = 65n
62
            IN
                  WE OUT
    MNWE1
63
    MNWE2
            INB
                  WE OUTB gnd nmos w = 10u l = 65n
64
65
                               gnd
66
    MNCSL1
             OUT
                   CSL
                         BL
                                    nmos w = 10u l = 65n
                                   nmos w = 10u l = 65n
    MNCSL2
             OUTB CSL
                         BLB gnd
67
68
     *** Voltage Equalization Circuit
69
70
                 EQ BLB
                            GND
                                 nmos w = 6u 1 = 650n
    MNEQR
            BL
                 EQ HVCC
71
    MNEQL1 BL
                           GND
                                 nmos w = 6u 1 = 650n
    MNEQL2 HVCC EQ BLB
                           GND
                                 nmos w = 6u 1 = 650n
72
73
74
     *** Sensing Circuit
            BL BLB SAN
                           GND
                                 nmos w = 5u l = 100n
75
    MNSC1
            SAN BL
    MNSC2
                     BLB
                            GND
                                 nmos w = 5u l = 100n
76
77
    MPSC1
            BL BLB SAP
                            VCC! pmos w = 10u l = 100n
    MPSC2
78
            SAP BL
                     BLB
                           VCC! pmos w = 10u l = 100n
79
     * XSAN BL BLB inv Wp = 0.2 Wn = 0.1
80
81
82
    MNCT
            BL
                   WL
                         c1
                              GND
                                    nmos w = 5u 1 = 65n
    MNR
                         BLB GND
83
            c2
                   WL
                                    nmos w = 5u 1 = 65n
84
85
    CCT
            c1
                    gnd
                              1p
86
    CR
            c2
                    gnd
                              1p
87
                                               pmos w = 10u l = 65n
    * MPRE1
              SAN
                      PRE
                               VCC!
                                      VCC!
88
89
     * MPRE2
              SAP
                      PRE
                               VCC!
                                      VCC!
                                              pmos w = 10u l = 65n
90
     * .probe PWR_BLB = 'I(Mn5)'*'V(BLB)'
91
92
     * .probe PWR_BL = 'I(Mn6)'*'V(BL)'
93
     .tran
             1p
                   28ns
94
     * .MEAS TRAN AvgPower AVG(power) FROM=1pS TO=10ns
95
96
97
     .option post
98
     .end
```