

# Code - HW1

## 記憶體積體電路 Memory Circuit Design

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### 1. DC Analysis-An Inverter

Listing 1: DC Analysis - An Inverter

```
1  *** Inverter ***
2  *** .protect
3  .inc "/home/bc/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5  ***
6  .param Vmax = 1
7  ***
8  .global VCC! VSS!
9  VCC    VCC! 0    dc Vmax
10 VSS    VSS! 0    dc 0
11
12 ***inverter
13 ** Mos D G S B
14 ** .ic 是初始偏壓值
15 .subckt inv in out Wp = 1 Wn = 1 VDD = 1
16 .ic VDD! = VDD
17 Mp out in VDD! VDD! pmos w= [Wp * 1u] l=65n m=1
18 Mn out in VSS! VSS! nmos w= [Wn * 1u] l=65n m=1
19 .ends
20
21 *** 1.a
22 xinv05 vin ratio05 inv Wp = 0.5 Wn = 1
23 xinv1 vin ratio1 inv Wp = 1 Wn = 1
24 xinv2 vin ratio2 inv Wp = 2 Wn = 1
25
26 *** 1.b
27 xinv4 vin V1 inv VDD = 1
28 xinv5 vin V08 inv VDD = 0.8
29 xinv6 vin V06 inv VDD = 0.6
30 xinv7 vin V04 inv VDD = 0.4
31
32 *** 訊號源
33 va vin VSS!
34
35 .dc va 0 Vmax 0.001V
36 .option post
37 *** 1.c 可以量 Ids
38 .probe dc I(xinv1.Mp)
```

```

39 .probe dc I(xinv1.Mn)
40
41 .probe dc I(xinv05.Mp)
42
43 .probe dc I(xinv2.Mp)
44 *** 1.d 去 lis 檔找資料, 繪圖
45 ** Way 1
46 .print Vo = V(ratio1)
47 .print Idd = I(xinv1.Mp)
48 ** 這是平均 power 不是題目要求
49 .meas dc pwr avg power from=0V to=1V
50 .end

```

## 2. Functionality of the Basic Gate

Please verify the functionality of the 2-to-1 NAND, NOR, XOR.

- NAND

Listing 2: Transient Analysis - An NAND

```

1  **NAND gate**
2  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
3  MP1 vout vain vdd vdd pmos W=3u L=0.065u
4  MP2 vout vbin vdd vdd pmos W=3u L=0.065u
5  MN1 vout vain NET1 NET1 nmos W=1.5u L=0.065u
6  MN2 NET1 vbin gnd gnd nmos W=1.5u L=0.065u
7
8  vdd vdd gnd dc 1
9  vain vain gnd pulse(0V 1V 0s 0.005ns 0.005ns 1.5ns 3ns)
10 vbin vbin gnd pulse(0V 1V 0s 0.005ns 0.005ns 3ns 6ns)
11
12 .tran 0.1ns 6ns
13 .option post=1
14
15 .print v(vout)
16 .print v(vain)
17 .print v(vbin)
18 .end

```

- NOR

Listing 3: Transient Analysis - An NOR

```

1  *** NOR Gate ***
2  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
3
4  MP1 NET1 vain vdd vdd pmos W=0.2u L=0.065u
5  MP2 vout vbin NET1 NET1 pmos W=0.2u L=0.065u
6  MN1 vout vain gnd gnd nmos W=0.1u L=0.065u
7  MN2 vout vbin gnd gnd nmos W=0.1u L=0.065u
8
9  vdd vdd gnd dc 1
10 vain vain gnd pulse(0V 1V 0s 0.005ns 0.005ns 1.5ns 3ns)
11 vbin vbin gnd pulse(0V 1V 0s 0.005ns 0.005ns 3ns 6ns)
12
13 .tran 0.1ns 6ns
14 .option post=1
15
16 .print v(vout)

```

```

17 .print v(vain)
18 .print v(vbin)
19 .end

```

## • XOR

Listing 4: Transient Analysis - An XOR

```

1  *** XOR Gate ***
2  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
3
4  ***
5  .param Vmax = 1
6  ***
7  .global VCC! VSS!
8  VCC    VCC! 0    dc Vmax
9  VSS    VSS! 0    dc 0
10
11
12 ***inverter
13 ** Mos D G S B
14 ** .ic 是初始偏壓值
15 .subckt inv in out Wp = 1 Wn = 1
16 Mp out in VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
17 Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
18 .ends
19
20 xinv1 a  abar  inv Wp = 0.2 Wn = 0.1
21 xinv2 b  bbar  inv Wp = 0.2 Wn = 0.1
22
23 * Mp vout b VDD! VDD! pmos w= 0.07u l=65n m=1
24 * Mn vout b NET1 VSS! nmos w= 0.5u l=65n m=1
25
26 MP1 4      b    VCC!    VCC!    pmos W=0.2u L=0.065u
27 MP2 vout  abar   4      VCC!    pmos W=0.2u L=0.065u
28 MP3 3      a    VCC!    VCC!    pmos W=0.2u L=0.065u
29 MP4 vout  bbar   3      VCC!    pmos W=0.2u L=0.065u
30
31 MN1 vout  abar  1      VSS!    nmos W=0.1u L=0.065u
32 MN2 1      bbar VSS!    VSS!    nmos W=0.1u L=0.065u
33 MN3 vout  a     2      VSS!    nmos W=0.1u L=0.065u
34 MN4 2      b    VSS!    VSS!    nmos W=0.1u L=0.065u
35
36 vain a VSS! pulse(1V 0V 0s 0.005ns 0.005ns 1.5ns 3ns)
37 vbin b VSS! pulse(1V 0V 0s 0.005ns 0.005ns 3ns 6ns)
38
39 .tran 0.1ns 6ns
40 .option post=1
41 .end

```

### 3. Functionality of the Transmission Gate

Please verify the functionality of transmission gate.

Listing 5: Transient Analysis - An Transmission Gate

```
1  *** Transmission Gate ***
2  *** .protect
3  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5  ***
6  .param Vmax = 1
7  ***
8  .global VDD! VSS!
9  VCC    VDD! 0    dc Vmax
10 VSS    VSS! 0    dc 0
11
12 ***inverter
13 .subckt inv in out Wp = 1 Wn = 1
14 Mp out in VDD! VDD! pmos w= [Wp * 1u] l=65n m=1
15 Mn out in VSS! VSS! nmos w= [Wn * 1u] l=65n m=1
16 .ends
17 *** TG : Transmission Gate
18 .subckt TG in out Wp = 1 Wn = 1
19 Mp out enbar in VDD! pmos w= [Wp * 1u] l=65n m=1
20 xinv en enbar inv
21 Mn out en in VSS! nmos w= [Wn * 1u] l=65n m=1
22 .ends
23
24 xtg1 vin vout TG Wp = 0.5 Wn = 1
25
26 v1 vin gnd pulse(0V 1V 0s 0.005ns 0.005ns 2ns 4ns)
27
28 .tran 0.1ns 6ns
29 .option post=1
30 .end
```

## 4. Functionality of the Basic Gate

Please verify the functionality of the 4-to-1 MUX.

Listing 6: Transient Analysis - An 4-to-1 MUX

```
1  *** 4-to-1 MUX ***
2  *** .protect
3  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5  ***
6  .param Vmax = 1
7  .param per1 = 'pw1*2' per2 = 'pw2*2' per3 = 'pw3*2' per4 = 'pw4 * 2' per5 =
   ↳ 'pw5*2' per6 = 'pw6*2' per7 = 'pw7*2'
8  .param pw1 = 4n pw2 = 8n pw3 = 16n pw4 = 32n pw5 = 64n pw6 = 128n pw7 =
   ↳ 256n
9  .param n = 0.4
10 .param p = 0.4
11 ***
12 .global VDD! VSS!
13 VCC VDD! 0 dc Vmax
14 VSS VSS! 0 dc 0
15
16 ***inverter
17 .subckt inv in out Wp = 2 Wn = 1
18 Mp out in VDD! VDD! pmos w= 'Wp * 1u' l=65n m=1
19 Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
20 .ends
21
22 *** TG : Transmission Gate
23 .subckt TG in out en enbar Wp = 1 Wn = 1
24 Mp out enbar in VDD! pmos w= 'Wp * 1u' l=65n m=1
25 Mn out en in VSS! nmos w= 'Wn * 1u' l=65n m=1
26 .ends
27
28 xinv0 s0 s0bar inv Wp = p Wn = n
29 xinv1 s1 s1bar inv Wp = p Wn = n
30
31 xt看1 d0 NET0 s0bar s0 TG Wp = p Wn = n
32 xt看2 d1 NET0 s0 s0bar TG Wp = p Wn = n
33 xt看3 d2 NET1 s0bar s0 TG Wp = p Wn = n
34 xt看4 d3 NET1 s0 s0bar TG Wp = p Wn = n
35 xt看5 NET1 vout s1 s1bar TG Wp = p Wn = n
36 xt看6 NET0 vout s1bar s1 TG Wp = p Wn = n
37
38
39 vs1 s1 gnd pulse(1V 0V 0s 0.005ns 0.005ns pw6 per6)
40 vs0 s0 gnd pulse(1V 0V 0s 0.005ns 0.005ns pw5 per5)
41 vd3 d3 gnd pulse(1V 0V 0s 0.005ns 0.005ns pw4 per4)
42 vd2 d2 gnd pulse(1V 0V 0s 0.005ns 0.005ns pw3 per3)
43 vd1 d1 gnd pulse(1V 0V 0s 0.005ns 0.005ns pw2 per2)
44 vd0 d0 gnd pulse(1V 0V 0s 0.005ns 0.005ns pw1 per1)
45
46 .tran 0.1ns per6
47 .option post=1
48
49 .end
```

## 5. Functionality of the Decoder

Please verify the functionality of the 3-to-8 decoder.

Listing 7: Transient Analysis - An 3-to-8 Decoder

```
1  *** 3-to-8 decoder ***
2  *** .protect
3  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5  ***
6  .param Vmax = 1
7  .param per1 = ['pw1*2'] per2 = ['pw2*2'] per3 = ['pw3*2'] per4 = ['pw4 * 2'] per5 =
   ↳ ['pw5*2'] per6 = ['pw6*2'] per7 = ['pw7*2']
8  .param pw1 = 4n pw2 = 8n pw3 = 16n pw4 = 32n pw5 = 64n pw6 = 128n pw7 =
   ↳ 256n
9  .param n = 0.4
10 .param p = 0.4
11 ***
12 .global VDD! VSS!
13 VCC VDD! 0 dc Vmax
14 VSS VSS! 0 dc 0
15
16 ***inverter
17 .subckt inv in out Wp = 2 Wn = 1
18 Mp out in VDD! VDD! pmos w= ['Wp * 1u'] l=65n m=1
19 Mn out in VSS! VSS! nmos w= ['Wn * 1u'] l=65n m=1
20 .ends
21
22 *** AND : Transmission Gate
23 .subckt AND in1 in2 in3 in4 out Wp = 2 Wn = 1
24 Mn1 1 in1 gnd gnd nmos w= ['Wn * 1u'] l=65n m=1
25 Mn2 2 in2 1 gnd nmos w= ['Wn * 1u'] l=65n m=1
26 Mn3 3 in3 2 gnd nmos w= ['Wn * 1u'] l=65n m=1
27 Mn4 nout in4 3 gnd nmos w= ['Wn * 1u'] l=65n m=1
28
29 Mp1 nout in1 VDD! VDD! pmos w= ['Wp * 1u'] l=65n m=1
30 Mp2 nout in2 VDD! VDD! pmos w= ['Wp * 1u'] l=65n m=1
31 Mp3 nout in3 VDD! VDD! pmos w= ['Wp * 1u'] l=65n m=1
32 Mp4 nout in4 VDD! VDD! pmos w= ['Wp * 1u'] l=65n m=1
33
34 xinv nout out inv
35 .ends
36
37 xinv0 a abar inv Wp = p Wn = n
38 xinv1 b bbar inv Wp = p Wn = n
39 xinv2 c cbar inv Wp = p Wn = n
40
41 xAND1 en abar bbar cbar d0 AND Wp = p Wn = n
42 xAND2 en a bbar cbar d1 AND Wp = p Wn = n
43 xAND3 en abar b cbar d2 AND Wp = p Wn = n
44 xAND4 en a b cbar d3 AND Wp = p Wn = n
45 xAND5 en abar bbar c d4 AND Wp = p Wn = n
46 xAND6 en a bbar c d5 AND Wp = p Wn = n
47 xAND7 en abar b c d6 AND Wp = p Wn = n
48 xAND8 en a b c d7 AND Wp = p Wn = n
49
50 vd3 en gnd pulse(1V 0V 0s 0.005ns 0.005ns pw4 per4)
51 vd2 c gnd pulse(1V 0V 0s 0.005ns 0.005ns pw3 per3)
```

```
52 vd1 b gnd pulse(1V 0V 0s 0.005ns 0.005ns pw2 per2)
53 vd0 a gnd pulse(1V 0V 0s 0.005ns 0.005ns pw1 per1)
54
55 .tran 0.1ns per4
56 .option post=1
57
58 .end
```