Code - HW2

記憶體積體電路 Memory Circuit Design

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1. DC Analysis

1.1. 6T SRAM

做 Decouple，畫雙曲線。
要 RSNM 圖，X-Y 軸分別為 VIN-Q1，和 Q1-VIN。
要 WNM 圖，X-Y 軸分別為 VIN-Q1，和 Q2-VIN。

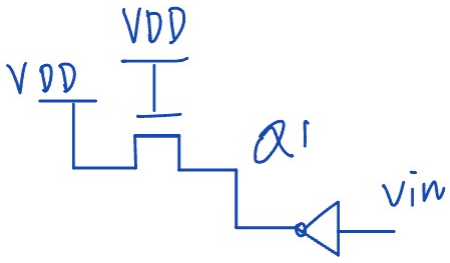

Fig. 1: Decouple (to VDD)

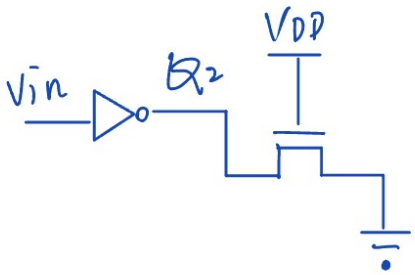

Fig. 2: Decouple (to GND)

List. 1: DC Analysis - 6T SRAM

```
*** SRAM 6T curve ***
*** .protect
.inc "/home/college/c109501201/Memory/65nm_bulk.pm"
.unprotect
***
.param V1 = 1
.param V08 = 0.8
.param V06 = 0.6
.param V04 = 0.4
***
.global VDD1! VSS! VDD08! VDD06! VDD04!
VDD1   VDD1! 0    dc V1
VDD08  VDD08! 0   dc V08
VDD06  VDD06! 0   dc V06
VDD04  VDD04! 0   dc V04
VSS    VSS! 0    dc  0

***inverter
```

```
** Mos D G S B
** .ic 是初始偏壓值
.subckt inv in out Wp = 1 Wn = 1 VDD = V1
.ic VDD! = VDD
Mp out in VDD! VDD! pmos w= 'Wp * 1u' l=65n m=1
Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
.ends

*** source
va vin gnd


*** Vdd = 1V read write
xinv1 vin 1 inv VDD = V1 Wp = 0.25 Wn = 0.2
Mn1 VDD1!  VDD1! 1 gnd nmos w = 0.2u l = 0.065u

*** Vdd = 1V write
xinv5 vin 5 inv VDD = V1 Wp = 0.25 Wn = 0.2
Mn5 5  VDD1! gnd gnd nmos w = 0.2u l = 0.065u

*** Vdd = 0.8V read write
xinv2 vin 2 inv VDD = V08 Wp = 0.25 Wn = 0.2
Mn2 VDD08! VDD08! 2 gnd nmos w = 0.2u l = 0.065u

*** Vdd = 0.8V write
xinv6 vin 6 inv VDD = V08 Wp = 0.25 Wn = 0.2
Mn6 6  VDD08! gnd gnd nmos w = 0.2u l = 0.065u

*** Vdd = 0.6V read write
xinv3 vin 3 inv VDD = V06 Wp = 0.25 Wn = 0.2
Mn3 VDD06! VDD06! 3 gnd nmos  w = 0.2u l = 0.065u

*** Vdd = 0.6V write
xinv7 vin 7 inv VDD = V06 Wp = 0.25 Wn = 0.2
Mn7 7  VDD06! gnd gnd nmos w = 0.2u l = 0.065u

*** Vdd = 0.4V read write
xinv4 vin 4 inv VDD = V04 Wp = 0.15 Wn = 0.1
Mn4 VDD04! VDD04! 4 gnd nmos w= 0.3u l = 0.1u

*** Vdd = 0.4V write write
xinv8 vin 8 inv VDD = V04 Wp = 0.15 Wn = 0.1
Mn8 8  VDD04! gnd gnd nmos w = 0.3u l = 0.1u

*** only the first dc is effective
.dc va 0 V06 0.02V
.dc va 0 V08 0.02V
.dc va 0 V1 0.02V
.dc va 0 V04 0.01V
.option post
.end
```

1.2. 8T SRAM

做 Decouple，畫雙曲線。
要 RSNM 圖，X-Y 軸分別為 Q-QB，和 QB-Q。

要 WNM 圖，X-Y 軸分別為 Q-QB，和 QB1-Q。

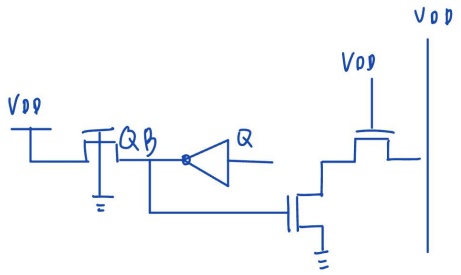

Fig. 3: Decouple (to VDD)

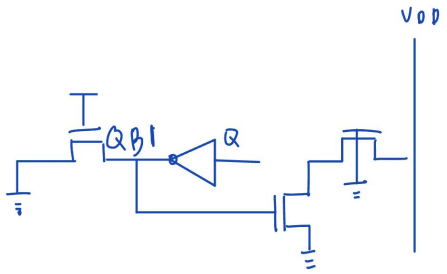

Fig. 4: Decouple (to GND)

List. 2: DC Analysis - 8T SRAM

```
1  * 8T SRAM Cell - HSPICE Netlist
2  * .protect
3  .include "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5
6  * Parameters
7  .param V1 = 1
8  .param V08 = 0.8
9  .param V06 = 0.6
10 .param V04 = 0.4
11
12 *** 改這裡
13 .param VDD = 'V04'
14
15
16 * Global Nodes
17 .global VDD! VSS!
18 * Power Supplies
19 VDD   VDD! 0 dc VDD
20 VSS    VSS! 0 dc 0
21
22 * Inverter Subcircuit
23 .subckt inv in out Wp=1 Wn=1 VDD=VDD
24 .IC VDD = VDD
25 Mpos out in VDD VDD PMOS L=65n W='Wp*1u' AD=1 PD=1
26 Mneg out in VSS! VSS! NMOS L=65n W='Wn*1u' AD=1 PD=1
27 .ends
28
29 * Source
30 VBLB BLB GND dc VDD
31 ** 注意 WL = 0V
32 Vw WL GND dc 0
33 VRDWL RDWL 0 dc VDD
34 VRDBL RDBL 0 dc VDD
35 VQ Q 0 dc 0
36 Vwl1 WL1 GND dc VDD
37 VBL0 BL0 GND dc 0
38 VRDW0 RDW0 GND dc 0
39 .param p1 = 0.7
40 .param n1 = 0.4
41 .param w1 = 0.6u
```

```
.param l1 = 0.065u
* Read Operation
MN8 RDBL RDWL X GND NMOS W=w1 L=l1
MN9 X QB GND GND NMOS W=w1 L=l1
xinv2 Q QB  inv VDD=VDD Wp=p1 Wn= n1
MN5 BLB WL QB GND NMOS W=w1 L=l1

* Write Operation
MN81 RDBL RDW0 X1 GND NMOS W=w1 L=l1
MN91 X1 QB1 GND GND NMOS W=w1 L=l1
xinv4 Q QB1  inv VDD=VDD Wp=p1 Wn= n1
MN51 BL0 WL1 QB1 GND NMOS W=w1 L=l1

* DC Analysis
.dc VQ 0 VDD 0.01V

.option post
.end
```

2. Transient Analysis

2.1. 6T SRAM

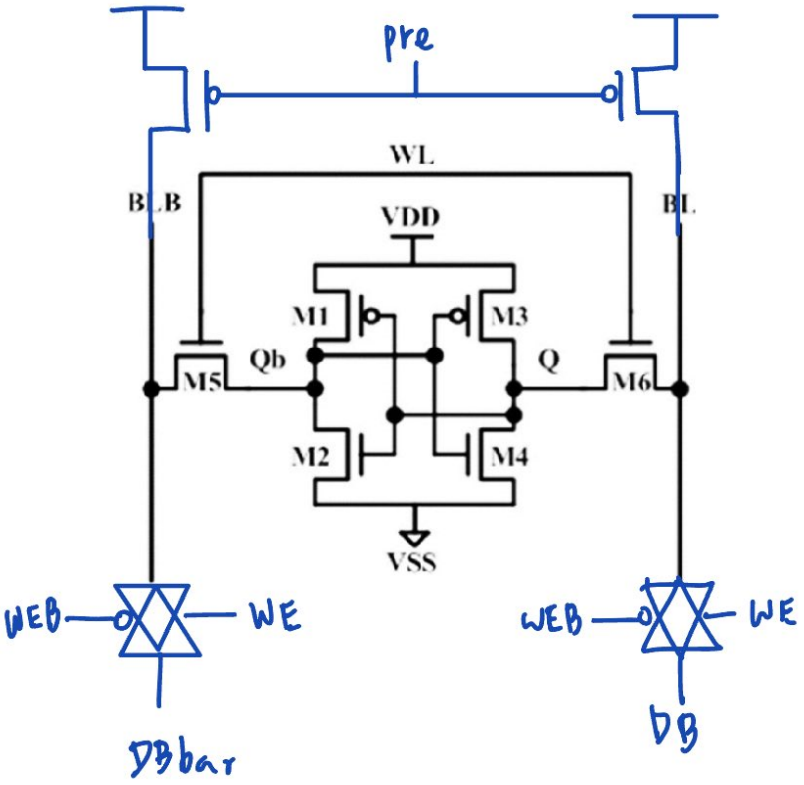

Fig. 5: Transient Analysis - 6T SRAM

List. 3: Transient Analysis - 6T SRAM

```
*** SRAM6T Transient Analysis ***
*** .protect
```

```
.inc "/home/college/c109501201/Memory/65nm_bulk.pm"
.unprotect
***

.param VDD = 0.8
***
.global VSS! VDD!
VDD  VDD! 0   dc VDD
VSS    VSS! 0    dc  0

***inverter
** Mos D G S B
** .ic 是初始偏壓值
.subckt inv in out Wp = 1 Wn = 1
Mp out in VDD! VDD! pmos w= 'Wp * 1u' l=65n m=1
Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
.ends

VWL   WL VSS! pulse(VDD 0V 0ns 0.05ns 0.05ns 2ns 4ns)
VPRE PRE VSS! pulse(0V VDD -1ns 0.05ns 0.05ns 5ns 8ns)
VWE   WE VSS! pulse(0V VDD 0ns 0.05ns 0.05ns 4ns 8ns)
VD    D VSS! pulse(VDD 0 0ns 0.05ns 0.05ns 8ns 16ns)
VDB DBbar VSS! pulse(0 VDD 0ns 0.05ns 0.05ns 8ns 16ns)
xweb WE WEB inv Wp = 0.25 Wn = 0.2

Mp1 BL PRE  VDD! VDD! pmos w = 0.1u l = 65n
Mp2 BLB PRE VDD! VDD! pmos w = 0.1u l = 65n

Mn1 D     WE BL  gnd nmos w = 0.1u l =65n
Mp3 D     WEB BL  gnd pmos w = 0.1u l =65n
Mn2 DBbar WE BLB gnd  nmos w =  0.1u l =65n
Mp4 DBbar WEB BLB gnd pmos w = 0.1u l =65n
*** read source
* Vpre pre VSS! pulse(0V 0.8V 0.5ns 0.05ns 0.05ns 2ns 4ns)

*** 要改
* .IC V(Q) = VDD
* VBL preBL VSS! pulse(0.8V 0V 0ns 0.05ns 0.05ns 4ns 16ns)
* VBLB preBLB VSS! pulse(0V 0.8V 0ns 0.05ns 0.05ns 8ns 12ns)
* .IC V(BL)=VDD
* .IC V(BLB)=VDD

*** Write Source
* .IC V(Q) = 0
* vblin BL VSS! pulse(0V 0.8V 0ns 0.5ns 0.5ns 1ns 4ns)
* vblbin BLB VSS! pulse(0.8V 0V 0ns 0.5ns 0.5ns 1ns 4ns)

xinv1 QB Q inv Wp = 0.25 Wn = 0.2
Mn6 Q WL BL  gnd nmos w = 0.3u l = 0.2u

xinv2 Q QB inv Wp = 0.25 Wn = 0.2
Mn5  QB WL BLB gnd nmos w = 0.3u l = 0.2u

*** Power Analysis
.probe PWR_BLB =  'I(Mn5)'*'V(BLB)'
.probe PWR_BL =  'I(Mn6)'*'V(BL)'
.tran    1p    17ns
.MEAS TRAN AvgPower AVG(power) FROM=1pS TO=10ns
```

```
61
62  .option post
63  .end
```

2.2. 8T SRAM

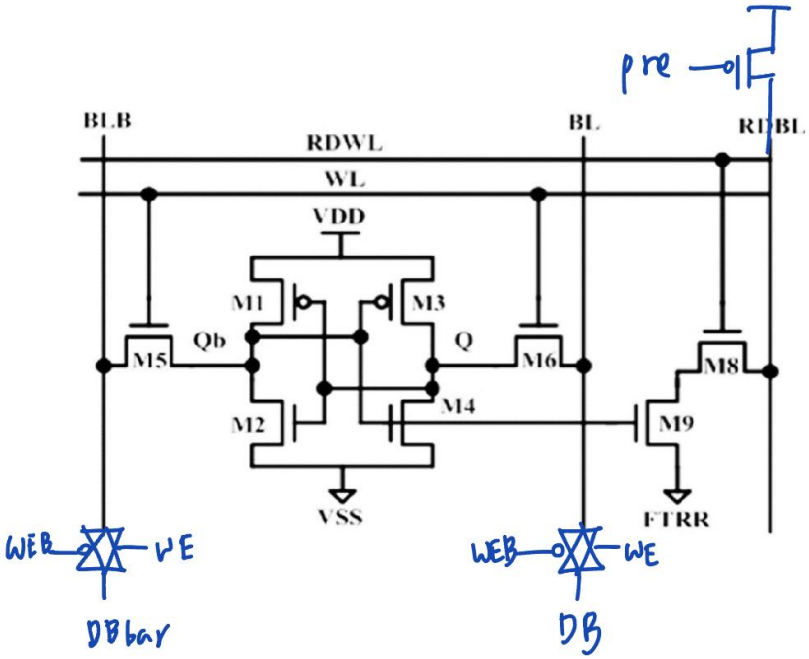

Fig. 6: Transient Analysis - 8T SRAM

List. 4: Transient Analysis - 8T SRAM

```
1   *** SRAM8T Transient Analysis ***
2   *** .protect
3   .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4   .unprotect
5   ***
6
7   .param VDD = 0.8
8   ***
9   .global VSS! VDD!
10  VDD  VDD! 0   dc VDD
11  VSS    VSS! 0    dc  0
12
13  ***inverter
14  ** Mos D G S B
15  ** .ic 是初始偏壓值
16  .subckt inv in out Wp = 1 Wn = 1
17  Mp out in VDD! VDD! pmos w= 'Wp * 1u' l=65n m=1
18  Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
19  .ends
20
21
22  VWL   WL VSS! pulse(VDD 0V 0ns 0.05ns 0.05ns 2ns 4ns)
23  VPRE PRE VSS! pulse(0V VDD -1ns 0.05ns 0.05ns 5ns 8ns)
```

```
VWE   WE VSS! pulse(0V VDD 0ns 0.05ns 0.05ns 4ns 8ns)
VD    D VSS! pulse(VDD 0 0ns 0.05ns 0.05ns 8ns 16ns)
VDB DBbar VSS! pulse(0 VDD 0ns 0.05ns 0.05ns 8ns 16ns)
VRDWL RDWL VSS! dc VDD
xweb WE WEB inv Wp = 0.25 Wn = 0.2

Mpl RDBL PRE  VDD! VDD! pmos w = 0.1u l = 65n

Mn1 D     WE BL  gnd nmos w = 0.1u l =65n
Mp3 D     WEB BL  gnd pmos w = 0.1u l =65n
Mn2 DBbar WE BLB gnd  nmos w =  0.1u l =65n
Mp4 DBbar WEB BLB gnd pmos w = 0.1u l =65n

*** Read source
* VRDWL RDWL  VSS! pulse(0V 0.8V 0.5ns 0.1ns 0.1ns 1ns 2ns)
* VWL WL VSS! dc 0
* .IC V(Q)=VDD
* .IC V(RDBL)=VDD
* VPRE PRE VSS! pulse(0V 0.8V 0.5ns 0.5ns 0.5ns 1ns 2ns)

* .IC V(BL)=VDD
* .IC V(BLB)=VDD

*** Write source
* .IC V(Q) = 0
* VWL WL  VSS! pulse(0V 0.8V 0.5ns 0.05ns 0.05ns 1ns 2ns)
* vblin BL VSS! pulse(0V 0.8V 0ns 0.5ns 0.5ns 1ns 4ns)
* vblbin BLB VSS! pulse(0.8V 0V 0ns 0.5ns 0.5ns 1ns 4ns)

* MPpre RDBL PRE VDD! VDD!  pmos W=0.5u L=65n

xin1 QB Q inv Wp=0.13 Wn=0.13
MN8 RDBL RDWL X GND NMOS W=0.5u L=65n
MN9 X QB GND GND NMOS W=0.5u L=65n
MN6 BL WL Q GND NMOS W=0.3u L=0.16u
xinv2 Q QB  inv Wp=0.13 Wn=0.13
MN5 BLB WL QB GND NMOS W=0.3u L=0.16u

*** Power Analysis
.probe PWR_BLB =  'I(MN5)'*'V(BLB)'
.probe PWR_BL =  'I(MN6)'*'V(BL)'

.tran    1p    16ns
.MEAS TRAN AvgPower AVG(power) FROM=1pS TO=10ns
.option post
.end
```

3. Power Analysis

2、3 題 Code 同一份。

Matlab Code for Question 1

List. 5: Matlab code for Q1

```
% Specify the Excel file path
excelFilePath = "D:\Document\Senior\Memory_Circuit_Design\HW2\SRAM8T.xlsx";
% Read data from Excel
data = xlsread(excelFilePath, 4);

close;
% Extract data
VI = data(:, 1);  % Assuming VI is in the first column
VOr = data(:, 2);
VOw = data(:, 3);
%VOgnd = data(:, 2);  % Assuming VO is in the second column
%VOVdd = data(:, 3);

% Plot SNM
figure(1);
width=500;% 宽度，像素数
height=500;% 高度
left=200;% 距屏幕左下角水平距离
bottem=200;% 距屏幕左下角垂直距离
set(gcf,'position',[left,bottem,width,height])
plot(VI, VOr, 'b-', 'LineWidth', 2);
hold on;
plot(VOr, VI, 'g-', 'LineWidth', 2);
hold on;

figure(2);
width=500;% 宽度，像素数
height=500;% 高度
left=200;% 距屏幕左下角水平距离
bottem=200;% 距屏幕左下角垂直距离
set(gcf,'position',[left,bottem,width,height])
plot(VI, VOr, 'b-', 'LineWidth', 2);
hold on;
plot(VOw, VI, 'g-', 'LineWidth', 2);
hold on;
```