HW2

記憶體積體電路 Memory Circuit Design

電機 4A　109501201　陳緯亭

November 16, 2023

1. **DC Analysis: Please compare the curves of RSNM and WNM for 6T, 8T SRAM cell with different VDD= 1V, 0.8V, 0.6V, and 0.4V. Also, with different VDD= 1V, 0.8V, 0.6V, and 0.4V, please extract the values of the RSNM and WNM, which are defined as the diagonal line of the maximal square between two curves of RSNM or WNM plots.**

下圖為 HSPICE 模擬後，貼入 excel 。再來用 Matlab 讀取繪製出來的圖形。方形量測與繪製使用 ImageJ 軟體。

1.1　6T SRAM

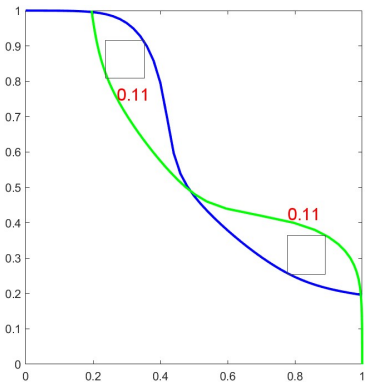

Fig. 1: RSNM $V_{DD} = 1V$

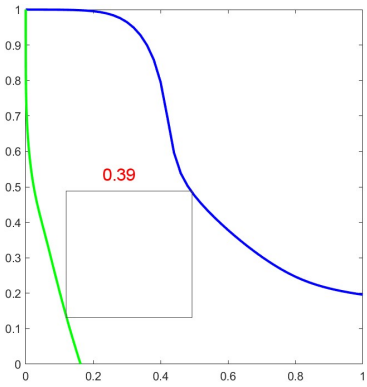

Fig. 2: WNM $V_{DD} = 1V$

對 V_{DD} = 1V，RSNM = 0.156V ，WNM = 0.552V

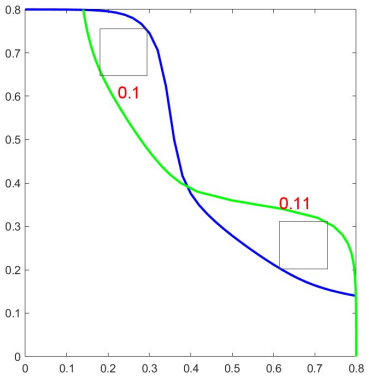

Fig. 3: RSNM $V_{DD} = 0.8V$

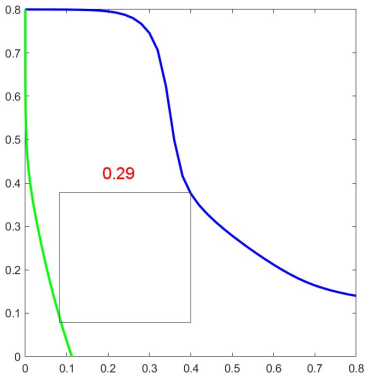

Fig. 4: WNM $V_{DD} = 0.8V$

對 V_{DD} = 0.8V，RSNM = 0.141V ，WNM = 0.410V

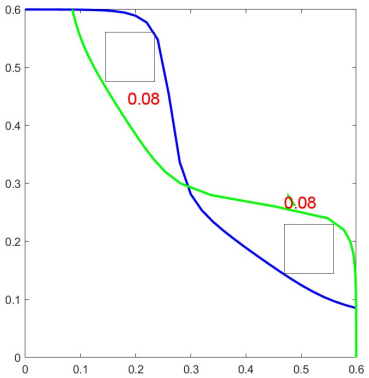

Fig. 5: RSNM $V_{DD} = 0.6V$

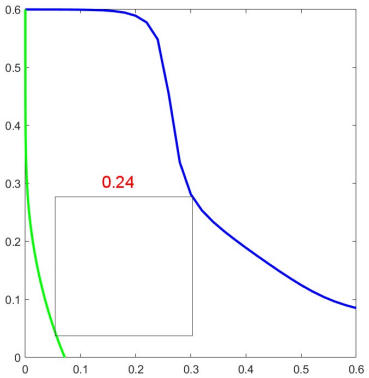

Fig. 6: WNM $V_{DD} = 0.6V$

對 V_{DD} = 0.6V，RSNM = 0.113V ，WNM = 0.339V

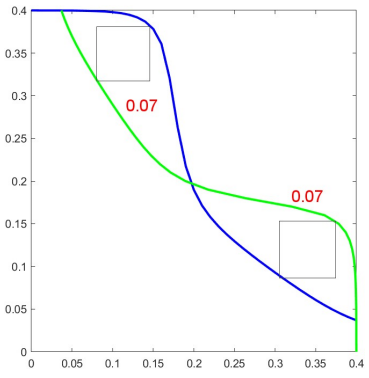

Fig. 7: RSNM $V_{DD} = 0.4V$

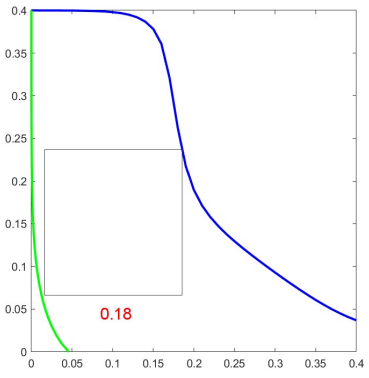

Fig. 8: WNM $V_{DD} = 0.4V$

對 V_{DD} = 0.4V，RSNM = 0.099V ，WNM = 0.255V

根據 Fig.1、Fig.3、Fig.5 和 Fig.7可以發現 RSNM 會隨著，VDD 變小逐漸變小，與之成正比。而且因為 Voltage dividend 的關係，在圖形開頭與結尾處會有一個空白區間。根據 Fig.2、Fig.4、Fig.6 和 Fig.8可以發現 WNM 也會隨著，VDD 變小逐漸變小，與之成正比。通常在同一 VDD 下，RSNM 都會小於 WNM。

1.2 8T SRAM

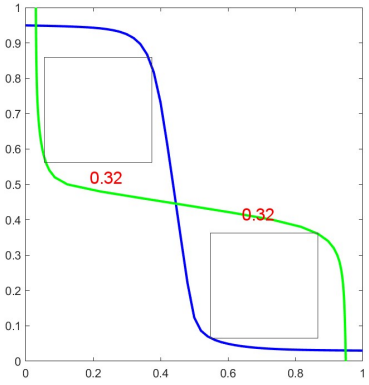

Fig. 9: RSNM $V_{DD} = 1V$

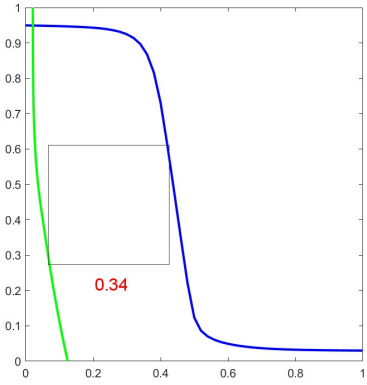

Fig. 10: WNM $V_{DD} = 1V$

對 V_{DD} = 1V，RSNM = 0.453V ，WNM = 0.481V

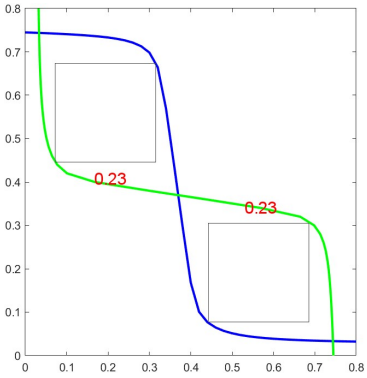

Fig. 11: RSNM $V_{DD} = 0.8V$

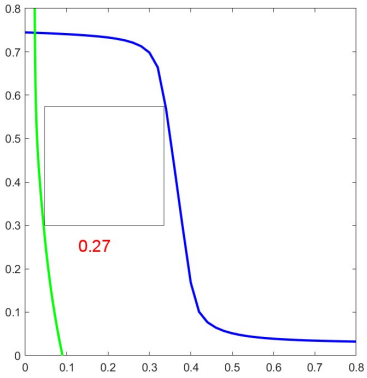

Fig. 12: WNM $V_{DD} = 0.8V$

對 V_{DD} = 0.8V，RSNM = 0.325V ，WNM = 0.382V

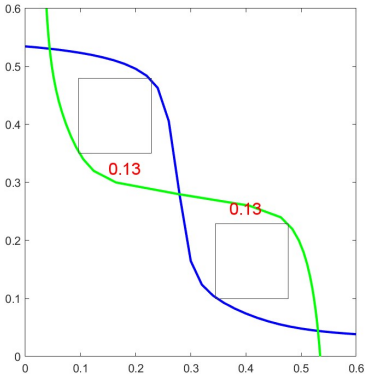

Fig. 13: RSNM $V_{DD} = 0.6V$

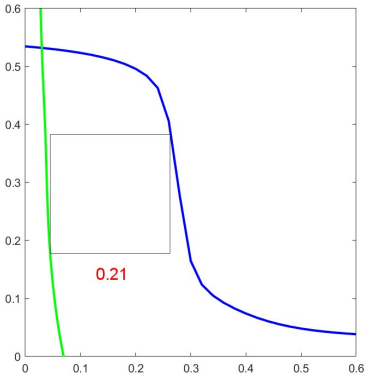

Fig. 14: WNM $V_{DD} = 0.6V$

對 V_{DD} = 0.6V，RSNM = 0.184V ，WNM = 0.297V

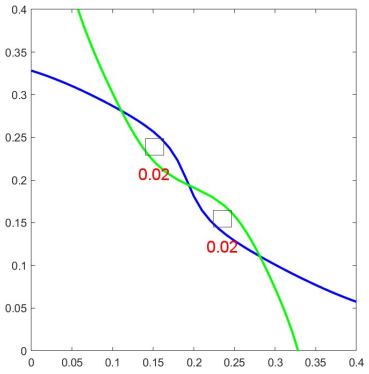

Fig. 15: RSNM $V_{DD} = 0.4V$

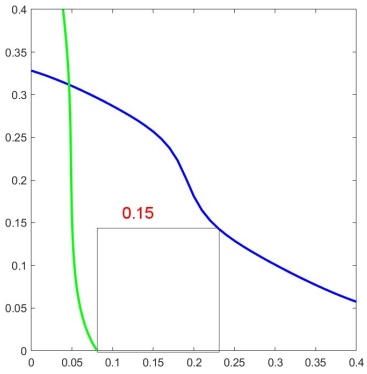

Fig. 16: WNM $V_{DD} = 0.4V$

對 V_{DD} = 0.4V，RSNM = 0.028V ，WNM = 0.212V

根據 Fig.9、Fig.11、Fig.13 和 Fig.15可以發現 RSNM 會隨著，VDD 變小逐漸變小，與之成正比。而且沒有 Voltage dividend 的問題，在圖形開頭與結尾無空白區間。根據 Fig.10、Fig.12、Fig.14 和 Fig.16可以發現 WNM 也會隨著，VDD 變小逐漸變小，與之成正比。通常在同一 VDD 下，RSNM 都會小於 WNM。

2. AC Analysis: Please show the BL (BLB) voltage transient curves of 6T, 8T SRAM during READ and WRITE. You may need toapply appropriate pulses on the WL or BL to READ or to WRITE the cells with VDD=0.8V and the pulse width equivalent to 2ns.

2.1 6T SRAM

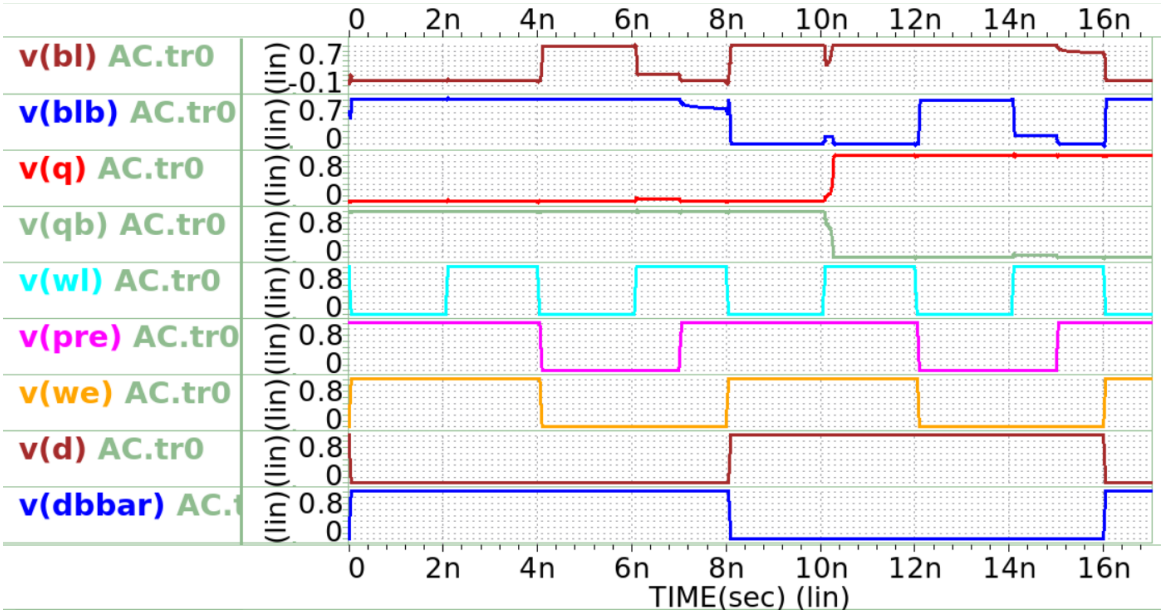

Fig. 17: Transient curves of 6T SRAM

Fig.17，操作依序為 WRITE-0、READ-0、WRITE-1、READ-1。
v(d) 和 v(dbbar) 分別決定寫入 v(BL) 和 v(BLB) 的值。v(we)，是決定寫入 d 和 dbar 資訊到 BL 和 BLB。v(pre) 是 Read 之前要先預充電。以下 Fig.18 - Fig.21為分段解釋。

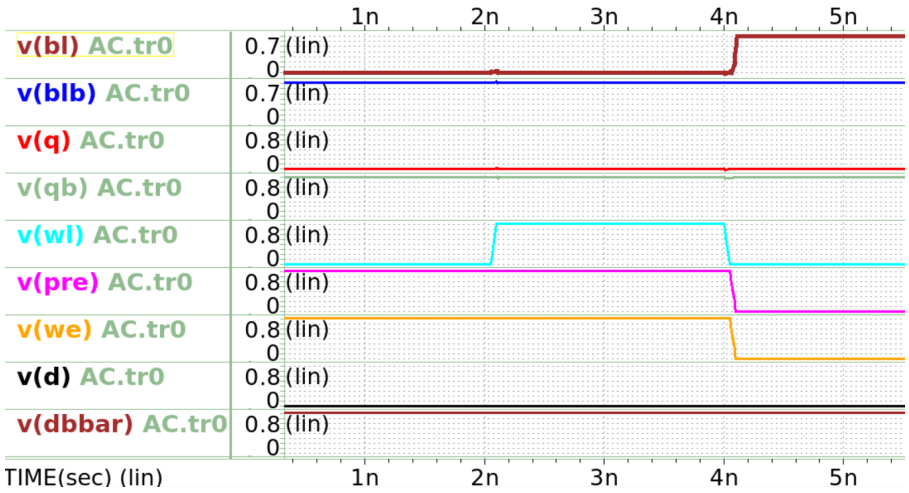

Fig. 18: 6T SRAM Write-0

Fig.18，在寫入值時，不需要 precharge 所以 v(pre) 為 VDD (pmos off)。v(d) = 0、v(dbbar) = VDD 才能寫 0 進去。

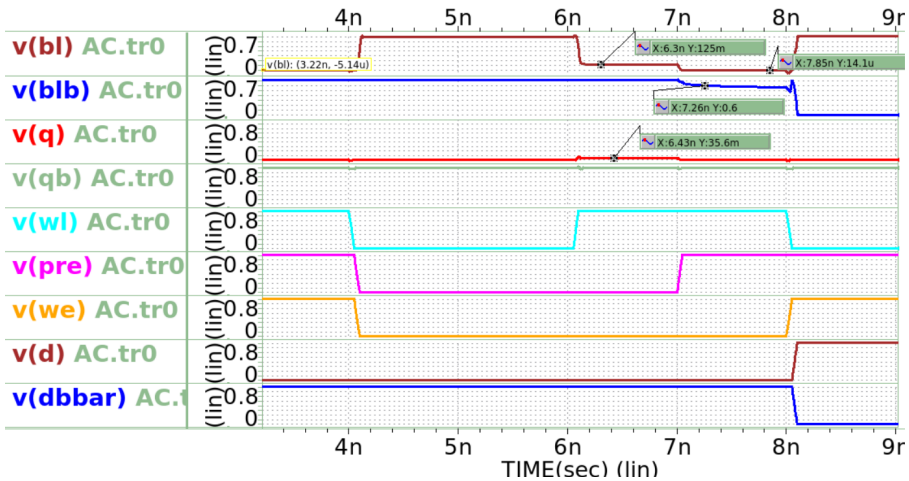

Fig. 19: 6T SRAM Read-0

Fig.19，在讀取值時，需要 precharge 所以 v(pre) 為 0 (pmos on)。v(d)。v(pre) 在 6T SRAM 為寫入狀態持續打開的話，會影響到電壓 v(BL) 會變得大一點，但不影響讀取。

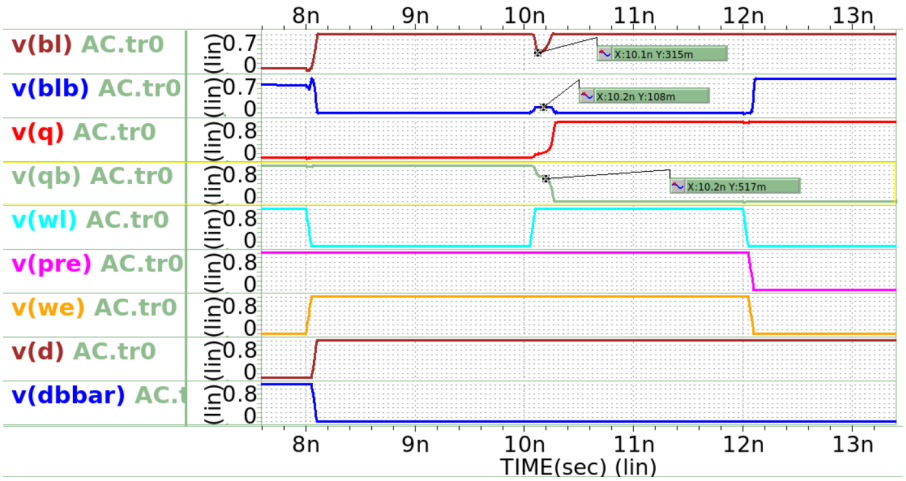

Fig. 20: 6T SRAM Write-1

Fig.20，在寫入值時，不需要 precharge 所以 v(pre) 為 VDD (pmos off)。v(d) = VDD、v(dbbar) = 0 才能寫 1 進去。

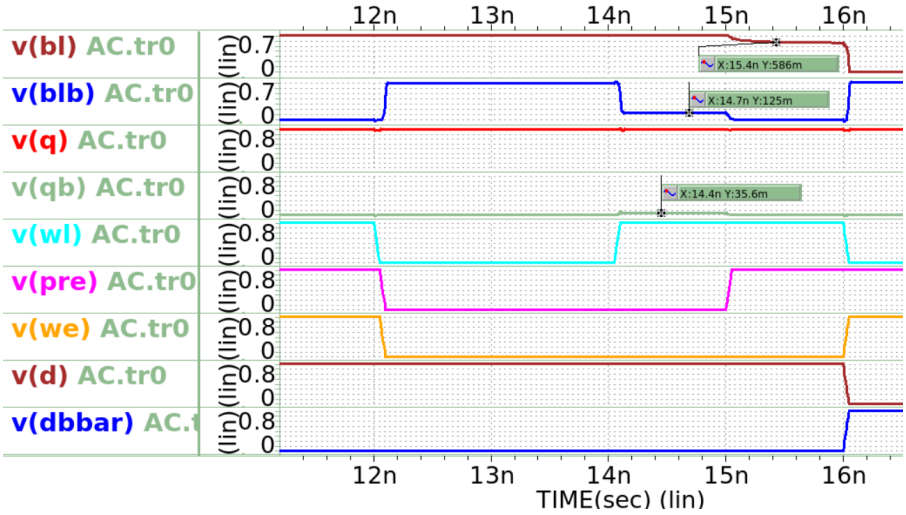

Fig. 21: 6T SRAM Read-1

Fig.21，在讀取值時，需要 precharge 所以 v(pre) 為 0 (pmos on)。v(d)。v(pre) 在 6T SRAM 為寫入狀態持續打開的話，會影響到電壓 v(BLB) 會變得大一點，但不影響讀取。

2.2 8T SRAM

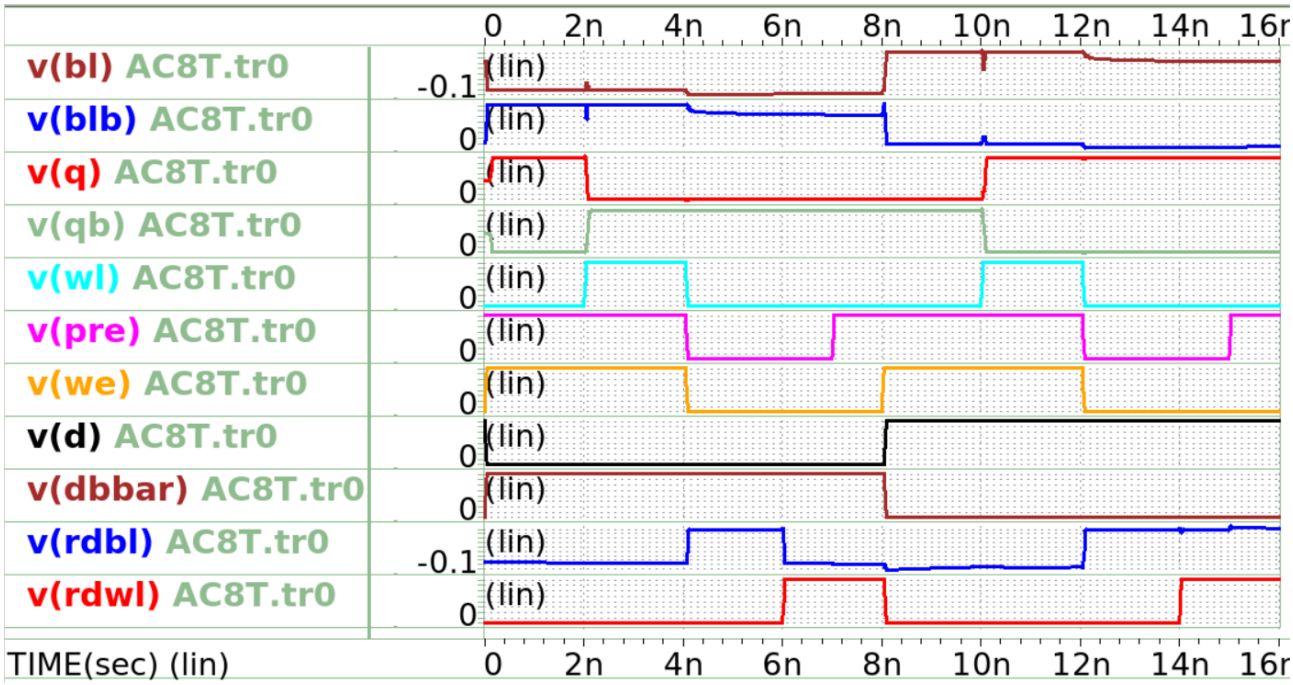

Fig. 22: Transient curves of 8T SRAM

Fig.22，操作依序為 WRITE-0、READ-0、WRITE-1、READ-1。v(d) 和 v(dbbar) 分別決定寫入 v(BL) 和 v(BLB) 的值。v(we)，是決定寫入 d 和 dbar 資訊到 BL 和 BLB。v(pre) 是 Read 之前要先預充電。r(rdwl) 決定是否要讀取，r(rdbl) 為讀取出來的電壓值。

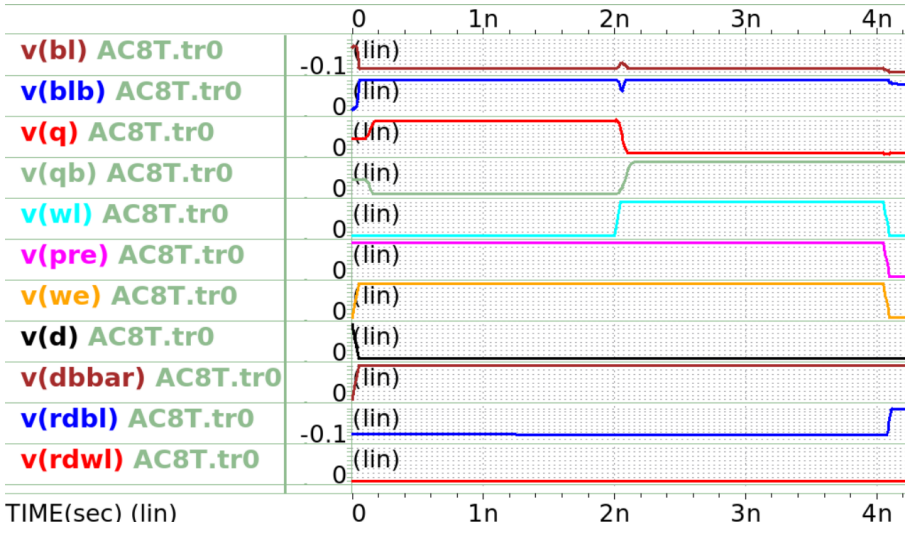

Fig. 23: 8T SRAM Write-0

Fig.23，在寫入值時，不需要 precharge 所以 v(pre) 為 VDD (pmos off)。v(d) = 0、v(dbbar) = VDD 才能寫 0 進去。

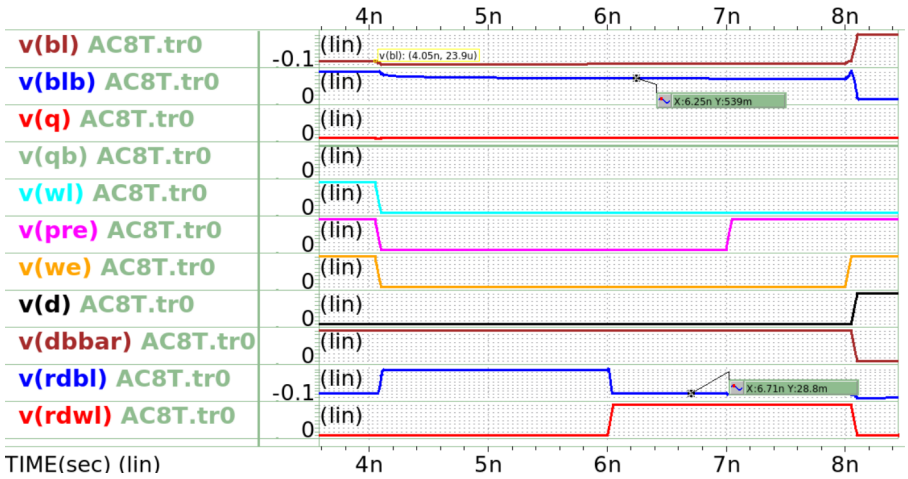

Fig. 24: 8T SRAM Read-0

Fig.24，在讀取值時，需要 precharge 所以 v(pre) 為 0 (pmos on)。v(we) 關閉，會影響到電壓 v(BLB) 會掉一點，但不影響讀取。

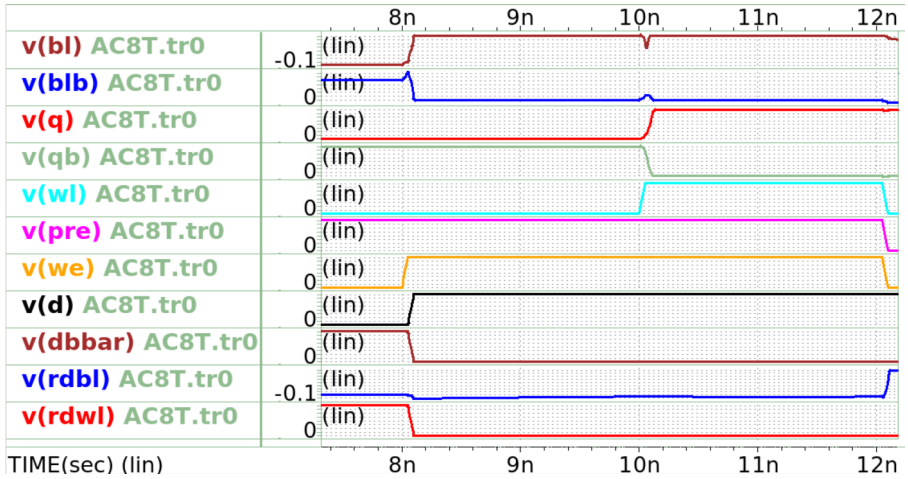

Fig. 25: 8T SRAM Write-1

Fig.25，在寫入值時，不需要 precharge 所以 v(pre) 為 VDD (pmos off)。v(d) = VDD、v(dbbar) = 0 才能寫 1 進去。

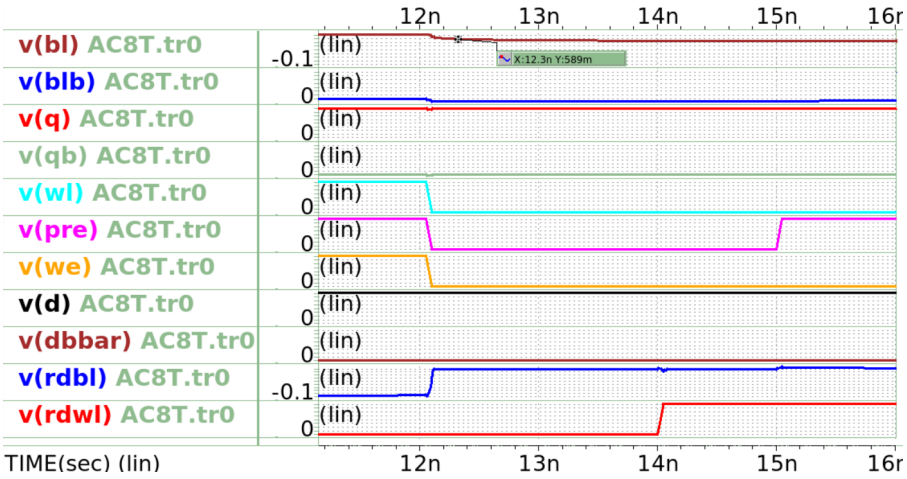

Fig. 26: 8T SRAM Read-1

Fig.26，在讀取值時，需要 precharge 所以 v(pre) 為 0 (pmos on)。v(we) 關閉，會影響到電壓 v(BL) 會掉一點，但不影響讀取。

3. **Power Analysis: Please show the BL (BLB) power transient curves of 6T, 8T SRAM during READ and WRITE. The powertransient curves can be calculated by multiplication of voltage and current transient curves. (P=IxV) You may need to applyappropriate pulses on the WL or BL to READ or to WRITE the cells with VDD=0.8V and the pulse width equivalent to 2ns.**

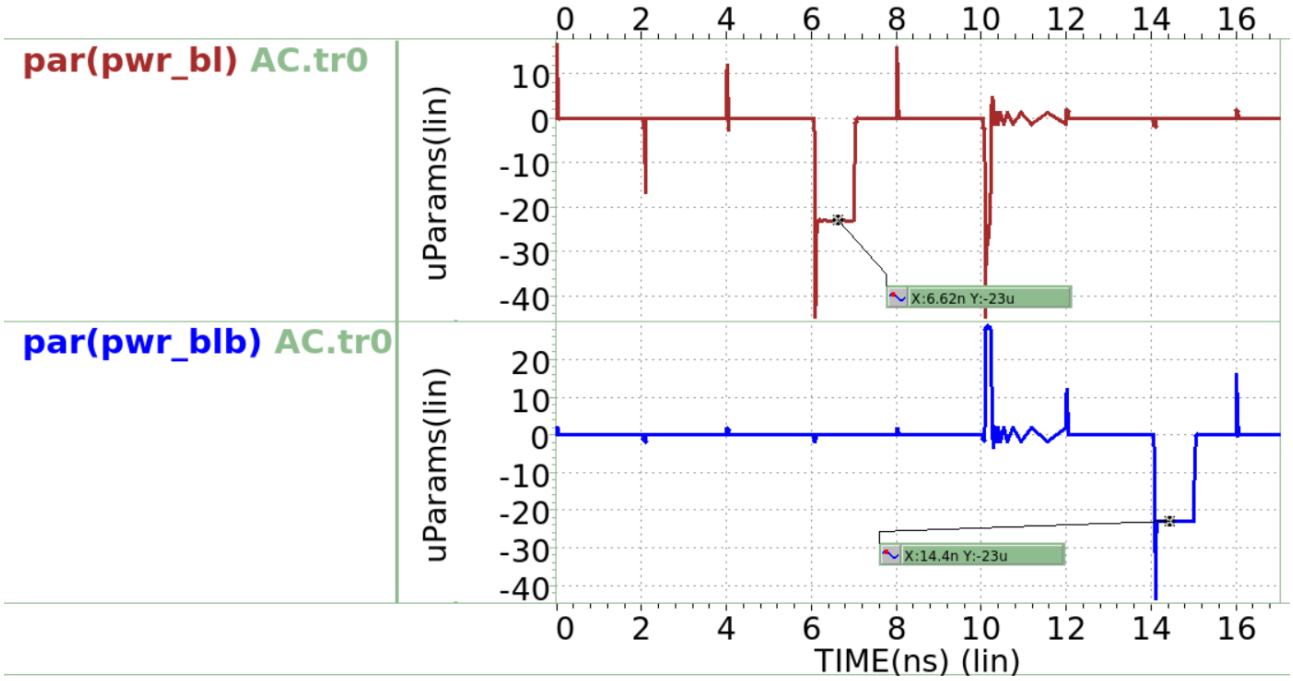

Fig. 27: 6T SRAM

根據 Fig.27，當 v(WL)、v(BL) 和 v(BLB)，有變動，會影響到 Power，可見讀寫線合一。圖上 Label 的小電流是 precharge 充電，同時讀取帶來的小電流所以有 Power。

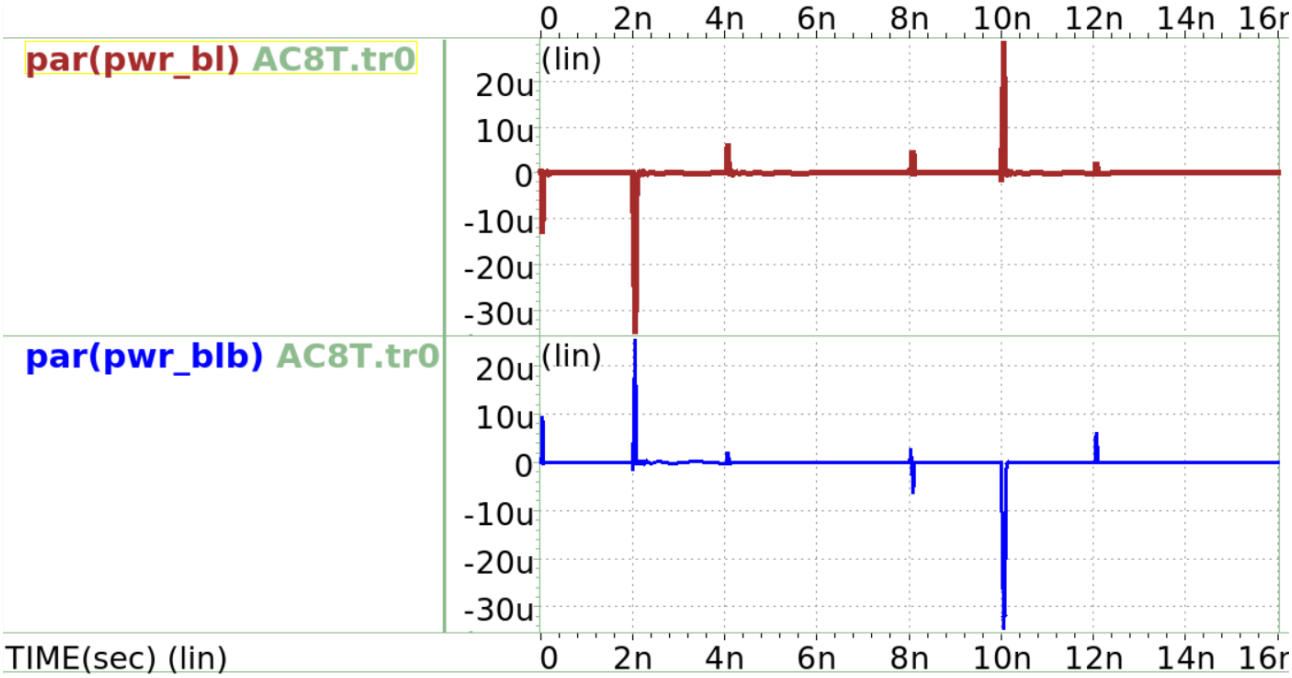

Fig. 28: 8T SRAM

根據 Fig.28，只有當 v(WL)、v(BL) 和 v(BLB)，有變動，才會影響到 Power。v(rdbl) 和 v(rdwl) 變動不會影響其 Power，可見讀寫線分離。

4. 參考資料

1. SNM Analysis of Sram Cells at 45nm, 32nm and 22nm Technology
2. A Low Power and High Read Stability SRAM Cell Using Single-ended Bit-line
3. Near-Threshold-SRAM
4. An efficient timing analysis model for 6T FinFET SRAM using current-based method
5. 1-Bit SRAM Cell in 45-nm CMOS Technology with Integrated Dynamic Power Supply