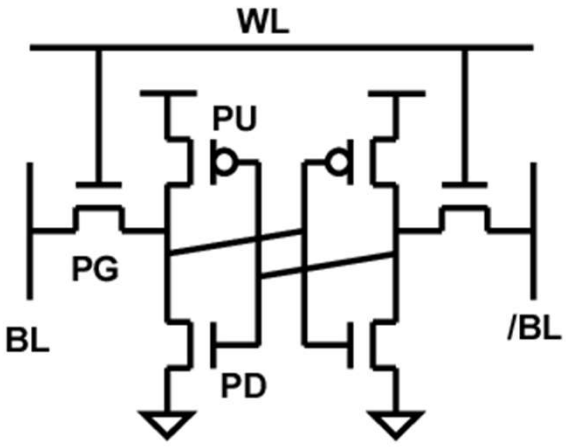
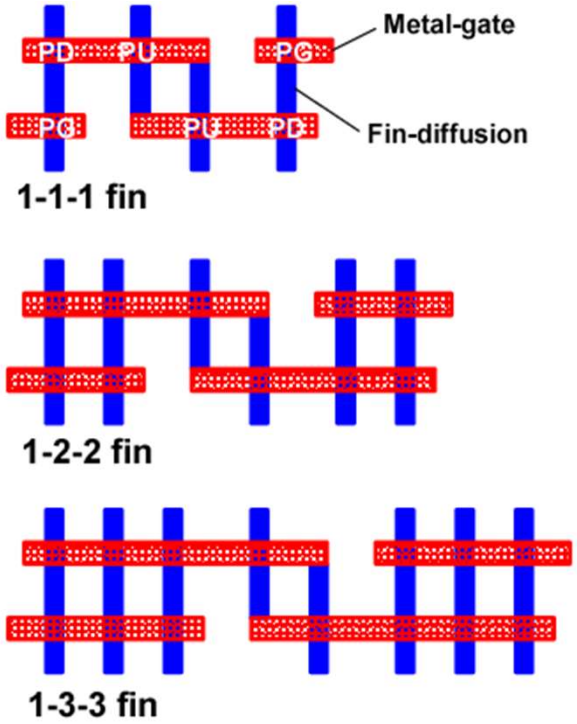
Final Project- 16-nm FinFET 6T SRAM Layouy



PU: Pull-up PMOS
PD: Pull-down NMOS
PG: Pass-gate NMOS
WL: wordline
BL, /BL: bitline pair

(a) Schematic



(b) Layout views

1. Construct the circuitry schematic layout of the 16-nm FinFET 6T SRAM Unit Cell.
2. Provide the proof screen-copy picture of the DRC and LVS verification for your layout.
3. Plot the RSNM and WNM of the 16-nm FinFET 6T SRAM unit cell with Vdd=0.8V, 0.6V, 0.4V.
4. Deadline: 23:59:59 pm, 15th, Jan, 2024.