

# Code - HW4

## 記憶體積體電路 Memory Circuit Design

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### 1. NAND-type TCAM

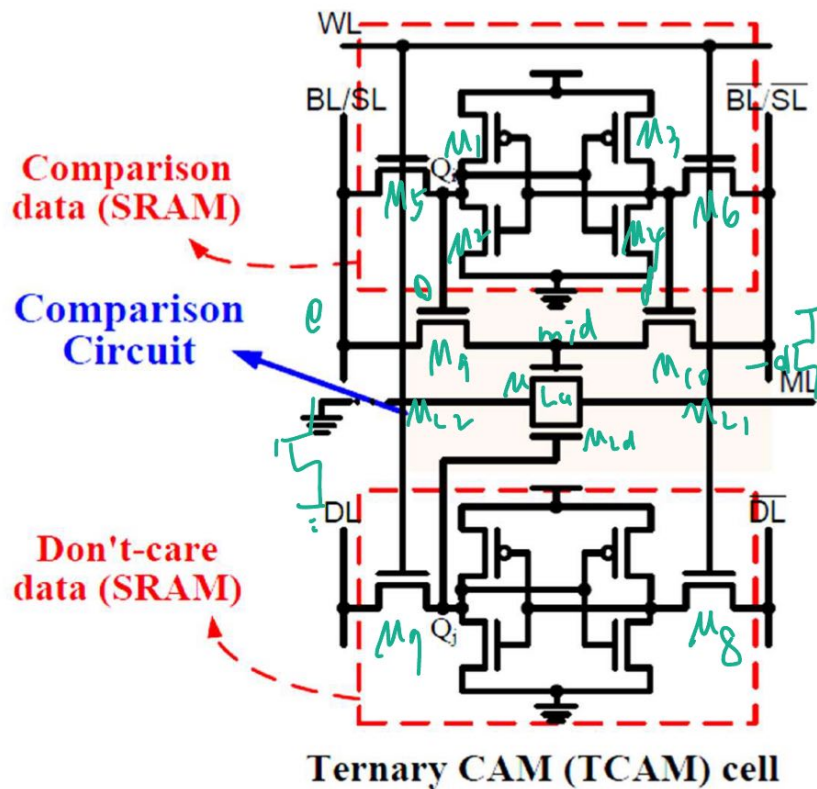


Fig. 1: NAND-type Circuit

List. 1: NAND-type TCAM

```
1  *** NAND-type TCAM ***
2  *** .protect
3  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5  ***
6
7  .param VDD = 1
8  ***
```

```

9  .global VSS! VDD!
10 VDD    VDD! 0    dc VDD
11 VSS    VSS! 0    dc 0
12
13 ***inverter
14 ** Mos D G S B
15 ** .ic 是初始偏壓值
16 .subckt inv in out Wp = 1 Wn = 1
17 Mp out in VDD! VDD! pmos w= 'Wp * 1u' l=65n m=1
18 Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
19 .ends
20
21 *** store
22 * VWL WL VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 1ns 2ns)
23 * VPRE PRE VSS! pulse(0 VDD -0.7ns 0.05ns 0.05ns 1.9ns 2ns)
24 * VB BL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 2ns 4ns)
25 * VD DL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 4ns 8ns)
26 * VWE WE VSS! pulse(0V VDD 0ns 0.05ns 0.05ns 4ns 8ns)
27 * xweb WE WEB inv Wp = 0.25 Wn = 0.1
28 xinVB BL BLB inv Wp = 0.25 Wn = 0.1
29 xinVD DL DLB inv Wp = 0.25 Wn = 0.1
30
31 *** search
32 VWL WL VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 1ns 2ns)
33 VPRE PRE VSS! pulse(0 VDD -0.7ns 0.05ns 0.05ns 1.5ns 2ns)
34 VD DL VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 8ns 16ns)
35 * VB BL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 2ns 4ns)
36 VB BL VSS! PWL(0n 0V 2n 0V 2.1n VDD 4n VDD 4.1n 0V 5.1n 0V 5.2n VDD 7.2n
↪ VDD 7.3n 0V)
37
38
39 * Mp1 BL PRE VDD! VDD! pmos w = 0.1u l = 65n
40 * Mp2 BLB PRE VDD! VDD! pmos w = 0.1u l = 65n
41
42 *** Comparison data (SRAM)
43 * MnB INB WE BL gnd nmos w = 0.1u l = 65n
44 * MpB INB WEB BL gnd pmos w = 0.1u l = 65n
45 * MnBB INBB WE BLB gnd nmos w = 0.1u l = 65n
46 * MpBB INBB WEB BLB gnd pmos w = 0.1u l = 65n
47
48
49
50 xinV1 QiB Qi inv Wp = 0.25 Wn = 0.1
51 Mn5 Qi WL BL gnd nmos w = 1u l = 0.2u
52
53 xinV2 Qi QiB inv Wp = 0.25 Wn = 0.1
54 Mn6 QiB WL BLB gnd nmos w = 1u l = 0.2u
55
56
57 *** Don't-care data (SRAM)
58 * MnD IND WE DL gnd nmos w = 0.1u l = 65n
59 * MpD IND WEB DL gnd pmos w = 0.1u l = 65n
60 * MnDB INDB WE DLB gnd nmos w = 0.1u l = 65n
61 * MpDB INDB WEB DLB gnd pmos w = 0.1u l = 65n
62
63 xinV3 QjB Qj inv Wp = 0.25 Wn = 0.1
64 Mn7 Qj WL DL gnd nmos w = 1u l = 0.2u
65

```

```

66      xinv4 Qj  QjB          inv Wp = 0.25 Wn = 0.1
67      Mn8  QjB WL  DLB gnd nmos w = 1u l = 0.2u
68
69      *** ML
70      MNmu  ML1  mid ML2  gnd nmos w = 5u l = 65n
71      MNmd  ML1  Qj  ML2  gnd nmos w = 5u l = 65n
72
73      Mpmlu ML1  PRE  VDD! VDD! pmos w = 1u l = 65n
74      Mnmlu ML2  PRE  gnd  gnd  nmos w = 1u l = 65n
75
76
77      *** mid
78      Mn9  BL  Qi  mid  gnd nmos w = 5u l = 65n
79      Mn10 BLB QiB mid  gnd nmos w = 5u l = 65n
80
81
82      * .probe PWR_BLB = 'I(Mn5)'*V(BLB)'
83      * .probe PWR_BL = 'I(Mn6)'*V(BL)'
84      .tran 1p 8ns
85      * .MEAS TRAN AvgPower AVG(power) FROM=1pS TO=10ns
86
87
88      .option post
89      .end
90

```

## 2. NOR-type TCAM

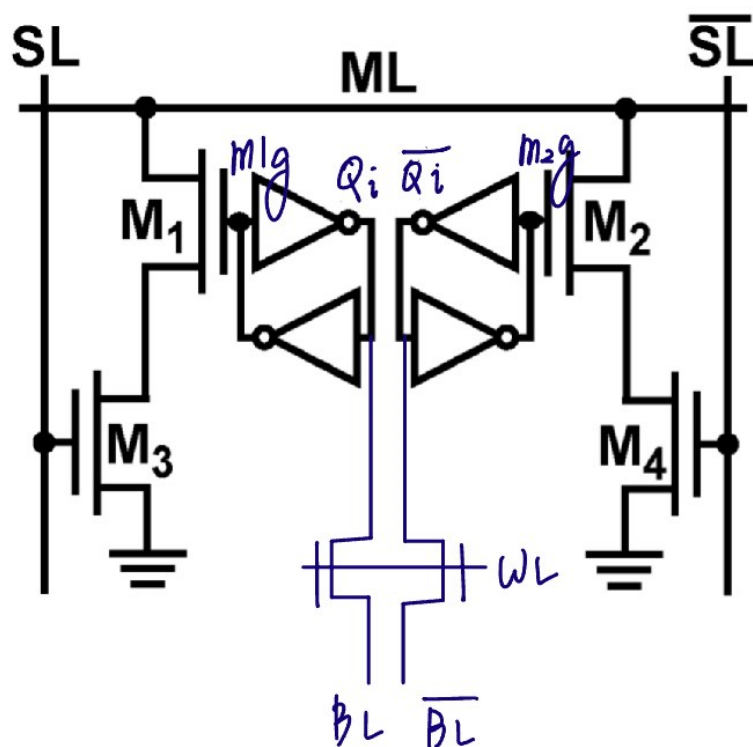


Fig. 2: NOR-type Circuit

## List. 2: NOR-type TCAM

```

1  *** NOR-type TCAM ***
2  *** .protect
3  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5  ***
6
7  .param VDD = 1
8  ***
9  .global VSS! VDD!
10 VDD    VDD! 0    dc VDD
11 VSS    VSS! 0    dc 0
12
13 ***inverter
14 ** Mos D G S B
15 ** .ic 是初始偏壓值
16 .subckt inv in out Wp = 1 Wn = 1
17 Mp out in VDD! VDD! pmos w= 'Wp * 1u' l=65n m=1
18 Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
19 .ends
20
21 *** store
22 * VWL   WL VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 1ns 2ns)
23 * VPRES PRE VSS! pulse(0 VDD -0.7ns 0.05ns 0.05ns 1.5ns 2ns)
24 * VS    SL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 2ns 4ns)
25 * VSB   SLB VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 2ns 4ns)
26 * VD    BL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 4ns 8ns)
27 * VDB   BLB VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 4ns 8ns)
28 * VWE   WE VSS! pulse(0V VDD 0ns 0.05ns 0.05ns 4ns 8ns)
29 * xweb  WE WEB inv Wp = 0.25 Wn = 0.1
30 * xinVB BL BLB inv Wp = 0.25 Wn = 0.1
31 * xinVD BL BLB inv Wp = 0.25 Wn = 0.1
32
33 *** search care mode
34 * VWL   WL VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 1ns 2ns)
35 * VPRES PRE VSS! pulse(0 VDD -0.7ns 0.05ns 0.05ns 1.5ns 2ns)
36 * VS    SL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 2ns 4ns)
37 * VSB   SLB VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 2ns 4ns)
38 * VD    BL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 4ns 8ns)
39 * VDB   BLB VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 4ns 8ns)
40
41
42 *** search don't care mode
43 VWL   WL VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 1ns 2ns)
44 VPRES PRE VSS! pulse(0 VDD -0.7ns 0.05ns 0.05ns 1.5ns 2ns)
45 VS    SL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 4ns 8ns)
46 VSB   SLB VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 2ns 4ns)
47 VD    BL VSS! dc VDD
48 VDB   BLB VSS! dc VDD
49
50 * VWL   WL VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 1ns 2ns)
51 * VPRES PRE VSS! pulse(0 VDD -0.7ns 0.05ns 0.05ns 1.5ns 2ns)
52 * VS    SL VSS! dc 0
53 * VSB   SLB VSS! dc 0
54 * VD    BL VSS! pulse(VDD 0 -0.1ns 0.05ns 0.05ns 4ns 8ns)
55 * VDB   BLB VSS! pulse(0 VDD 0.1ns 0.05ns 0.05ns 2ns 4ns)
56
57

```

```

58 *** precharge
59 Mpmlu ML PRE VDD! VDD! pmos w = 1u l = 65n
60
61
62 xinv1 m1g Qi inv Wp = 0.25 Wn = 0.1
63 xinv2 Qi m1g inv Wp = 0.25 Wn = 0.1
64 MNwd Qi WL BL gnd nmos w = 5u l = 65n
65
66 xinv3 m2g QiB inv Wp = 0.25 Wn = 0.1
67 xinv4 QiB m2g inv Wp = 0.25 Wn = 0.1
68 MNwdb QiB WL BLB gnd nmos w = 5u l = 65n
69
70
71 MN1 ML m1g 1 gnd nmos w = 1u l = 0.2u
72 MN3 1 SL gnd gnd nmos w = 1u l = 0.2u
73
74 MN2 ML m2g 2 gnd nmos w = 1u l = 0.2u
75 MN4 2 SLB gnd gnd nmos w = 1u l = 0.2u
76
77
78 .tran 1p 8ns
79 .MEAS TRAN AvgPower AVG(power) FROM=1pS TO=10ns
80
81
82 .option post
83 .end
84
85

```