

# Final Project

## 記憶體積體電路 Memory Circuit Design

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### 1. Construct the circuitry schematic layout of the 16-nm FinFET 6T SRAM Unit Cell.

Layout 盡可能密集，不要太分散。

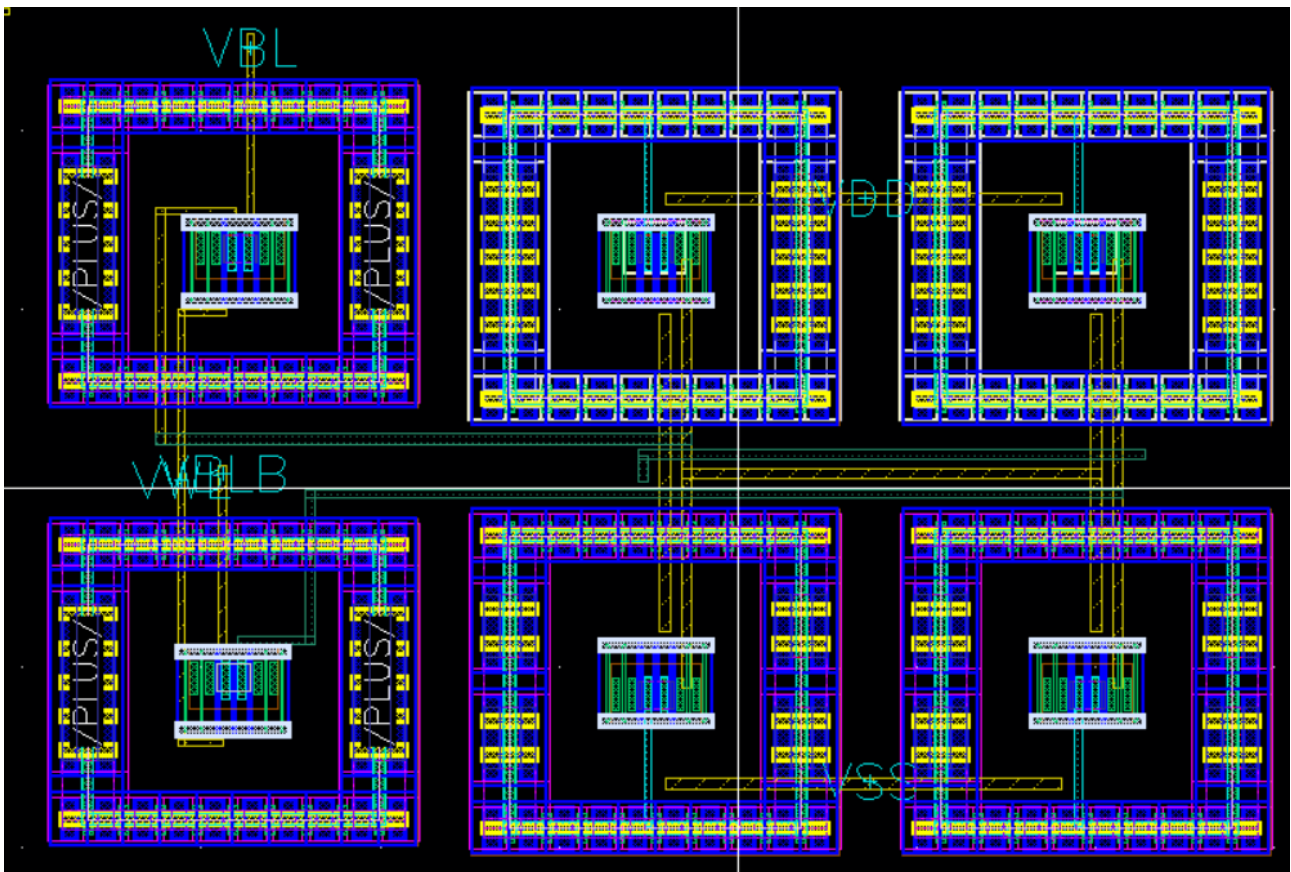


Fig. 1: Layout of the 16-nm FinFET 6T SRAM Unit Cell

## 2. Provide the proof screen-copy picture of the DRC and LVS verification for your layout.

Calibre - RVE v2019.2\_26.18 : SRAM6T.drc.results

File View Highlight Tools Window Setup Help

Show All ▾ SRAM6T, 259 Results (in 39 of 41 Checks) 📄

Check / Cell /	Results	Flat
Check OD.DN.1.T	1	1
Check LUP.1	1	2
Check G.4.VTSPI	4	44
Check G.4.VTSNi	7	92
Check G.4.VIA2i	5	9
Check G.4.VIA1i	4	36
Check G.4.VIA0ii	29	194
Check G.4.SRDPO	12	24
Check G.4.PPI	6	90
Check G.4.POI	19	266
Check G.4.PODE_GATE	16	260
Check G.4.ODi	22	158
Check G.4.NWi	3	42
Check G.4.NPi	5	46
Check G.4.M3i	5	8
Check G.4.M2i	14	35
Check G.4.M1ii	12	38
Check G.4.M0_POI	21	74
Check G.4.M0_ODiii	29	172
Check G.4.FINFET_boundary1	6	6
Check G.4.CPOi	6	12
Check DM11.R.1	1	1
Check DM10.R.1	1	1
Check DM9.R.1	1	1
Check DM8.R.1	1	1
Check DM7.R.1	1	1
Check DM6.R.1	1	1
Check DM5.R.1	1	1
Check DM4.R.1	1	1
Check DM3.S.7	4	6
Check DM3.R.1	1	1
Check DM2.S.7	6	9
Check DM2.R.1	1	1

Fig. 2: DRC.results

Calibre - RVE v2019.2\_26.18 : SRAM6T.drc.results

File View Highlight Tools Window Setup Help

Show All ▾ SRAM6T, 259 Results (in 39 of 41 Checks) 📄

Check / Cell /	Results	Flat
Check G.4.PPI	6	90
Check G.4.POI	19	266
Check G.4.PODE_GATE	16	260
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Check G.4.M3i	5	8
Check G.4.M2i	14	35
Check G.4.M1ii	12	38
Check G.4.M0_POI	21	74
Check G.4.M0_ODiii	29	172
Check G.4.FINFET_boundary1	6	6
Check G.4.CPOi	6	12
Check DM11.R.1	1	1
Check DM10.R.1	1	1
Check DM9.R.1	1	1
Check DM8.R.1	1	1
Check DM7.R.1	1	1
Check DM6.R.1	1	1
Check DM5.R.1	1	1
Check DM4.R.1	1	1
Check DM3.S.7	4	6
Check DM3.R.1	1	1
Check DM2.S.7	6	9
Check DM2.R.1	1	1
Check DM1.R.1	1	1
Check DENSITY_PRINT_FILES	0	0
Check CPO.DN.3.T	1	1
Check CMD.DN.3.T	1	1
Check CHIP.BOUND.R.3	1	1
Check CHIP.BOUND.EN.2__CHIP.BOUND.R.1	7	7
Check AP.DN.1.T	1	1

Fig. 3: DRC.results

Calibre - RVE v2019.2\_26.18 : svdb SRAM6T

File View Highlight Tools Window Setup Help

Navigator ▾ Info ⓘ Extraction Results ✓ Comparison Results x

Results

- Extraction Results
- Comparison Results

ERC

- Softchk Database
- ERC Results
- ERC Summary

Reports

- Extraction Report
- LVS Report

Rules

- Rules File

View

- Info
- Finder
- Schematics

Setup

- Options

Layout Cell / Type /	Source Cell	Nets	Instances	Ports
SRAM6T	SRAM6T	7L, 7S	4L, 4S	5L, 5S

Cell SRAM6T Summary (Clean)

CELL COMPARISON RESULTS ( TOP LEVEL )

LAYOUT CELL NAME: SRAM6T  
SOURCE CELL NAME: SRAM6T

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	5	5	
Nets:	19	7	*
Instances:	4	4	MN (4 pins)
	2	2	MP (4 pins)
	6	0	npode_svt_mac (3 pins)
	4	0	ppode_svt_mac (3 pins)
Total Inst:	18	6	

Fig. 4: LVS.results

### 3. Plot the RSNM and WNM of the 16-nm FinFET 6T SRAM unit cell with $V_{dd}=0.8V, 0.6V, 0.4V$ .

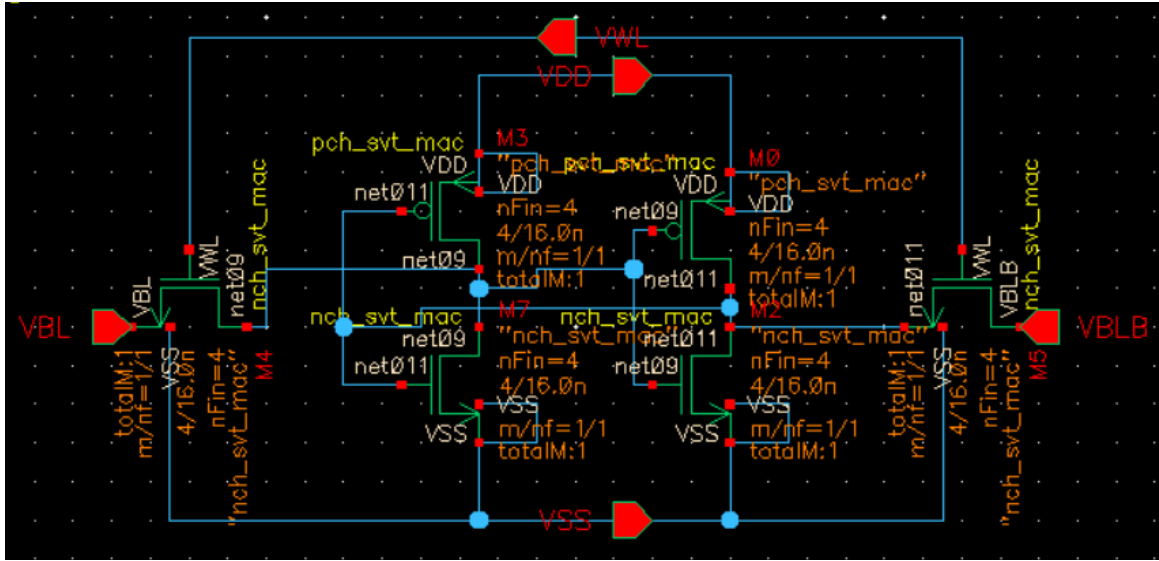


Fig. 5: 16-nm FinFet 6T SRAM schematic

#### 3.1. $V_{dd}=0.8V$

對  $V_{dd} = 0.8V$  ,  $RSNM = 0.217 V$  ,  $WNM = 0.480 V$  。

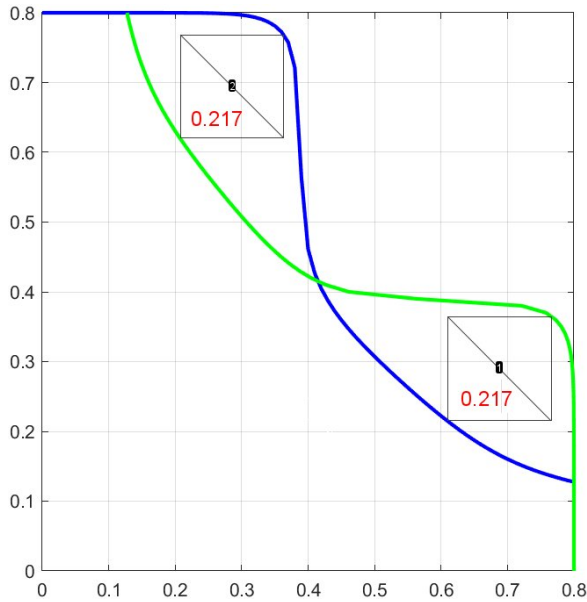


Fig. 6: RSNM

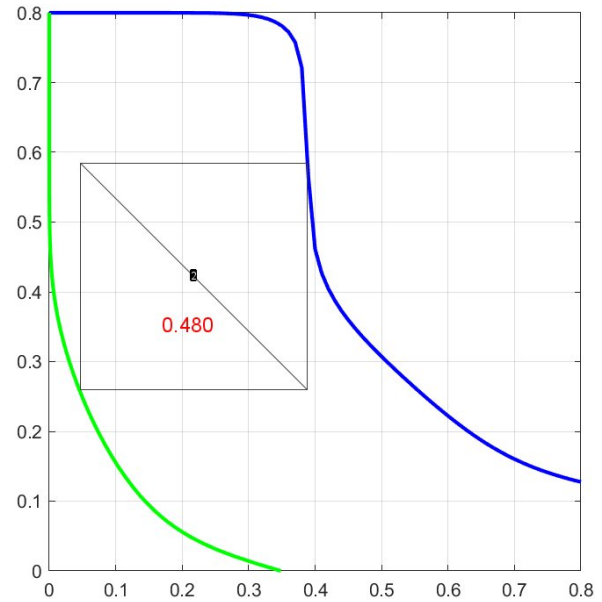


Fig. 7: WNM

#### 3.2. $V_{dd}=0.6V$

對  $V_{dd} = 0.6V$  ,  $RSNM = 0.173 V$  ,  $WNM = 0.365 V$  。

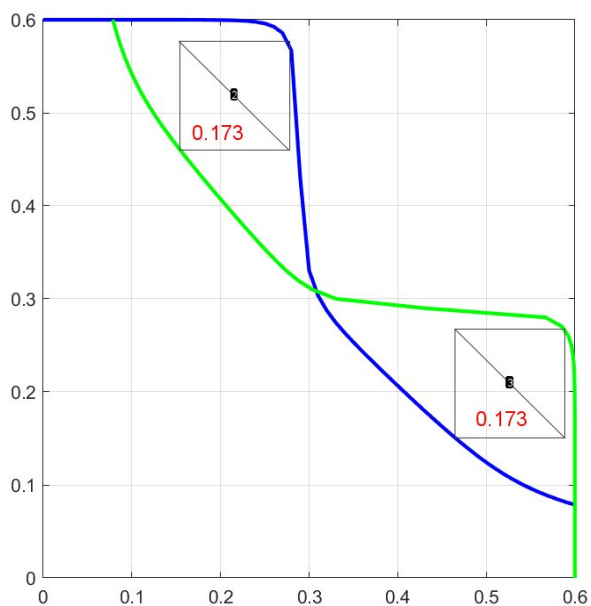


Fig. 8: RSNM

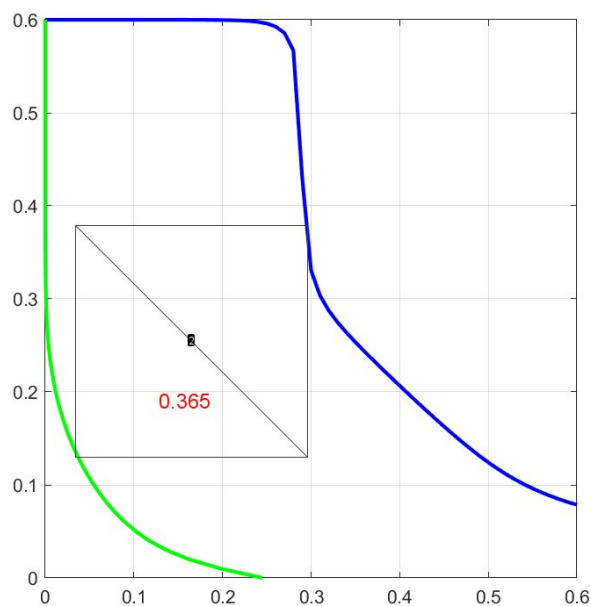


Fig. 9: WNM

### 3.3. Vdd=0.4V

對  $V_{dd} = 0.4V$ ，RSNM = 0.108 V，WNM = 0.263 V。

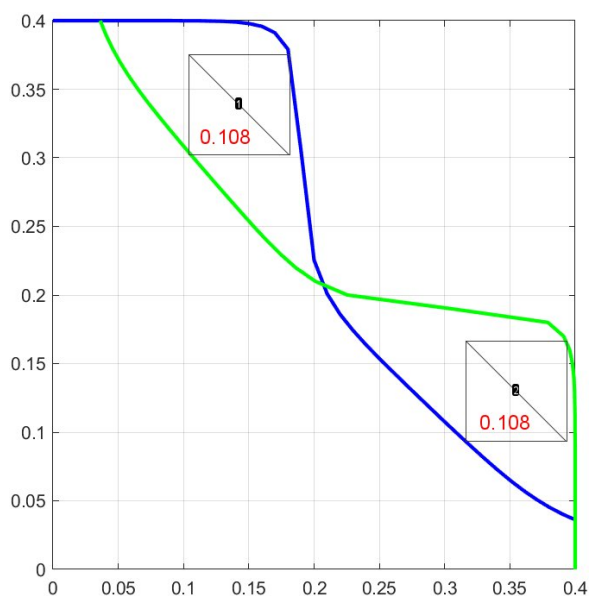


Fig. 10: RSNM

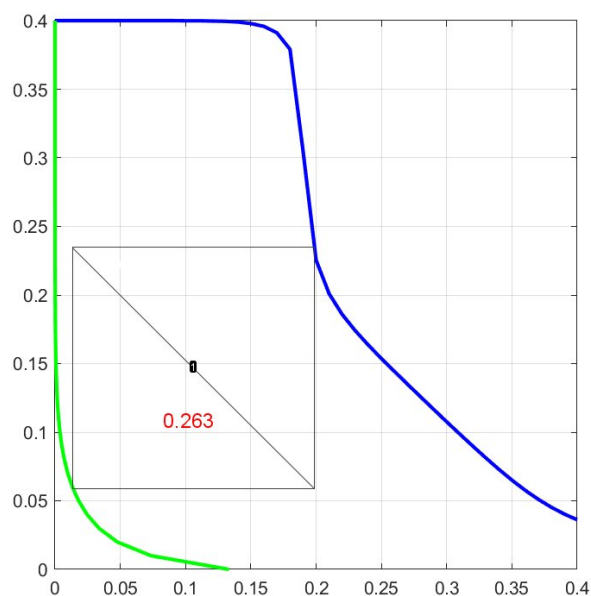


Fig. 11: WNM

根據 Fig. 6、Fig. 8、Fig. 10 可以發現 RSNM 會隨著，VDD 變小逐漸變小，與之成正比。而且因為 Voltage dividend 的關係，在圖形開頭與結尾處會有一個空白區間。根據 Fig. 7、Fig. 9、Fig. 11 可以發現 WNM 也會隨著，VDD 變小逐漸變小，與之成正比。通常在同一 VDD 下，RSNM 都會小於 WNM。