Final Project

記憶體積體電路 Memory Circuit Design

電機 4A　109501201　陳緯亭

January 11, 2024

1. Construct the circuitry schematic layout of the 16-nm FinFET 6T SRAM Unit Cell.

Layout 盡可能密集，不要太分散。

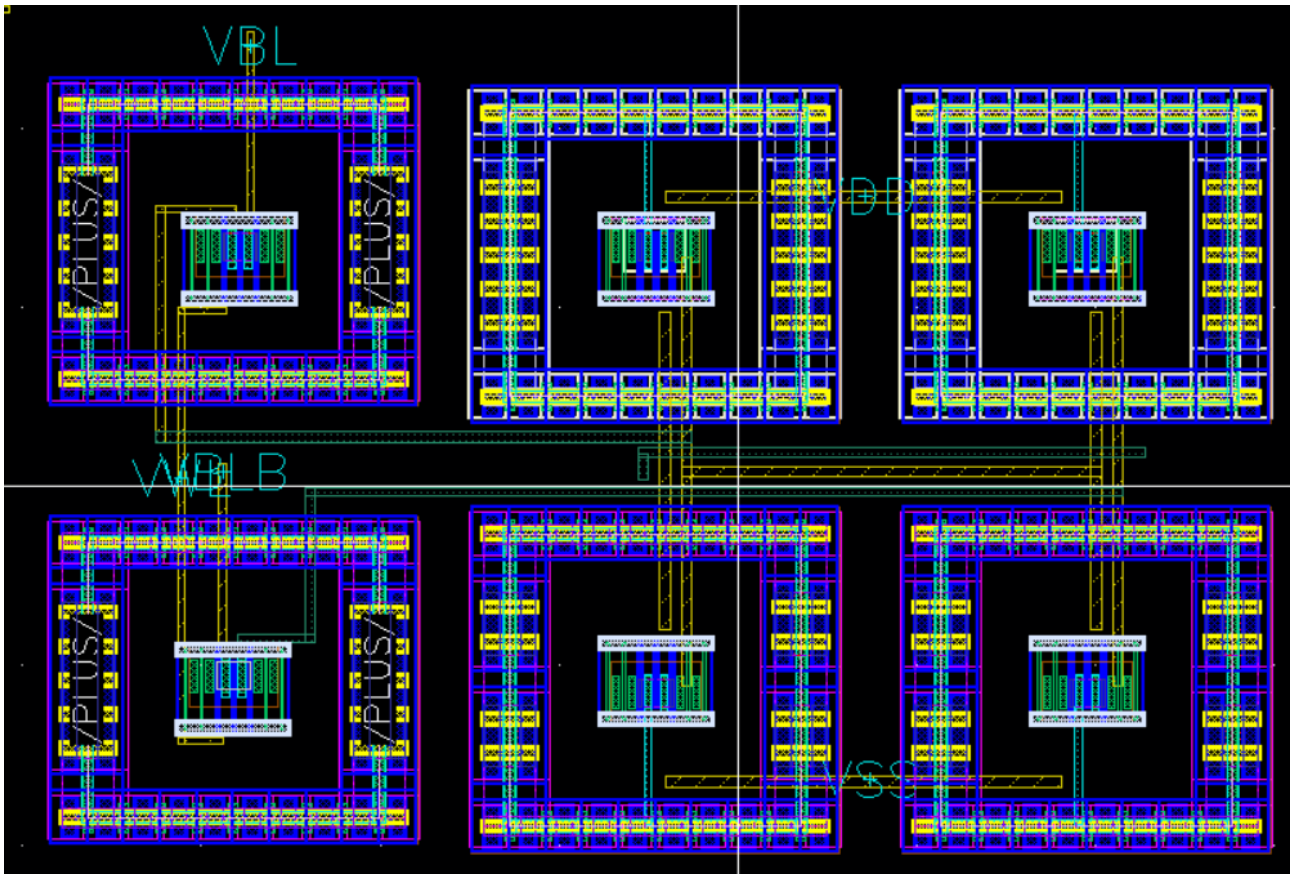

Fig. 1: Layout of the 16-nm FinFET 6T SRAM Unit Cell

2. Provide the proof screen-copy picture of the DRC and LVS verification for your layout.

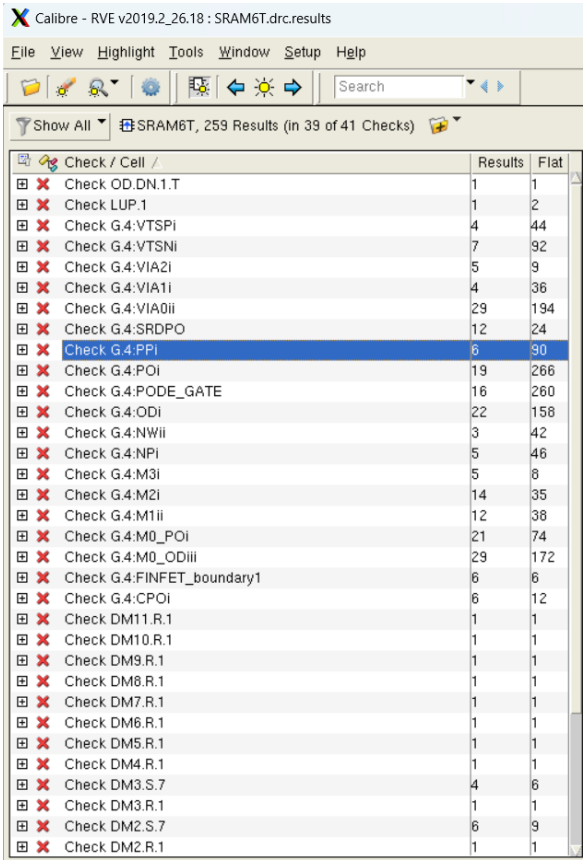

Fig. 2: DRC.results

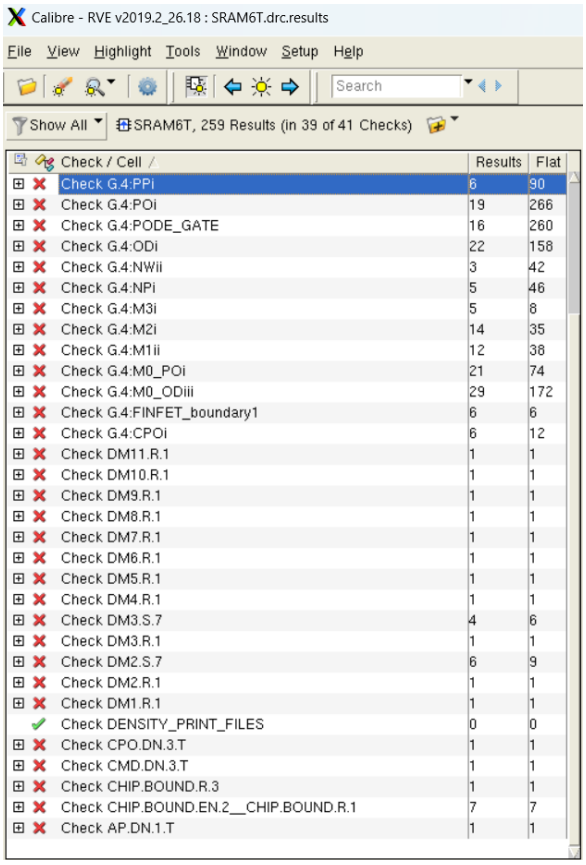

Fig. 3: DRC.results

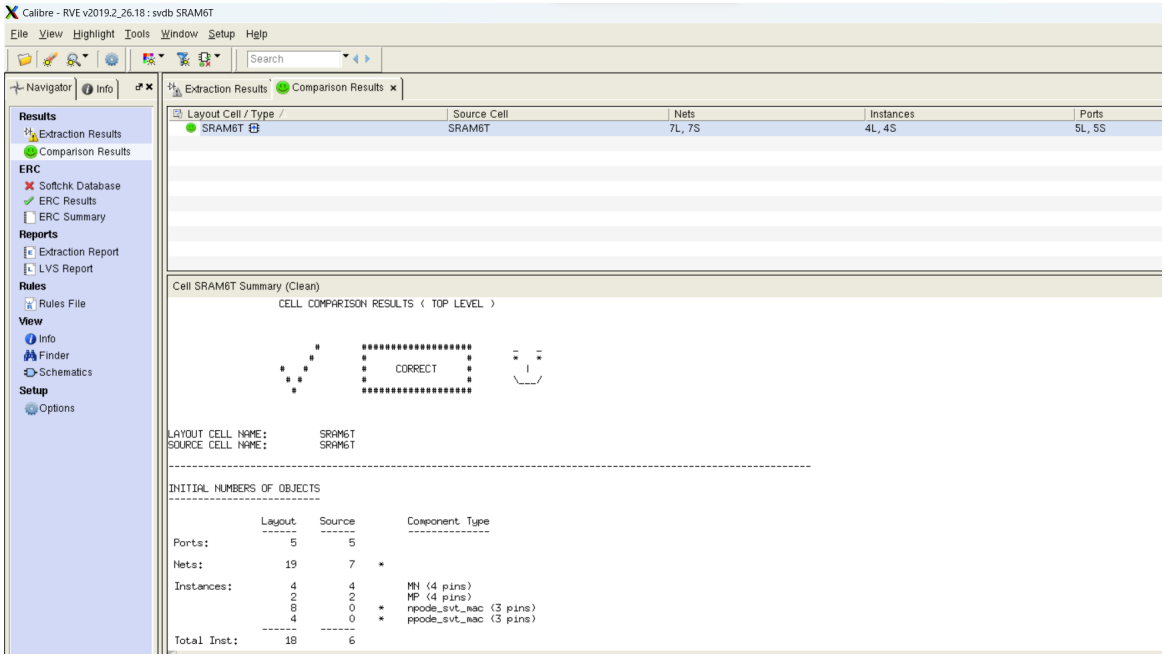

Fig. 4: LVS.results

3. Plot the RSNM and WNM of the 16-nm FinFET 6T SRAM unit cell with Vdd=0.8V, 0.6V, 0.4V.

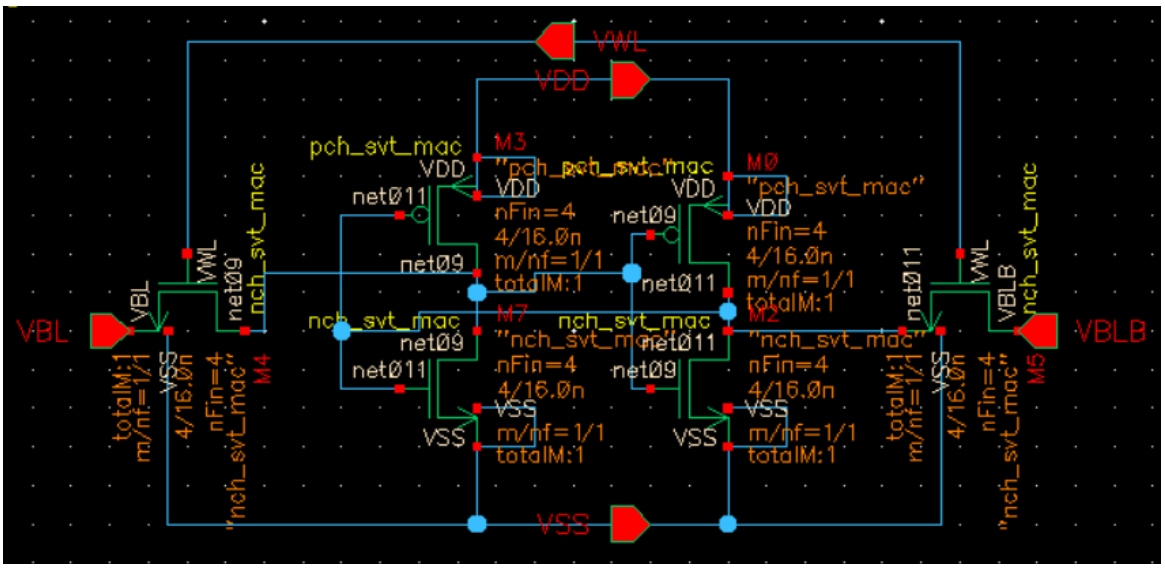

Fig. 5: 16-nm FinFet 6T SRAM schematic

3.1. Vdd=0.8V

對 Vdd = 0.8V ，RSNM = 0.217 V ，WNM = 0.480 V。

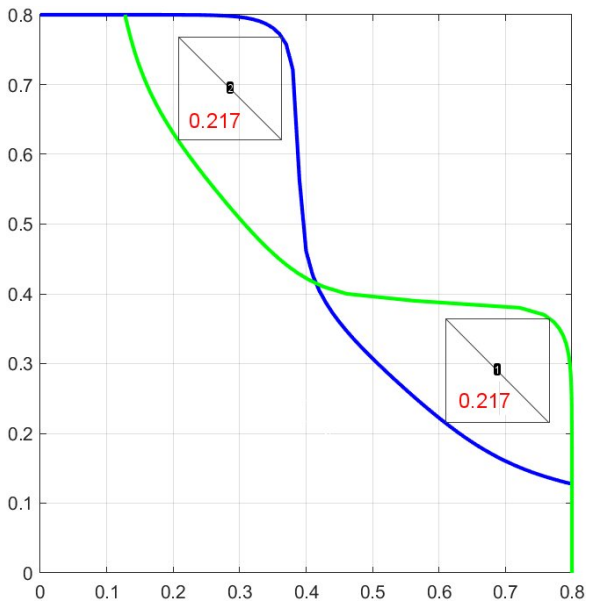

Fig. 6: RSNM

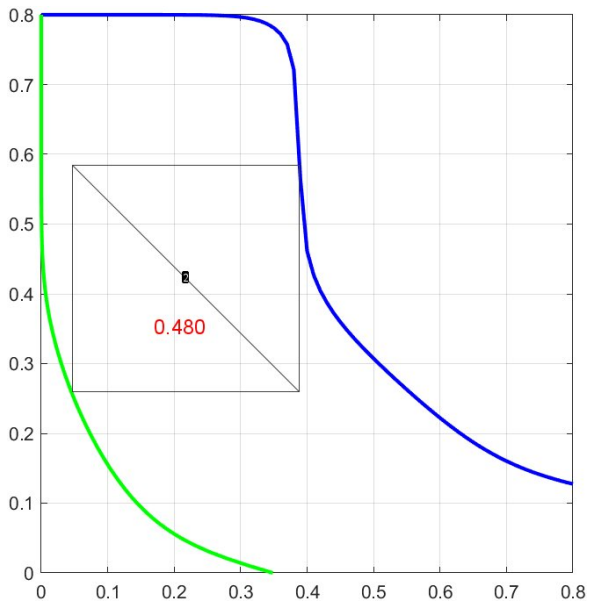

Fig. 7: WNM

3.2. Vdd=0.6V

對 Vdd = 0.6V ，RSNM = 0.173 V ，WNM = 0.365 V。

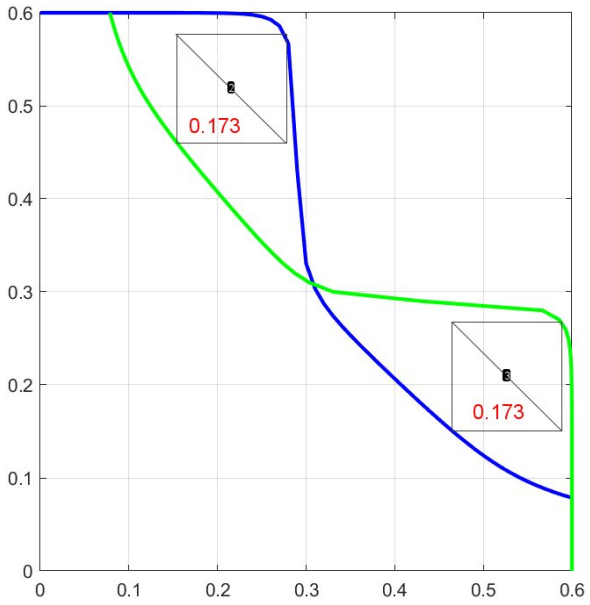

Fig. 8: RSNM

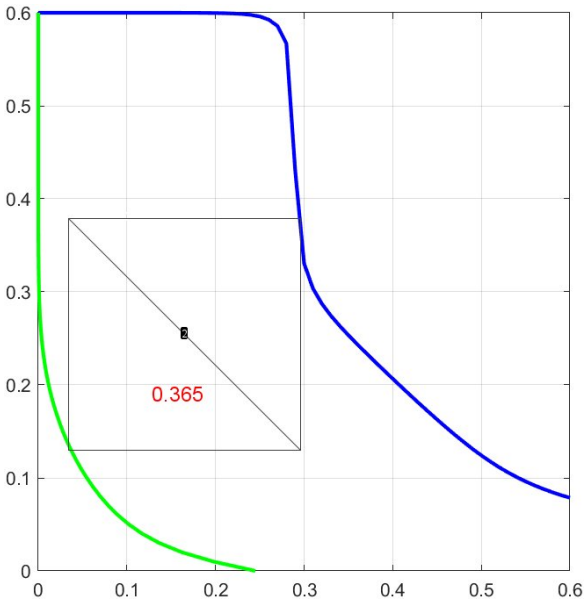

Fig. 9: WNM

3.3. Vdd=0.4V

對 Vdd = 0.4V ，RSNM = 0.108 V ，WNM = 0.263 V。

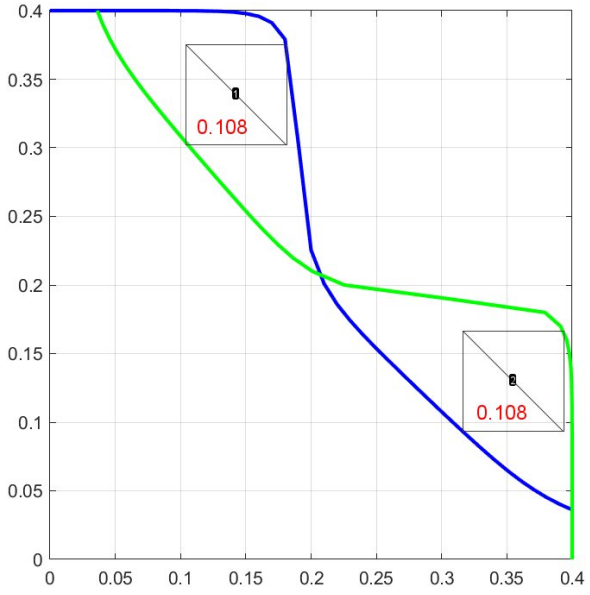

Fig. 10: RSNM

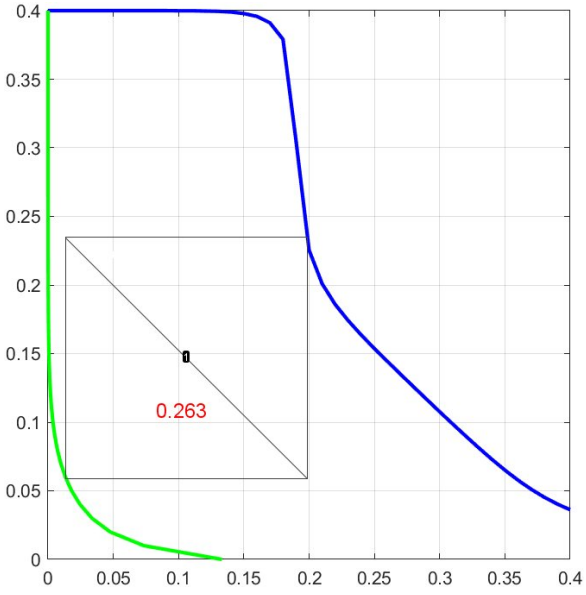

Fig. 11: WNM

根據 Fig. 6、Fig. 8、Fig. 10可以發現 RSNM 會隨著，VDD 變小逐漸變小，與之成正比。而且因為 Voltage dividend 的關係，在圖形開頭與結尾處會有一個空白區間。根據 Fig. 7、Fig. 9、Fig. 11 可以發現 WNM 也會隨著，VDD 變小逐漸變小，與之成正比。通常在同一 VDD 下，RSNM 都會小於 WNM。