Code - HW5

記憶體積體電路 Memory Circuit Design

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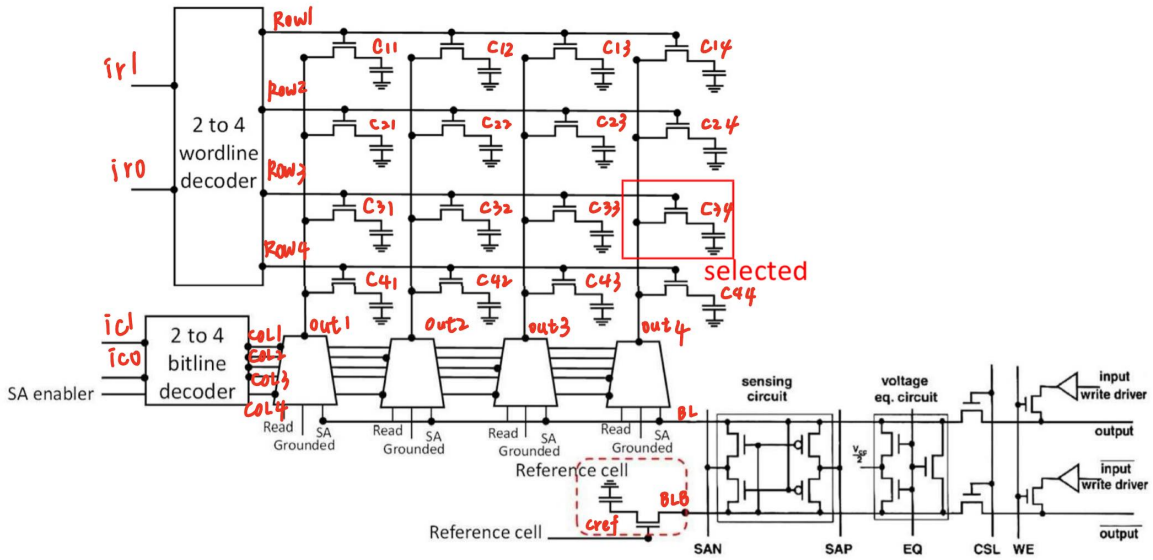

Fig. 1: 4x4 mini 1T1C DRAM array

List. 1: Main code for 4x4 mini 1T1C DRAM array

```
*** 4x4 mini 1T1C DRAM array ***
*** Basic Sense Amplifier Circuit Diagram - DRAM ***
*** .protect
.inc "/home/college/c109501201/Memory/65nm_bulk.pm"
.inc "/home/college/c109501201/HW5/subskt.sp"
.unprotect

.param VCC = 1
.param VOVER = 'VCC + 0.5'
***
.global VSS! VCC!
VCC  VCC! 0   dc VCC
VSS  VSS! 0   dc  0

.IC V(SAN) = 0
.IC V(SAP) = 0

VWL     WL    VSS! pulse(0 'VCC+0.5' -5ns  0.05ns 0.05ns 12ns 14ns)
```

```
VINPUT  INPUT VSS! pulse(0     VCC  0.5ns  0.05ns 0.05ns 13.5ns  25ns)

VWE     WE    VSS! pulse(0  'VCC+0.5'  0.5ns  0.05ns 0.05ns 6ns 14ns)
VEQ     EQ    VSS! pulse(VCC    0      -6ns 0.05ns 0.05ns 13ns 14ns)
VCSL    CSL   VSS! pulse(0  'VCC+0.5'  0.5ns  0.05ns 0.05ns 5.5ns 13ns)
VHVCC   HVCC  VSS! dc VCC/2

xinvinput  INPUT INPUTB inv Wp = 0.2 Wn = 0.1

xbuf  INPUT   IN    buf
xbufB INPUTB  INB   buf

*** Write Enable
MNWE1   IN    WE  OUT   gnd  nmos  w = 10u l = 65n
MNWE2   INB   WE  OUTB  gnd  nmos  w = 10u l = 65n


MNCSL1   OUT   CSL   BL   gnd   nmos w = 20u l = 65n
MNCSL2   OUTB  CSL   BLB  gnd   nmos w = 20u l = 65n

*** Voltage Equalization Circuit
MNEQR   BL   EQ  BLB   GND   nmos w = 6u l = 650n
MNEQL1  BL   EQ  HVCC  GND   nmos w = 6u l = 650n
MNEQL2  HVCC EQ  BLB   GND   nmos w = 6u l = 650n

*** Sensing Circuit
MNSC1   BL  BLB  SAN   GND   nmos w = 5u l = 100n
MNSC2   SAN BL   BLB   GND   nmos w = 5u l = 100n
MPSC1   BL  BLB  SAP   VCC!  pmos w = 10u l = 100n
MPSC2   SAP BL   BLB   VCC!  pmos w = 10u l = 100n

* MNCT    CO       WL    BL   GND   nmos w = 10u l = 65n
MNR     cref     WL    BLB  GND   nmos w = 5u l = 65n

* CCT     c1      gnd      1p
CR      cref      gnd      1p


VIR1     IR1    VSS! dc VCC
VIR0     IR0    VSS! dc 0

VIC1     IC1    VSS! dc VCC
VIC0     IC0    VSS! dc VCC


xD1 IR1 IR0 ROW4 ROW3 ROW2 ROW1 D2to4
xD2 IC1 IC0 WL COL4 COL3 COL2 COL1 D2to4sen

xinvcol0 COL1 COL1B inv
xinvcol1 COL2 COL2B inv
xinvcol2 COL3 COL3B inv
xinvcol3 COL4 COL4B inv

*** SA
xTGc0  out1 BL COL1 COL1B TG
xTGc1  out2 BL COL2 COL2B TG
xTGc2  out3 BL COL3 COL3B TG
xTGc3  out4 BL COL4 COL4B TG
```

```
77
78
79  *** Grounded
80  MNG0  out1 COL1B  gnd  gnd  nmos w = 0.1u l = 65n
81  MNG1  out2 COL2B  gnd  gnd  nmos w = 0.1u l = 65n
82  MNG2  out3 COL3B  gnd  gnd  nmos w = 0.1u l = 65n
83  MNG3  out4 COL4B  gnd  gnd  nmos w = 0.1u l = 65n
84
85
86
87
88  .param W1 = 6u
89  MN11  out1  ROW1 c11  gnd   nmos w = W1 l = 65n
90  MN12  out2  ROW1 c12  gnd   nmos w = W1 l = 65n
91  MN13  out3  ROW1 c13  gnd   nmos w = W1 l = 65n
92  MN14  out4  ROW1 c14  gnd   nmos w = W1 l = 65n
93
94  MN21  out1  ROW2 c21  gnd   nmos w = W1 l = 65n
95  MN22  out2  ROW2 c22  gnd   nmos w = W1 l = 65n
96  MN23  out3  ROW2 c23  gnd   nmos w = W1 l = 65n
97  MN24  out4  ROW2 c24  gnd   nmos w = W1 l = 65n
98
99  MN31  out1  ROW3 c31  gnd   nmos w = W1 l = 65n
100 MN32  out2  ROW3 c32  gnd   nmos w = W1 l = 65n
101 MN33  out3  ROW3 c33  gnd   nmos w = W1 l = 65n
102 MN34  out4  ROW3 c34  gnd   nmos w = W1 l = 65n
103
104 MN41  out1  ROW4 c41  gnd   nmos w = W1 l = 65n
105 MN42  out2  ROW4 c42  gnd   nmos w = W1 l = 65n
106 MN43  out3  ROW4 c43  gnd   nmos w = W1 l = 65n
107 MN44  out4  ROW4 c44  gnd   nmos w = W1 l = 65n
108
109 *** Initialize
110 .IC V(c11) = VCC
111 .IC V(c12) = VCC
112 .IC V(c13) = VCC
113 .IC V(c14) = VCC
114 .IC V(c21) = 0
115 .IC V(c22) = 0
116 .IC V(c23) = 0
117 .IC V(c24) = VCC
118 .IC V(c31) = 0
119 .IC V(c32) = 0
120 .IC V(c33) = 0
121 .IC V(c34) = 0
122 .IC V(c41) = VCC
123 .IC V(c42) = 0
124 .IC V(c43) = 0
125 .IC V(c44) = 0
126
127 .param Cp = 1p
128 C11     c11     gnd     Cp
129 C12     c12     gnd     Cp
130 C13     c13     gnd     Cp
131 C14     c14     gnd     Cp
132
133 C21     c21     gnd     Cp
134 C22     c22     gnd     Cp
```

```
C23     c23     gnd     Cp
C24     c24     gnd     Cp

C31     c31     gnd     Cp
C32     c32     gnd     Cp
C33     c33     gnd     Cp
C34     c34     gnd     Cp

C41     c41     gnd     Cp
C42     c42     gnd     Cp
C43     c43     gnd     Cp
C44     c44     gnd     Cp


.tran    1p    28ns

.option post
.end
```

List. 2: Sub-Circuits

```
*** subcircuit ***
***inverter
.subckt inv in out Wp = 0.1 Wn = 0.065
Mp out in VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
.ends
*** TG : Transmission Gate
.subckt TG in out en enbar Wp = 0.4 Wn = 0.2
Mp out enbar in VCC! pmos w= 'Wp * 1u' l=65n m=1
Mn out   en  in VSS! nmos w= 'Wn * 1u' l=65n m=1
.ends

*** buf : buffer
.subckt buf in out
xinv1 in 1  inv Wp = 10 Wn = 1
xinv2 1 out inv Wp = 20 Wn = 1
.ends

*** D2to4 : 2 to 4 decoder
.subckt D2to4 in1 in0 out3 out2 out1 out0
xinv0 in1 in1B inv
xinv1 in0 in0B inv

xAND1  in1B in0B out0 AND Wp = 0.2 Wn = 0.1
xAND2  in1B in0  out1 AND Wp = 0.2 Wn = 0.1
xAND3  in1  in0B out2 AND Wp = 0.2 Wn = 0.1
xAND4  in1  in0  out3 AND Wp = 0.2 Wn = 0.1
.ends

*** D2to4 : 2 to 4 decoder Having SA enabler
.subckt D2to4sen in1 in0 sen out3 out2 out1 out0
xinv0 in1 in1B inv
xinv1 in0 in0B inv

xAND1  in1B in0B sen out0 AND3 Wp = 0.2 Wn = 0.1
xAND2  in1B in0  sen out1 AND3 Wp = 0.2 Wn = 0.1
xAND3  in1  in0B sen out2 AND3 Wp = 0.2 Wn = 0.1
```

```
xAND4  in1  in0  sen out3 AND3 Wp = 0.2 Wn = 0.1
.ends


*** AND Gate for 2 inputs
.subckt AND in1 in2 out Wp = 0.2 Wn = 0.1
Mn1  1    in1     gnd gnd  nmos  w= 'Wn * 1u' l=65n m=1
Mn2  nout in2     1   gnd  nmos  w= 'Wn * 1u' l=65n m=1

Mp1  nout in1     VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
Mp2  nout in2     VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
xinv nout out inv
.ends

*** AND for 3 inputs
.subckt AND3 in1 in2 in3 out Wp = 0.2 Wn = 0.1
Mn1  1    in1     gnd gnd  nmos  w= 'Wn * 1u' l=65n m=1
Mn2  2    in2     1   gnd  nmos  w= 'Wn * 1u' l=65n m=1
Mn3  nout in3     2   gnd  nmos  w= 'Wn * 1u' l=65n m=1


Mp1  nout in1     VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
Mp2  nout in2     VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
Mp3  nout in3     VCC! VCC! pmos w= 'Wp * 1u' l=65n m=1
xinv nout out inv
.ends

```