HW1

記憶體積體電路 Memory Circuit Design

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1. DC Analysis-An Invertor

(a) Plot the transfer curve in function of the V_{input} as x axle against V_{output} as y axle with $V_{dd} = 1V$ and different ratios of W_p/W_n, such as 0.5, 1 and 2.

Table 1: The settings of W_p and W_n

Node	W_p/W_n	$W_p(\mu\text{m})$	$W_n(\mu\text{m})$
ratio05	0.5	0.5	1
ratio1	1	1	1
ratio2	2	1	0.5

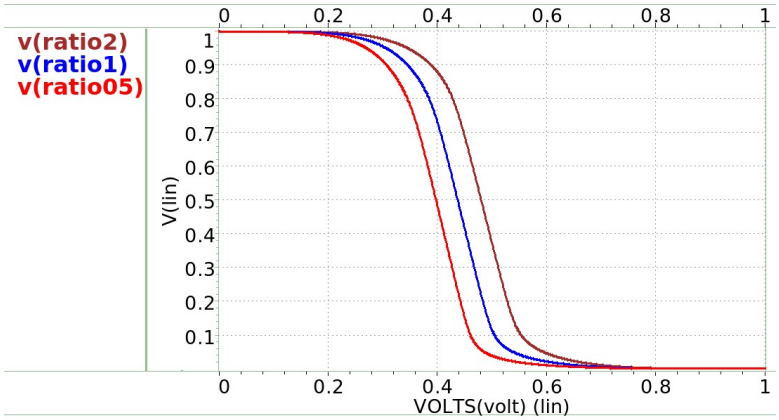

Fig. 1: Beta ratio effects

According to the Fig. 1, the transition is from high to low. When $W_p/W_n = 1$, the curve can be going through the center where this point here is $V_{dd}/2$. When $W_p/W_n > 1$, this make the curve shift to the right. That is because the PMOS is too strong that leads to the NMOS needs large gate source voltage to match the current in the PMOS, and vice versa. When $W_p/W_n < 1$, this make the curve shift to the left. The conclusion is the ratio W_p/W_n is changed the transitions region shifts.

(b) Plot the transfer curve in function of the V_{input} as x axle against V_{output} as y axle with different values of V_{dd} = 1 V, 0.8 V, 0.6 V, and 0.4 V.

Table 2: The settings of V_{dd}

Node	V_{DD} **(V)**
V1	1
V08	0.8
V06	0.6
V04	0.4

For the DC operating points, the currents through the centre of the NMOS and PMOS devices must be equal and approximate to $V_{out} = V_{dd}/2$. The below figure indicates that these points are at about V_{out} = 0.5, 0.4, 0.3, and 0.2 V.

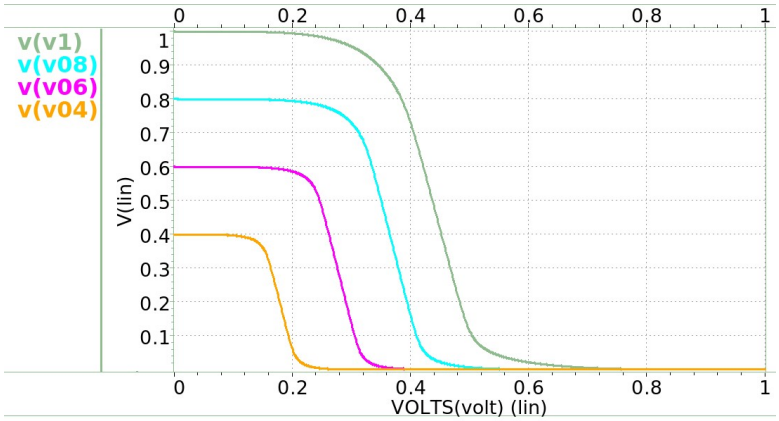

Fig. 2: Voltage transfer characteristics (VPC)

(c) Plot the I_{dd}, which flows from the gorund to the V_{dd}, in function of the V_{input}. You may sweep the V_{input} from 0V to V_{dd} to collect the data of I_{dd} and plot it.

Table 3: The settings of W_p and W_n

Signal Name	W_p/W_n	$W_p(\mu\text{m})$	$W_n(\mu\text{m})$
xinv05.i(mp)	0.5	0.5	1
xinv1.i(mp)	1	1	1
xinv2.i(mp)	2	1	0.5

According to Fig 3, this demonstrates that when $V_{in} = 0$ or $V_{in} = V_{dd}$, the pmos is switched off. No current flows in this area. A peak current is reached, which leads to the maximum current drawn from the supply. However, the direction of I_{dd} is opposite

to the direction of the supply to ground. Therefore, the diagram is inverted.

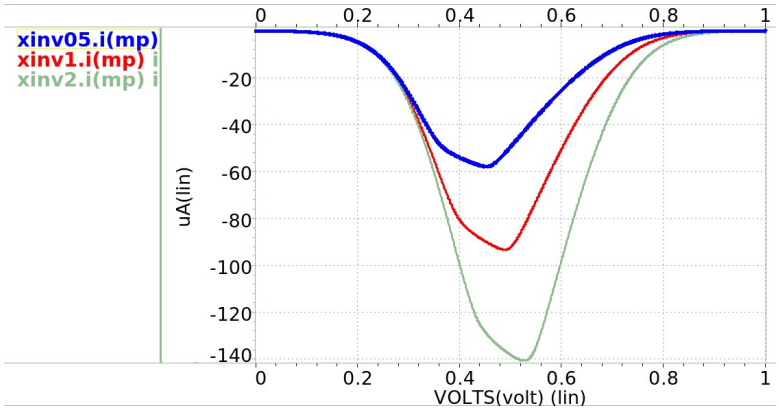

Fig. 3: The current drawn from the ground

(d) Plot the output power, which is defined as $P_{output} = V_{output} \times I_{dd}$. You may sweep the V_{input} from 0V to V_{dd} to collect the data of I_{dd} and V_{output}.

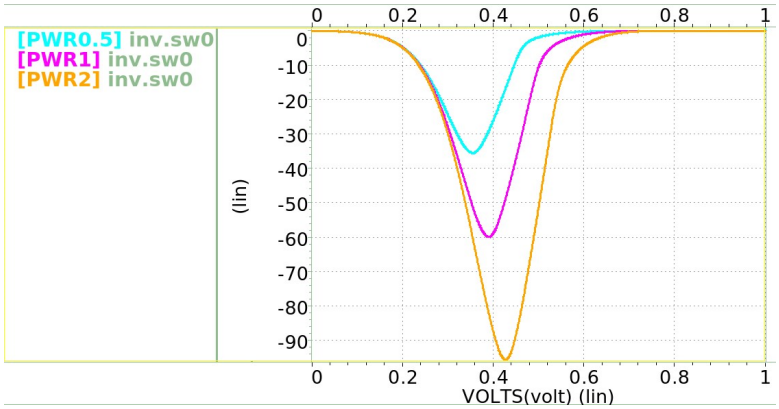

Fig. 4: DC Analysis - P_{output}

Table 4: The settings of W_p and W_n

Signal Name	W_p/W_n	$W_p(\mu\text{m})$	$W_n(\mu\text{m})$
PWR0.5	0.5	0.5	1
PWR1	1	1	1
PWR2	2	1	0.5

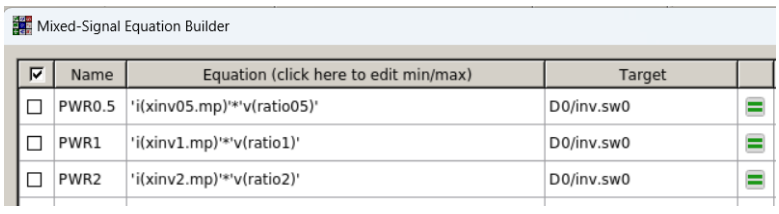

Fig. 5: The power consumption calculated by the equation builder

2. Functionality of the Basic Gate

Please verify the functionality of the 2-to-1 NAND, NOR, XOR.

- NAND

Table 5: 4 output results of NAND

vain	vbin	vout
0	0	1
0	1	1
1	0	1
1	1	0

There are two kinds of input $vain$ and $vbin$. This means that there are 4 output results which shown in Table 5.

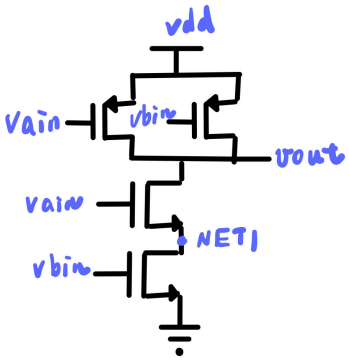

Fig. 6: 4T Nand Gate

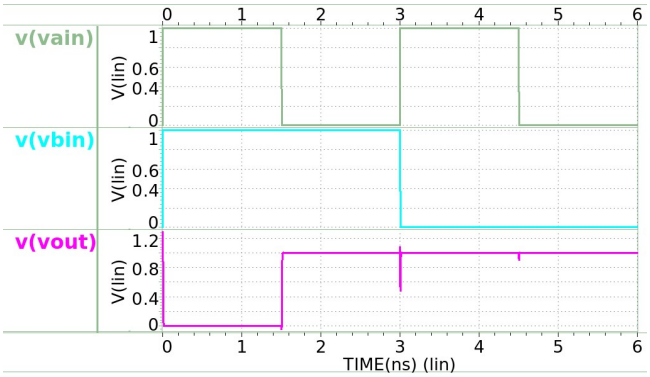

Fig. 7: Waveform for NAND's functionality

- NOR

Table 6: 4 output results of NOR

vain	vbin	vout
0	0	1
0	1	0
1	0	0
1	1	0

There are two kinds of input $vain$ and $vbin$. This means that there are 4 output results which shown in Table 6.

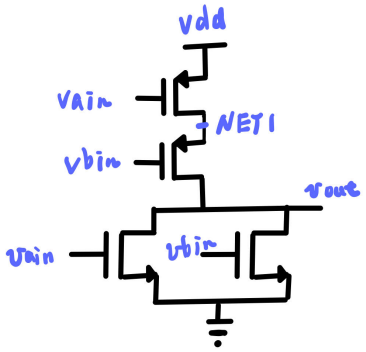

Fig. 8: 4T NOR Gate

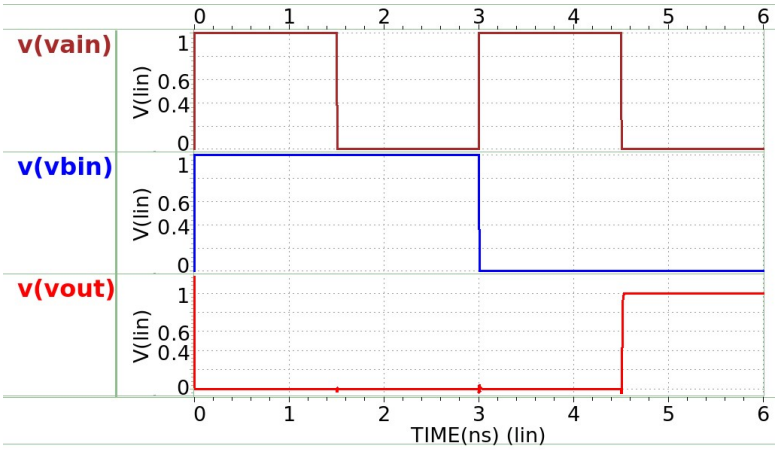

Fig. 9: Waveform for NOR's functionality

- XOR

Table 7: 4 output results of XOR

a	b	vout
0	0	0
0	1	1
1	0	1
1	1	0

There are two kinds of input a and b. This means that there are 4 output results which shown in Table 7.

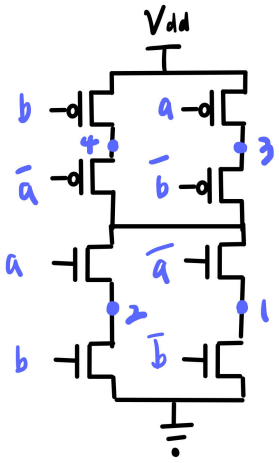

Fig. 10: 12T XOR Gate

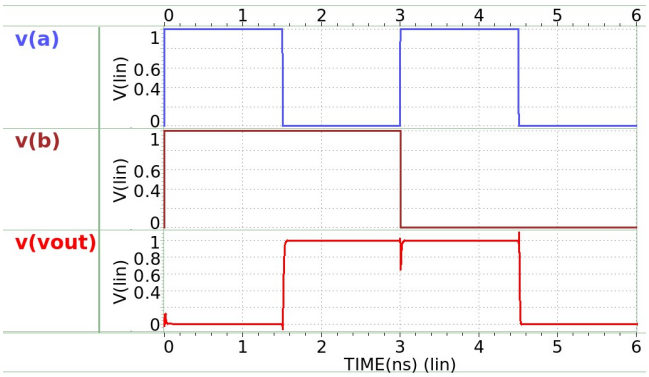

Fig. 11: Waveform for XOR's functionality

3. Functionaliy of the Transmission Gate

Please verify the functionality of transmission gate.

Table 8: 4 output results of TG

en	vin	vout
1	0	0
1	1	1
0	0	High impedance or floating
0	1	High impedance or floating

There are two kinds of input vin and en. This means that there are 4 output results which shown in Table 8.

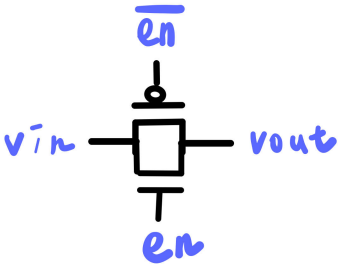

Fig. 12: 4T Transmission Gate

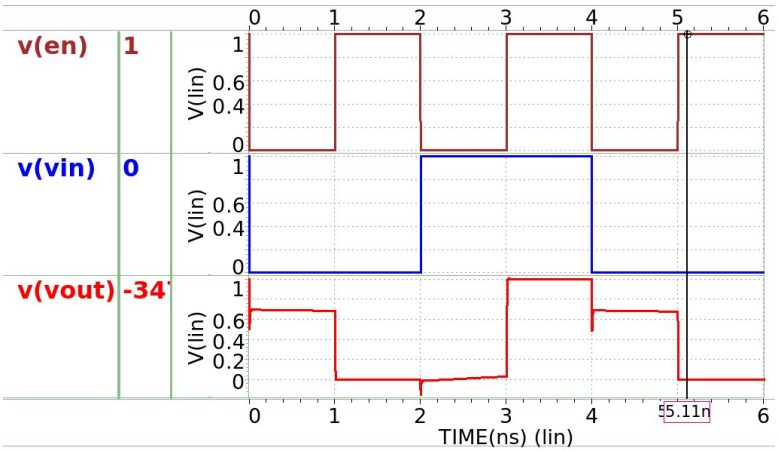

Fig. 13: Waveform for TG's functionality

4. Functionality of the Basic Gate

Please verify the functionality of the 4-to-1 MUX.

There are two kinds of main control signal s_0 and s_1. The result is shown in Fig. 8.

Table 9: 4 output results of 4-to-1 MUX

$s1$	$s0$	vout
0	0	d0
0	1	d1
1	0	d2
1	1	d3

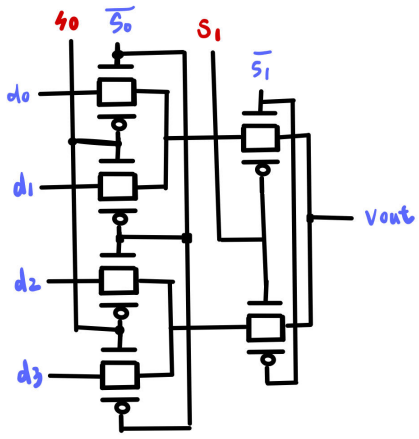

Fig. 14: 14T 4-to-1 MUX

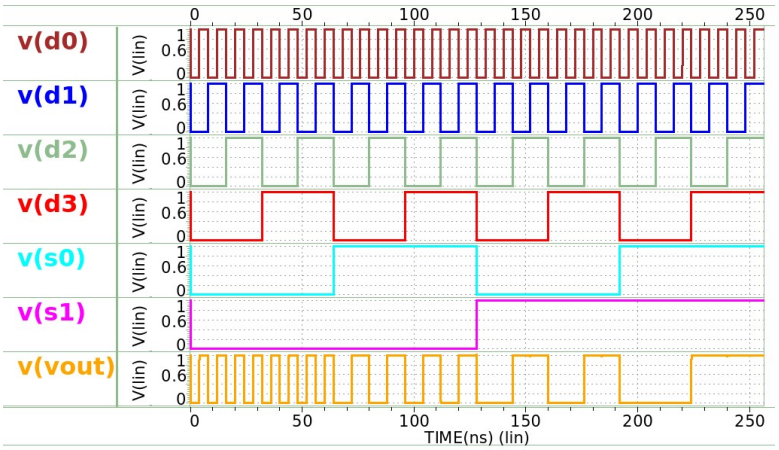

Fig. 15: Waveform for 4-to-1 MUX's functionality

5. Functionality of the Decoder

Please verify the functionality of the 3-to-8 decoder.

Table 10: 9 output results of 3-to-8 Decoder

en	c	b	a	$d0$	$d1$	$d2$	$d3$	$d4$	$d5$	$d6$	$d7$
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

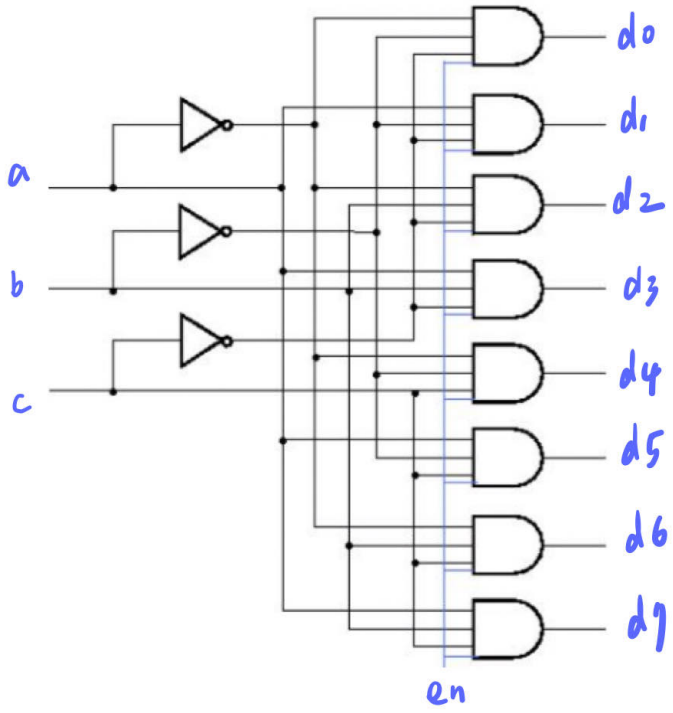

Fig. 16: 86T 3-to-8 decoder

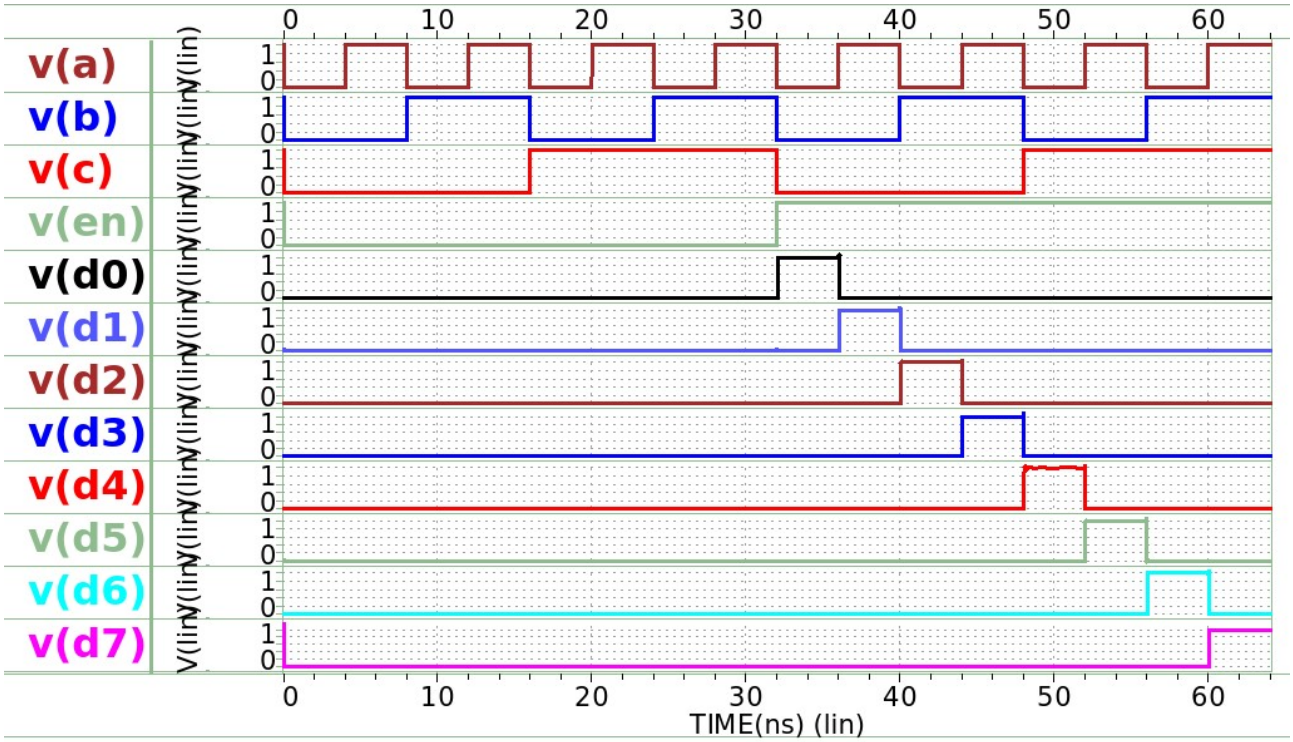

Fig. 17: Waveform for 3-to-8 decoder's functionality