

Code - Final Project

記憶體積體電路 Memory Circuit Design

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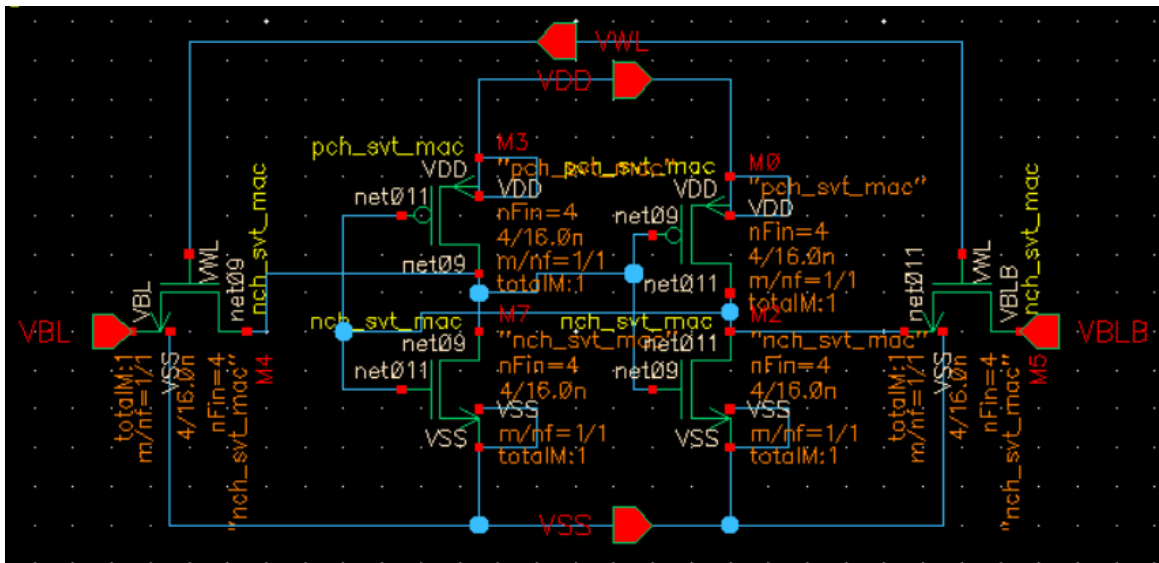


Fig. 1: 16-nm FinFet 6T SRAM schematic

List. 1: 16-nm FinFET 6T SRAM unit cell

```
1 *****
2 * auCdl Netlist:
3 *
4 * Library Name: 109501201
5 * Top Cell Name: SRAM6T
6 * View Name: schematic
7 * Netlisted on: Jan 5 02:19:39 2024
8 *****
9 .TEMP 25
10 .OPTION POST = 2
11 .LIB
12 ↳ "/E/memory_student/s109501201/sh/N16ADFP_SPICE_MODEL/n16adfp_spice_model_v1d0_usage.l"
13 ↳ TTMacro_MOS_MOSCAP
14 *****
15 *.INCLUDE /E/cad_install/sh/N16ADFP_iPDK/tsmcN16/./Calibre/lvs/source.added
16 *.BIPOLAR
17 *.RESI = 2000
18 *.RESVAL
19 *.CAPVAL
20 *.DIOPERI
21 *.DIOAREA
22 *.EQUATION
```

```

21 *.SCALE METER
22 *.MEGA
23
24 *****
25 * Library Name: 109501201
26 * Cell Name: SRAM6T
27 * View Name: schematic
28 *****
29
30 *.SUBCKT SRAM6T VBL VBLB VDD VSS VWL
31 *.PININFO VBL:I VBLB:I VDD:I VSS:I VWL:I
32 MM3 net09 net011 VDD VDD pch_svt_mac l=16.0n nfin=4 m=1
33 MM0 net011 net09 VDD VDD pch_svt_mac l=16.0n nfin=4 m=1
34 MM5 VBLB VWL net011 VSS nch_svt_mac l=16.0n nfin=4 m=1
35 MM4 net09 VWL VBL VSS nch_svt_mac l=16.0n nfin=4 m=1
36 MM2 net011 net09 VSS VSS nch_svt_mac l=16.0n nfin=4 m=1
37 MM7 net09 net011 VSS VSS nch_svt_mac l=16.0n nfin=4 m=1
38 *.ENDS
39
40
41 *****
42 *** change this Vdd = 0.8, 0.6, 0.4
43 .param V1 = 0.4
44
45 *****
46 .global VDD VSS
47 VSS VSS 0 dc 0
48 VDD VDD 0 dc V1
49
50
51 ***** source *****
52
53 VWL VWL gnd dc V1
54 VBL VBL gnd dc V1
55 VBLB VBLB gnd dc 0
56 **** change this net011(find RSNM) or net09(find WNM)
57 VIN net09 gnd
58
59 ***** circuit *****
60 * XSRAM VBL VBLB VDD! VSS! VWL SRAM6T
61
62
63 *** only the first dc is effective
64 .dc VIN 0 V1 0.01V
65
66 .probe WNM = 'V(net011)'
67 .probe RSNM = 'V(net09)'
68 .option post
69 .end

```