

# Code - HW2

## 記憶體積體電路 Memory Circuit Design

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November 16, 2023

### 1. DC Analysis

#### 1.1. 6T SRAM

做 Decouple，畫雙曲線。

要 RSNM 圖，X-Y 軸分別為 VIN-Q1，和 Q1-VIN。

要 WNM 圖，X-Y 軸分別為 VIN-Q1，和 Q2-VIN。

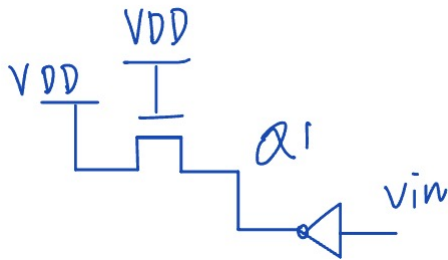


Fig. 1: Decouple (to VDD)

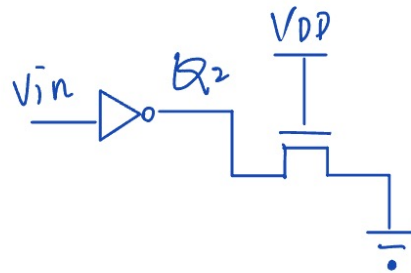


Fig. 2: Decouple (to GND)

List. 1: DC Analysis - 6T SRAM

```
1  *** SRAM 6T curve ***
2  *** .protect
3  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5  ***
6  .param V1 = 1
7  .param V08 = 0.8
8  .param V06 = 0.6
9  .param V04 = 0.4
10 ***
11 .global VDD1! VSS! VDD08! VDD06! VDD04!
12 VDD1 VDD1! 0 dc V1
13 VDD08 VDD08! 0 dc V08
14 VDD06 VDD06! 0 dc V06
15 VDD04 VDD04! 0 dc V04
16 VSS VSS! 0 dc 0
17
18 ***inverter
```

```

19  ** Mos D G S B
20  ** .ic 是初始偏壓值
21  .subckt inv in out Wp = 1 Wn = 1 VDD = V1
22  .ic VDD! = VDD
23  Mp out in VDD! VDD! pmos w= [Wp * 1u] l=65n m=1
24  Mn out in VSS! VSS! nmos w= [Wn * 1u] l=65n m=1
25  .ends
26
27  *** source
28  va vin gnd
29
30
31  *** Vdd = 1V read write
32  xinv1 vin 1 inv VDD = V1 Wp = 0.25 Wn = 0.2
33  Mn1 VDD1! VDD1! 1 gnd nmos w = 0.2u l = 0.065u
34
35  *** Vdd = 1V write
36  xinv5 vin 5 inv VDD = V1 Wp = 0.25 Wn = 0.2
37  Mn5 5 VDD1! gnd gnd nmos w = 0.2u l = 0.065u
38
39  *** Vdd = 0.8V read write
40  xinv2 vin 2 inv VDD = V08 Wp = 0.25 Wn = 0.2
41  Mn2 VDD08! VDD08! 2 gnd nmos w = 0.2u l = 0.065u
42
43  *** Vdd = 0.8V write
44  xinv6 vin 6 inv VDD = V08 Wp = 0.25 Wn = 0.2
45  Mn6 6 VDD08! gnd gnd nmos w = 0.2u l = 0.065u
46
47  *** Vdd = 0.6V read write
48  xinv3 vin 3 inv VDD = V06 Wp = 0.25 Wn = 0.2
49  Mn3 VDD06! VDD06! 3 gnd nmos w = 0.2u l = 0.065u
50
51  *** Vdd = 0.6V write
52  xinv7 vin 7 inv VDD = V06 Wp = 0.25 Wn = 0.2
53  Mn7 7 VDD06! gnd gnd nmos w = 0.2u l = 0.065u
54
55  *** Vdd = 0.4V read write
56  xinv4 vin 4 inv VDD = V04 Wp = 0.15 Wn = 0.1
57  Mn4 VDD04! VDD04! 4 gnd nmos w= 0.3u l = 0.1u
58
59  *** Vdd = 0.4V write write
60  xinv8 vin 8 inv VDD = V04 Wp = 0.15 Wn = 0.1
61  Mn8 8 VDD04! gnd gnd nmos w = 0.3u l = 0.1u
62
63  *** only the first dc is effective
64  .dc va 0 V06 0.02V
65  .dc va 0 V08 0.02V
66  .dc va 0 V1 0.02V
67  .dc va 0 V04 0.01V
68  .option post
69  .end

```

## 1.2. 8T SRAM

做 Decouple，畫雙曲線。

要 RSNM 圖，X-Y 軸分別為 Q-QB，和 QB-Q。

要 WNM 圖，X-Y 軸分別為 Q-QB，和 QB1-Q。

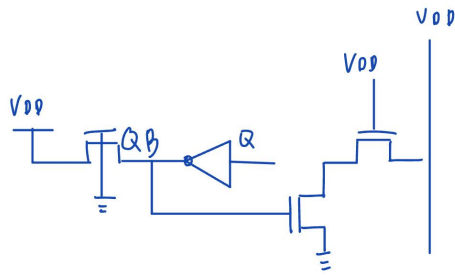


Fig. 3: Decouple (to VDD)

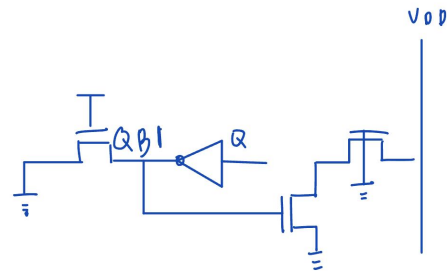


Fig. 4: Decouple (to GND)

## List. 2: DC Analysis - 8T SRAM

```

1  * 8T SRAM Cell - HSPICE Netlist
2  * .protect
3  .include "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5
6  * Parameters
7  .param V1 = 1
8  .param V08 = 0.8
9  .param V06 = 0.6
10 .param V04 = 0.4
11
12 *** 改這裡
13 .param VDD = 'V04'
14
15
16 * Global Nodes
17 .global VDD! VSS!
18 * Power Supplies
19 VDD VDD! 0 dc VDD
20 VSS VSS! 0 dc 0
21
22 * Inverter Subcircuit
23 .subckt inv in out Wp=1 Wn=1 VDD=VDD
24 .IC VDD = VDD
25 Mpos out in VDD VDD PMOS L=65n W='Wp*1u' AD=1 PD=1
26 Mneg out in VSS! VSS! NMOS L=65n W='Wn*1u' AD=1 PD=1
27 .ends
28
29 * Source
30 VBLB BLB GND dc VDD
31 ** 注意 WL = 0V
32 Vw WL GND dc 0
33 VRDWL RDWL 0 dc VDD
34 VRDBL RDBL 0 dc VDD
35 VQ Q 0 dc 0
36 Vw11 WL1 GND dc VDD
37 VBLO BL0 GND dc 0
38 VRDWO RDWO GND dc 0
39 .param p1 = 0.7
40 .param n1 = 0.4
41 .param w1 = 0.6u

```

```

42 .param l1 = 0.065u
43 * Read Operation
44 MN8 RDBL RDWL X GND NMOS W=w1 L=l1
45 MN9 X QB GND GND NMOS W=w1 L=l1
46 xinv2 Q QB inv VDD=VDD Wp=p1 Wn= n1
47 MN5 BLB WL QB GND NMOS W=w1 L=l1
48
49 * Write Operation
50 MN81 RDBL RDWO X1 GND NMOS W=w1 L=l1
51 MN91 X1 QB1 GND GND NMOS W=w1 L=l1
52 xinv4 Q QB1 inv VDD=VDD Wp=p1 Wn= n1
53 MN51 BL0 WL1 QB1 GND NMOS W=w1 L=l1
54
55 * DC Analysis
56 .dc VQ 0 VDD 0.01V
57
58 .option post
59 .end

```

## 2. Transient Analysis

### 2.1. 6T SRAM

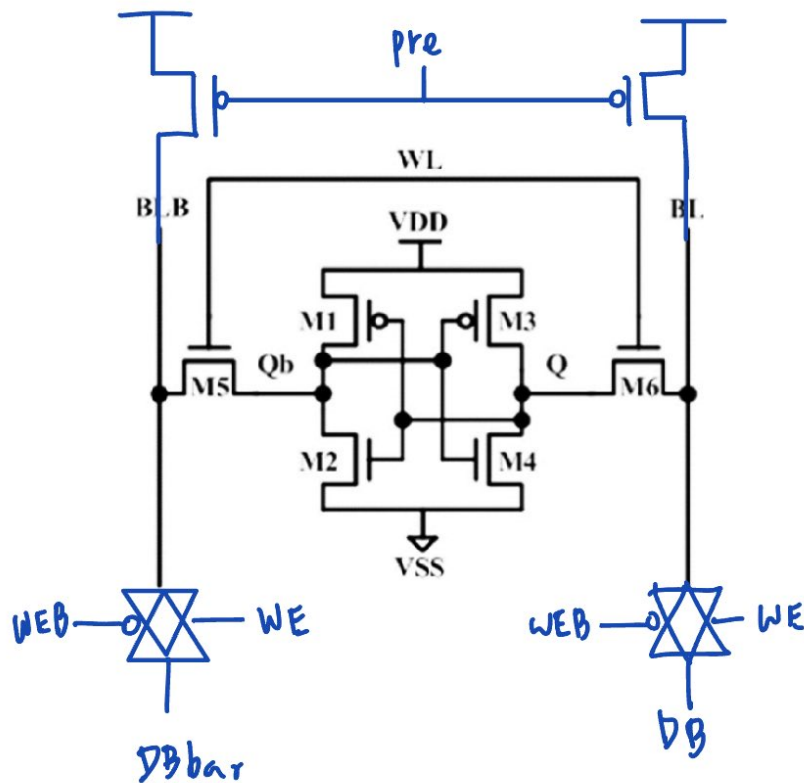


Fig. 5: Transient Analysis - 6T SRAM

List. 3: Transient Analysis - 6T SRAM

```

1 *** SRAM6T Transient Analysis ***
2 *** .protect

```

```

3 .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4 .unprotect
5 ***
6
7 .param VDD = 0.8
8 ***
9 .global VSS! VDD!
10 VDD VDD! 0 dc VDD
11 VSS VSS! 0 dc 0
12
13 ***inverter
14 ** Mos D G S B
15 ** .ic 是初始偏壓值
16 .subckt inv in out Wp = 1 Wn = 1
17 Mp out in VDD! VDD! pmos w= 'Wp * 1u' l=65n m=1
18 Mn out in VSS! VSS! nmos w= 'Wn * 1u' l=65n m=1
19 .ends
20
21 VWL WL VSS! pulse(VDD 0V 0ns 0.05ns 0.05ns 2ns 4ns)
22 VPRE PRE VSS! pulse(0V VDD -1ns 0.05ns 0.05ns 5ns 8ns)
23 VWE WE VSS! pulse(0V VDD 0ns 0.05ns 0.05ns 4ns 8ns)
24 VD D VSS! pulse(VDD 0 0ns 0.05ns 0.05ns 8ns 16ns)
25 VDB DBbar VSS! pulse(0 VDD 0ns 0.05ns 0.05ns 8ns 16ns)
26 xweb WE WEB inv Wp = 0.25 Wn = 0.2
27
28 Mp1 BL PRE VDD! VDD! pmos w = 0.1u l = 65n
29 Mp2 BLB PRE VDD! VDD! pmos w = 0.1u l = 65n
30
31 Mn1 D WE BL gnd nmos w = 0.1u l =65n
32 Mp3 D WEB BL gnd pmos w = 0.1u l =65n
33 Mn2 DBbar WE BLB gnd nmos w = 0.1u l =65n
34 Mp4 DBbar WEB BLB gnd pmos w = 0.1u l =65n
35 *** read source
36 * Vpre pre VSS! pulse(0V 0.8V 0.5ns 0.05ns 0.05ns 2ns 4ns)
37
38 *** 要改
39 * .IC V(Q) = VDD
40 * VBL preBL VSS! pulse(0.8V 0V 0ns 0.05ns 0.05ns 4ns 16ns)
41 * VBLB preBLB VSS! pulse(0V 0.8V 0ns 0.05ns 0.05ns 8ns 12ns)
42 * .IC V(BL)=VDD
43 * .IC V(BLB)=VDD
44
45 *** Write Source
46 * .IC V(Q) = 0
47 * vblin BL VSS! pulse(0V 0.8V 0ns 0.5ns 0.5ns 1ns 4ns)
48 * vblbin BLB VSS! pulse(0.8V 0V 0ns 0.5ns 0.5ns 1ns 4ns)
49
50 xinv1 QB Q inv Wp = 0.25 Wn = 0.2
51 Mn6 Q WL BL gnd nmos w = 0.3u l = 0.2u
52
53 xinv2 Q QB inv Wp = 0.25 Wn = 0.2
54 Mn5 QB WL BLB gnd nmos w = 0.3u l = 0.2u
55
56 *** Power Analysis
57 .probe PWR_BLB = 'I(Mn5)' * 'V(BLB)'
58 .probe PWR_BL = 'I(Mn6)' * 'V(BL)'
59 .tran 1p 17ns
60 .MEAS TRAN AvgPower AVG(power) FROM=1pS TO=10ns

```

```

61
62 .option post
63 .end

```

## 2.2. 8T SRAM

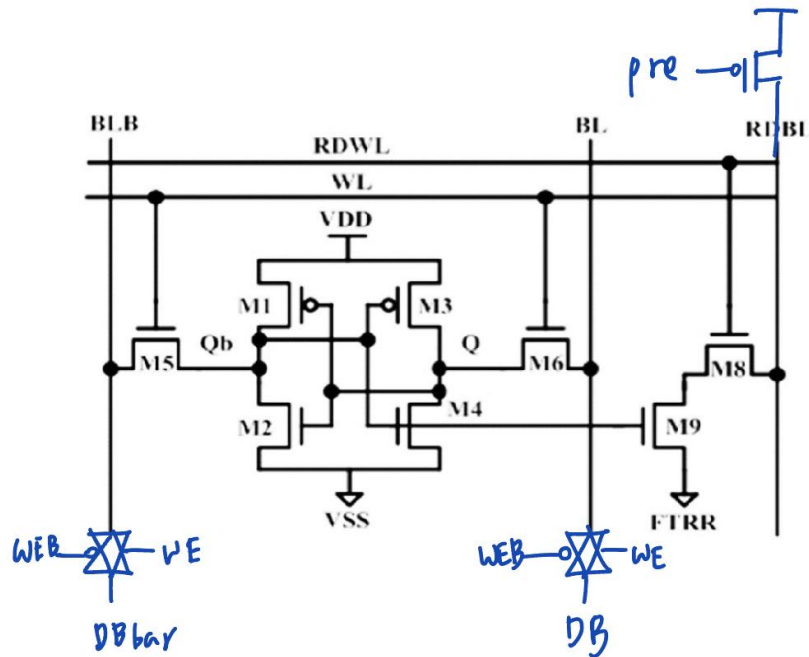


Fig. 6: Transient Analysis - 8T SRAM

List. 4: Transient Analysis - 8T SRAM

```

1  *** SRAM8T Transient Analysis ***
2  *** .protect
3  .inc "/home/college/c109501201/Memory/65nm_bulk.pm"
4  .unprotect
5  ***
6
7  .param VDD = 0.8
8  ***
9  .global VSS! VDD!
10 VDD VDD! 0 dc VDD
11 VSS VSS! 0 dc 0
12
13 ***inverter
14 ** Mos D G S B
15 ** .ic 是初始偏壓值
16 .subckt inv in out Wp = 1 Wn = 1
17 Mp out in VDD! VDD! pmos w= [Wp * 1u] l=65n m=1
18 Mn out in VSS! VSS! nmos w= [Wn * 1u] l=65n m=1
19 .ends
20
21
22 VWL WL VSS! pulse(VDD 0V 0ns 0.05ns 0.05ns 2ns 4ns)
23 VPRE PRE VSS! pulse(0V VDD -1ns 0.05ns 0.05ns 5ns 8ns)

```

```

24 VWE WE VSS! pulse(0V VDD 0ns 0.05ns 0.05ns 4ns 8ns)
25 VD D VSS! pulse(VDD 0 0ns 0.05ns 0.05ns 8ns 16ns)
26 VDB DBbar VSS! pulse(0 VDD 0ns 0.05ns 0.05ns 8ns 16ns)
27 VRDWL RDWL VSS! dc VDD
28 xweb WE WEB inv Wp = 0.25 Wn = 0.2
29
30 Mpl RDBL PRE VDD! VDD! pmos w = 0.1u l = 65n
31
32 Mn1 D WE BL gnd nmos w = 0.1u l = 65n
33 Mp3 D WEB BL gnd pmos w = 0.1u l = 65n
34 Mn2 DBbar WE BLB gnd nmos w = 0.1u l = 65n
35 Mp4 DBbar WEB BLB gnd pmos w = 0.1u l = 65n
36
37 *** Read source
38 * VRDWL RDWL VSS! pulse(0V 0.8V 0.5ns 0.1ns 0.1ns 1ns 2ns)
39 * VWL WL VSS! dc 0
40 * .IC V(Q)=VDD
41 * .IC V(RDBL)=VDD
42 * VPRE PRE VSS! pulse(0V 0.8V 0.5ns 0.5ns 0.5ns 1ns 2ns)
43
44 * .IC V(BL)=VDD
45 * .IC V(BLB)=VDD
46
47 *** Write source
48 * .IC V(Q) = 0
49 * VWL WL VSS! pulse(0V 0.8V 0.5ns 0.05ns 0.05ns 1ns 2ns)
50 * vblin BL VSS! pulse(0V 0.8V 0ns 0.5ns 0.5ns 1ns 4ns)
51 * vblbin BLB VSS! pulse(0.8V 0V 0ns 0.5ns 0.5ns 1ns 4ns)
52
53 * MPpre RDBL PRE VDD! VDD! pmos W=0.5u L=65n
54
55 xin1 QB Q inv Wp=0.13 Wn=0.13
56 MN8 RDBL RDWL X GND NMOS W=0.5u L=65n
57 MN9 X QB GND GND NMOS W=0.5u L=65n
58 MN6 BL WL Q GND NMOS W=0.3u L=0.16u
59 xinv2 Q QB inv Wp=0.13 Wn=0.13
60 MN5 BLB WL QB GND NMOS W=0.3u L=0.16u
61
62 *** Power Analysis
63 .probe PWR_BLB = I(MN5)*V(BLB)
64 .probe PWR_BL = I(MN6)*V(BL)
65
66 .tran 1p 16ns
67 .MEAS TRAN AvgPower AVG(power) FROM=1pS TO=10ns
68 .option post
69 .end

```

### 3. Power Analysis

2、3 題 Code 同一份。

## Matlab Code for Question 1

List. 5: Matlab code for Q1

```

1  % Specify the Excel file path
2  excelFilePath = "D:\Document\Senior\Memory_Circuit_Design\HW2\SRAM8T.xlsx";
3  % Read data from Excel
4  data = xlsread(excelFilePath, 4);
5
6  close;
7  % Extract data
8  VI = data(:, 1); % Assuming VI is in the first column
9  VOr = data(:, 2);
10 VOW = data(:, 3);
11 %VOgnd = data(:, 2); % Assuming VO is in the second column
12 %VOVdd = data(:, 3);
13
14 % Plot SNM
15 figure(1);
16 width=500;% 宽度，像素数
17 height=500;% 高度
18 left=200;% 距屏幕左下角水平距离
19 bottem=200;% 距屏幕左下角垂直距离
20 set(gcf,'position',[left,bottem,width,height])
21 plot(VI, VOr, 'b-', 'LineWidth', 2);
22 hold on;
23 plot(VOr, VI, 'g-', 'LineWidth', 2);
24 hold on;
25
26 figure(2);
27 width=500;% 宽度，像素数
28 height=500;% 高度
29 left=200;% 距屏幕左下角水平距离
30 bottem=200;% 距屏幕左下角垂直距离
31 set(gcf,'position',[left,bottem,width,height])
32 plot(VI, VOr, 'b-', 'LineWidth', 2);
33 hold on;
34 plot(VOW, VI, 'g-', 'LineWidth', 2);
35 hold on;

```