

Cell 製作 (hspice)



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10-T NOR-type CAM

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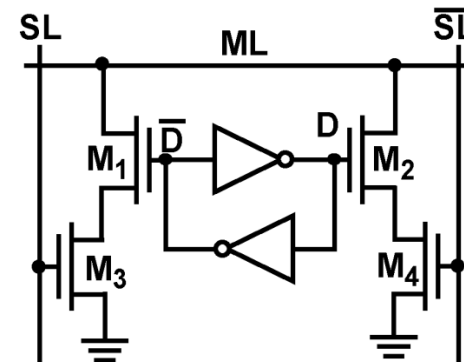
1  .Title 10-T NOR-type CAM
2  .param Vin = 2
3  ***
4  .protect
5  .lib '/cad/cell_lib/crn90g_3d3_lk_v1d2.l' tt
6  .unprotect
7  ***
8  .global VD! Vdd!
9  Vdd      Vdd! 0      dc 2
10 *** Data 的值
11 VD      D 0      dc 2
12
13 *** SL 的值
14 Vsl SLin 0 dc 2
15
16
17 ***inverter
18 .subckt inv in out
19 Mp out in Vdd! Vdd! pch w=0.12u l=0.1u m=1
20 Mn out in 0 0 nch w=0.12u l=0.1u m=1
21 .ends
22
23 ***buffer
24 .subckt buf in out
25 Mp1 out1 in Vdd! Vdd! pch w=0.12u l=0.1u m=1
26 Mn1 out1 in 0 0 nch w=0.12u l=0.1u m=1
27 Mp2 out out1 Vdd! Vdd! pch w=0.12u l=0.1u m=1
28 Mn2 out out1 0 0 nch w=0.12u l=0.1u m=1
29 .ends
30
31 *** searchline 的值
32 Vslpre slpre 0 pulse(0V 2V 1ms 1ms 1ms 19ms 50ms)
33
34 Vmlpre mlpre 0 pulse(2V 0V 5ms 1ms 1ms 16ms 50ms)

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35
36 xinv1 Dbar D inv
37 xinv2 D Dbar inv
38 xinv3 SL SLbar inv
39
40 xbuf1 SLin SL buf
41
42 M1      ML      Dbar s1      nch w=0.12u l=0.1u m=1
43 M2      ML      D      s2      nch w=0.12u l=0.1u m=1
44 M3      s1      SL      0      nch w=0.12u l=0.1u m=1
45 M4      s2      SLbar 0      nch w=0.12u l=0.1u m=1
46 Mpre    ML      mlpres Vdd! pch w=0.12u l=0.1u m=1
47 Mpsl0    SL      slpre 0      nch w=0.12u l=0.1u m=1
48 Mpsl0b   SLbar slpre 0      nch w=0.12u l=0.1u m=1
49
50 .tran 0 50m 1u
51 ***.dc sweep Vsl 0 vin 0.01
52 ***.dc sweep VD 0 2 0.01
53 .options post
54
55 .end

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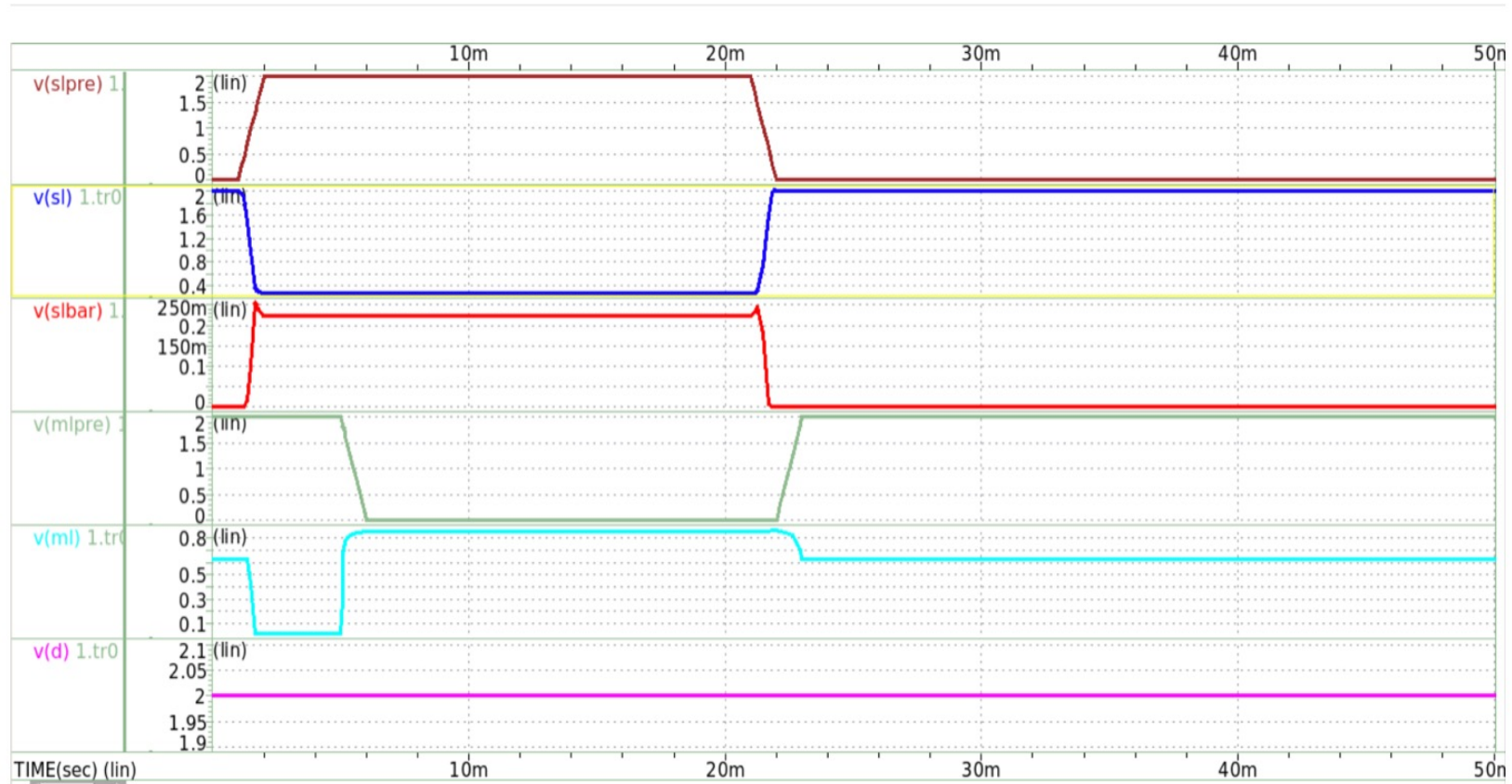


XNOR

D	SL	ML
0	0	1
0	1	0
1	0	0
1	1	1

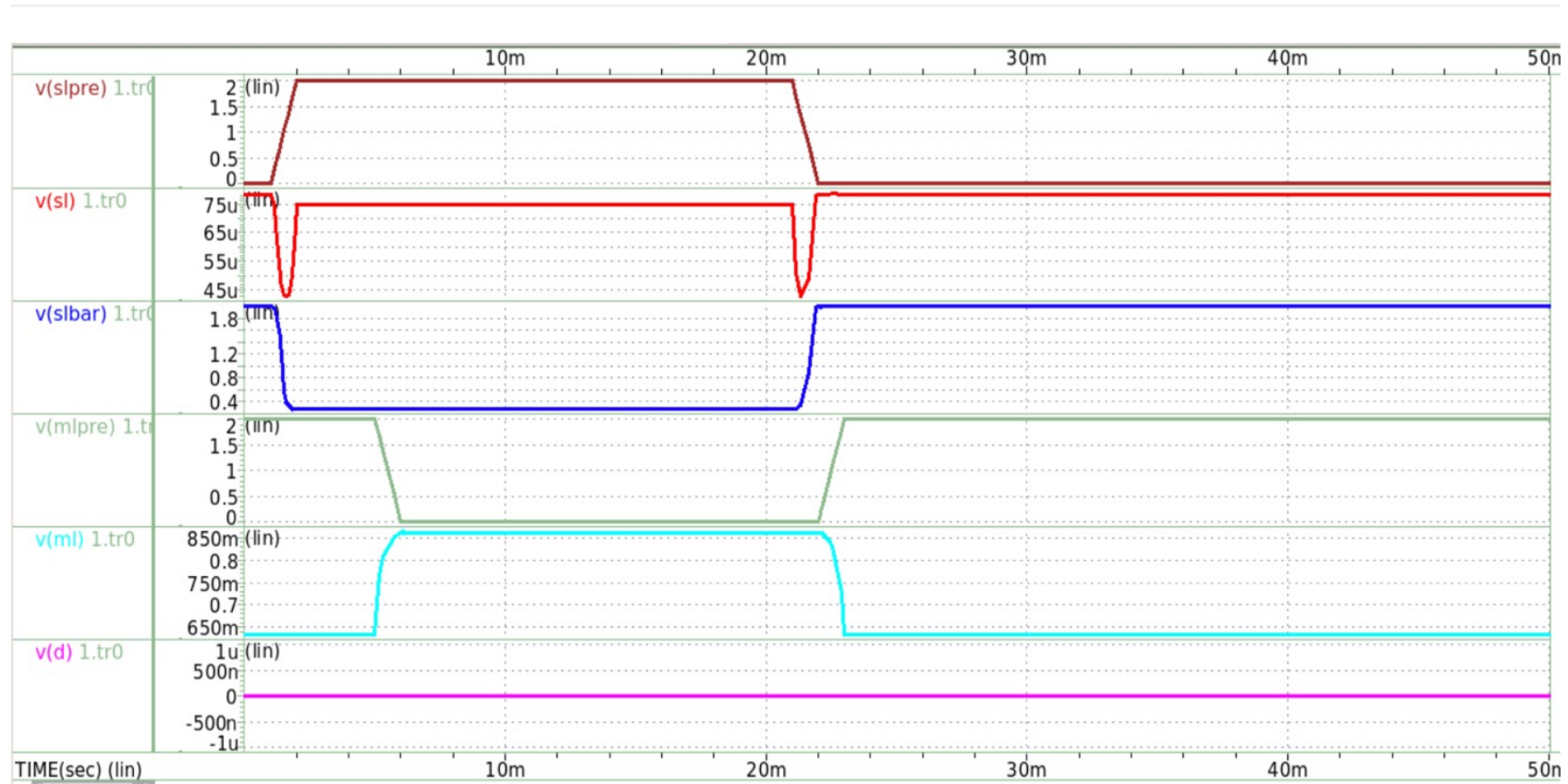
10-T NOR-type CAM

- SL=1, Data=1



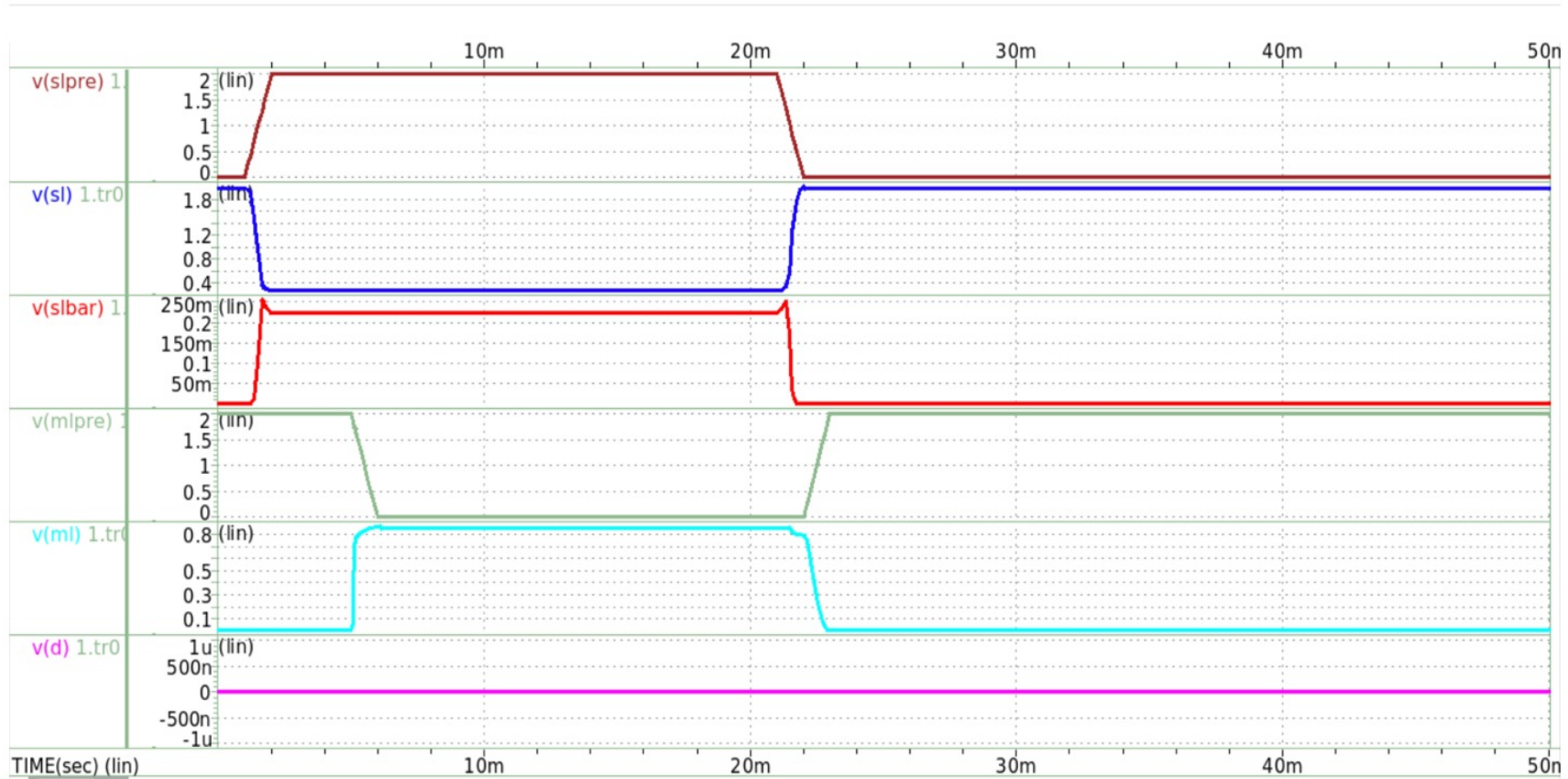
10-T NOR-type CAM

- SL=0, Data=0



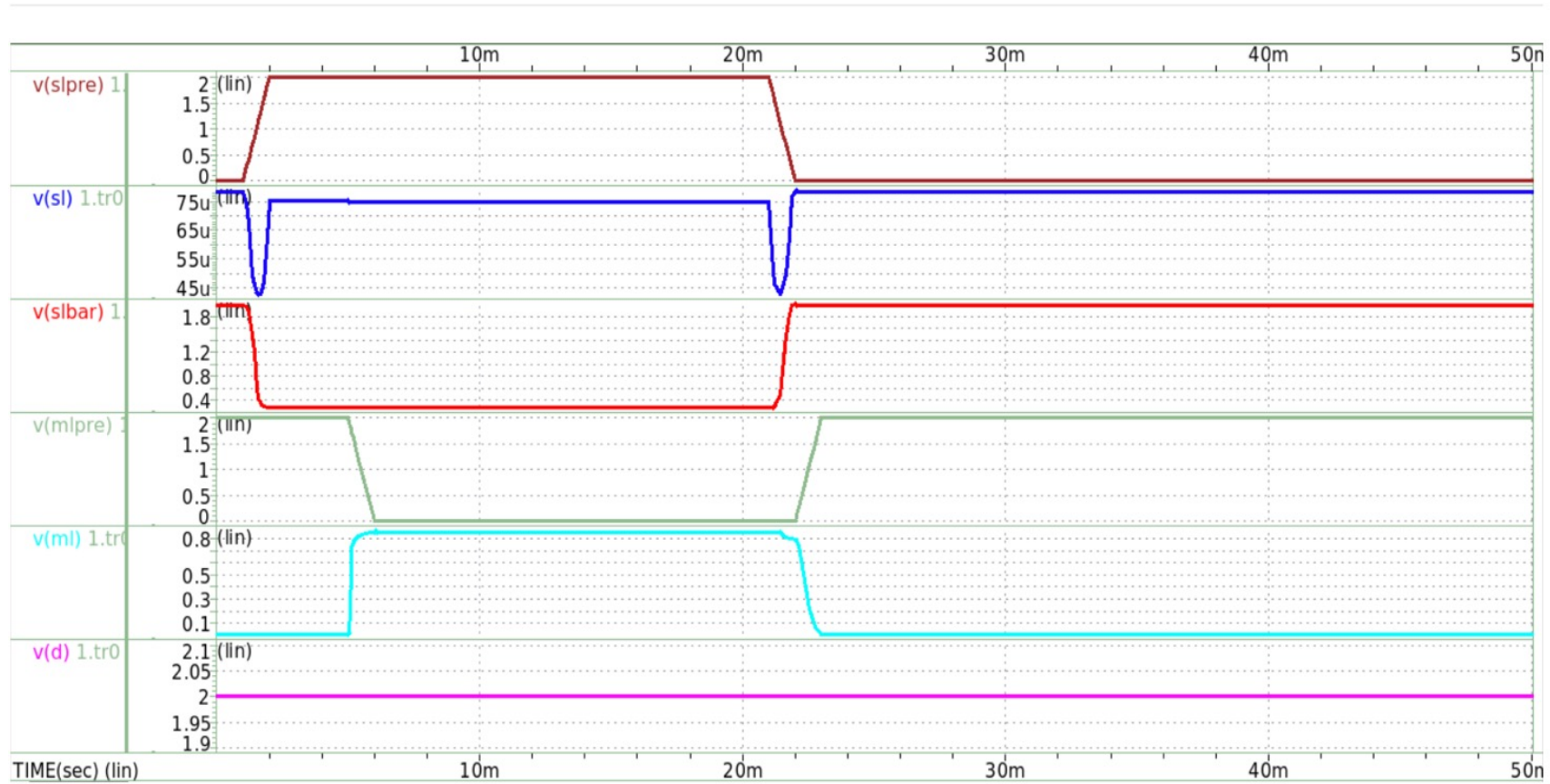
10-T NOR-type CAM

- SL=1, Data=0



10-T NOR-type CAM

- SL=0, Data=1



9-T NAND-type CAM

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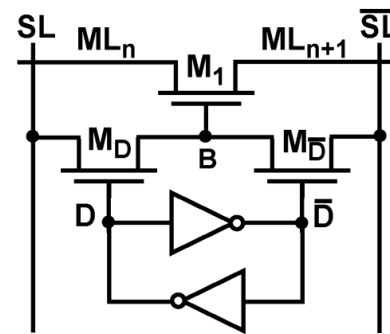
1  .Title 9-T NAND-type CAM
2  ***
3  .protect
4  .lib '/cad/cell_lib/crn90g_3d3_lk_v1d2.l' tt
5  .unprotect
6  ***
7  .global VD! VDD! VSS!
8  VDD    VDD! 0    dc 2
9  VSS    VSS! 0    dc 0
10
11 ***inverter
12 .subckt inv in out
13 Mp out in Vdd! Vdd! pch w=0.12u l=0.1u m=1
14 Mn out in 0 0 nch w=0.12u l=0.1u m=1
15 .ends
16
17 ***buffer
18 .subckt buf in out
19 Mp1 out1 in Vdd! Vdd! pch w=0.12u l=0.1u m=1
20 Mn1 out1 in 0 0 nch w=0.12u l=0.1u m=1
21 Mp2 out out1 Vdd! Vdd! pch w=0.12u l=0.1u m=1
22 Mn2 out out1 0 0 nch w=0.12u l=0.1u m=1
23 .ends
24
25 .param vin = 2
26 *** searchline 的值
27 Vslpre slpre 0 pulse(0V 2V 1ms 1ms 1ms 19ms 50ms)
28
29 Vmlpre mlpre 0 pulse(2V 0V 5ms 1ms 1ms 16ms 50ms)
30
31 *** SL 的值
32 Vsl SLin 0 dc 2

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```

34 *** Data 的值
35 VD D 0 dc 2
36
37 Veval eval 0 pulse(0V 2V 20ms 1ms 1ms 13ms 50ms)
38
39 xinv1 Dbar D inv
40 xinv2 D Dbar inv
41 xinv3 SL SLbar inv
42
43 xbuf1 SLin SL buf
44
45 MD SL D B nch w=0.12u l=0.1u m=1
46 MDbar B Dbar SLbar nch w=0.12u l=0.1u m=1
47 M1 MLC B ML nch w=0.12u l=0.1u m=1
48 Meval MLC eval 0 nch w=0.12u l=0.1u m=1
49
50 Mpre ML mlpre Vdd! pch w=0.12u l=0.1u m=1
51 Mpsl0 SL slpre 0 nch w=0.12u l=0.1u m=1
52 Mpsl0b SLbar slpre 0 nch w=0.12u l=0.1u m=1
53
54 .tran 0 50m 1u
55 .options post
56 .end

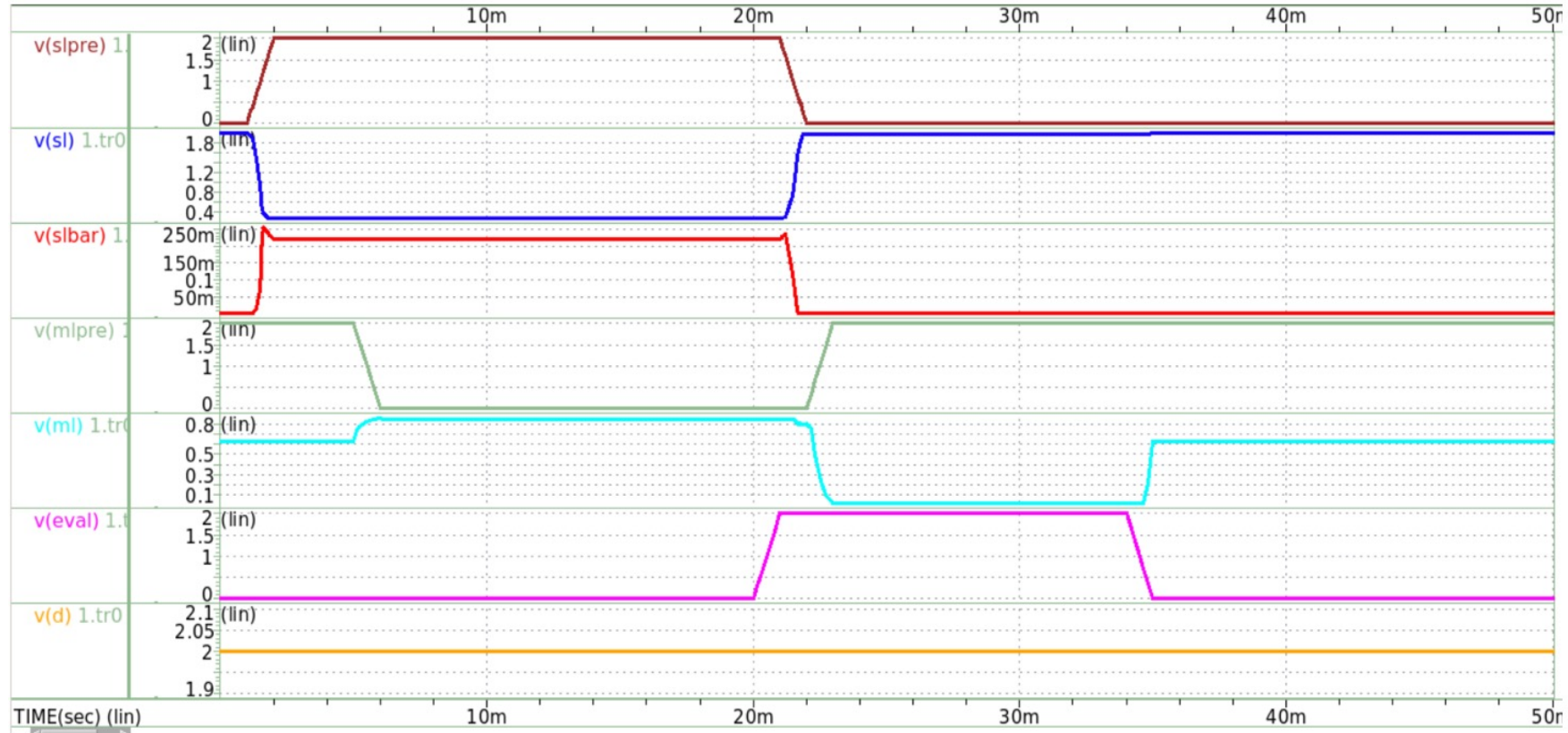
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- When the circuit is matching, matchline will be 0 which means logic 1. (when $ML_{eval}=1$)

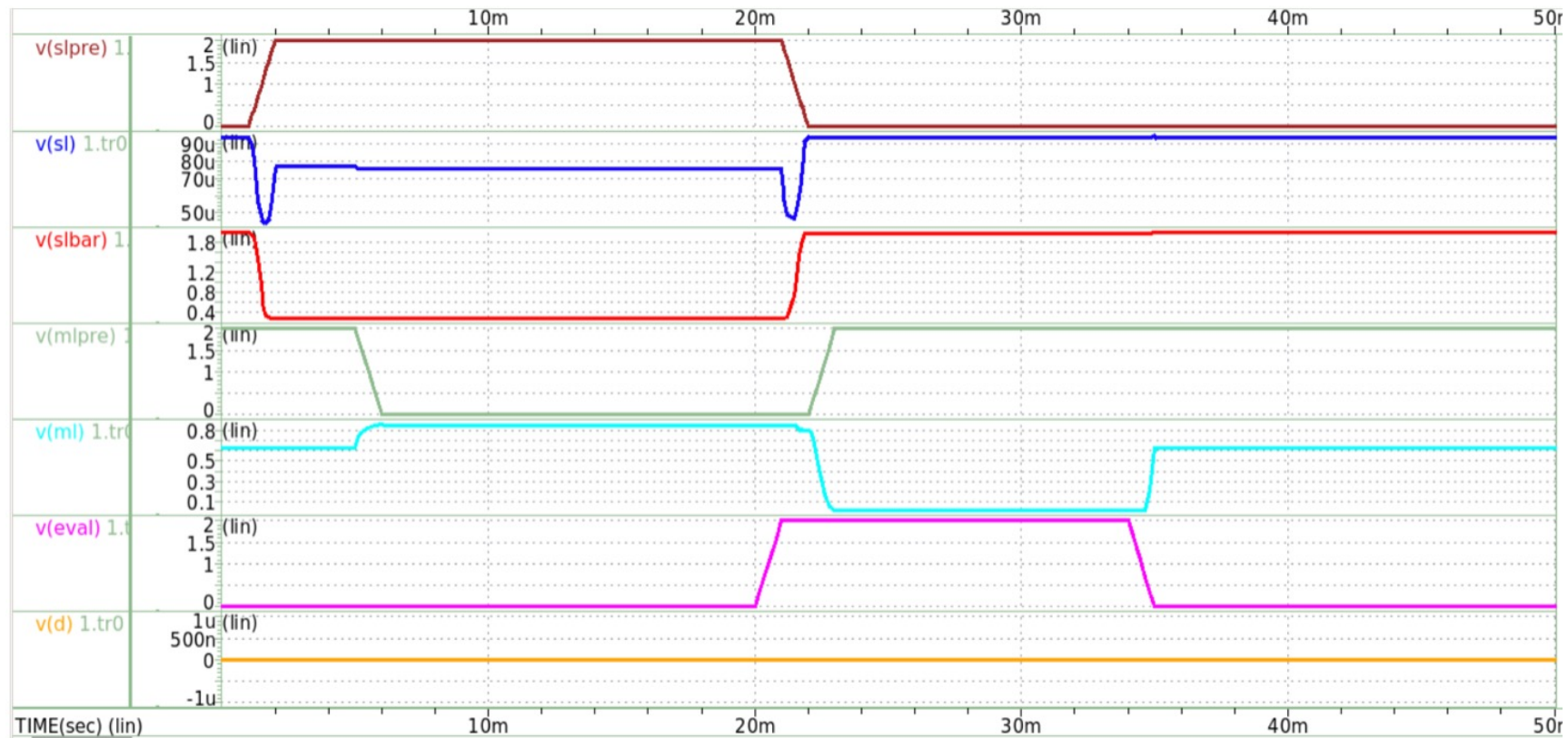
9-T NAND-type CAM

- SL=1, Data=1



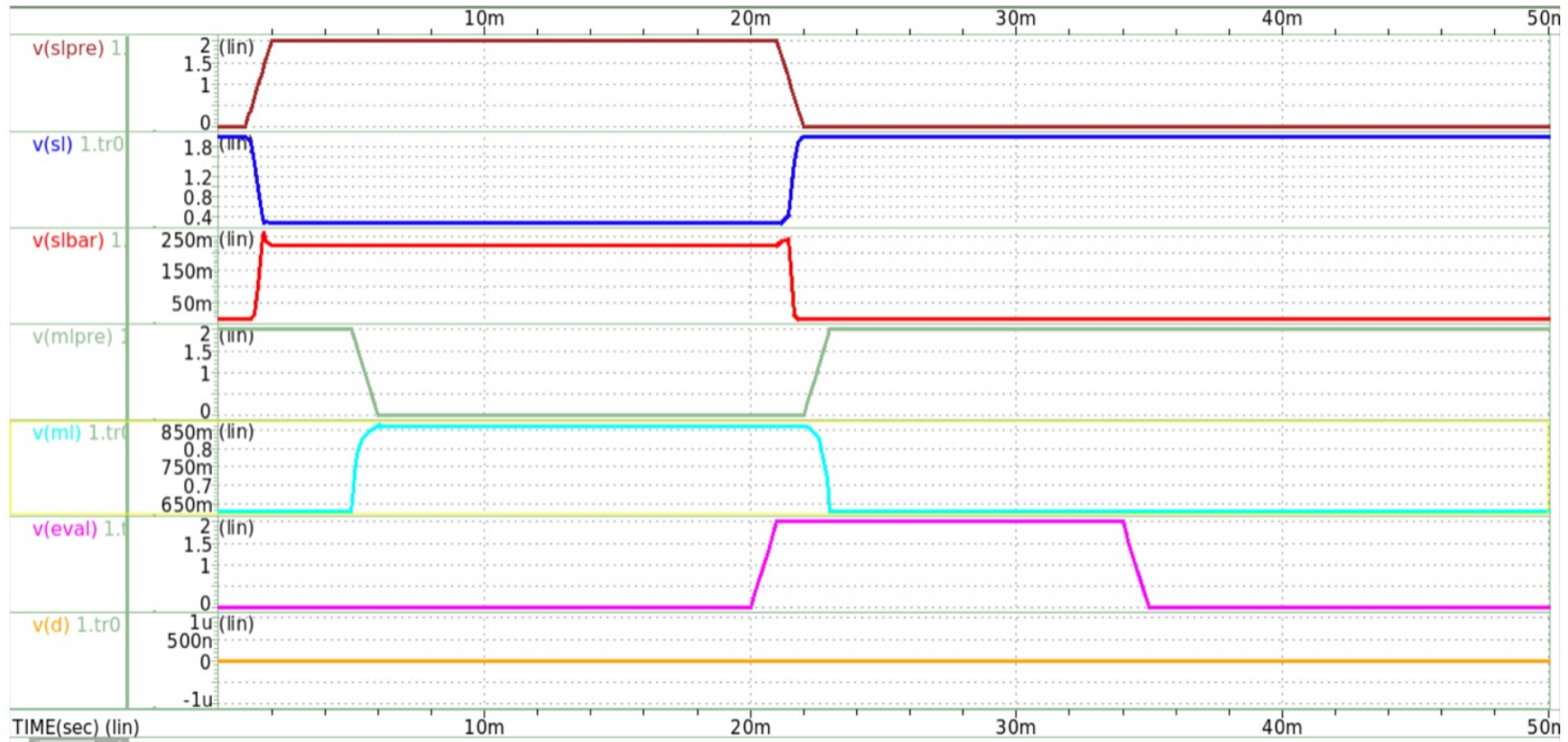
9-T NAND-type CAM

- SL=0, Data=0



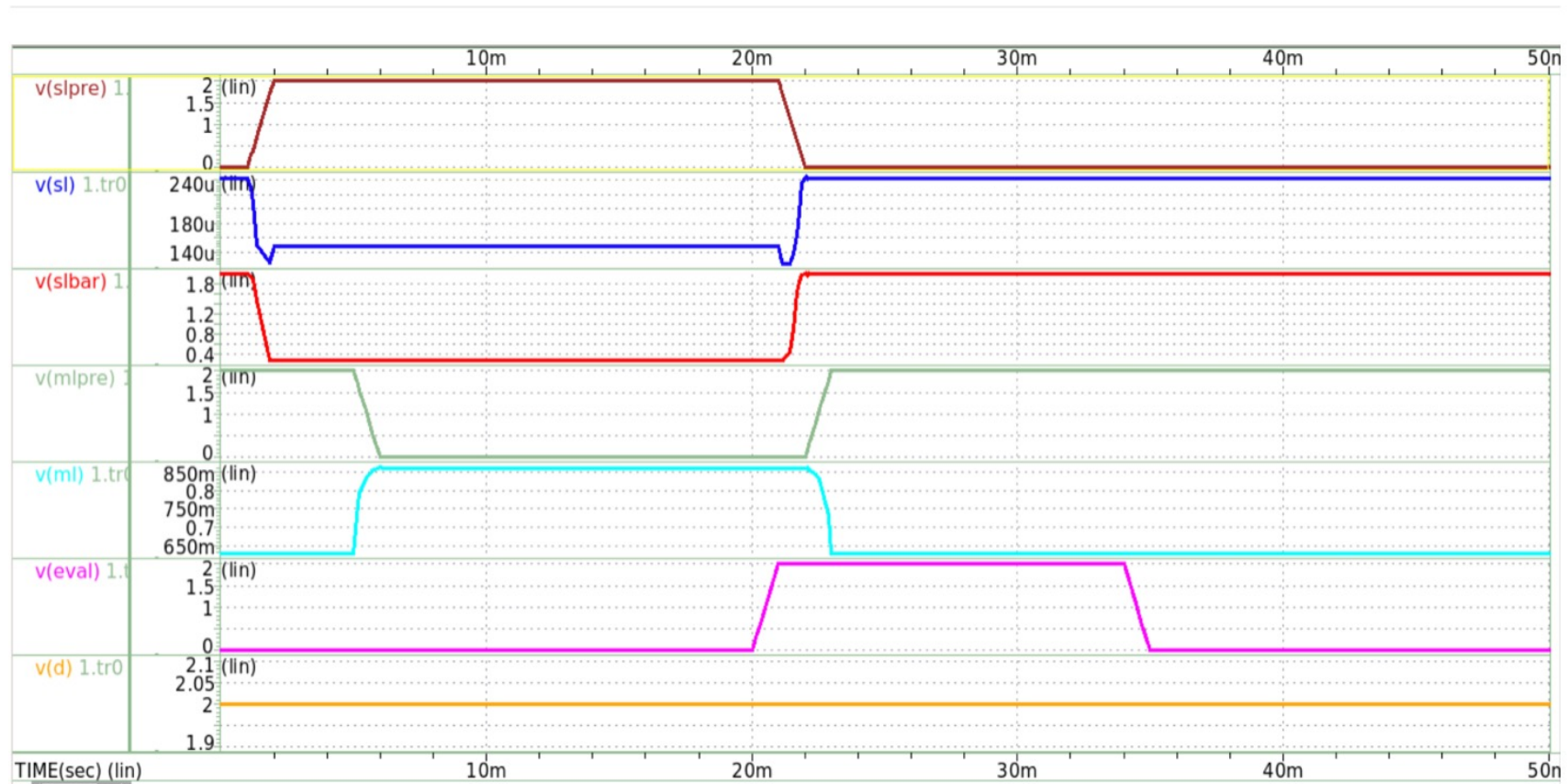
9-T NAND-type CAM

- SL=1, Data=0



9-T NAND-type CAM

- SL=0, Data=1



9-T NOR-type CAM

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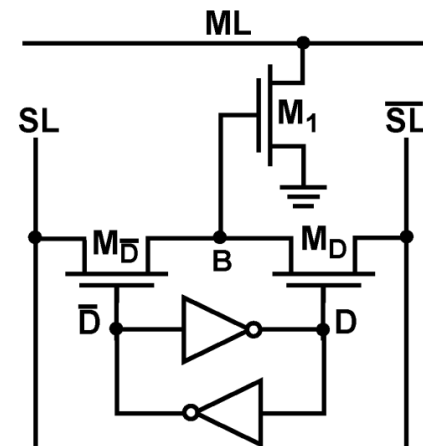
1  .Title 9-T NOR-type CAM
2  ***
3  .protect
4  .lib '/cad/cell_lib/crn90g_3d3_lk_v1d2.l' tt
5  .unprotect
6  ***
7  .global VD! VDD! VSS!
8  VDD    VDD! 0    dc 2
9  VSS    VSS! 0    dc 0
10
11
12  .subckt inv in out
13
14  Mp out in Vdd! Vdd! pch w=0.12u l=0.1u m=1
15  Mn out in 0 0 nch w=0.12u l=0.1u m=1
16  .ends
17
18  ***buffer
19  .subckt buf in out
20  Mp1 out1 in Vdd! Vdd! pch w=0.12u l=0.1u m=1
21  Mn1 out1 in 0 0 nch w=0.12u l=0.1u m=1
22  Mp2 out out1 Vdd! Vdd! pch w=0.12u l=0.1u m=1
23  Mn2 out out1 0 0 nch w=0.12u l=0.1u m=1
24  .ends
25
26  *** searchline 的值
27  Vslpre slpre 0 pulse(0V 2V 1ms 1ms 1ms 19ms 50ms)
28
29  Vmlpre mlpre 0 pulse(2V 0V 5ms 1ms 1ms 16ms 50ms)
30
31  *** searchline 的值
32  Vsl SLin 0 dc 2
33  *** Data 的值
34  VD VD! 0    dc 0

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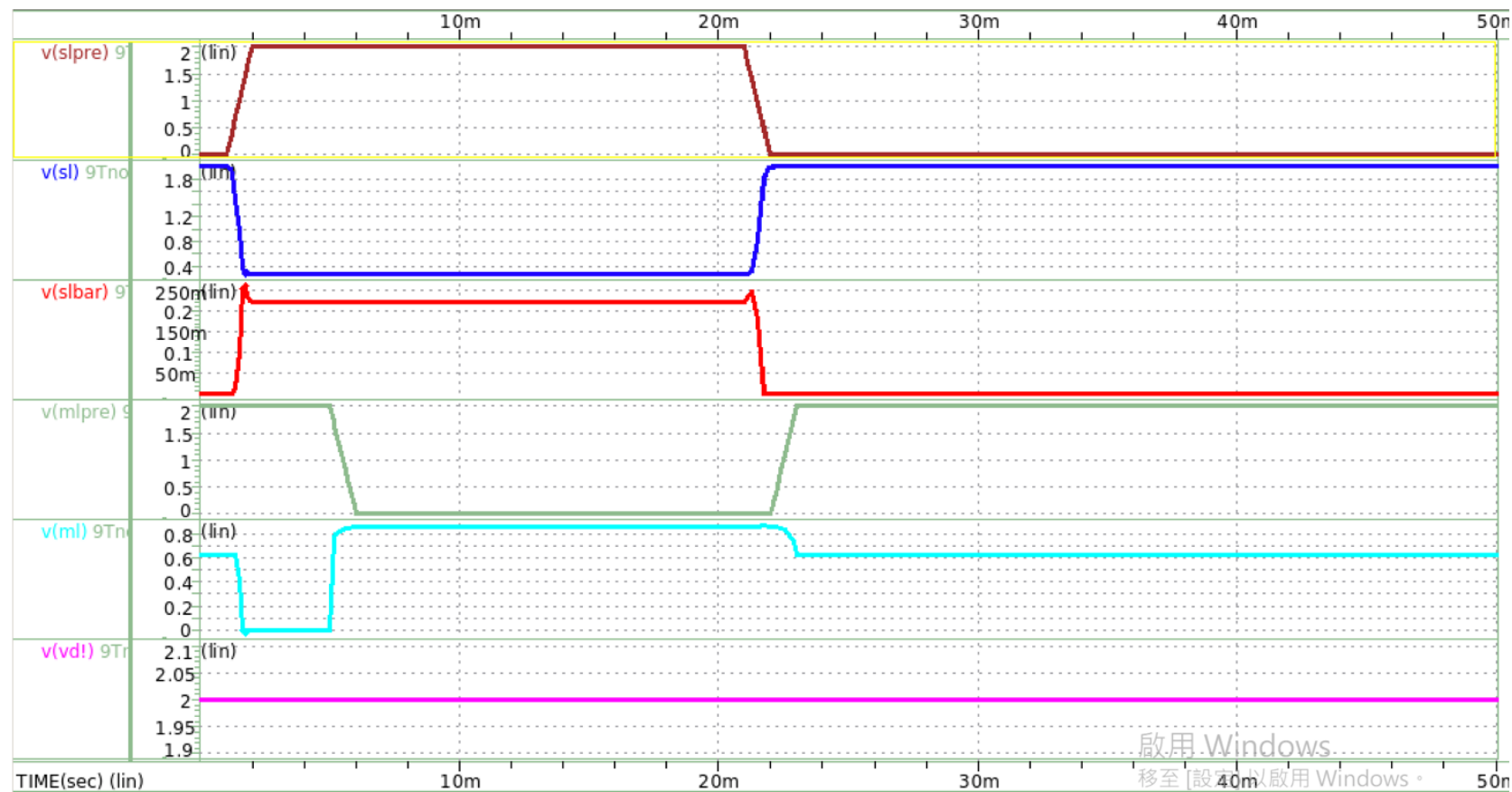
36  xbuf1 SLin SL buf
37  xinv1 Dbar VD! inv
38  xinv2 VD! Dbar inv
39  xinv3 SL SLbar inv
40  MD    B VD! SLbar nch w=0.12u l=0.1u m=1
41  MDbar SL Dbar B nch w=0.12u l=0.1u m=1
42  M1    ML B VSS! nch w=0.12u l=0.1u m=1
43  Mpre   ML mlpres Vdd! pch w=0.12u l=0.1u m=1
44  Mpsl0  SL slpre 0 nch w=0.12u l=0.1u m=1
45  Mpsl0b SLbar slpre 0 nch w=0.12u l=0.1u m=1
46
47  .tran 0 50m 1u
48  ***.dc sweep VD 0 2 0.01
49  .options post
50
51  .end

```



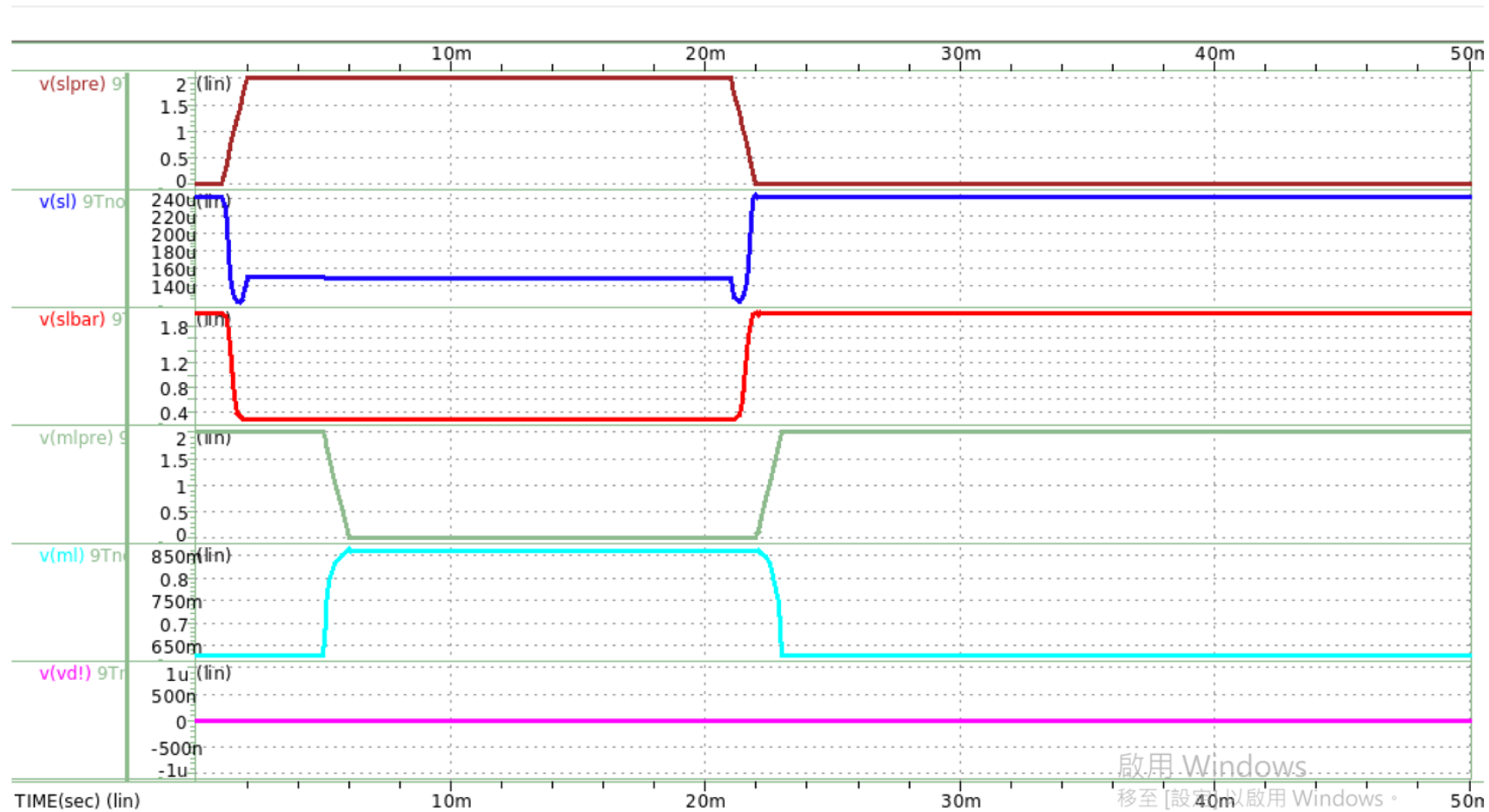
9-T NOR-type CAM

- SL=1, Data=1



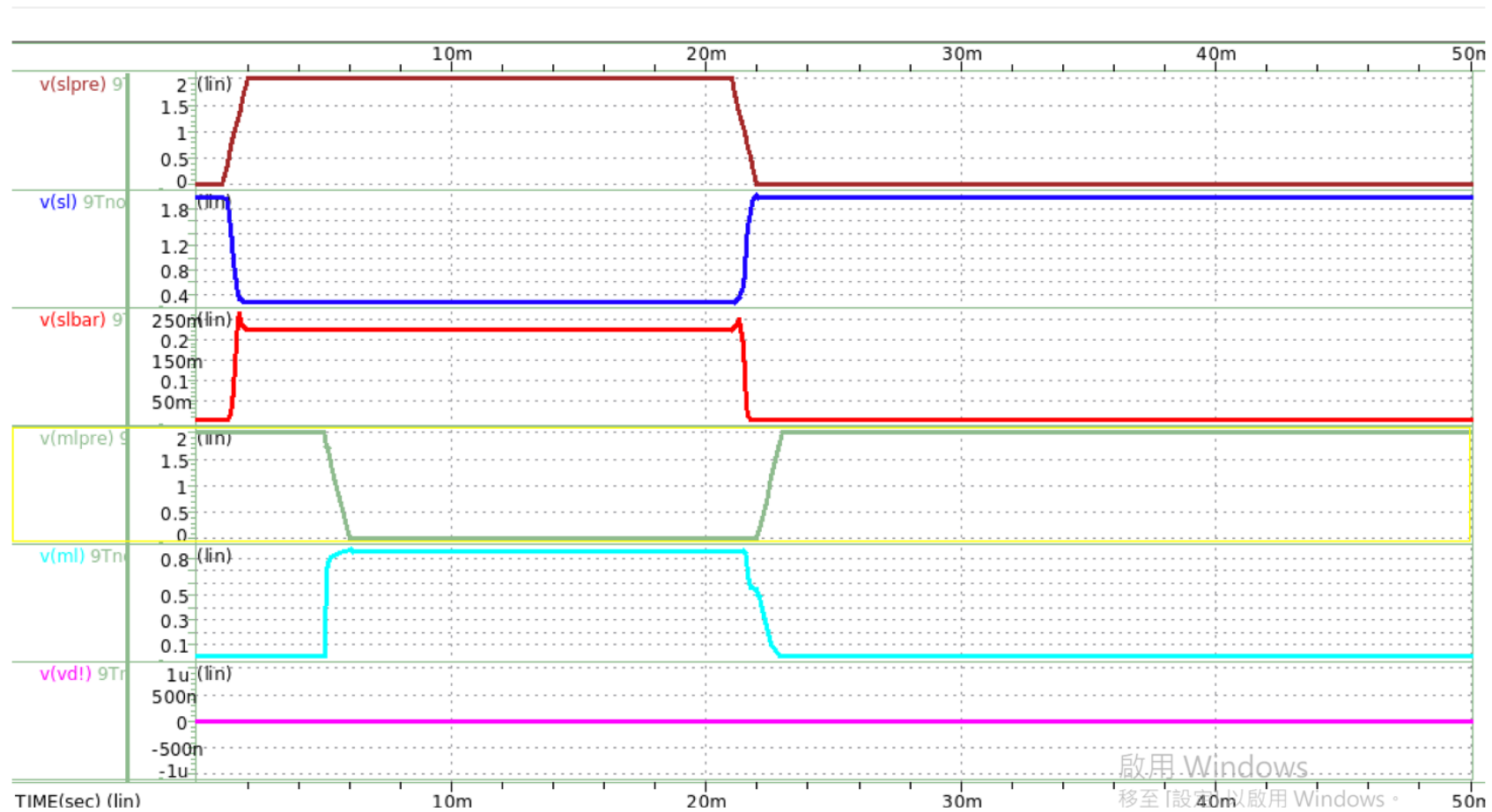
9-T NOR-type CAM

- SL=0, Data=0



9-T NOR-type CAM

- SL=1, Data=0



9-T NOR-type CAM

- SL=0, Data=1

