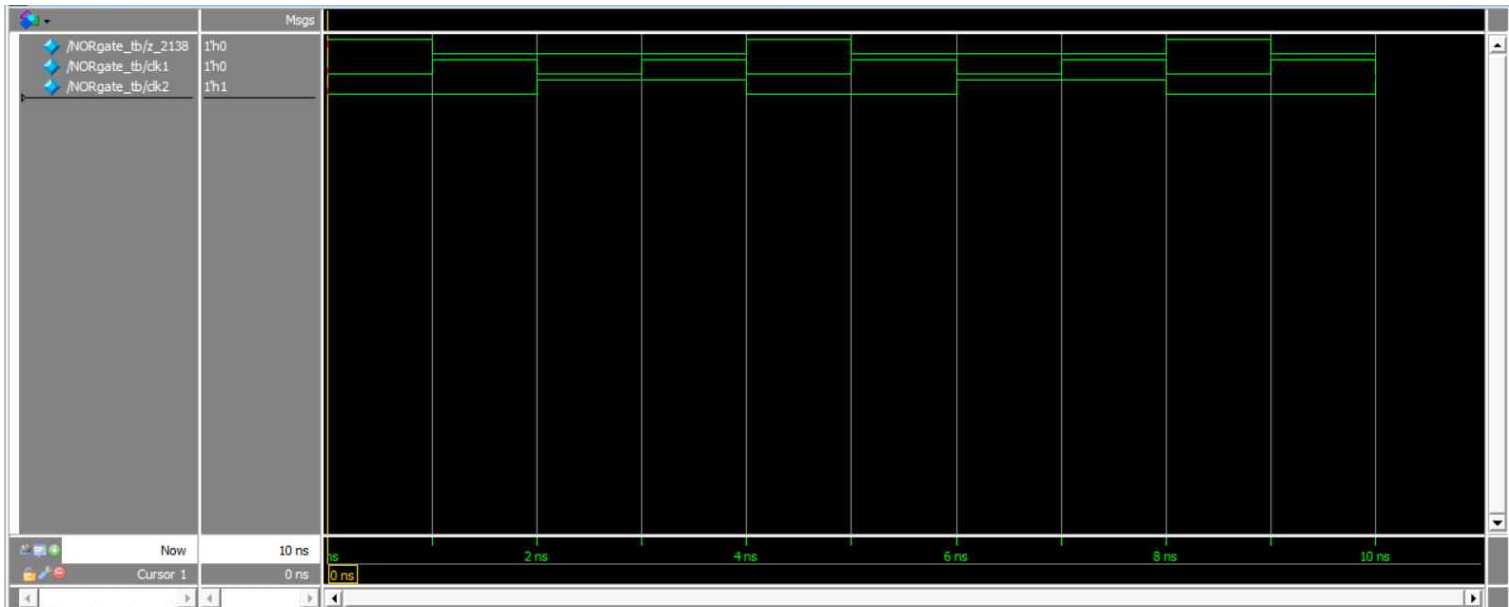2015112138 Sejin Kwon

File Name : NORgate.v // be defined physically

```
module NORgate (a,b,z);
        input a,b; // define input a and b.
        output z; // define output z.

        assign z= (~a)&(~b); // NORgate can be indicated by (~a)&(~b)

endmodule
```

File Name : NORgate_tb.v // be defined logically

```verilog
module NORgate_tb();
      wire z_2138; //one output wire : z_2138
      reg clk1,clk2; //two input reg : clk1, clk2

      NORgate u1 (clk1,clk2,z_2138); // be defined physically

      initial begin
            clk1=0; //clk1 and clk2 initializes as '0'
            clk2=0;
      end

      always begin
            #1 clk1=~clk1; //clk1 is turned to inverse every 1ns
            #1 clk2=~clk2; //clk2 is turned to inverse every 2ns
               clk1=~clk1;
      end
endmodule
```