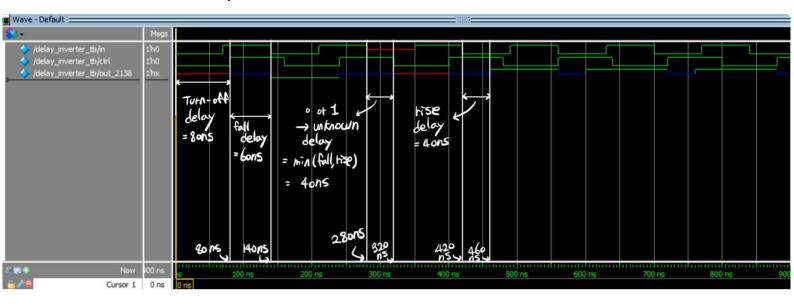
## 2015112138 Sejin Kwon



## delay\_inverter\_tb.v

```
`timescale 1ns/1ns // set time scale
module delay_inverter_tb();
        reg in,ctrl;
        wire out_2138; // set input, ctrl, output.
        notif1 #(40,60,80) n1(out_2138,in,ctrl);
// set rise delay to 40, fall delay to 60 and turn-off delay to 80
        initial begin // initialize input value.
                in = 0;
                ctrl = 0;
                #280 in = 1'bx; // to test with unknown value
                #70 in = 0;
        end
        always //change value to test
                #70 in = \simin;
        always
                #80 ctrl = ~ctrl;
endmodule
```