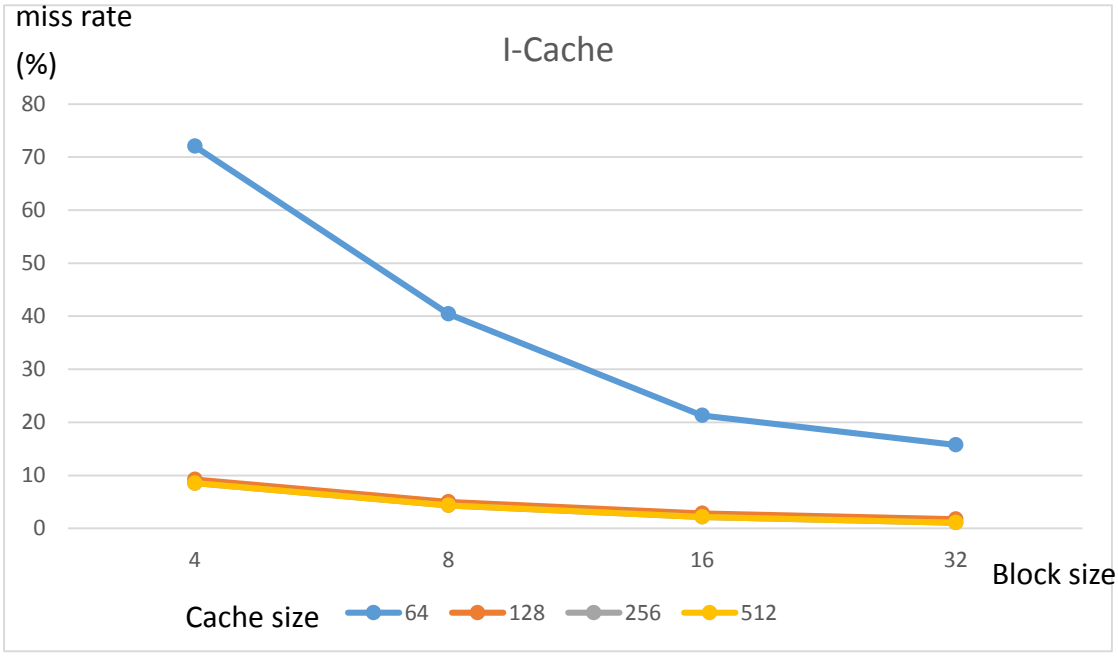
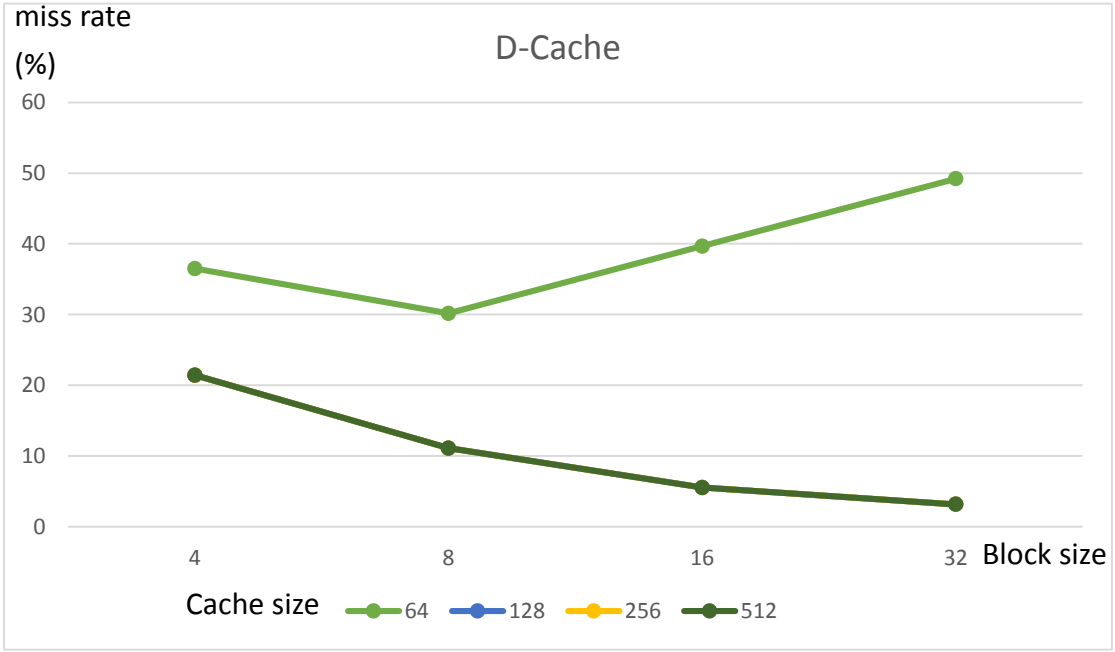
A. Basic Problem



較大的 cache，擁有較多的 block，故能減少 collision。

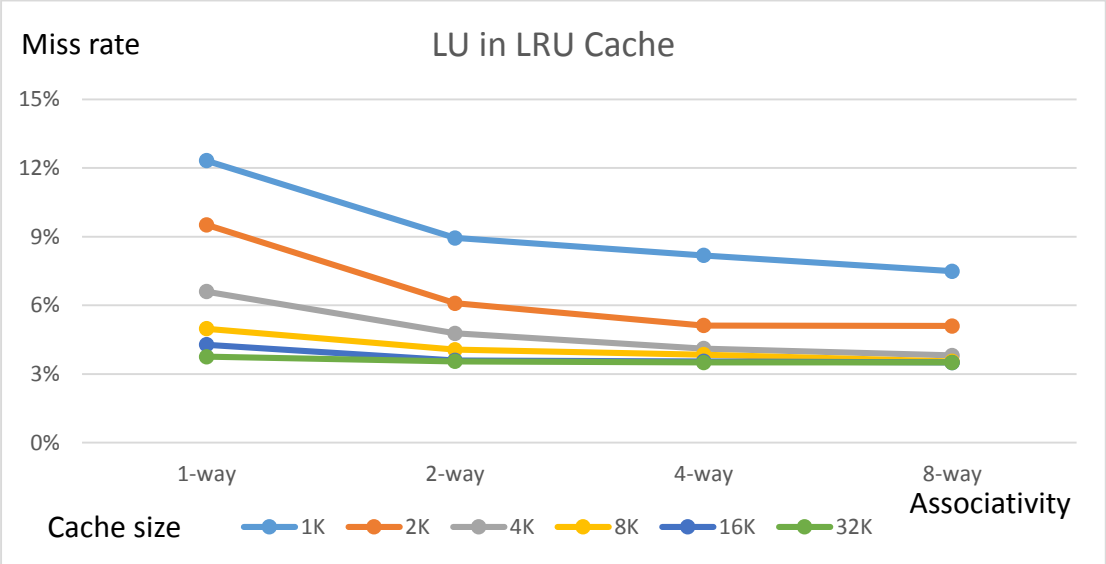
較大的 block size 可以讓一個 block 擁有較多空間，此 icache 中要尋找的 address 有利於使改變 block size 有更顯著的效率。



(128、256、512 皆為同一個曲線)

從 Cache size 為 64 的曲線可看出，改變 block size 大小有可能會造成 miss rate 上升，因為 block size 越大，能擁有的 block 就越少，此 D-cache 的 address 明顯反映出 block 數的減少帶來的負面影響。

B. Advanced Problem



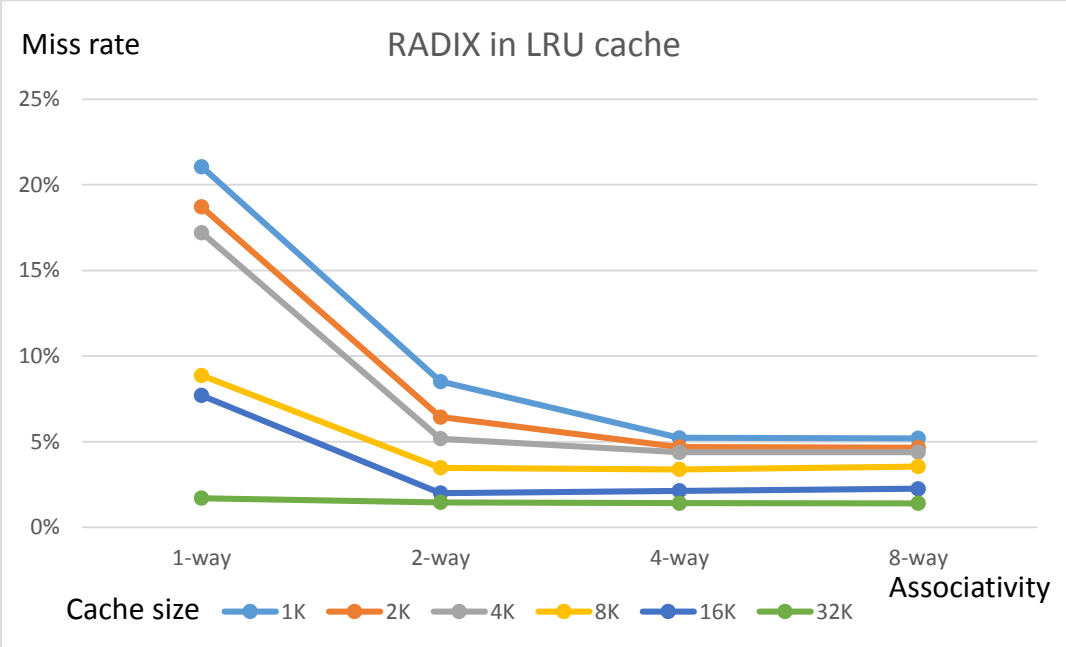
Total Bits

Cache size / Associativity	1K	2K	4K	8K	16K	32K
1-way	8928	17792	35456	70656	140800	280576
2-way	8960	17856	35584	70912	141312	281600
4-way	8992	17920	35712	71168	141824	282624
8-way	9024	17984	35840	71424	142336	283648

增加 associativity -> Less collisions for an index-> reduce miss rate

隨著 cache size 增加 -> 更多 blocks -> Less collisions-> reduce miss rate

Limited variety in address causes little improvement between large cases.



Total Bits

Cache size / Associativity	1K	2K	4K	8K	16K	32K
1-way	8928	17792	35456	70656	140800	280567
2-way	8960	17856	35584	70912	141312	281600
4-way	8992	17920	35712	71168	141824	282624
8way	9024	17984	35840	71424	142336	283648

More associativity and larger cache size are quite like the case in LU.