Lab2: Design a Postfix Calculator

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Lab 2: Design a Postfix Calculator

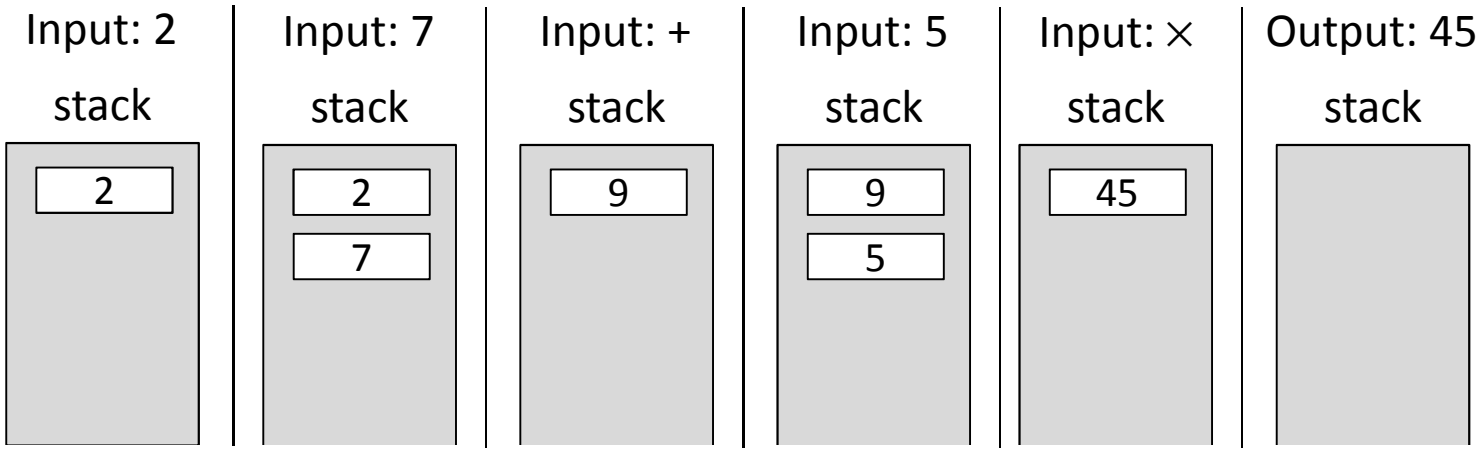
- In this lab, you will design a postfix calculator and use the ISE simulator to evaluate its correctness
  - The postfix calculator has an 4-bit input port that input a 4-bit operand or a 4-bit operator per clock cycle
  - The postfix calculator has an internal stack memory that stores operands and temporary results
  - The calculator only supports three operand +, −, ×
  - The expression has no more than 8 operands
- You will demo to your TA during the lab hours on 10/12
  - The testbench postfix_tb.v can be used to test your design

Postfix Expression

- In normal arithmetic expressions, we put operator in between two operands, for example, 2 + 7. This is called infix expression
- For postfix expression, the operator is written behind the operands, for example, the infix expression “2 + 7” is written as “2 7 +” in postfix notation
- For long expressions, postfix notation does not require parentheses for computation precedence, for example, “(2 + 7) × 5” can be written as “2 7 + 5 ×”

Postfix Computation

- A postfix expression is usually computed with the help of a stack storage using the following rules
  - If an operand is read from the input string, push it to the stack
  - If an operator is read from the input string, pop two operands from the stack and perform the computation, the result is push back to the stack
- For example, to compute 2 7 + 5 ×



Module Specification (1/2)

- Module name: POSTFIX
- I/O ports:
  - Input ports: CLK, RESET, OP_MODE, IN_VALID, IN[3:0]
  - Output ports: OUT[15:0], OUT_VALID
- CLK is the clock signal for synchronous design
  - All signals are sampled at the positive edge of CLK
- RESET is the asynchronous, active low reset signal
- OP_MODE is high if IN[3:0] is an operator; low if IN[3:0] is an operand
- IN_VALID is high when IN[3:0] has valid input
  - High-to-low transition of IN_VALID signals the end of the input

Module Specification (2/2)

- When OP_MODE is high, the operator code of IN[3:0] is as follows:

IN[3:0] when OP_MODE == 1'b1	Operator
0001	+
0010	–
0100	×

- OUT[15:0] is a signed integer in two's complement
- OUT_VALID is high when the result is in OUT[15:0]
- OUT_VALID should go high in less than three cycles after IN_VALID becomes low

Timing Diagram

- The timing diagram of the sample input 2 7 + 5 * is as follows: