Lab1: Design an 8-bit Subtractor

National Chiao Tung University
Chun-Jen Tsai
9/18/2015

Lab 1: Design an 8-bit Subtractor

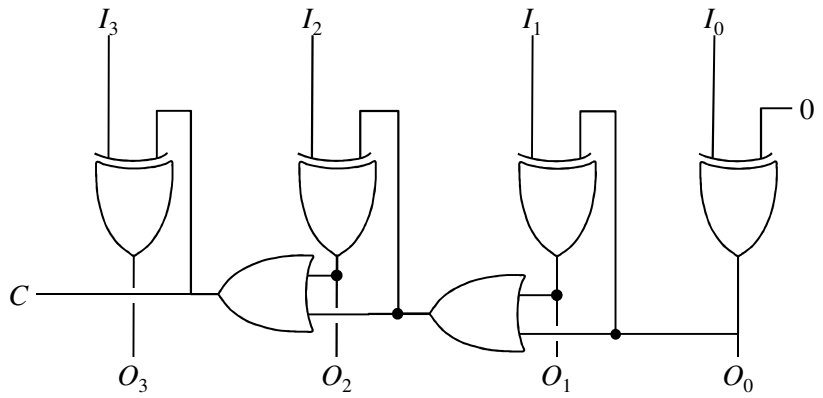
- Through this lab, you will learn how to use the EDA tool for this course
  - Please read the tutorial, *dlb15_Intro_to_EDA_Tools.pdf*, by yourself and start practicing in the lab
  - You should review your old textbook on Digital Circuit Design by Mano to get a feel of the Verilog HDL
- Lab target: design an 8-bit subtractor and use ISim to verify that your design is correct
  - You must demo to your TA BEFORE 9/28 that your circuit works well and that you know how to use the CAD tool for simulation

Design of an 8-bit Subtractor

- An 8-bit subtractor can be constructed by a circuit module that computes the two's complement of the subtrahend and add it to the minuend
  - In the tutorial, *dlb15_Intro_to_ EDA_Tools.pdf*, you have learned how to design a 4-bit full adder
- Your subtractor should have two 8-bit input ports and one 9-bit output port
  - Any negative numbers are in 2's complement
- Only gate-level operators are allowed, see next slide
- You must design your own testbench to make sure your logic works. At demo time, the TA will ask you to add extra test patterns to your testbench

Gate-Level Operators Only, Please

- You cannot use high-level (RTL-level) operators such as “complement”, “negative”, or even “subtraction” operators in your design
- For 2’s complement, you can use the logic diagram as follows (*I*’s are input bits, *O*’s are output bits):



logic diagram of 4-bit 2’s complement