Lab 6: Matrix Multiplication Circuit Design

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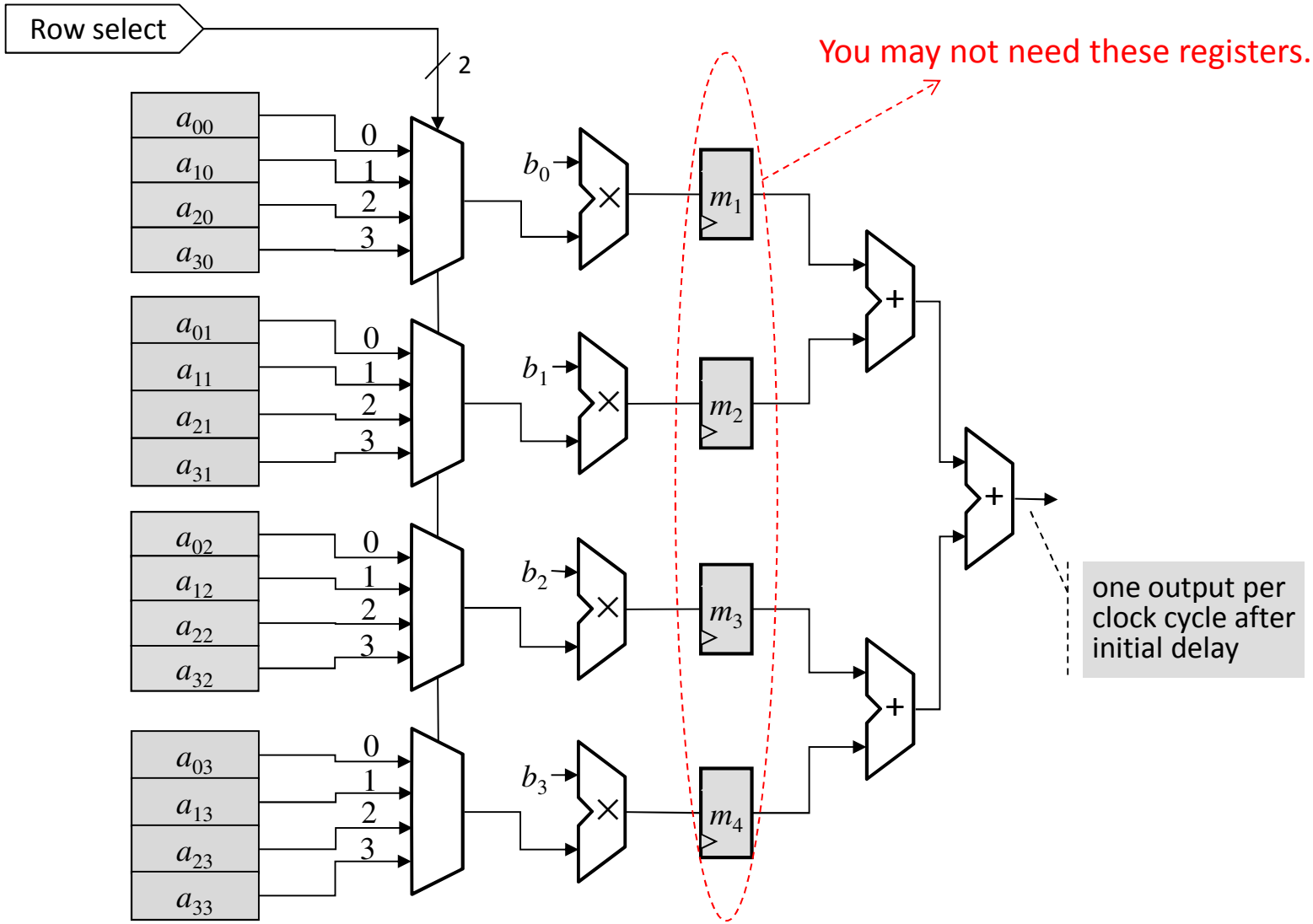
Lab 6: Matrix Multiplication

- In this lab, you will design a circuit to do 4x4 matrix multiplications
  - Read two 4x4 matrices from the UART port
  - Each matrix has 16 unsigned 8-bit elements
  - When the west button is pressed, it triggers the multiplication of the two matrices
  - The output matrix has 16 unsigned 18-bit elements
  - Print the output matrix through the UART to a terminal window
- You will demo the design to your TA during the lab hours on 11/16

Design Constraint of Lab6

- You can use no more than 16 multipliers to implement your system
  - Spartan-3E XC3S500E FPGA has 20 18-bit multipliers
- Your grade will be based on correctness, logic usage, performance, and your skill of coding

Suggested Datapath of $A_{4\times4} \times b_{4\times1}$



Design a FSM to Re-use the Datapath

- You can design a FSM to control the row select signal so that the $A_{4\times4} \times b_{4\times1}$ datapath can finish computation in 4+1 clock cycles
- For $A_{4\times4} \times B_{4\times4}$, you can duplicate the matrix-vector multiplication module four times, so, supposedly, 4×4 matrix multiplication can be computed in five clock cycles

Input-Output of the System

- A binary data file of the two matrices will be send from the TeraTerm window to the FPGA via the UART port
  - The binary data file is of 32 bytes
- You must design a module to convert the resulting matrix into ASCII text and print it to the TeraTerm window
  - Each number (18-bit) of the matrix is displayed with 5 hex digits, for example, 7C4 should be printed as 007C4
  - There must be a space character between two numbers
  - Print a CR/LF pattern (i.e., 0D 0A) after each row of numbers