Operation, Control, and Applications of the Modular Multilevel Converter: A Review

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***Abstract*—The modular multilevel converter (MMC) has been a subject of increasing importance for medium/high-power energy conversion systems. Over the past few years, significant research has been done to address the technical challenges associated with the operation and control of the MMC. In this paper, a general overview of the basics of operation of the MMC along with its control challenges are discussed, and a review of state-of-the-art control strategies and trends is presented. Finally, the applications of the MMC and their challenges are highlighted.**

***Index Terms*—Capacitor voltage balancing, circulating current control, high-voltage direct current (HVDC) transmission, modular multilevel converter (MMC), modulation techniques, redundancy, variable-speed drive systems.**

I. Introduction

THE modular multilevel converter (MMC) has become the most attractive multilevel converter topology for medium/high-power applications, specifically for voltage-sourced converter high-voltage direct current (VSC–HVDC) transmission systems [1]–[14]. In comparison with other multilevel converter topologies, the salient features of the MMC include: 1) its modularity and scalability to meet any voltage level requirements, 2) its high efficiency, which is of significant importance for high-power applications, 3) its superior harmonic performance, specifically in high-voltage applications where a large number of identical submodules (SMs) with low-voltage ratings are stacked up, thereby the size of passive filters can be reduced, and 4) absence of dc-link capacitors.

Over the past few years, there has been a significant effort towards addressing the technical challenges associated with the operation and control of the MMC as well as broadening its applications. The main intention of this review paper is to provide a better understanding of the MMC and its associated technical issues for various applications. This paper provides a comprehensive review on the most recent advances and contributions on the operational issues, modeling, control, and modulation techniques of the MMC. This paper also highlights the emerging applications of the MMC and outlines their associated challenges.

The rest of this paper is organized as follows. Section II introduces the MMC circuit topology along with various SM circuit configurations that can be used in the design of the converter. This is followed by a review of latest contributions on MMC modulation techniques, design constraints, and various operational issues, such as capacitor voltage balancing and circulating current control presented in Section III. Section IV covers the latest developments in the operation and control of the MMC under special conditions, i.e., operation under unbalanced grid conditions and fault-tolerant operation. The promising applications of the MMC along with their technical challenges are reviewed in Section V. The concluding remarks are presented in Section VI.

II. MMC Topology

Fig. 1 shows a schematic diagram of a three-phase MMC. The MMC, as shown in Fig. 1, consists of two arms per phase-leg where each arm comprises N series-connected, nominally identical SMs, and a series inductor L_o. While the SMs in each arm are controlled to generate the required ac phase voltage, the arm inductor suppresses the high-frequency components in the arm current. The upper (lower) arm of three phase-legs are represented by subscript "*p*" ("*n*").

The SMs of the MMC of Fig. 1 can be realized by the following circuits:

1) The half-bridge circuit or chopper-cell [15], [16]: As shown in Fig. 2(a), the output voltage of a half-bridge SM is either equal to its capacitor voltage v_C (switched-on/inserted state) or zero (switched-off/bypassed state), depending on the switching states of the complimentary switch pairs, i.e., $S1$ and $S2$ [4].
2) The full-bridge circuit or bridge-cell [15], [16]: As shown in Fig. 2(b), the output voltage of a full-bridge SM is either equal to its capacitor voltage v_C (switched-on/inserted state) or zero (switched-off/bypassed state), depending on the switching states of the four switches $S1$ to $S4$. Since the number of semiconductor devices of a full-bridge SM is twice of a half-bridge SM, the power losses as well as the cost of an MMC based on the full-bridge SMs are significantly higher than that of an MMC based on the half-bridge SMs [4].
3) The clamp-double circuit: As shown in Fig. 2(c), a clamp-double SM consists of two half-bridge SMs, two additional diodes and one extra integrated gate bipolar

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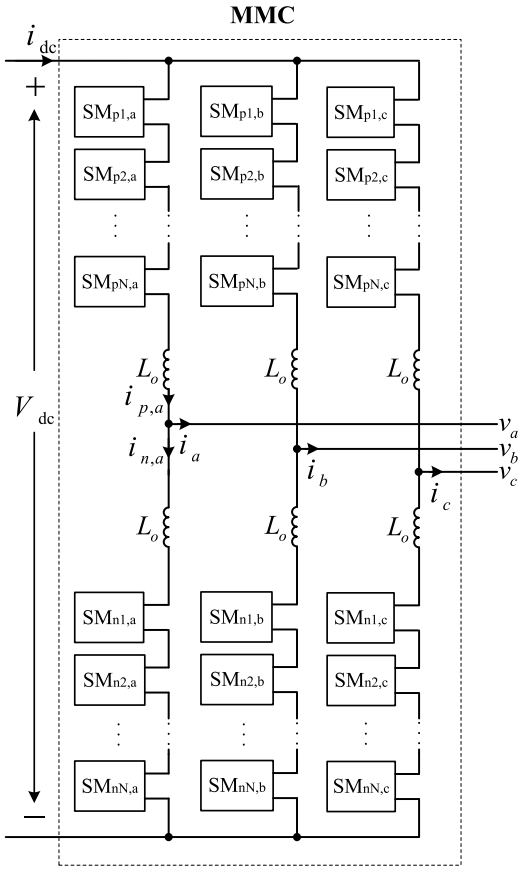

Fig. 1. Schematic representation of the MMC.

transistor (IGBT) with its anti-parallel diode. During normal operation, the switch $S5$ is always switched ON and the clamp-double SM acts equivalent to two series-connected half-bridge SMs. Compared to the half- and full-bridge MMCs with the same number of voltage levels, the clamp-double MMC has higher semiconductor losses than the half-bridge MMC and lower than the full-bridge MMC [4].

4) The three-level converter circuit: As shown in Fig. 2(d) and (e), a three-level SM is comprised of either a three-level neutral-point-clamped (NPC) or a three-level flying capacitor (FC) converter [17], [18]. The three-level FC MMC has the similar semiconductor losses with the half-bridge MMC. However, the three-level NPC MMC has higher semiconductor losses than the half-bridge MMC and lower than the full-bridge MMC. From a manufacturing perspective and control, this SM circuit is not very attractive.
5) The five-level cross-connected circuit: As shown in Fig. 2(f), a five-level cross-connected SM also consists of two half-bridge SMs connected back-to-back by two extra IGBTs with their anti-parallel diodes. Its semiconductor losses are the same as the clamp-double SM [19].

A comparison of various SM circuits, in terms of voltage levels, dc-side short-circuit fault handling capability, and power losses, is provided in Table I. The dc-side short circuit fault is one of the major challenges associated with the MMC–HVDC

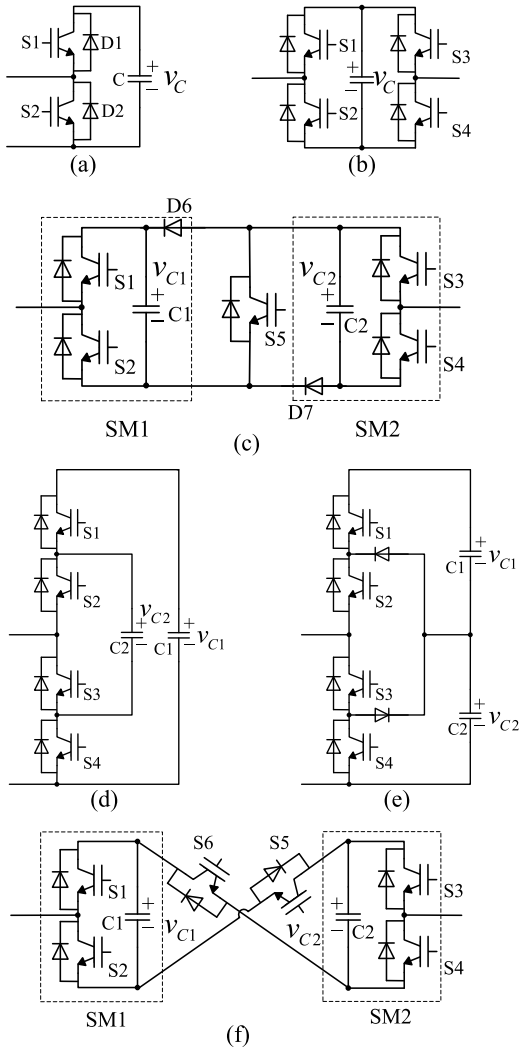

Fig. 2. Various SM topologies: (a) the half-bridge, (b) the full-bridge, (c) the clamp-double, (d) the three-level FC, (e) the three-level NPC, and (f) the five-level cross-connected SM.

system and will be discussed in Section V-A. Among all of the SM circuit configurations, the half-bridge SM has been the most popular SM adopted for the MMC [1]–[12]. This is due to the presence of only two switches in the SM which results in a lower number of components and higher efficiency for the MMC. Hereafter, the half-bridge SM-based MMC is considered. It should be noted that there are a few converter configurations derived from the MMC topology [15], [16]. This paper is only focused on the so called double-star MMC configuration in [15], [16], which is shown in Fig. 1.

III. Modulation, Design, Control, and Modeling of the MMC

A. Modulation Techniques

Various pulse-width modulation (PWM) techniques, based on using a single reference waveform, that have been developed/proposed for the MMC include:

1) Carrier-disposition PWM techniques (CD-PWM) [20], [21]: These techniques require N identical triangular

TABLE I
COMPARISON OF VARIOUS SM CIRCUITS

SM circuit	Voltage levels	DC-fault handling	Losses
Half-bridge	0, v_C	No	Low
Full-bridge	0, $+v_C$	Yes	High
Clamp-double	0, v_{C1}, v_{C2}, $(v_{C1}+v_{C2})$	Yes	Moderate
Three-level FC	0, v_{C1}, v_{C2}, $(v_{C1}-v_{C2})$	No	Low
Three-level NPC	0, v_{C2}, $(v_{C1}+v_{C2})$	No	Moderate
Five-level cross-connected	0, v_{C1}, v_{C2}, $+(v_{C1}+v_{C2})$	Yes	Moderate

carrier waveforms displaced symmetrically with respect to the zero axis. The comparison of the phase voltage reference waveform with the carriers produces the desired switched output phase voltage level. Voltage transitions corresponding to a triangular carrier are associated with the insertion/bypass of a particular SM. Based on the phase shift among the carrier waveforms, these techniques are further classified into: a) phase disposition (PD), b) phase opposition disposition (POD), and c) alternate phase opposition disposition (APOD), shown in Fig. 3(a)–(c), respectively. The disadvantages of using these techniques include unequal distribution of voltage ripple across the SM capacitors that impact the harmonic distortion of the ac-side voltages and large magnitude of circulating currents. To improve the harmonic distortion of the ac-side voltages, a simple carrier rotation technique [22], a modified carrier rotation technique [23], or a signal rotation technique [20] is used to equalize the voltage distribution across all the SM capacitors. In spite of the proposed SM capacitor voltage balancing techniques, the output voltages have a relatively high total harmonic distortion (THD) [20]. To improve the performance of these techniques, a modified PD PWM technique with an SM capacitor voltage balancing technique is proposed in [8]. In this technique, which is based on the PD carrier waveforms, voltage transitions corresponding to a triangular carrier are no longer assigned to a particular SM. In this technique, comparison of the reference waveform with the carrier waveforms produces an $(N+1)$-level waveform that determines the number of SMs to be inserted in the upper and lower arms, respectively. Depending upon the direction of the arm current and the status of the SM capacitor voltages, the determined number of SMs out of the N SMs in the upper (lower) arm are inserted so as to minimize the difference between the SM capacitor voltages. Mei *et al.* in [24] propose a PD PWM technique with selective loop bias mapping method for balancing the SM capacitors. This method implements carrier rotation using the following feedback: a) the maximum/minimum SM capacitor voltages and b) the direction of arm current. The advantages of this technique include: a) absence of additional reference signals to control the SM capacitor voltages and b) ease of implementation in a simple field-implemented gate array (FPGA) even with a large number of SMs.

2) Subharmonic techniques [20]: In these techniques, there are $2N$ identical carrier per phase-leg, either sawtooth

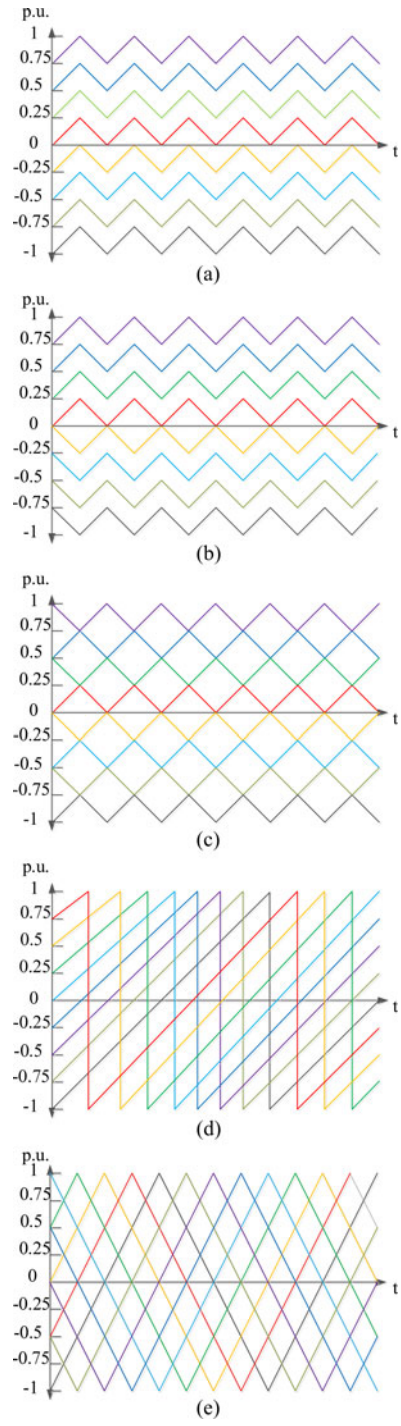

Fig. 3. Multilevel carriers: (a) PD, (b) POD, (c) APOD, (d) saw-tooth, and (e) phase-shifted carriers [20].

waveforms or triangular waveforms, with a phase shift of $\theta = 360^\circ/2N$ with respect to each other, as shown in Fig. 3(d) and (e). Assuming the same number of switching transitions for both the PD PWM and subharmonic techniques, the PD PWM technique produces better line-to-line voltage THD [25], [26].

Additionally, there are several modulation techniques based on using multiple reference waveforms. These modulation techniques include [27]:

1) Direct modulation: In this modulation technique, the upper and lower arm voltages of phase-j are controlled by two complementary sinusoidal reference waveforms, as given by

$$n_{p,j,\mathrm{ref}} = N\frac{\frac{V_{\mathrm{dc}}}{2} - v_{j,\mathrm{ref}}}{V_{\mathrm{dc}}} \tag{1a}$$

$$n_{n,j,\mathrm{ref}} = N\frac{\frac{V_{\mathrm{dc}}}{2} + v_{j,\mathrm{ref}}}{V_{\mathrm{dc}}} \tag{1b}$$

where $v_{j,\mathrm{ref}}$ represents the reference output voltage and $n_{p,j,\mathrm{ref}}$ and $n_{n,j,\mathrm{ref}}$ are the reference waveforms for the number of inserted SMs in the upper and lower arms, respectively. The reference waveforms in (1) are compared with the PD carrier waveforms, which vary between 0 and N, to determine the required number of inserted SMs in the upper and lower arms. The major drawback of the direct modulation technique is the presence of circulating currents, which increase the converter power losses and rating values of the components.

2) Indirect modulation: In this technique, the upper- and lower-arm reference waveforms of phase-j are given by

$$n_{p,j,\mathrm{ref}} = N\frac{\frac{V_{\mathrm{dc}}}{2} - v_{j,\mathrm{ref}} - v^{\Sigma}_{\mathrm{reg},j} - v^{\mathrm{circ}}_{\mathrm{reg},j}}{\sum_{i=0}^{N} v_{cp,i,j}} \tag{2a}$$

$$n_{n,j,\mathrm{ref}} = N\frac{\frac{V_{\mathrm{dc}}}{2} + v_{j,\mathrm{ref}} - v^{\Sigma}_{\mathrm{reg},j} - v^{\mathrm{circ}}_{\mathrm{reg},j}}{\sum_{i=0}^{N} v_{cn,i,j}} \tag{2b}$$

where $v_{cx,i,j}$ represents the capacitor voltage of SM-i in arm-x of phase-j, and $v^{\Sigma}_{\mathrm{reg},j}$ and $v^{\mathrm{circ}}_{\mathrm{reg},j}$ are used to control the total energy in the phase-j leg and balance the energy between the arms, respectively. Similar to the direct modulation technique, the reference waveforms are compared with the PD carrier waveforms to determine the number of inserted SMs in the upper and lower arms. This technique can be further classified into:

   a) Closed-loop control [28]: In the closed-loop control, the term $\sum_{i=0}^{N} v_{cx,i,j}$ in (2) is calculated based on the actual measured capacitor voltages. Furthermore, $v^{\Sigma}_{\mathrm{reg},j}$ and $v^{\mathrm{circ}}_{\mathrm{reg},j}$ are obtained from the closed-loop control of the total energy stored in phase-j leg capacitors and the energy balance between the arms, respectively. The balance between the energy stored in each arm relies on temporarily driving a fundamental frequency sinusoidal circulating current. The advantages of this technique lie in i) the control of the average SM capacitor voltage, which allows operation under low output voltage with high number of voltage levels, and ii) the control of the energy imbalance between the upper and lower arms.

   b) Open-loop control [29]: In the open-loop control, the term $\sum_{i=0}^{N} v_{cx,i,j}$ in (2) is calculated based on the estimated capacitor voltages. Additionally, $v^{\Sigma}_{\mathrm{reg},j} = 0$ and $v^{\mathrm{circ}}_{\mathrm{reg},j}$ is estimated so as to eliminate the harmonics in the circulating currents and guarantee stable operation of the converter. The estimations are obtained by solving the equations describing the dynamics of the converter, using the measured output currents and dc-link voltage. The advantages of this technique lie in the absence of voltage sensors, and simple and fast control. Nevertheless, accurate estimation of the real parameters necessary to describe the dynamics of the system is its main drawback.

3) Phase-shifted carrier-based PWM technique (PSC PWM) [30]: In this technique, each SM of the MMC is controlled independently, and the voltage balancing task of the SMs is divided into an averaging control and a balancing control. The reference waveforms of each SM in the upper and lower arms are given by

$$m_{p,i,j} = \frac{\frac{V_{\mathrm{dc}}}{2N} - \frac{v_{j,ref}}{N} + v_{a,j} + v_{b,i,j}}{v_{cp,i,j}}, \tag{3a}$$

$$m_{n,i,j} = \frac{\frac{V_{\mathrm{dc}}}{2N} + \frac{v_{j,ref}}{N} + v_{a,j} + v_{b,i,j}}{v_{cn,i,j}} \tag{3b}$$

where $v_{a,j}$ and $v_{b,i,j}$ are the averaging and balancing controller outputs, respectively. The averaging and balancing techniques control the average SM capacitor voltage in each phase-leg and the individual SM capacitor voltage, respectively. Comparison of each SM voltage reference waveform with its triangular carrier generates the switching signals for the corresponding SM. The triangular carrier waveforms of each phase-leg are implemented based on the subharmonic techniques. The main drawbacks of this technique are its implementation effort that significantly increases as the number of SMs increases and instability under certain operating conditions [31]. The latter drawback is improved in [31] and [15] by introducing another term, the arm balance control, in the reference waveforms based on the difference in the capacitor voltages of the upper and lower arms.

A brief comparison of the aforementioned modulation strategies is provided in Table II. The control strategies of the MMC are summarized in the block diagram of Fig. 4. In addition to the aforementioned PWM techniques, a SHE–PWM technique is proposed in [32], in which the switching patterns are determined to eliminate the low-order harmonics of the output voltage waveform. The switching patterns are calculated and stored in lookup tables for various modulation indices and the output-voltage phase angle.

Modulation techniques based on fundamental frequency switching have been proposed and investigated in [33]–[36]. A nearest level control (NLC) modulation technique is proposed in [33], in which the voltage level nearest to the desired voltage waveform is selected. Compared to the SHE–PWM, the NLC

TABLE II
COMPARISON OF MODULATION STRATEGIES

Property	Modified PD-PWM [8]	Direct modulation [27]	Indirect modulation [28], [29]	PSC-PWM [30]
No. of reference waveforms	1	2	2	2N
Additional controllers required for stability	No	No	Yes	Yes
Presence of circulating current	Yes	Yes	No	No
Implementation effort	Moderate	Moderate	Low (open-loop)-moderate (closed-loop)	High as $N \uparrow$

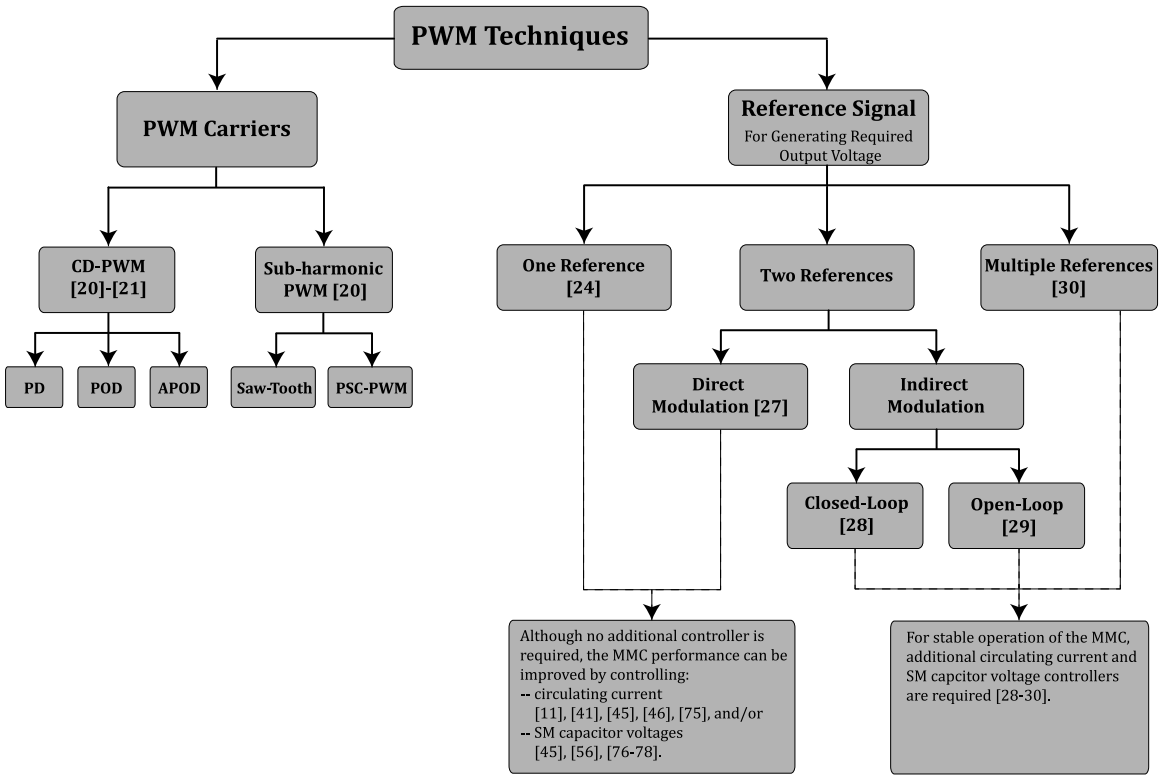

Fig. 4. Overview of various PWM techniques for the MMC.

technique is easy to implement, requires less computational efforts, and uses a lower switching frequency when compared to the PWM techniques. The technique proposed in [35] is based on a fixed pulse pattern fed into the SMs to maintain the stability of the stored energy in each SM, without measuring the capacitor voltages or any other feedback control, and to remove certain output voltage harmonics at any arbitrary modulation index and output-voltage phase angle. The technique proposed in [36] optimizes the pulse patterns to minimize the harmonic distortion of the output voltage. The main advantages of fundamental frequency switching techniques are the reduced switching frequency and low THD of the output voltage without any limitation on the output-voltage frequency. This is opposed to the PWM techniques where the carrier frequency imposes a limit on the output-voltage frequency.

B. SM Capacitor Voltage Balancing

Similar to any other multilevel converter topology, the MMC needs an active voltage balancing strategy to balance and maintain the SM capacitor voltages at $V_{\rm dc}/N$. Deng and Zhen in [37] propose a voltage balancing strategy, which uses the phase-shifted carrier PWM (PSC–PWM) scheme to control the high-frequency components of the MMC arm currents. The capacitor voltage balancing is achieved by assigning appropriate PWM pulses to the SMs of each arm. This voltage balancing strategy does not require the measurement of arm currents, which adds to the control simplicity and reduces the number of sensors. Hagiwara and Akagi in [30] present a voltage balancing strategy, which uses a closed-loop controller for each SM. In [11], a predictive strategy for the control of an MMC is developed, in which the SM capacitor voltages are balanced based on a predefined cost function. The most widely accepted voltage balancing strategy is based on a sorting method [8], [38]–[40]. To carry out the capacitor voltage balancing task based on the sorting method, the SM capacitor voltages of each arm are measured and sorted. If the upper (lower) arm current is positive, out of N SMs in the corresponding arm, $n_{p,j}$ ($n_{n,j}$) SMs with the lowest voltages are identified and inserted. Consequently, the corresponding inserted SM capacitors are charged, and their voltages increase. If the upper (lower) arm current is negative, out of N

SMs in the corresponding arm, $n_{p,j}$ ($n_{n,j}$) of the SMs with the highest voltages are identified and inserted. Consequently, the corresponding inserted SM capacitors are discharged, and their voltages decrease [8]. Regardless of the direction of the upper (lower) arm current, if an SM in the arm is bypassed, the corresponding capacitor voltage remains unchanged. Although the sorting method guarantees capacitor voltage balancing under all of the MMC operating conditions, it produces unnecessary switching transitions among the SMs. Even if the number of required on-state SMs within two consecutive control periods are not changed, the SM insertion/bypassing may happen. This results in increased switching frequency and subsequently power losses, which are undesirable, specifically for high-power systems. The proposed/investigated methods to reduce the switching frequency of an MMC are mainly based on:

1) A closed-loop modified sorting method in conjunction with a phase-shifted carrier PWM strategy, in which the insertion/bypassing of the SMs is carried out based on capacitor voltage measurements [39], [41]. In this method, only a limited number of SMs are sorted within each control cycle. That is, within each control cycle and based on the required voltage level, if additional SMs need to be switched on (off) within each arm, only the off-state (on-state) SMs will be considered for sorting and switching.
2) An open-loop method in conjunction with the selective harmonic elimination (SHE) PWM strategy [35].
3) A hybrid balancing strategy, which combines a predictive error sorting method and the conventional voltage sorting algorithm [42]. This strategy is based on sorting the absolute errors between the one-step forward predicted capacitor voltages and their nominal values. That is, within each control period, the SMs with the minimum predictive voltage errors are chosen to be inserted.
4) A fundamental-frequency balancing strategy, which is based on the conventional sorting method executed at the pre-specified phase angles [42].
5) An optimized capacitor voltage balancing strategy, in which the measured SM capacitor voltages are adjusted before sorting. This strategy focuses on the SMs whose capacitor voltages exceed certain voltage limits, while the switching states of the other SMs remain the same. A maintaining factor is introduced and multiplied by the capacitor voltages of the off-state SMs whose capacitor voltages exceed the voltage limits to increase their possibility of being inserted/bypassed in the following switching cycle [43].
6) A predictive algorithm to calculate and distribute the amount of charge stored in the SM capacitors [44].

C. Mathematical Model

The circuit diagram of a three-phase MMC based on half-bridge SMs is depicted in Fig. 5. Compared to Fig. 1, an additional arm resistor R_o, which models the power losses within each arm of the MMC, is included.

The mathematical model of the MMC, presented in this section, is based on the most widely accepted model in the literature [8], [11], [45]–[47].

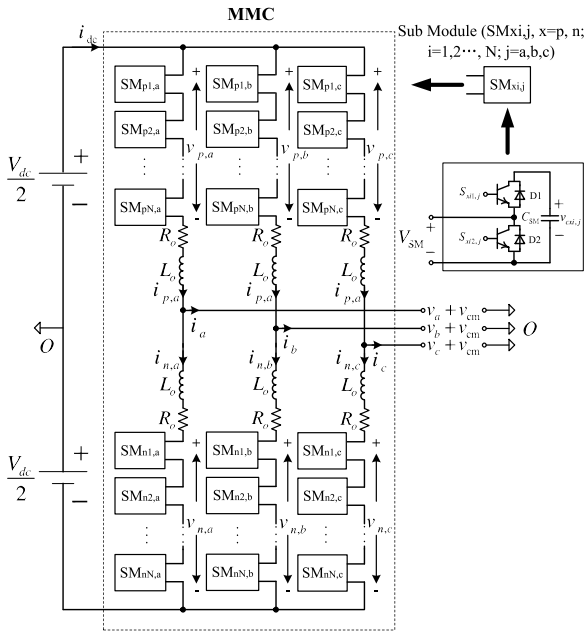

Fig. 5. Circuit diagram of an MMC.

In the MMC of Fig. 5, the upper and lower arm currents of phase-j, $j = a, b, c$, i.e., $i_{p,j}$ and $i_{n,j}$ are expressed by

$$i_{p,j} = \frac{i_{\rm dc}}{3} + i_{{\rm circ},j} + \frac{i_j}{2} \tag{4a}$$

$$i_{n,j} = \frac{i_{\rm dc}}{3} + i_{{\rm circ},j} - \frac{i_j}{2} \tag{4b}$$

where $i_{{\rm circ},j}$ represents the circulating current within phase-j, i_j is the ac-side phase-j current, and $i_{\rm dc}$ is the current in the dc link. The circulating current, based on (4), is given by

$$i_{{\rm circ},j} = \frac{i_{p,j} + i_{n,j}}{2} - \frac{i_{\rm dc}}{3}. \tag{5}$$

The mathematical equations that govern the dynamic behavior of the MMC phase-j are

$$\frac{V_{\rm dc}}{2} - v_{p,j} = L_o \frac{di_{p,j}}{dt} + R_o i_{p,j} + v_j + v_{\rm cm} \tag{6a}$$

$$\frac{V_{\rm dc}}{2} - v_{n,j} = L_o \frac{di_{n,j}}{dt} + R_o i_{n,j} - v_j - v_{\rm cm} \tag{6b}$$

where $v_{p,j}$ and $v_{n,j}$ represent the upper and lower arm voltages of the MMC phase-j, respectively, and v_j and $v_{\rm cm}$ represent the fundamental and common-mode voltage components, respectively. Subtracting (6b) from (6a) and substituting for $i_{p,j}$ and $i_{n,j}$ from (4), the MMC phase voltage is expressed by

$$v_j + v_{\rm cm} = \frac{v_{n,j} - v_{p,j}}{2} - \frac{R_o}{2} i_j - \frac{L_o}{2} \frac{di_j}{dt}. \tag{7}$$

Furthermore, adding (6a) with (6b) and substituting for $i_{{\rm circ},j}$ from (5), the internal dynamics of the MMC circulating current is expressed by

$$L_o \frac{di_{{\rm circ},j}}{dt} + R_o i_{{\rm circ},j} = \frac{V_{\rm dc}}{2} - \frac{v_{n,j} + v_{p,j}}{2} - R_o \frac{i_{\rm dc}}{3}. \tag{8}$$

The upper- and lower-arm voltages of the MMC phase-j are also described by

$$v_{p,j} = n_{p,j} v_{cp,j} \tag{9a}$$

$$v_{n,j} = n_{n,j} v_{cn,j} \tag{9b}$$

where $v_{cp,j}$ and $v_{cn,j}$ are the individual SM capacitor voltages of the upper and lower arms, respectively. Equation (9) is based on the assumption that an active capacitor voltage strategy balances and maintains the capacitor voltages of all SMs within each arm of the MMC equally, i.e., $v_{cxi,j,k} = v_{cx,j,k}$ for $\forall i \in \{1, 2, \ldots, N\}$. Substituting for $v_{p,j}$ and $v_{n,j}$ from (9) in (7) and (8), the following expressions are obtained

$$v_j + v_{\rm cm} = \frac{n_{n,j} v_{cn,j} - n_{p,j} v_{cp,j}}{2} - \frac{R_o}{2} i_j - \frac{L_o}{2} \frac{di_j}{dt} \tag{10a}$$

$$L_o \frac{di_{\rm circ,j}}{dt} + R_o i_{\rm circ,j} = \frac{V_{\rm dc}}{2} - \frac{n_{n,j} v_{cn,j} + n_{p,j} v_{cp,j}}{2} - R_o \frac{i_{\rm dc}}{3}. \tag{10b}$$

Additionally,

$$P_{\rm dc} = P_{\rm ac} + P_{\rm loss} \implies V_{\rm dc} i_{\rm dc} = \sum_{j=a,b,c} v_j i_j + P_{\rm loss} \tag{11}$$

where $P_{\rm loss}$ represents the power losses of the converter.

Each SM capacitor voltage of the MMC is modeled by the power processed by each arm. The power processed by each arm is given by

$$p_{p,j} = v_{p,j} i_{p,j} = n_{p,j} v_{cp,j} i_{p,j} \tag{12a}$$

$$p_{n,j} = v_{n,j} i_{n,j} = n_{n,j} v_{cn,j} i_{n,j}. \tag{12b}$$

The power processed by each phase arm of the MMC can also be expressed by

$$p_{p,j} = \frac{dW_{p,j}}{dt} = \frac{d\left(\frac{\rm N}{2} C_{\rm SM} v_{cp,j}^2\right)}{dt} = v_{cp,j} N C_{\rm SM} \frac{dv_{cp,j}}{dt} \tag{13a}$$

$$p_{n,j} = \frac{dW_{n,j}}{dt} = \frac{d\left(\frac{\rm N}{2} C_{\rm SM} v_{cn,j}^2\right)}{dt} = v_{cn,j} N C_{\rm SM} \frac{dv_{cn,j}}{dt} \tag{13b}$$

where $C_{\rm SM}$ represents the SM capacitor value. Based on (12) and (13), the dynamics of each SM capacitor voltage ripple is expressed by

$$\frac{dv_{cp,j}}{dt} = \frac{i_{p,j}}{N C_{\rm SM}} n_{p,j} = \frac{1}{N C_{\rm SM}} \left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} + \frac{i_j}{2}\right) n_{p,j} \tag{14a}$$

$$\frac{dv_{cn,j}}{dt} = \frac{i_{n,j}}{N C_{\rm SM}} n_{n,j} = \frac{1}{N C_{\rm SM}} \left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} - \frac{i_j}{2}\right) n_{n,j}. \tag{14b}$$

Equations (4), (10), (11), and (14) provide a generalized dynamic model of the MMC, which can be used for control purposes. Similar to this generalized dynamic model of the MMC, references [27] and [28] present a dynamic model of the MMC consisting of the summation of the capacitor voltages in each arm as a state variable, instead of the individual SM capacitor voltages used in the generalized dynamic model.

Reference [46] substitutes for $n_{p,j}$ and $n_{n,j}$ in the generalized dynamic model of the MMC for the direct and indirect modulation strategies to determine the MMC dynamic model for the respective modulation strategies. Substituting for $n_{p,j}$ and $n_{n,j}$ results in a continuous dynamic model, as only the low-frequency components of $n_{p,j}$ and $n_{n,j}$ are considered. Other types of continuous dynamic models as well as the frequency-domain models have been developed in [48] and [49], respectively. The main advantage of these models over the detailed generalized dynamic model lies in faster computation of the system states, specifically for an MMC with a large number of SMs. However, these models do not consider the higher order frequency components. A further simplification of the continuous dynamic models with reduced computational complexity is presented in [50], in which the terminal behavioral model of the MMC in the form of a simplified boost-buck converter model is derived.

D. MMC Design Constraints

The design of MMC, which includes sizing the capacitor and inductor as well as the number of SMs, is based on a few performance indices including arm current ripple, short circuit current, capacitor voltage ripple, reliability, and power losses.

1) Capacitor and Inductor Sizing: The arm inductor L_o functions as a filter to attenuate the high-frequency harmonics in the arm current as well as a dc-side short-circuit current limiter. Therefore, sizing of the arm inductor depends upon the filtering needs and the short-circuit current limit [5], [51], [52]. Additionally, sizing of the arm inductor needs to consider the suppression of undesired low-frequency harmonics in the arm current [53]. To reduce the size of the MMC, reference [54] proposes an integrated arm inductor based MMC, in which the arm inductors in each phase-leg use the same core. The description and design of the integrated arm inductor, based on the need to suppress circulating current, mitigate switching ripple, and limit fault current, is provided in detail in [54].

The SM capacitor is sized based on the tradeoff between its size/cost and voltage ripple [51]. The SM capacitor voltage ripple, under a wide range of operating conditions, has been analyzed in [55]–[59]. Given a permissible peak-to-peak ripple magnitude for the SM capacitor voltage $\delta v_{c,pp}$, the cell capacitance based on [55] is determined by

$$C_{\rm SM} = \frac{P}{3 N m V_c \delta v_{c,pp} \omega \cos\phi} \left(1 - \left(\frac{m \cos\phi}{2}\right)^2\right)^{\frac{3}{2}} \tag{15}$$

where $C_{\rm SM}$ is the SM capacitance, P is the real power transferred, V_c is the nominal voltage of the SM capacitor, m is the modulation index, and $\cos\phi$ is the power factor. Upon

substitution of the low-frequency components of $n_{p,j}$ in (14), as described in [46], (15) is obtained. A more detailed description of the peak-to-peak capacitor voltage ripple along with the SM capacitor design technique is provided in [60].

Based on the relationship between the stored energy and the power transfer capability, an SM capacitor sizing method is also developed in [61].

2) Power Loss Calculation: Compared to the two-level VSC system, in which the semiconductor losses are greater than 1% [13], the semiconductor losses in the MMC can be potentially reduced to less than 1% [13], [62].

The semiconductor losses include the conduction losses and the switching losses. The conduction losses can be determined based on the current flowing through the SMs and the semiconductor device data-sheets from the manufacturer. The switching losses depend on the insertion and bypassing transitions of the SMs, which are due to a) the switching transitions to generate the desired voltage levels based on the reference waveforms and b) selected modulation and capacitor voltage balancing strategies, as discussed in the previous sections.

There are mainly two methods to evaluate the semiconductor losses of the MMC. The first one is based on the simulation model and real-time simulation data [40], [63]–[67]. Though this method has a heavy computational load, it can provide accurate results regardless of the modulation/control strategy, voltage level, and SM circuit topology. The other method, described in [62] and [63], is based on analytical analysis and can potentially reduce the calculation time. However, it is a challenge to guarantee the accuracy since this method is based on the ideal assumptions and specified modulation/control strategies.

The need to calculate the power losses for the design process arises from the tradeoff among power/voltage quality, filtering size, and the efficiency in MMC, based on which the numbers of SMs required in each arm and the switching frequency are decided.

3) Reliability: The MMC, due to its structural modularity, can improve fault tolerance by augmenting redundant SMs in its structure [12], [68], thereby, increasing its reliability. However, beyond a certain maximum redundancy limit, the control hardware limits the converter reliability. That is, any increase in the number of redundant SMs greater than the maximum limit results in deterioration of the converter reliability [69].

E. Circulating Current Control

Circulating currents flowing through the three-phase legs of the MMC originate from the voltage differences among the three phase legs [53], [70] and contain negative sequence components with the frequencies twice the fundamental one [70]. Circulating currents do not have any impact on the ac-side voltages and currents. However, if not properly controlled/suppressed, they increase the peak and rms values of the phase-leg currents, which consequently increase the converter power losses as well as the ripple magnitude of the SM capacitor voltages. Although proper sizing of the arm inductors can suppress the circulating currents to some extent [53], a circulating current controller technique is necessary to effectively control/suppress them [53]. Circulating currents have been modeled and analyzed in [70]–[72]. Reference [71] proposes a circulating current model based on controlling the circulating currents as current controlled voltage sources. This can then be used to control the voltage to reduce the impact of ac components in the circulating currents. Perez and Rodriguez in [72] model the circulating currents along with the dc and ac currents as first-order models, which can be used to easily simulate the system and model the control systems. The ac components of the arm currents, including the circulating currents, are estimated in [70]. This helps in the design of the arm inductor and the SM capacitors to reduce the ac components in the circulating currents.

To control the circulating currents, various techniques have been proposed in the technical literature [11], [28]–[30], [41], [45], [46], [57], [73], [74]. The indirect modulation techniques in [28]–[30], which inherently limit the circulating currents, have already been explained in the previous section. Harnefors *et al.* [46] use an active resistance (proportional controller) to control circulating current, which includes an estimate of the resistance of the arm. The technique suffers from inaccurate estimation of the arm resistance as well as steady-state errors due to the usage of only a proportional controller [75]. Based on the double line-frequency $acb - dq$ transformation, Tu *et al.* [41] eliminate the circulating currents by controlling their dq components with a pair of PI controllers. The main problem associated with this technique is its robustness under ac-side imbalances/faults. Debnath and Saeedifard [45], She *et al.* [73], and Li *et al.* [74] target the elimination of the ac components of the circulating currents through a proportional resonant (PR) controller. Debnath and Saeedifard [45] also includes the control of the dc component of the circulating current so as to improve the stability of the system under unbalanced conditions. The reference for the dc component of the circulating currents is generated from the average SM capacitor voltage controller. The advantage of this technique lies in improved performance under any grid-side imbalance or fault. Yang *et al.* [57] propose a modified switching function to remove the circulating currents in the MMC used in a STATic COMpensator (STATCOM) application. The modified switching function is based on the predicted capacitor voltage ripple, which may become difficult to predict accurately under all operating conditions. A model-based predictive control (MPC) to eliminate the circulating current components is proposed in [11]. In the MPC-based techniques, the control of the circulating currents is necessary to avoid the voltage imbalance between the upper- and lower-arm capacitors. The main drawback of the proposed technique is the calculation effort, specifically for the MMC with a large number of SMs.

F. SM Capacitor Voltage Ripple Reduction Techniques

The SM capacitor voltage ripple has been studied extensively in [55], [57]–[59] is mainly dominated by the fundamental and second-harmonic components. This impacts the sizing of the SM capacitor to maintain the SM capacitor voltage ripple within reasonable limits. In [56], [76]–[78], it is shown that the ripple magnitude of the SM capacitor voltage can be reduced by injecting

appropriate harmonic components in the circulating currents. Based on the power processed by each arm, in [76], an appropriate second-harmonic circulating current is determined to reduce the ripple magnitude of the SM capacitor voltage. Using second- and fourth-harmonic components in the circulating currents, the method in [56] optimizes the energy variation within each arm. Picas *et al.* [78] carry out a similar optimization to [56], except that instead of minimizing energy variation within each arm, it minimizes the peak-to-peak capacitor voltage ripple. Picas *et al.* [77] optimize the rms value of the SM capacitor voltage ripple using the second harmonic component of the circulating current. One of the main drawbacks of the aforementioned capacitor voltage ripple reduction techniques is that they are based on open-loop control. Debnath and Saeedifard [45] propose a closed-loop control technique to mitigate the second-harmonic component of the capacitor voltage ripple and mathematically prove that the proposed technique indirectly leads to reduced ripple magnitude of the capacitor voltage. All of the proposed capacitor voltage ripple reduction techniques lead to increased peak and rms values of the arm currents, which consequently, increase the power losses and current rating of the components. Engel and Doncker [56] investigate an optimization problem to reduce the capacitor voltage ripple by keeping the rms value of the arm current within certain limits, thereby, limiting the power losses in the converter.

In addition to SM capacitor voltage ripple reduction strategies, references [49] and [79] shape the capacitor voltage ripple to maximize the operating region (defined by the power limits). While [79] uses only a second-harmonic circulating current, [49] uses a second-harmonic circulating current and a third-harmonic common-mode phase voltage.

G. Precharging the SM Capacitors and Startup Procedure

At the startup of the MMC, all SM capacitors are required to be charged to a certain equal voltage level before it reaches its normal operation. To reduce the surge currents and the startup time, a fast and smooth startup procedure is preferred. Precharging the SM capacitors and startup procedure of the MMC from the de-energized conditions have been explored in [55], [80]–[86]. The first precharging scheme introduced in [55], [83], and [84] is based on using a dc circuit breaker (CB) and an auxiliary dc source with a voltage equal to the nominal voltage of each SM capacitor. Due to the requirement for a dc CB, this charging scheme is costly [81]. Das *et al.* [80] propose a startup technique, in which an additional resistor is connected in series with the SMs of each arm. The resistor, which is inserted/bypassed by its parallel connected switch, is sized to limit the peak arm current. The main disadvantage of this technique lies in the additional resistive losses while charging the MMC capacitors. Shi *et al.* [81] explain a startup technique where the dc link of the MMC is connected to a diode-bridge rectifier. The startup procedure is performed in two stages: 1) charging the dc-link capacitor and SM capacitors through the diode-bridge rectifier to $V_{\rm dc}$ and $\frac{V_{\rm dc}}{2\rm N}$, respectively, assuming that all the SM capacitors are inserted into the dc-link and the inrush currents are limited by ac-side series resistors, and 2) bypassing the ac-side resistors and then gradually decreasing the number of inserted SMs in each phase-leg from $2N$ to N so as to let the capacitors charge from $\frac{V_{\rm dc}}{2\rm N}$ to $\frac{V_{\rm dc}}{N}$ as well as limit the arm currents. Xu *et al.* [82] propose a precharging circuit comprised of four thyristors per SM of the MMC. Although, by this method, the SMs can be precharged synchronously, and the startup procedure is accelerated, it adds additional complexity and cost to the system.

IV. MMC Operation Under Special Conditions

A. Unbalanced Grid Conditions

The majority of the technical literature on modeling and control of the MMC primarily assume balanced system conditions [1]–[7], [9], [10], [12]. Control of the MMC under unbalanced grid conditions has been reported in [8], [9], [87]– [89]. Under unbalanced grid conditions, the main control objectives are: i) to keep the ac-side currents balanced by suppressing their negative-sequence components, ii) to regulate the net dc-bus voltage, and iii) to control the circulating current and SM capacitor voltages.

Saeedifard and Iravani [8] present a generalized PWM strategy to control the MMC under unbalanced grid conditions, in which the MMC dynamics can be visualized as two decoupled subsystems, the positive- and the negative-sequence subsystems; and each subsystem can be controlled independently. The control strategy presented in [8], however, ignores the internal dynamics of the MMC and is only focused on the external dynamics. Furthermore, in the event of asymmetrical faults on the MMC side or in a transformer-less configuration, the zero-sequence current components become present, which lead to the dc-bus voltage ripple.

Tu *et al.* [87] propose a dc-voltage ripple suppressing controller to remove the zero-sequence voltage components of the dc side under unbalanced grid conditions and to keep the net dc-bus voltage constant. However, under unbalanced grid voltage, there is a double-line-frequency ripple in real power component. In [88] and [89], the circulating currents are analyzed as three components: positive-, negative-, and zero-sequence circulating currents under unbalanced grid conditions. Moon *et al.* [88] propose a circulating currents control method with ac-side positive- and negative-sequence current control to minimize the circulating currents and reduce the ac-side real power ripple under unbalanced conditions. In [89], based on the instantaneous power theory and by using a PR controller, a control strategy is proposed to eliminate the real power ripple and suppress the harmonics in the circulating currents. Guan and Xu in [9] proposed a zero-sequence ac-side current controller, along with the positive- and negative-sequence ac-side current controllers, to operate the MMC–HVDC system with/without the interface transformer under unbalanced grid conditions. In [90], based on a notch filter and a proportional integral resonant controller, a control strategy is proposed to eliminate the dc power ripple by removing the harmonics in the zero-sequence circulating currents under unbalanced grid conditions.

B. Fault Tolerant Operation

As mentioned earlier, the structural modularity of the MMC adds to its redundancy and fault tolerance. In case of any component/SM failure, the failed SM needs to be detected and bypassed. When an open-circuit fault occurs, the output voltage and current of the MMC are distorted. Furthermore, the capacitor voltage of the failed SM may rise up, leading to further, vast destruction.

Given the large numbers of identical SMs and the symmetrical structure of the converter, locating a faulty SM is challenging if adding additional sensors to each SM and/or the converter is not desirable. The extra sensors add to the cost and complexity of the system. In [91], a sliding mode observer-based fault detection method has been proposed. The method, based upon the measured converter arm currents and the SM capacitor voltages, which are already available as the measurement inputs to the control system, detects and locates the faulty SM as well as its failed switch.

V. Applications

A. HVDC Systems

The MMC, initially proposed for HVDC applications, has become the most promising type of VSC for HVDC systems. One of the major challenges associated with the MMC–HVDC system with the conventional half-bridge SMs is the lack of dc-side short-circuit fault handling capability. This problem is of severe concern, particularly for HVDC transmission systems with overhead lines. The existing solutions to interrupt and clear the dc-side short-circuit fault of the MMC–HVDC systems can be summarized as follows:

1) Opening the ac-side CBs. This solution is not sufficiently fast as it takes a few cycles, e.g., two to three cycles, for the CB to trip. Consequently, the freewheeling diodes of the MMC that form an uncontrolled rectifier should tolerate the high fault current for a few cycles. Although parallel connection of a protective thyristor within each SM can bypass the short circuit current flowing through the diodes, the fault current interruption relies on tripping the ac CBs [6], [62], [92]–[94]. Li *et al.* [95] propose a protection strategy to handle the nonpermanent dc-side faults. However, this strategy cannot ensure fast interruption of the fault current.
2) Employing the dc-side CBs. Although a solid-state dc CB for HVDC applications has recently been developed, the technology is not sufficiently mature and cost effective [13], [94], [96]–[99].
3) Embedding the dc fault handling capability in the HVDC converter configuration [4], [13], [19], [62].

In case of a half-bridge MMC–HVDC system, during a dc-side short-circuit fault, the fault current, as shown in Fig. 6(a), flows from the ac-side towards the dc side through the antiparallel diodes of the SMs. Therefore, the half-bridge SMs do not provide any capability of blocking the dc-side short-circuit fault current for the MMC–HVDC system. As shown in Fig. 1, the arm inductors L_o are used to limit the rate of

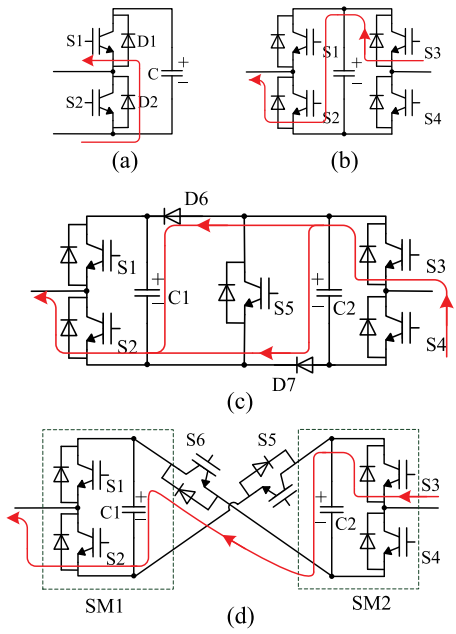

Fig. 6. DC-side short-circuit fault current path for: (a) a half-bridge, (b) a full-bridge, (c) a clamp-double, and (d) a five-level cross-connected SM.

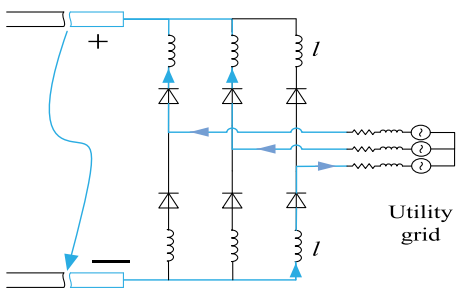

Fig. 7. Equivalent circuit of the MMC system during a dc-side short-circuit fault.

the fault current, i.e., $di_{\rm dc}/dt$. The equivalent circuit of the MMC of Fig. 1 during a dc-side short-circuit fault when all the switches are blocked is shown in Fig. 7. In case of a full-bridge MMC–HVDC system, subsequent to a dc-side short-circuit fault, when all of the IGBTs of the SMs are blocked, the capacitor voltages can generate reversed voltages to block the ac-side currents, as shown in Fig. 6(b). Thus, the full-bridge SMs can provide dc-side short-circuit fault handling capability. In case of a clamp-double MMC–HVDC system, during a dc-side short-circuit fault, when all of the IGBTs are blocked, the two capacitors of the clamp-double SM connected in parallel can generate an opposing voltage to block the short-circuit current, as shown in Fig. 6(c). In case of a five-level cross-connected MMC–HVDC system, after a fault occurrence, when all of the IGBTs are blocked, the two capacitors of the five-level cross-connected SM connected in series can produce an opposing voltage to drive the short-circuit current to zero, as shown in Fig. 6(d). In the MMC–HVDC system based on the clamp-double SMs, although the SMs have the capability to block the dc-side short-circuit current, they can only generate $nv_C/2$ or $V_{\rm dc}/2$ reversed voltage per arm, which is half of the reversed voltage

produced by the full-bridge/the five-level cross-connected SMs per arm. The MMC topology with full-bridge, double-clamp, or five-level cross-connected SMs eliminates the current path of the freewheeling diodes and can potentially interrupt the fault current within a fraction of a second. However, compared to the MMC with half-bridge SMs, this solution sacrifices the cost and power losses [4], [13], [19], [62].

B. Variable-Speed Drives

Application of the MMC to medium-voltage variable-speed drives has been shown to be advantageous over other multilevel converters such as the NPC and series connected H-bridge converter, with respect to the installed silicon area and dc-link energy [100]. However, this application has its own unique control challenges. The main challenge is the large ripple magnitude of the SM capacitor voltages at low frequencies.

The peak-to-peak ripple magnitude of the SM capacitor voltages is given by [83]

$$\delta v_{c,pp} = \frac{I_o}{2C_{\rm SM}\omega}\left(1-\left(\frac{m\cos\phi}{2}\right)^2\right)^{\frac{3}{2}} \tag{16}$$

where $i_{{\rm circ},j} \approx 0$, I_o is the ac-side phase current (i_j) magnitude, m is the magnitude of m_j (the phase-j reference waveform), ω is the ac-side angular frequency, and ϕ is the ac-side power factor angle. As shown in (16), the ripple magnitude of the SM capacitor voltages is inversely proportional to the ac-side frequency and directly proportional to the ac-side phase current magnitude. Consequently, in constant-torque applications, the ripple magnitude of the SM capacitor voltages at low frequencies becomes pronounced. This issue is less pronounced in quadrature torque applications since the current magnitude is proportional to the frequency. Therefore, there is a need to actively mitigate the low-frequency ripple components of the SM capacitor voltages when the MMC is used in variable-frequency constant-torque applications.

The existing capacitor voltage ripple reduction techniques are based on the removal of low-frequency components in the capacitor voltage ripple by introducing a common-mode voltage at the ac-side voltage and a circulating current in the phase-legs of the MMC [101]–[104]. The techniques include:

1) A sine-wave technique: A sinusoidal common-mode phase voltage and circulating current injection technique is proposed in [101], [103], and [104]. The common-mode phase voltage reference and the circulating current are given by

$$m_{\rm cm} = M_{\rm cm}\sin\omega_{\rm cm}t \tag{17a}$$

$$i_{{\rm circ},j} = i_j\left(\frac{1-m_j^2}{M_{\rm cm}}\right)\sin\omega_{\rm cm}t + \frac{m_j i_j}{2} - \frac{i_{\rm dc}}{3} \tag{17b}$$

where $M_{\rm cm}$ and $\omega_{\rm cm}$ are the magnitude and the angular frequency of the common-mode voltage, respectively. The reference waveforms of the SPWM technique, which are used to control the upper and lower arms of phase-j to generate the common-mode voltage are given by

$$m_{p,j} = \frac{1-m_j-m_{\rm cm}}{2} - m_{{\rm circ},j} \tag{18a}$$

$$m_{n,j} = \frac{1+m_j+m_{\rm cm}}{2} - m_{{\rm circ},j} \tag{18b}$$

where $m_{{\rm circ},j}$ is used to control the circulating currents. Based on the PWM strategy, the low-frequency components (averaged over the switching period) in $n_{p,j}$ and $n_{n,j}$ are given by

$$\tilde{n}_{p,j} = N m_{p,j} = N\left(\frac{1-m_j-m_{\rm cm}}{2} - m_{{\rm circ},j}\right) \tag{19a}$$

$$\tilde{n}_{n,j} = N m_{n,j} = N\left(\frac{1+m_j+m_{\rm cm}}{2} - m_{{\rm circ},j}\right) \tag{19b}$$

where $\tilde{x}$ represents the low-frequency components in x. Considering the low-frequency components, (14) becomes

$$\frac{d\tilde{v}_{cp,j}}{dt} = \frac{1}{NC_{\rm SM}}\left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} + \frac{i_j}{2}\right)\tilde{n}_{p,j} \tag{20a}$$

$$\frac{d\tilde{v}_{cn,j}}{dt} = \frac{1}{NC_{\rm SM}}\left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} - \frac{i_j}{2}\right)\tilde{n}_{n,j}. \tag{20b}$$

Due to the attenuating effects of the SM capacitor, the high-frequency (switching frequency and higher) components of the SM capacitor voltages are negligible. Therefore

$$v_{cp,j} \approx \tilde{v}_{cp,j} \tag{22a}$$

$$v_{cn,j} \approx \tilde{v}_{cn,j}. \tag{22b}$$

Substituting for $m_{\rm cm}$ from (17a), $i_{{\rm circ},j}$ from (17b), $\tilde{n}_{p,j}$ from (19a), and $\tilde{v}_{cp,j}$ from (22a) in (20a), the upper-arm phase-j SM capacitor voltages are deduced as

$$\begin{aligned}\frac{dv_{cp,j}}{dt} &\approx \left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} + \frac{i_j}{2}\right)\frac{1}{C_{\rm SM}} \\ &\quad\times\left(\frac{1-m_j-m_{\rm cm}}{2} - m_{{\rm circ},j}\right) \\ &= \frac{1}{C_{\rm SM}}\left[\left(-\frac{m_j M_{\rm cm}}{4} - \frac{M_{\rm cm}}{4}\right.\right. \\ &\quad\left.+\frac{\left(1-m_j-m_j^2+m_j^3\right)}{2M_{\rm cm}}\right) i_j\sin\omega_{\rm cm}t \\ &\quad\left.+\frac{\left(1-m_j^2\right)}{4} i_j\cos 2\omega_{\rm cm}t\right].\end{aligned} \tag{23}$$

Assuming a sufficiently fast closed-loop circulating current controller, $i_{{\rm circ},j} = i_{{\rm circ},j,{\rm ref}}$. Considering appropriate phase shifts, similar expressions can be concluded for voltage ripple of the SM capacitors in the lower arm of phase-j. As shown in (23), the SM capacitor voltages do not contain low-frequency components. This contributes to reducing the magnitude of the voltage ripple.

Although by the sine-wave technique, the ripple magnitude of the SM capacitor voltages is reduced, the large magnitude of the circulating current increases the converter power losses and rating values of the components. To resolve this problem, a square-wave technique has been proposed in [102].

2) A square-wave technique: As opposed to the sinusoidal common-mode voltage and circulating current injection, to reduce the peak and rms values of the circulating current, a square-wave common-mode voltage and circulating current injection technique is proposed in [102]. The main drawback of the square-wave injection technique lies in the control of the circulating currents. The circulating current in phase-j, $i_{\mathrm{circ},j}$, of the MMC is controlled by the voltage across the arm inductor, which is given by $v_{\mathrm{circ},j} = L_o \frac{di_{\mathrm{circ},j}}{dt}$. To inject a square-wave circulating current, at certain instances $v_{\mathrm{circ},j} \to \infty$, which is impossible to attain. In reality, the maximum attainable $v_{\mathrm{circ},j}$ is limited and depends on the MMC circuit parameters. This limitation, consequently, impacts the control of the circulating current and the ripple magnitude of the SM capacitor voltages. Furthermore, because of the finite rise/fall time of the square-wave circulating current, additional harmonic components are introduced into the circulating current that would further impact the results.
3) A hybrid technique: A square-wave common-mode voltage and a sinusoidal circulating current (with or without a third harmonic component) is proposed in [105]. The advantage of this technique over the sine-wave technique is the reduction in peak/rms value of circulating currents and the SM capacitor voltage ripple. The common-mode reference voltage waveform and the circulating current are given by

$$m_{\mathrm{cm}} = \begin{cases} M_{\mathrm{cm}} & \text{if } 0 < t \le \dfrac{1}{2f_{\mathrm{cm}}} \\ -M_{\mathrm{cm}} & \text{if } \dfrac{1}{2f_{\mathrm{cm}}} < t \le \dfrac{1}{f_{\mathrm{cm}}} \end{cases}, \quad (24a)$$

$$i_{\mathrm{circ},j} = i_j \left(m_1 \sin\omega_{\mathrm{cm}} t + m_3 \sin 3\omega_{\mathrm{cm}} t\right) \times \left(\frac{1-m_j^2}{\frac{4}{\pi}M_{\mathrm{cm}}}\right) + \frac{m_j i_j}{2} - \frac{i_{\mathrm{dc}}}{3} \quad (24b)$$

where f_{cm} is the common-mode frequency. m_1 and m_3 in (24b) are determined to minimize the rms value of $i_{\mathrm{circ},j}$ and to mitigate the low-frequency components of the SM capacitor voltage ripple. Substituting for m_{cm} from (24a), $i_{\mathrm{circ},j}$ from (24b), $\tilde{n}_{p,j}$ from (19a), and $\tilde{v}_{cp,j}$ from (22a) in (20a), the upper-arm phase-j SM capacitor voltages are deduced as (21). To mitigate the low-frequency components of the SM capacitor voltage ripple, the last term in (21) should be enforced to zero, i.e.,

$$1 - m_1 - \frac{m_3}{3} = 0. \quad (25)$$

Two of the solutions for (25) include: i) $m_1 = 1, m_3 = 0$, and ii) $m_1 = 0.9, m_3 = 0.3$ [105]. While the former solution uses less voltage across the arm inductor to control its circulating current and may use a higher common-mode voltage, the latter minimizes the peak/rms value of the circulating current for a given common-mode voltage peak. That is, the two solutions provide a trade-off in terms of the performance parameters like peak/rms value of circulating current and SM capacitor voltage ripple. Therefore, the solution and the common-mode frequency chosen for a particular application is based on a Pareto optimal front of the performance parameters.

The application of the MMC in quadrature torque motor drives has been investigated in [106] and [107]. An inner current control strategy, comprising the arm current control through the control of the individual SM capacitor voltages as well as the control of the average SM capacitor voltage in each phase, along with a motor control to limit the inrush current during startup is presented in [106]. In [107], a startup technique for an induction machine with fan/blower-type load is presented where the SM capacitor voltages are slowly increased from a small value to their nominal value as the speed of the machine is built. This strategy assists in maintaining the capacitor voltages within the voltage limits. However, it is assumed that the synchronous frequency at startup is sufficiently high to have a small capacitor voltage ripple which may not be the case in all variable-speed drives. An optimized pulse pattern modulation for high-speed drives is implemented in [36]. The advantages of this technique have been explained in Section III-A. Energy balancing control strategies at low-frequency and normal mode of operation are proposed in [108] for the application of MMC in variable-speed drives. The strategies include a low-frequency mode based on the technique proposed in [101], a normal mode at other frequencies, and a switchover mode between the two modes of operation. Dimensioning of the MMC for propulsion system of electric ships, considering the induction machine and load characteristics, is presented in [109], in which the control

$$\frac{dv_{cp,j}}{dt} \approx -\frac{1}{C_{\mathrm{SM}}}\left[\frac{i_j\left(1-m_j^2\right)}{2}\left(\left(\frac{m_1}{3}-\frac{m_3}{2}\right)\cos 2\omega_{\mathrm{cm}}t + \left(\frac{m_1}{6}+\frac{m_3}{2}\right)\cos 4\omega_{\mathrm{cm}}t\right) + \frac{i_j\left(1-m_j^2\right)}{2}\frac{m_3}{6}\cos 6\omega_{\mathrm{cm}}t \right.$$
$$- \frac{i_j}{4}\left(1+m_j\right)\sum_{k=0}^{\infty}\frac{4M_{\mathrm{cm}}}{\pi\left(2k+1\right)}\sin\left\{\left(2k+1\right)\omega_{\mathrm{cm}}t\right\} + \left(1-m_j\right)\frac{\pi i_j\left(1-m_j^2\right)}{8M_{\mathrm{cm}}}\left(m_1\sin\omega_{\mathrm{cm}}t + m_3\sin 3\omega_{\mathrm{cm}}t\right)$$
$$\left. - \frac{i_j\left(1-m_j^2\right)}{2}\left(m_1\sin\omega_{\mathrm{cm}}t + m_3\sin 3\omega_{\mathrm{cm}}t\right)\sum_{k=2}^{\infty}\frac{1}{\left(2k+1\right)}\sin\left\{\left(2k+1\right)\omega_{\mathrm{cm}}t\right\}\right] + \frac{i_j\left(1-m_j^2\right)}{4}\left(1-m_1-\frac{m_3}{3}\right) \quad (21)$$

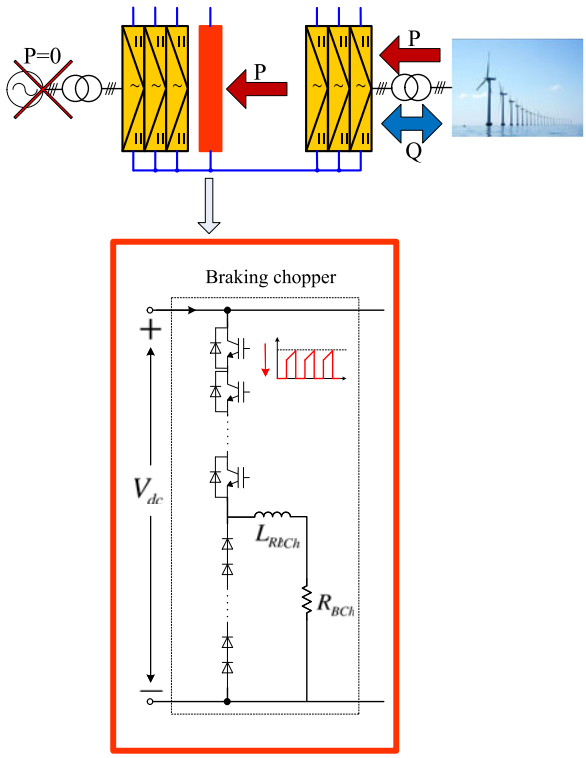

Fig. 8. Conventional braking chopper circuit.

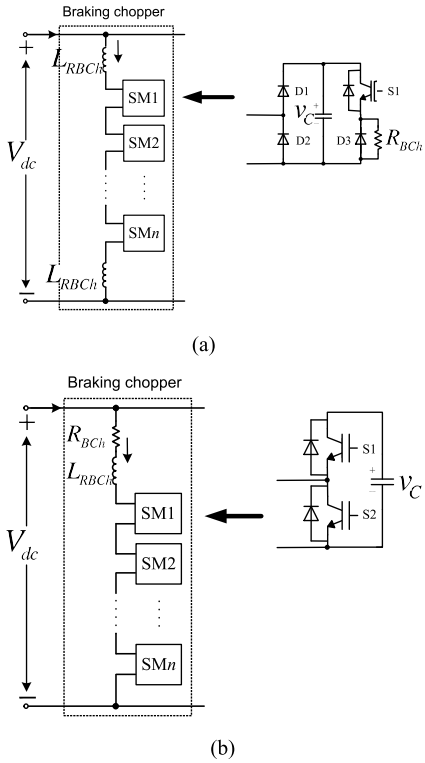

Fig. 9. Modular braking chopper circuits based on the MMC concept.

strategy proposed in [101] is adopted to control the ripple magnitude of SM capacitor voltages at startup and low frequencies. Dimensioning of the MMC for drive applications, including the calculation of the current/voltage rating and the size of the SM capacitors and arm inductances based on the strategy in [101], has been investigated in [110].

Antonopoulos *et al.* [111] present an analysis to select the average SM capacitor voltage within the mid-frequency operating range (one-third of the base speed to the base speed) of MMC-based variable-speed drives. The objective of the analysis is to optimize the difference between the total arm energy and the inserted arm energy and to improve the efficiency and the quality of the output voltages.

C. Dynamic Braking Chopper

In many applications, a dc braking chopper is required to absorb and dissipate the energy. One example is the MMC-based HVDC transmission system of an offshore wind farm. In case of inability of the receiving end (onshore station) of the MMC–HVDC system to accept the power in-feed from the wind farm, e.g., a nonpermanent fault on the onshore grid, the grid code does not tolerate any influence on the operation of the offshore station. Therefore, as shown in Fig. 8, the onshore station needs to absorb and dissipate the rated power of the wind farm without interrupting the operation of the wind farm during onshore faults. Conventionally, this is handled by installing a braking resistor connected to the dc side of the offshore VSC–HVDC converter station in the arrangement shown in Fig. 8. The circuit of Fig. 8 acts like a dc–dc buck converter, which is realized by series connection of a large number of devices to meet the high voltage rating of the switches. The conventional braking chopper of Fig. 8 cannot be applied to the MMC–HVDC converters because of the inductive current flowing through the MMC phase-legs. Alternatively, a modular design with series connected SMs, as shown in Fig. 9, which enables installation of a modular chopper configuration on the onshore side with minimal requirement for cost and space has been proposed and investigated [112], [113].

D. Other Applications

Benefits and salient features of the MMC for HVDC systems make it a prominent choice for flexible ac transmission system (FACTS) applications as well [6], [114]–[119]. The investigation and installation of the MMC-based STATCOM have been reported in [6], in which, based upon the half-bridge SMs, the MMC–STATCOM performs active filtering as well. Guying *et al.* [119] present an MMC-based unified power-flow controller. A shunt active power filter based on the MMC has been presented and discussed in [120].

One of the other potential applications of the MMC is in railway electric traction systems, in which the MMC, as a medium-voltage transformerless converter, is used to supply the traction motors [76], [121]. The application of the MMC for the propulsion system of electric ships has also been reported in [109] and [122].

In [123] and [124], the MMC topology has been investigated for grid connection of energy storage systems. Trintis *et al.* in [123] introduce a modular converter with integrated energy storage based on the MMC to interface low/medium-voltage batteries to the grid. Hillers and Biela in [124] study the optimal

design of the MMC for transformerless grid connection of a standalone high-power energy storage system.

In [125], a power electronic transformer based on an MMC followed by an isolated dual-active-bridge dc–dc converter and an inverter is proposed. Mei *et al.* [126] and Iannuzzi *et al.* [127] discuss the possibility of using MMC as an interface between the grid and photovoltaic panels.

On the subject of dc–dc converters, a family of medium/high voltage dc–dc converters based on the MMC topology has been recently introduced and investigated in [128]–[131]. Norrga *et al.* in [131] propose a methodology to optimize the design of the dc–dc converter based on MMC with regard to silicon area.

VI. Conclusion

The salient features of the MMC, i.e., its modularity and scalability enable it to conceptually meet any voltage level requirements with superior harmonic performance reduced rating values of the converter components and improved efficiency. Over the past few years, the MMC has become a subject of interest for various medium to high voltage/power systems and industrial applications including HVDC transmission systems, FACTS, medium-voltage variable-speed drives, and medium/high voltage dc–dc converters.

For power system applications, e.g., HVDC systems and FACTS, the MMC has reached a certain level of maturity and seems to stand as the most promising technology as a number of MMC–HVDC systems and STATCOMs has been successfully implemented and installed.

For medium-voltage variable-speed drives, there is still a plenty of room for further development to address the operational and control issues of the MMC, specifically under constant-torque low-speed operation. One major problem that needs to be addressed is to minimize the magnitude of the capacitor voltage ripple of the converter SMs at low frequencies without sacrificing the converter efficiency, thereby making a reasonable tradeoff between the converter size/volume/cost and efficiency.

The introduction of a family of modular multilevel dc–dc converters, originated from the MMC topology, has opened up a new avenue on research and development of medium/high voltage dc–dc converters. To take the full advantage of these converters for various applications, advanced modulation strategies that enable high-voltage conversion ratio, high efficiency and reduced component stresses are required.

With a significant amount of MMC-derived converter topologies and applications, it is concluded that development of novel modulation and control strategies will be a major driving factor to shape the future of MMC applications.

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