浙江大學

本科生毕业论文（设计）

题目：**BPA** 电网模型导入 **DIgSILENT** 的研究和开发

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第 1 章　文献综述

1.1　概述

1.1.1　项目研究背景

作为一个具有时变性的大型复杂系统，电力系统在国名经济和生活中扮演着至关重要的角色。在进行电力系统的规划、设计、运行和维护时，为了保证其可靠、安全地运行，需要准确地考察电力系统的动态特性和静态特性，需要有一个强有力的工具来分析实际电力系统的运行情况。然而电力系统的特点决定了难以采用试验的方法来实现，必须采用仿真的手段，仿真可以分为物理仿真和数字仿真。随着计算机和数值计算技术的迅猛发展，电力系统数字仿真技术得到了飞速发展，并以其良好的经济性和便利性成为分析、研究电力系统的必要工具。目前电力系统数字仿真不仅为电力系统的规划、设计提供了基础，而且为电力系统调度、运行的安全性和可靠性等方面提供了依据。

电力系统仿真软件以数学模型代替实际电力系统，用数值方法对系统的运行特性进行试验和研究，它已经成为电力系统研究人员不可缺少的有力工具。在电力系统的规划、设计和运行中，电力系统仿真软件可以用来确定规划方案、拟定运行方式、整定自动装置的控制参数、进行事故分析和辅助运行人员做出正确的决策，大大提高电网的运行效率。

电力系统的发展也为电力系统数字仿真提出了更高的要求，采用单一的电力仿真软件对大电网进行仿真已经不足以满足实际研究的需要。这主要体现在以下几个方面：

- 第一，不同软件采用的系统元件数学模型或者数字仿真数值计算方法可能不同，在功能上也会有差异；
- 第二，不同的软件在计算规模上有差别；

- 第三，由于新型电力元件的不断出现，某些软件在元件模型库上可能存在不足，软件不允许用户自定义模型等等。

因此在对大规模电力系统进行仿真时需要综合比较以选择适当的仿真工具。

1.1.2 项目发展历史、现状和趋势

电力系统仿真软件的开发研究起源于上世纪五、六十年代，受到当时的计算机价格、内存容量和计算速度等多方面的严重限制。八十年代以来，随着计算机软件和硬件的高速发展，先进数学计算方法的引入，电力系统仿真软件取得了长足的进步，功能日益强大，计算效率大大提高，使用也更加方便灵活。目前，国际上有多种电力系统仿真软件，在世界上不同国家和地区的各级电力企业、研究所和高校中得到了较为广泛的应用，对各国电力系统的实践和研究发挥了很大的作用。我国电力系统仿真软件的开发和研究也起步较早，在上世纪七十年代有较大的发展。

目前，国内的电力科研单位一般都有一种或者几种电力系统仿真软件，其中最为普遍的是 BPA 和 PSASP 软件，国内电网数据文件也普遍采用这两种软件的数据格式。在利用其它软件进行计算时，如何运用已有的数据文件，准确快速的进行新数据的整理和输入，是研究人员经常遇到的问题。对于一个小系统，手工填写数据是可行的，但是对于大规模的系统，如果以人工方式填写数据，不仅需要耗费大量的人力和物力，并且出现错误的可能性也会增加。由于电力系统的数据文件都是基于系统的物理模型，有很多共同的属性，所以通过编写数据转换程序对这些仿真软件的数据格式进行自动转换是可行的，也是必要的。

随着电网规模的不断增大，仿真软件也在不断的提升。它们的运行规模在不断扩大，运行速度不断提升，功能不断增加，精度不断提高，元件模型与实际越来越贴近，各个仿真软件在不同方面的优缺点也愈见明显，所以需要建立一个统一的数据库。

早期的电力系统仿真软件实际上是一个程序包，针对不同的分析功能需要采用相应的计算程序并调用相应格式的数据，这使得用户操作起来极为繁琐，而且也增加了出错几率。新一代的分析软件打破了这种传统模式，在将各种计算功能集成在一个统一的软件平台的同时，引入了数据库的观念，将不同计算过程所要调用的数据

统一存放在一个分级的面向对象的数据库中。这样，用户就不再像往常一样，需要编辑、组织和维护众多不同类型的文件以及其中所包含的数据。软件通过一个有效的数据管理器，将用户和内建数据库连接起来。

1.2 项目的研究意义

电力系统在国民经济中有着非常重要的作用，随着电力系统技术的发展，针对大型电力系统的仿真计算不仅为电力系统的规划，而且为电力系统的计划、调度、运行的安全性与可靠性等方面，都提供了强大的技术支持，电力系统无法离开仿真这个工具已是不争的事实。电力系统规划的方案是靠仿真得到的; 新元件的接入、运行方式的确定是用仿真结果作为依据的; 新方法研究、新装置设计、参数确定是用仿真来确认的。电力系统仿真软件已经成为电力系统研究、计算、运行的有力工具。

由于电力系统仿真软件是指导电力系统运行、规划和决策的最基本工具，所以，一般网省局都规定: 对新引进的程序必须与现有程序进行认真的比较，证明其结果一致，方可在实际电网中推广应用。

与此同时，采用单一的电力仿真软件对大电网进行仿真已经不足以满足实际研究的需要。这主要体现在以下几个方面：第一，不同软件采用的系统元件数学模型或者数字仿真数值计算方法可能不同，在功能上也会有差异，比如电力系统常用的数据格式是基于 BPA 文本文件，其缺陷是不易于实现自定义等高级操作，随着大规模新能源接入后其更新速度赶不上科研需要，PSS/E 自定义功能强大，易于实现自定义等功能，但其缺陷是难以实现电磁暂态仿真，只能实现三相对称的机电暂态仿真，DIgSILENT 功能更为强大，但在大规模计算时的速度不能和 PSS/E 媲美；第二：不同的软件在计算规模上有差别，后文中也将会提及；第三：由于新型电力元件的不断出现，某些软件在元件模型库上可能存在不足，软件不允许用户自定义模型等等。因此，在对大规模电力系统进行仿真时需要综合比较以选择适当的仿真工具。

对于不同软件间的数据转换，针对简单的网络，手动的模型转换和仿真验证还是可以接受的。但是如果面临较大的网络，手动的转换是十分耗费人力和时间的。然而，现有的分析软件或多或少都存在数据兼容的问题: 即不同的软件开发商定义了不同的数据格式，而这些数据格式不被其它软件所识别。虽然有些软件自带了一些数

据格式的转换程序，但其功能只限于少数软件间的格式转换，对某些具体情况并不适用。例如，PSS/E 这种在国际上有着众多用户的软件并且针对国际上常用的数据格式也有数据转换接口程序，但是 DIgSILENT 针对 PSS/E 的数据的转换程序做的并不好，只能实现比较简单数据的转换。而对于 BPA 到 DIgSILENT 的数据转化软件更是如此，因此，需要开发第三方提供的数据接口程序。

1.3 该项目的国内进展情况

对于 BPA 和 DIgSILENT 之间的数据导入问题，刘庆等学者 [1] 进行了研究，他们首先分析了 BPA 和 DIgSILENT 的数学模型，得到了转换公式，用来完成两种仿真软件一次设备模型之间的参数转换，接着通过 DIgSILENT 的 DPL 语言和 DGS 接口，结合 VC6 和 DPL 实现方案，设计了软件的整体结构，用于将 BPA 模型参数自动导入到 DIgSILENT 中。文献 [2] 综合比较了当前主要使用的各种电力系统仿真软件的功能特点和应用情况，分析了各自的优势。文献 [4] 总结了我国常用的电力系统仿真软件，以及其现状和发展趋势，并编写了 DIgSlLENT 与仿真软件 PSS/E 以及 PSASP 之间的数据转换程序。文献 [3] 集中介绍了 DIgSlLENT 在电力系统应用方面的主要功能和特点。文献 [5], [6] 对 BPA 常用的潮流数据卡进行了分析，得到了 BPA 与 PSS/E 模型的区别和相应的转换关系，并使用 C++ 完成了数据转换程序。文献 [7] 介绍了 DIgSILENT 软件的详细功能。

国内已有很多学者使用 DIgSlLENT 建模仿真，分析电网数据，为决策提供依据，文献 [8]-[10] 均选择 DIgSlLENT 作为仿真平台，研究风电站并网的运行和控制。

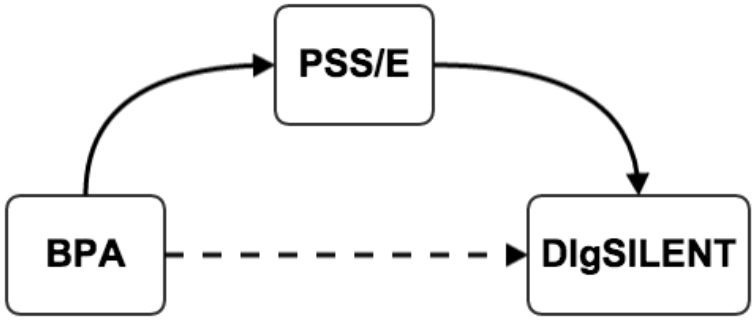

图 1.1 BPA、PSS/E、DIgSILENT 数据转换研究现状示意图

如图 1.1 所示，在之前的研究中，转换 BPA 数据至 PSS/E 数据的程序已经比较成熟，同时 PSS/E 至 DIgSILENT 的转换也得到了较好地实现，因此之前主要是通过 PSS/E 为中介来从 BPA 数据转换到 DIgSILENT，这样就带来很大的不便。在 BPA 数据不经过 PSS/E 直接转换到 DIgSILENT 方面，杨迪行学长通过 DIgSILENT 自带的 DPL 语言实现了其转换，但 DPL 语言实用性不强，在诸多方面不及 Python 应用灵活、功能强大，在新版本的 DIgSILENT 中新加入了 Python 的 API 接口，也为这种实现提供了可能性。

1.4 项目研究的主要内容

本项目基于 DIgSILENT 平台，致力于研究从 BPA 到 DIgSILENT 的数据转换问题：将 BPA 的数据导入 DIgSILENT 中，利用 Python 语言编程，实现从外部数据的读取，并且将读到的数据在 DIgSILENT 中建立相应的模型并予以赋值，从而在 DIgSILENT 得到与 BPA 中相同的数据模型，进而可以利用两个软件不同的优势进行数据的计算。论文的工作主要从以下几个方面展开:

- 对 Python 在 DIgSILENT 中的 API 接口进行介绍，分析其在 BPA 至 DIgSILENT 数据转换的应用和功能方面的优势。
- 对 DIgSILENT 和 BPA 数据的介绍。分别对 DIgSILENT 和 BPA 的数据特点进行具体的介绍，包括发电机模型，负荷模型等在两个不同软件的不同特点。
- 从 DIgSILENT 里找到 BPA 软件中数据对应的模型及其参数位置。
- 用 Python 语言进行编程，将外部数据所代表的模型意义完全的在 DIgSILENT 中重现出来，即在 DIgSILENT 中重新建立模型，并赋予响应的参数值。建立他们之间的关系。

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第 2 章　外文文献翻译

2.1　外文文献原稿

Operation, Control, and Applications of the Modular Multilevel Converter: A Review

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***Abstract*—The modular multilevel converter (MMC) has been a subject of increasing importance for medium/high-power energy conversion systems. Over the past few years, significant research has been done to address the technical challenges associated with the operation and control of the MMC. In this paper, a general overview of the basics of operation of the MMC along with its control challenges are discussed, and a review of state-of-the-art control strategies and trends is presented. Finally, the applications of the MMC and their challenges are highlighted.**

***Index Terms*—Capacitor voltage balancing, circulating current control, high-voltage direct current (HVDC) transmission, modular multilevel converter (MMC), modulation techniques, redundancy, variable-speed drive systems.**

I. Introduction

THE modular multilevel converter (MMC) has become the most attractive multilevel converter topology for medium/high-power applications, specifically for voltage-sourced converter high-voltage direct current (VSC–HVDC) transmission systems [1]–[14]. In comparison with other multilevel converter topologies, the salient features of the MMC include: 1) its modularity and scalability to meet any voltage level requirements, 2) its high efficiency, which is of significant importance for high-power applications, 3) its superior harmonic performance, specifically in high-voltage applications where a large number of identical submodules (SMs) with low-voltage ratings are stacked up, thereby the size of passive filters can be reduced, and 4) absence of dc-link capacitors.

Over the past few years, there has been a significant effort towards addressing the technical challenges associated with the operation and control of the MMC as well as broadening its applications. The main intention of this review paper is to provide a better understanding of the MMC and its associated technical issues for various applications. This paper provides a comprehensive review on the most recent advances and contributions on the operational issues, modeling, control, and modulation techniques of the MMC. This paper also highlights the emerging applications of the MMC and outlines their associated challenges.

The rest of this paper is organized as follows. Section II introduces the MMC circuit topology along with various SM circuit configurations that can be used in the design of the converter. This is followed by a review of latest contributions on MMC modulation techniques, design constraints, and various operational issues, such as capacitor voltage balancing and circulating current control presented in Section III. Section IV covers the latest developments in the operation and control of the MMC under special conditions, i.e., operation under unbalanced grid conditions and fault-tolerant operation. The promising applications of the MMC along with their technical challenges are reviewed in Section V. The concluding remarks are presented in Section VI.

II. MMC Topology

Fig. 1 shows a schematic diagram of a three-phase MMC. The MMC, as shown in Fig. 1, consists of two arms per phase-leg where each arm comprises N series-connected, nominally identical SMs, and a series inductor L_o. While the SMs in each arm are controlled to generate the required ac phase voltage, the arm inductor suppresses the high-frequency components in the arm current. The upper (lower) arm of three phase-legs are represented by subscript "*p*" ("*n*").

The SMs of the MMC of Fig. 1 can be realized by the following circuits:

1) The half-bridge circuit or chopper-cell [15], [16]: As shown in Fig. 2(a), the output voltage of a half-bridge SM is either equal to its capacitor voltage v_C (switched-on/inserted state) or zero (switched-off/bypassed state), depending on the switching states of the complimentary switch pairs, i.e., $S1$ and $S2$ [4].
2) The full-bridge circuit or bridge-cell [15], [16]: As shown in Fig. 2(b), the output voltage of a full-bridge SM is either equal to its capacitor voltage v_C (switched-on/inserted state) or zero (switched-off/bypassed state), depending on the switching states of the four switches $S1$ to $S4$. Since the number of semiconductor devices of a full-bridge SM is twice of a half-bridge SM, the power losses as well as the cost of an MMC based on the full-bridge SMs are significantly higher than that of an MMC based on the half-bridge SMs [4].
3) The clamp-double circuit: As shown in Fig. 2(c), a clamp-double SM consists of two half-bridge SMs, two additional diodes and one extra integrated gate bipolar

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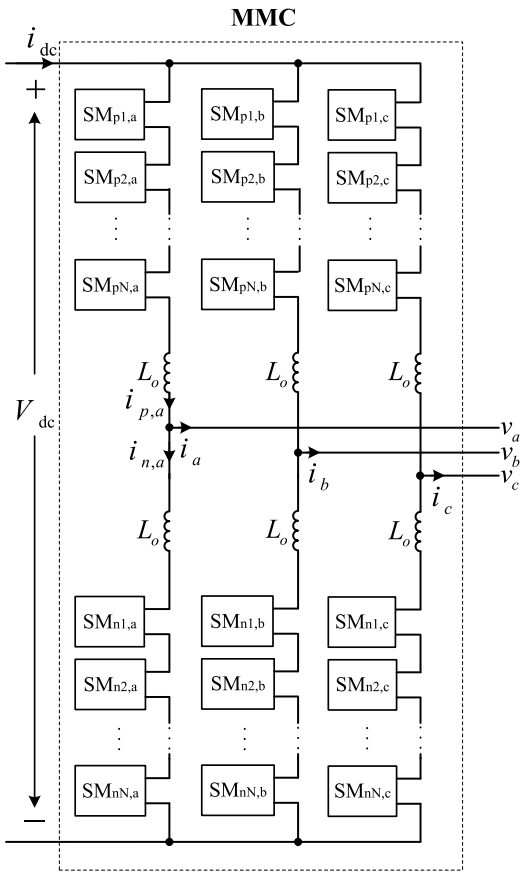

Fig. 1. Schematic representation of the MMC.

transistor (IGBT) with its anti-parallel diode. During normal operation, the switch $S5$ is always switched ON and the clamp-double SM acts equivalent to two series-connected half-bridge SMs. Compared to the half- and full-bridge MMCs with the same number of voltage levels, the clamp-double MMC has higher semiconductor losses than the half-bridge MMC and lower than the full-bridge MMC [4].

4) The three-level converter circuit: As shown in Fig. 2(d) and (e), a three-level SM is comprised of either a three-level neutral-point-clamped (NPC) or a three-level flying capacitor (FC) converter [17], [18]. The three-level FC MMC has the similar semiconductor losses with the half-bridge MMC. However, the three-level NPC MMC has higher semiconductor losses than the half-bridge MMC and lower than the full-bridge MMC. From a manufacturing perspective and control, this SM circuit is not very attractive.
5) The five-level cross-connected circuit: As shown in Fig. 2(f), a five-level cross-connected SM also consists of two half-bridge SMs connected back-to-back by two extra IGBTs with their anti-parallel diodes. Its semiconductor losses are the same as the clamp-double SM [19].

A comparison of various SM circuits, in terms of voltage levels, dc-side short-circuit fault handling capability, and power losses, is provided in Table I. The dc-side short circuit fault is one of the major challenges associated with the MMC–HVDC

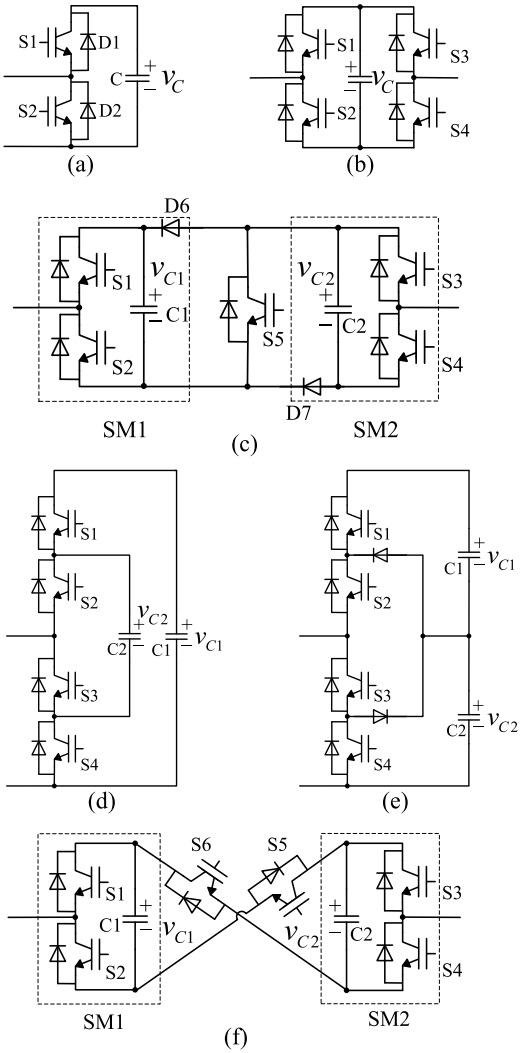

Fig. 2. Various SM topologies: (a) the half-bridge, (b) the full-bridge, (c) the clamp-double, (d) the three-level FC, (e) the three-level NPC, and (f) the five-level cross-connected SM.

system and will be discussed in Section V-A. Among all of the SM circuit configurations, the half-bridge SM has been the most popular SM adopted for the MMC [1]–[12]. This is due to the presence of only two switches in the SM which results in a lower number of components and higher efficiency for the MMC. Hereafter, the half-bridge SM-based MMC is considered. It should be noted that there are a few converter configurations derived from the MMC topology [15], [16]. This paper is only focused on the so called double-star MMC configuration in [15], [16], which is shown in Fig. 1.

III. Modulation, Design, Control, and Modeling of the MMC

A. Modulation Techniques

Various pulse-width modulation (PWM) techniques, based on using a single reference waveform, that have been developed/proposed for the MMC include:

1) Carrier-disposition PWM techniques (CD-PWM) [20], [21]: These techniques require N identical triangular

TABLE I
COMPARISON OF VARIOUS SM CIRCUITS

SM circuit	Voltage levels	DC-fault handling	Losses
Half-bridge	0, v_C	No	Low
Full-bridge	0, $+v_C$	Yes	High
Clamp-double	0, v_{C1}, v_{C2}, $(v_{C1}+v_{C2})$	Yes	Moderate
Three-level FC	0, v_{C1}, v_{C2}, $(v_{C1}-v_{C2})$	No	Low
Three-level NPC	0, v_{C2}, $(v_{C1}+v_{C2})$	No	Moderate
Five-level cross-connected	0, v_{C1}, v_{C2}, $+(v_{C1}+v_{C2})$	Yes	Moderate

carrier waveforms displaced symmetrically with respect to the zero axis. The comparison of the phase voltage reference waveform with the carriers produces the desired switched output phase voltage level. Voltage transitions corresponding to a triangular carrier are associated with the insertion/bypass of a particular SM. Based on the phase shift among the carrier waveforms, these techniques are further classified into: a) phase disposition (PD), b) phase opposition disposition (POD), and c) alternate phase opposition disposition (APOD), shown in Fig. 3(a)–(c), respectively. The disadvantages of using these techniques include unequal distribution of voltage ripple across the SM capacitors that impact the harmonic distortion of the ac-side voltages and large magnitude of circulating currents. To improve the harmonic distortion of the ac-side voltages, a simple carrier rotation technique [22], a modified carrier rotation technique [23], or a signal rotation technique [20] is used to equalize the voltage distribution across all the SM capacitors. In spite of the proposed SM capacitor voltage balancing techniques, the output voltages have a relatively high total harmonic distortion (THD) [20]. To improve the performance of these techniques, a modified PD PWM technique with an SM capacitor voltage balancing technique is proposed in [8]. In this technique, which is based on the PD carrier waveforms, voltage transitions corresponding to a triangular carrier are no longer assigned to a particular SM. In this technique, comparison of the reference waveform with the carrier waveforms produces an $(N+1)$-level waveform that determines the number of SMs to be inserted in the upper and lower arms, respectively. Depending upon the direction of the arm current and the status of the SM capacitor voltages, the determined number of SMs out of the N SMs in the upper (lower) arm are inserted so as to minimize the difference between the SM capacitor voltages. Mei *et al.* in [24] propose a PD PWM technique with selective loop bias mapping method for balancing the SM capacitors. This method implements carrier rotation using the following feedback: a) the maximum/minimum SM capacitor voltages and b) the direction of arm current. The advantages of this technique include: a) absence of additional reference signals to control the SM capacitor voltages and b) ease of implementation in a simple field-implemented gate array (FPGA) even with a large number of SMs.

2) Subharmonic techniques [20]: In these techniques, there are $2N$ identical carrier per phase-leg, either sawtooth

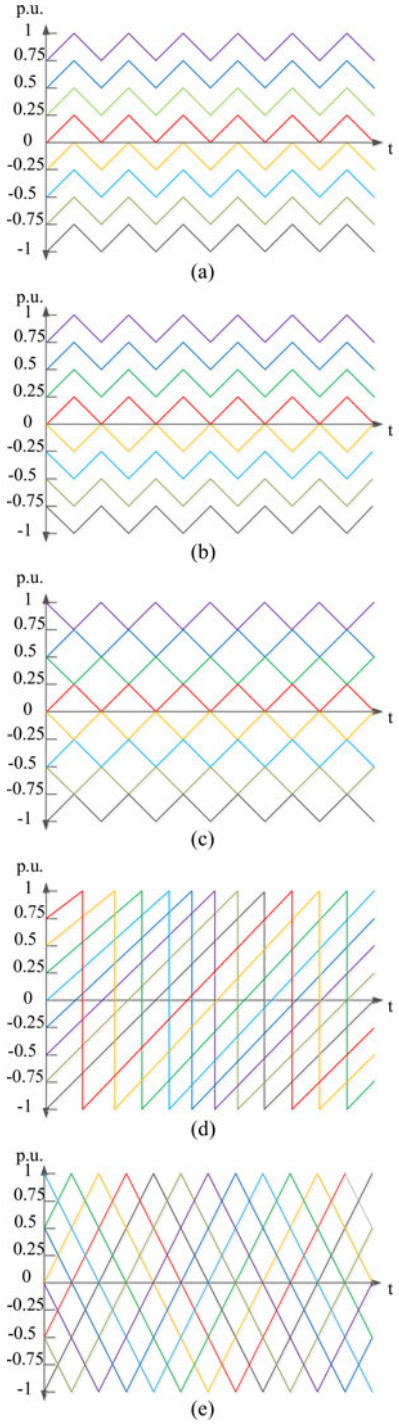

Fig. 3. Multilevel carriers: (a) PD, (b) POD, (c) APOD, (d) saw-tooth, and (e) phase-shifted carriers [20].

waveforms or triangular waveforms, with a phase shift of $\theta = 360^\circ/2N$ with respect to each other, as shown in Fig. 3(d) and (e). Assuming the same number of switching transitions for both the PD PWM and subharmonic techniques, the PD PWM technique produces better line-to-line voltage THD [25], [26].

Additionally, there are several modulation techniques based on using multiple reference waveforms. These modulation techniques include [27]:

1) Direct modulation: In this modulation technique, the upper and lower arm voltages of phase-j are controlled by two complementary sinusoidal reference waveforms, as given by

$$n_{p,j,\mathrm{ref}} = N\frac{\frac{V_{\mathrm{dc}}}{2} - v_{j,\mathrm{ref}}}{V_{\mathrm{dc}}} \tag{1a}$$

$$n_{n,j,\mathrm{ref}} = N\frac{\frac{V_{\mathrm{dc}}}{2} + v_{j,\mathrm{ref}}}{V_{\mathrm{dc}}} \tag{1b}$$

where $v_{j,\mathrm{ref}}$ represents the reference output voltage and $n_{p,j,\mathrm{ref}}$ and $n_{n,j,\mathrm{ref}}$ are the reference waveforms for the number of inserted SMs in the upper and lower arms, respectively. The reference waveforms in (1) are compared with the PD carrier waveforms, which vary between 0 and N, to determine the required number of inserted SMs in the upper and lower arms. The major drawback of the direct modulation technique is the presence of circulating currents, which increase the converter power losses and rating values of the components.

2) Indirect modulation: In this technique, the upper- and lower-arm reference waveforms of phase-j are given by

$$n_{p,j,\mathrm{ref}} = N\frac{\frac{V_{\mathrm{dc}}}{2} - v_{j,\mathrm{ref}} - v^{\Sigma}_{\mathrm{reg},j} - v^{\mathrm{circ}}_{\mathrm{reg},j}}{\sum_{i=0}^{N} v_{cp,i,j}} \tag{2a}$$

$$n_{n,j,\mathrm{ref}} = N\frac{\frac{V_{\mathrm{dc}}}{2} + v_{j,\mathrm{ref}} - v^{\Sigma}_{\mathrm{reg},j} - v^{\mathrm{circ}}_{\mathrm{reg},j}}{\sum_{i=0}^{N} v_{cn,i,j}} \tag{2b}$$

where $v_{cx,i,j}$ represents the capacitor voltage of SM-i in arm-x of phase-j, and $v^{\Sigma}_{\mathrm{reg},j}$ and $v^{\mathrm{circ}}_{\mathrm{reg},j}$ are used to control the total energy in the phase-j leg and balance the energy between the arms, respectively. Similar to the direct modulation technique, the reference waveforms are compared with the PD carrier waveforms to determine the number of inserted SMs in the upper and lower arms. This technique can be further classified into:

   a) Closed-loop control [28]: In the closed-loop control, the term $\sum_{i=0}^{N} v_{cx,i,j}$ in (2) is calculated based on the actual measured capacitor voltages. Furthermore, $v^{\Sigma}_{\mathrm{reg},j}$ and $v^{\mathrm{circ}}_{\mathrm{reg},j}$ are obtained from the closed-loop control of the total energy stored in phase-j leg capacitors and the energy balance between the arms, respectively. The balance between the energy stored in each arm relies on temporarily driving a fundamental frequency sinusoidal circulating current. The advantages of this technique lie in i) the control of the average SM capacitor voltage, which allows operation under low output voltage with high number of voltage levels, and ii) the control of the energy imbalance between the upper and lower arms.
   b) Open-loop control [29]: In the open-loop control, the term $\sum_{i=0}^{N} v_{cx,i,j}$ in (2) is calculated based on the estimated capacitor voltages. Additionally, $v^{\Sigma}_{\mathrm{reg},j} = 0$ and $v^{\mathrm{circ}}_{\mathrm{reg},j}$ is estimated so as to eliminate the harmonics in the circulating currents and guarantee stable operation of the converter. The estimations are obtained by solving the equations describing the dynamics of the converter, using the measured output currents and dc-link voltage. The advantages of this technique lie in the absence of voltage sensors, and simple and fast control. Nevertheless, accurate estimation of the real parameters necessary to describe the dynamics of the system is its main drawback.

3) Phase-shifted carrier-based PWM technique (PSC PWM) [30]: In this technique, each SM of the MMC is controlled independently, and the voltage balancing task of the SMs is divided into an averaging control and a balancing control. The reference waveforms of each SM in the upper and lower arms are given by

$$m_{p,i,j} = \frac{\frac{V_{\mathrm{dc}}}{2N} - \frac{v_{j,ref}}{N} + v_{a,j} + v_{b,i,j}}{v_{cp,i,j}}, \tag{3a}$$

$$m_{n,i,j} = \frac{\frac{V_{\mathrm{dc}}}{2N} + \frac{v_{j,ref}}{N} + v_{a,j} + v_{b,i,j}}{v_{cn,i,j}} \tag{3b}$$

where $v_{a,j}$ and $v_{b,i,j}$ are the averaging and balancing controller outputs, respectively. The averaging and balancing techniques control the average SM capacitor voltage in each phase-leg and the individual SM capacitor voltage, respectively. Comparison of each SM voltage reference waveform with its triangular carrier generates the switching signals for the corresponding SM. The triangular carrier waveforms of each phase-leg are implemented based on the subharmonic techniques. The main drawbacks of this technique are its implementation effort that significantly increases as the number of SMs increases and instability under certain operating conditions [31]. The latter drawback is improved in [31] and [15] by introducing another term, the arm balance control, in the reference waveforms based on the difference in the capacitor voltages of the upper and lower arms.

A brief comparison of the aforementioned modulation strategies is provided in Table II. The control strategies of the MMC are summarized in the block diagram of Fig. 4. In addition to the aforementioned PWM techniques, a SHE–PWM technique is proposed in [32], in which the switching patterns are determined to eliminate the low-order harmonics of the output voltage waveform. The switching patterns are calculated and stored in lookup tables for various modulation indices and the output-voltage phase angle.

Modulation techniques based on fundamental frequency switching have been proposed and investigated in [33]–[36]. A nearest level control (NLC) modulation technique is proposed in [33], in which the voltage level nearest to the desired voltage waveform is selected. Compared to the SHE–PWM, the NLC

TABLE II
COMPARISON OF MODULATION STRATEGIES

Property	Modified PD-PWM [8]	Direct modulation [27]	Indirect modulation [28], [29]	PSC-PWM [30]
No. of reference waveforms	1	2	2	2N
Additional controllers required for stability	No	No	Yes	Yes
Presence of circulating current	Yes	Yes	No	No
Implementation effort	Moderate	Moderate	Low (open-loop)-moderate (closed-loop)	High as $N \uparrow$

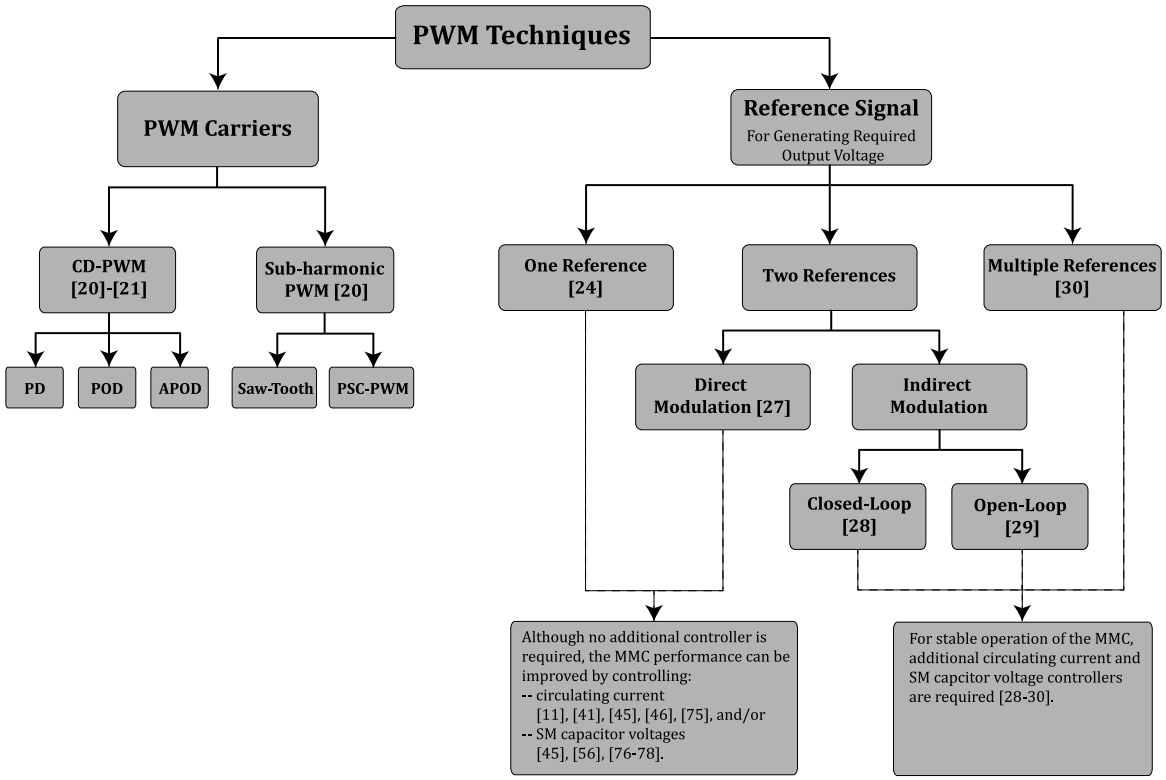

Fig. 4. Overview of various PWM techniques for the MMC.

technique is easy to implement, requires less computational efforts, and uses a lower switching frequency when compared to the PWM techniques. The technique proposed in [35] is based on a fixed pulse pattern fed into the SMs to maintain the stability of the stored energy in each SM, without measuring the capacitor voltages or any other feedback control, and to remove certain output voltage harmonics at any arbitrary modulation index and output-voltage phase angle. The technique proposed in [36] optimizes the pulse patterns to minimize the harmonic distortion of the output voltage. The main advantages of fundamental frequency switching techniques are the reduced switching frequency and low THD of the output voltage without any limitation on the output-voltage frequency. This is opposed to the PWM techniques where the carrier frequency imposes a limit on the output-voltage frequency.

B. SM Capacitor Voltage Balancing

Similar to any other multilevel converter topology, the MMC needs an active voltage balancing strategy to balance and maintain the SM capacitor voltages at $V_{\rm dc}/N$. Deng and Zhen in [37] propose a voltage balancing strategy, which uses the phase-shifted carrier PWM (PSC–PWM) scheme to control the high-frequency components of the MMC arm currents. The capacitor voltage balancing is achieved by assigning appropriate PWM pulses to the SMs of each arm. This voltage balancing strategy does not require the measurement of arm currents, which adds to the control simplicity and reduces the number of sensors. Hagiwara and Akagi in [30] present a voltage balancing strategy, which uses a closed-loop controller for each SM. In [11], a predictive strategy for the control of an MMC is developed, in which the SM capacitor voltages are balanced based on a predefined cost function. The most widely accepted voltage balancing strategy is based on a sorting method [8], [38]–[40]. To carry out the capacitor voltage balancing task based on the sorting method, the SM capacitor voltages of each arm are measured and sorted. If the upper (lower) arm current is positive, out of N SMs in the corresponding arm, $n_{p,j}$ ($n_{n,j}$) SMs with the lowest voltages are identified and inserted. Consequently, the corresponding inserted SM capacitors are charged, and their voltages increase. If the upper (lower) arm current is negative, out of N

SMs in the corresponding arm, $n_{p,j}$ ($n_{n,j}$) of the SMs with the highest voltages are identified and inserted. Consequently, the corresponding inserted SM capacitors are discharged, and their voltages decrease [8]. Regardless of the direction of the upper (lower) arm current, if an SM in the arm is bypassed, the corresponding capacitor voltage remains unchanged. Although the sorting method guarantees capacitor voltage balancing under all of the MMC operating conditions, it produces unnecessary switching transitions among the SMs. Even if the number of required on-state SMs within two consecutive control periods are not changed, the SM insertion/bypassing may happen. This results in increased switching frequency and subsequently power losses, which are undesirable, specifically for high-power systems. The proposed/investigated methods to reduce the switching frequency of an MMC are mainly based on:

1) A closed-loop modified sorting method in conjunction with a phase-shifted carrier PWM strategy, in which the insertion/bypassing of the SMs is carried out based on capacitor voltage measurements [39], [41]. In this method, only a limited number of SMs are sorted within each control cycle. That is, within each control cycle and based on the required voltage level, if additional SMs need to be switched on (off) within each arm, only the off-state (on-state) SMs will be considered for sorting and switching.
2) An open-loop method in conjunction with the selective harmonic elimination (SHE) PWM strategy [35].
3) A hybrid balancing strategy, which combines a predictive error sorting method and the conventional voltage sorting algorithm [42]. This strategy is based on sorting the absolute errors between the one-step forward predicted capacitor voltages and their nominal values. That is, within each control period, the SMs with the minimum predictive voltage errors are chosen to be inserted.
4) A fundamental-frequency balancing strategy, which is based on the conventional sorting method executed at the pre-specified phase angles [42].
5) An optimized capacitor voltage balancing strategy, in which the measured SM capacitor voltages are adjusted before sorting. This strategy focuses on the SMs whose capacitor voltages exceed certain voltage limits, while the switching states of the other SMs remain the same. A maintaining factor is introduced and multiplied by the capacitor voltages of the off-state SMs whose capacitor voltages exceed the voltage limits to increase their possibility of being inserted/bypassed in the following switching cycle [43].
6) A predictive algorithm to calculate and distribute the amount of charge stored in the SM capacitors [44].

C. Mathematical Model

The circuit diagram of a three-phase MMC based on half-bridge SMs is depicted in Fig. 5. Compared to Fig. 1, an additional arm resistor R_o, which models the power losses within each arm of the MMC, is included.

The mathematical model of the MMC, presented in this section, is based on the most widely accepted model in the literature [8], [11], [45]–[47].

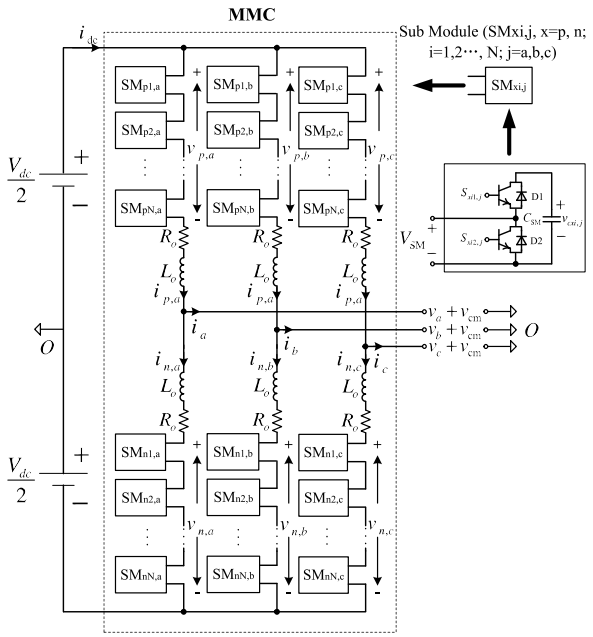

Fig. 5. Circuit diagram of an MMC.

In the MMC of Fig. 5, the upper and lower arm currents of phase-j, $j = a, b, c$, i.e., $i_{p,j}$ and $i_{n,j}$ are expressed by

$$i_{p,j} = \frac{i_{\rm dc}}{3} + i_{{\rm circ},j} + \frac{i_j}{2} \tag{4a}$$

$$i_{n,j} = \frac{i_{\rm dc}}{3} + i_{{\rm circ},j} - \frac{i_j}{2} \tag{4b}$$

where $i_{{\rm circ},j}$ represents the circulating current within phase-j, i_j is the ac-side phase-j current, and $i_{\rm dc}$ is the current in the dc link. The circulating current, based on (4), is given by

$$i_{{\rm circ},j} = \frac{i_{p,j} + i_{n,j}}{2} - \frac{i_{\rm dc}}{3}. \tag{5}$$

The mathematical equations that govern the dynamic behavior of the MMC phase-j are

$$\frac{V_{\rm dc}}{2} - v_{p,j} = L_o \frac{di_{p,j}}{dt} + R_o i_{p,j} + v_j + v_{\rm cm} \tag{6a}$$

$$\frac{V_{\rm dc}}{2} - v_{n,j} = L_o \frac{di_{n,j}}{dt} + R_o i_{n,j} - v_j - v_{\rm cm} \tag{6b}$$

where $v_{p,j}$ and $v_{n,j}$ represent the upper and lower arm voltages of the MMC phase-j, respectively, and v_j and $v_{\rm cm}$ represent the fundamental and common-mode voltage components, respectively. Subtracting (6b) from (6a) and substituting for $i_{p,j}$ and $i_{n,j}$ from (4), the MMC phase voltage is expressed by

$$v_j + v_{\rm cm} = \frac{v_{n,j} - v_{p,j}}{2} - \frac{R_o}{2} i_j - \frac{L_o}{2} \frac{di_j}{dt}. \tag{7}$$

Furthermore, adding (6a) with (6b) and substituting for $i_{{\rm circ},j}$ from (5), the internal dynamics of the MMC circulating current is expressed by

$$L_o \frac{di_{{\rm circ},j}}{dt} + R_o i_{{\rm circ},j} = \frac{V_{\rm dc}}{2} - \frac{v_{n,j} + v_{p,j}}{2} - R_o \frac{i_{\rm dc}}{3}. \tag{8}$$

The upper- and lower-arm voltages of the MMC phase-j are also described by

$$v_{p,j} = n_{p,j} v_{cp,j} \tag{9a}$$

$$v_{n,j} = n_{n,j} v_{cn,j} \tag{9b}$$

where $v_{cp,j}$ and $v_{cn,j}$ are the individual SM capacitor voltages of the upper and lower arms, respectively. Equation (9) is based on the assumption that an active capacitor voltage strategy balances and maintains the capacitor voltages of all SMs within each arm of the MMC equally, i.e., $v_{cxi,j,k} = v_{cx,j,k}$ for $\forall i \in \{1, 2, \ldots, N\}$. Substituting for $v_{p,j}$ and $v_{n,j}$ from (9) in (7) and (8), the following expressions are obtained

$$v_j + v_{\rm cm} = \frac{n_{n,j} v_{cn,j} - n_{p,j} v_{cp,j}}{2} - \frac{R_o}{2} i_j - \frac{L_o}{2} \frac{di_j}{dt} \tag{10a}$$

$$L_o \frac{di_{\rm circ,j}}{dt} + R_o i_{\rm circ,j} = \frac{V_{\rm dc}}{2} - \frac{n_{n,j} v_{cn,j} + n_{p,j} v_{cp,j}}{2} - R_o \frac{i_{\rm dc}}{3}. \tag{10b}$$

Additionally,

$$P_{\rm dc} = P_{\rm ac} + P_{\rm loss} \implies V_{\rm dc} i_{\rm dc} = \sum_{j=a,b,c} v_j i_j + P_{\rm loss} \tag{11}$$

where $P_{\rm loss}$ represents the power losses of the converter.

Each SM capacitor voltage of the MMC is modeled by the power processed by each arm. The power processed by each arm is given by

$$p_{p,j} = v_{p,j} i_{p,j} = n_{p,j} v_{cp,j} i_{p,j} \tag{12a}$$

$$p_{n,j} = v_{n,j} i_{n,j} = n_{n,j} v_{cn,j} i_{n,j}. \tag{12b}$$

The power processed by each phase arm of the MMC can also be expressed by

$$p_{p,j} = \frac{dW_{p,j}}{dt} = \frac{d\left(\frac{\rm N}{2} C_{\rm SM} v_{cp,j}^2\right)}{dt} = v_{cp,j} N C_{\rm SM} \frac{dv_{cp,j}}{dt} \tag{13a}$$

$$p_{n,j} = \frac{dW_{n,j}}{dt} = \frac{d\left(\frac{\rm N}{2} C_{\rm SM} v_{cn,j}^2\right)}{dt} = v_{cn,j} N C_{\rm SM} \frac{dv_{cn,j}}{dt} \tag{13b}$$

where $C_{\rm SM}$ represents the SM capacitor value. Based on (12) and (13), the dynamics of each SM capacitor voltage ripple is expressed by

$$\frac{dv_{cp,j}}{dt} = \frac{i_{p,j}}{N C_{\rm SM}} n_{p,j} = \frac{1}{N C_{\rm SM}} \left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} + \frac{i_j}{2}\right) n_{p,j} \tag{14a}$$

$$\frac{dv_{cn,j}}{dt} = \frac{i_{n,j}}{N C_{\rm SM}} n_{n,j} = \frac{1}{N C_{\rm SM}} \left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} - \frac{i_j}{2}\right) n_{n,j}. \tag{14b}$$

Equations (4), (10), (11), and (14) provide a generalized dynamic model of the MMC, which can be used for control purposes. Similar to this generalized dynamic model of the MMC, references [27] and [28] present a dynamic model of the MMC consisting of the summation of the capacitor voltages in each arm as a state variable, instead of the individual SM capacitor voltages used in the generalized dynamic model.

Reference [46] substitutes for $n_{p,j}$ and $n_{n,j}$ in the generalized dynamic model of the MMC for the direct and indirect modulation strategies to determine the MMC dynamic model for the respective modulation strategies. Substituting for $n_{p,j}$ and $n_{n,j}$ results in a continuous dynamic model, as only the low-frequency components of $n_{p,j}$ and $n_{n,j}$ are considered. Other types of continuous dynamic models as well as the frequency-domain models have been developed in [48] and [49], respectively. The main advantage of these models over the detailed generalized dynamic model lies in faster computation of the system states, specifically for an MMC with a large number of SMs. However, these models do not consider the higher order frequency components. A further simplification of the continuous dynamic models with reduced computational complexity is presented in [50], in which the terminal behavioral model of the MMC in the form of a simplified boost-buck converter model is derived.

D. MMC Design Constraints

The design of MMC, which includes sizing the capacitor and inductor as well as the number of SMs, is based on a few performance indices including arm current ripple, short circuit current, capacitor voltage ripple, reliability, and power losses.

1) Capacitor and Inductor Sizing: The arm inductor L_o functions as a filter to attenuate the high-frequency harmonics in the arm current as well as a dc-side short-circuit current limiter. Therefore, sizing of the arm inductor depends upon the filtering needs and the short-circuit current limit [5], [51], [52]. Additionally, sizing of the arm inductor needs to consider the suppression of undesired low-frequency harmonics in the arm current [53]. To reduce the size of the MMC, reference [54] proposes an integrated arm inductor based MMC, in which the arm inductors in each phase-leg use the same core. The description and design of the integrated arm inductor, based on the need to suppress circulating current, mitigate switching ripple, and limit fault current, is provided in detail in [54].

The SM capacitor is sized based on the tradeoff between its size/cost and voltage ripple [51]. The SM capacitor voltage ripple, under a wide range of operating conditions, has been analyzed in [55]–[59]. Given a permissible peak-to-peak ripple magnitude for the SM capacitor voltage $\delta v_{c,pp}$, the cell capacitance based on [55] is determined by

$$C_{\rm SM} = \frac{P}{3 N m V_c \delta v_{c,pp} \omega \cos\phi} \left(1 - \left(\frac{m \cos\phi}{2}\right)^2\right)^{\frac{3}{2}} \tag{15}$$

where $C_{\rm SM}$ is the SM capacitance, P is the real power transferred, V_c is the nominal voltage of the SM capacitor, m is the modulation index, and $\cos\phi$ is the power factor. Upon

substitution of the low-frequency components of $n_{p,j}$ in (14), as described in [46], (15) is obtained. A more detailed description of the peak-to-peak capacitor voltage ripple along with the SM capacitor design technique is provided in [60].

Based on the relationship between the stored energy and the power transfer capability, an SM capacitor sizing method is also developed in [61].

2) Power Loss Calculation: Compared to the two-level VSC system, in which the semiconductor losses are greater than 1% [13], the semiconductor losses in the MMC can be potentially reduced to less than 1% [13], [62].

The semiconductor losses include the conduction losses and the switching losses. The conduction losses can be determined based on the current flowing through the SMs and the semiconductor device data-sheets from the manufacturer. The switching losses depend on the insertion and bypassing transitions of the SMs, which are due to a) the switching transitions to generate the desired voltage levels based on the reference waveforms and b) selected modulation and capacitor voltage balancing strategies, as discussed in the previous sections.

There are mainly two methods to evaluate the semiconductor losses of the MMC. The first one is based on the simulation model and real-time simulation data [40], [63]–[67]. Though this method has a heavy computational load, it can provide accurate results regardless of the modulation/control strategy, voltage level, and SM circuit topology. The other method, described in [62] and [63], is based on analytical analysis and can potentially reduce the calculation time. However, it is a challenge to guarantee the accuracy since this method is based on the ideal assumptions and specified modulation/control strategies.

The need to calculate the power losses for the design process arises from the tradeoff among power/voltage quality, filtering size, and the efficiency in MMC, based on which the numbers of SMs required in each arm and the switching frequency are decided.

3) Reliability: The MMC, due to its structural modularity, can improve fault tolerance by augmenting redundant SMs in its structure [12], [68], thereby, increasing its reliability. However, beyond a certain maximum redundancy limit, the control hardware limits the converter reliability. That is, any increase in the number of redundant SMs greater than the maximum limit results in deterioration of the converter reliability [69].

E. Circulating Current Control

Circulating currents flowing through the three-phase legs of the MMC originate from the voltage differences among the three phase legs [53], [70] and contain negative sequence components with the frequencies twice the fundamental one [70]. Circulating currents do not have any impact on the ac-side voltages and currents. However, if not properly controlled/suppressed, they increase the peak and rms values of the phase-leg currents, which consequently increase the converter power losses as well as the ripple magnitude of the SM capacitor voltages. Although proper sizing of the arm inductors can suppress the circulating currents to some extent [53], a circulating current controller technique is necessary to effectively control/suppress them [53]. Circulating currents have been modeled and analyzed in [70]–[72]. Reference [71] proposes a circulating current model based on controlling the circulating currents as current controlled voltage sources. This can then be used to control the voltage to reduce the impact of ac components in the circulating currents. Perez and Rodriguez in [72] model the circulating currents along with the dc and ac currents as first-order models, which can be used to easily simulate the system and model the control systems. The ac components of the arm currents, including the circulating currents, are estimated in [70]. This helps in the design of the arm inductor and the SM capacitors to reduce the ac components in the circulating currents.

To control the circulating currents, various techniques have been proposed in the technical literature [11], [28]–[30], [41], [45], [46], [57], [73], [74]. The indirect modulation techniques in [28]–[30], which inherently limit the circulating currents, have already been explained in the previous section. Harnefors *et al.* [46] use an active resistance (proportional controller) to control circulating current, which includes an estimate of the resistance of the arm. The technique suffers from inaccurate estimation of the arm resistance as well as steady-state errors due to the usage of only a proportional controller [75]. Based on the double line-frequency $acb - dq$ transformation, Tu *et al.* [41] eliminate the circulating currents by controlling their dq components with a pair of PI controllers. The main problem associated with this technique is its robustness under ac-side imbalances/faults. Debnath and Saeedifard [45], She *et al.* [73], and Li *et al.* [74] target the elimination of the ac components of the circulating currents through a proportional resonant (PR) controller. Debnath and Saeedifard [45] also includes the control of the dc component of the circulating current so as to improve the stability of the system under unbalanced conditions. The reference for the dc component of the circulating currents is generated from the average SM capacitor voltage controller. The advantage of this technique lies in improved performance under any grid-side imbalance or fault. Yang *et al.* [57] propose a modified switching function to remove the circulating currents in the MMC used in a STATic COMpensator (STATCOM) application. The modified switching function is based on the predicted capacitor voltage ripple, which may become difficult to predict accurately under all operating conditions. A model-based predictive control (MPC) to eliminate the circulating current components is proposed in [11]. In the MPC-based techniques, the control of the circulating currents is necessary to avoid the voltage imbalance between the upper- and lower-arm capacitors. The main drawback of the proposed technique is the calculation effort, specifically for the MMC with a large number of SMs.

F. SM Capacitor Voltage Ripple Reduction Techniques

The SM capacitor voltage ripple has been studied extensively in [55], [57]–[59] is mainly dominated by the fundamental and second-harmonic components. This impacts the sizing of the SM capacitor to maintain the SM capacitor voltage ripple within reasonable limits. In [56], [76]–[78], it is shown that the ripple magnitude of the SM capacitor voltage can be reduced by injecting

appropriate harmonic components in the circulating currents. Based on the power processed by each arm, in [76], an appropriate second-harmonic circulating current is determined to reduce the ripple magnitude of the SM capacitor voltage. Using second- and fourth-harmonic components in the circulating currents, the method in [56] optimizes the energy variation within each arm. Picas *et al.* [78] carry out a similar optimization to [56], except that instead of minimizing energy variation within each arm, it minimizes the peak-to-peak capacitor voltage ripple. Picas *et al.* [77] optimize the rms value of the SM capacitor voltage ripple using the second harmonic component of the circulating current. One of the main drawbacks of the aforementioned capacitor voltage ripple reduction techniques is that they are based on open-loop control. Debnath and Saeedifard [45] propose a closed-loop control technique to mitigate the second-harmonic component of the capacitor voltage ripple and mathematically prove that the proposed technique indirectly leads to reduced ripple magnitude of the capacitor voltage. All of the proposed capacitor voltage ripple reduction techniques lead to increased peak and rms values of the arm currents, which consequently, increase the power losses and current rating of the components. Engel and Doncker [56] investigate an optimization problem to reduce the capacitor voltage ripple by keeping the rms value of the arm current within certain limits, thereby, limiting the power losses in the converter.

In addition to SM capacitor voltage ripple reduction strategies, references [49] and [79] shape the capacitor voltage ripple to maximize the operating region (defined by the power limits). While [79] uses only a second-harmonic circulating current, [49] uses a second-harmonic circulating current and a third-harmonic common-mode phase voltage.

G. Precharging the SM Capacitors and Startup Procedure

At the startup of the MMC, all SM capacitors are required to be charged to a certain equal voltage level before it reaches its normal operation. To reduce the surge currents and the startup time, a fast and smooth startup procedure is preferred. Precharging the SM capacitors and startup procedure of the MMC from the de-energized conditions have been explored in [55], [80]–[86]. The first precharging scheme introduced in [55], [83], and [84] is based on using a dc circuit breaker (CB) and an auxiliary dc source with a voltage equal to the nominal voltage of each SM capacitor. Due to the requirement for a dc CB, this charging scheme is costly [81]. Das *et al.* [80] propose a startup technique, in which an additional resistor is connected in series with the SMs of each arm. The resistor, which is inserted/bypassed by its parallel connected switch, is sized to limit the peak arm current. The main disadvantage of this technique lies in the additional resistive losses while charging the MMC capacitors. Shi *et al.* [81] explain a startup technique where the dc link of the MMC is connected to a diode-bridge rectifier. The startup procedure is performed in two stages: 1) charging the dc-link capacitor and SM capacitors through the diode-bridge rectifier to $V_{\rm dc}$ and $\frac{V_{\rm dc}}{2\rm N}$, respectively, assuming that all the SM capacitors are inserted into the dc-link and the inrush currents are limited by ac-side series resistors, and 2) bypassing the ac-side resistors and then gradually decreasing the number of inserted SMs in each phase-leg from $2N$ to N so as to let the capacitors charge from $\frac{V_{\rm dc}}{2\rm N}$ to $\frac{V_{\rm dc}}{N}$ as well as limit the arm currents. Xu *et al.* [82] propose a precharging circuit comprised of four thyristors per SM of the MMC. Although, by this method, the SMs can be precharged synchronously, and the startup procedure is accelerated, it adds additional complexity and cost to the system.

IV. MMC Operation Under Special Conditions

A. Unbalanced Grid Conditions

The majority of the technical literature on modeling and control of the MMC primarily assume balanced system conditions [1]–[7], [9], [10], [12]. Control of the MMC under unbalanced grid conditions has been reported in [8], [9], [87]– [89]. Under unbalanced grid conditions, the main control objectives are: i) to keep the ac-side currents balanced by suppressing their negative-sequence components, ii) to regulate the net dc-bus voltage, and iii) to control the circulating current and SM capacitor voltages.

Saeedifard and Iravani [8] present a generalized PWM strategy to control the MMC under unbalanced grid conditions, in which the MMC dynamics can be visualized as two decoupled subsystems, the positive- and the negative-sequence subsystems; and each subsystem can be controlled independently. The control strategy presented in [8], however, ignores the internal dynamics of the MMC and is only focused on the external dynamics. Furthermore, in the event of asymmetrical faults on the MMC side or in a transformer-less configuration, the zero-sequence current components become present, which lead to the dc-bus voltage ripple.

Tu *et al.* [87] propose a dc-voltage ripple suppressing controller to remove the zero-sequence voltage components of the dc side under unbalanced grid conditions and to keep the net dc-bus voltage constant. However, under unbalanced grid voltage, there is a double-line-frequency ripple in real power component. In [88] and [89], the circulating currents are analyzed as three components: positive-, negative-, and zero-sequence circulating currents under unbalanced grid conditions. Moon *et al.* [88] propose a circulating currents control method with ac-side positive- and negative-sequence current control to minimize the circulating currents and reduce the ac-side real power ripple under unbalanced conditions. In [89], based on the instantaneous power theory and by using a PR controller, a control strategy is proposed to eliminate the real power ripple and suppress the harmonics in the circulating currents. Guan and Xu in [9] proposed a zero-sequence ac-side current controller, along with the positive- and negative-sequence ac-side current controllers, to operate the MMC–HVDC system with/without the interface transformer under unbalanced grid conditions. In [90], based on a notch filter and a proportional integral resonant controller, a control strategy is proposed to eliminate the dc power ripple by removing the harmonics in the zero-sequence circulating currents under unbalanced grid conditions.

B. Fault Tolerant Operation

As mentioned earlier, the structural modularity of the MMC adds to its redundancy and fault tolerance. In case of any component/SM failure, the failed SM needs to be detected and bypassed. When an open-circuit fault occurs, the output voltage and current of the MMC are distorted. Furthermore, the capacitor voltage of the failed SM may rise up, leading to further, vast destruction.

Given the large numbers of identical SMs and the symmetrical structure of the converter, locating a faulty SM is challenging if adding additional sensors to each SM and/or the converter is not desirable. The extra sensors add to the cost and complexity of the system. In [91], a sliding mode observer-based fault detection method has been proposed. The method, based upon the measured converter arm currents and the SM capacitor voltages, which are already available as the measurement inputs to the control system, detects and locates the faulty SM as well as its failed switch.

V. Applications

A. HVDC Systems

The MMC, initially proposed for HVDC applications, has become the most promising type of VSC for HVDC systems. One of the major challenges associated with the MMC–HVDC system with the conventional half-bridge SMs is the lack of dc-side short-circuit fault handling capability. This problem is of severe concern, particularly for HVDC transmission systems with overhead lines. The existing solutions to interrupt and clear the dc-side short-circuit fault of the MMC–HVDC systems can be summarized as follows:

1) Opening the ac-side CBs. This solution is not sufficiently fast as it takes a few cycles, e.g., two to three cycles, for the CB to trip. Consequently, the freewheeling diodes of the MMC that form an uncontrolled rectifier should tolerate the high fault current for a few cycles. Although parallel connection of a protective thyristor within each SM can bypass the short circuit current flowing through the diodes, the fault current interruption relies on tripping the ac CBs [6], [62], [92]–[94]. Li *et al.* [95] propose a protection strategy to handle the nonpermanent dc-side faults. However, this strategy cannot ensure fast interruption of the fault current.
2) Employing the dc-side CBs. Although a solid-state dc CB for HVDC applications has recently been developed, the technology is not sufficiently mature and cost effective [13], [94], [96]–[99].
3) Embedding the dc fault handling capability in the HVDC converter configuration [4], [13], [19], [62].

In case of a half-bridge MMC–HVDC system, during a dc-side short-circuit fault, the fault current, as shown in Fig. 6(a), flows from the ac-side towards the dc side through the antiparallel diodes of the SMs. Therefore, the half-bridge SMs do not provide any capability of blocking the dc-side short-circuit fault current for the MMC–HVDC system. As shown in Fig. 1, the arm inductors L_o are used to limit the rate of

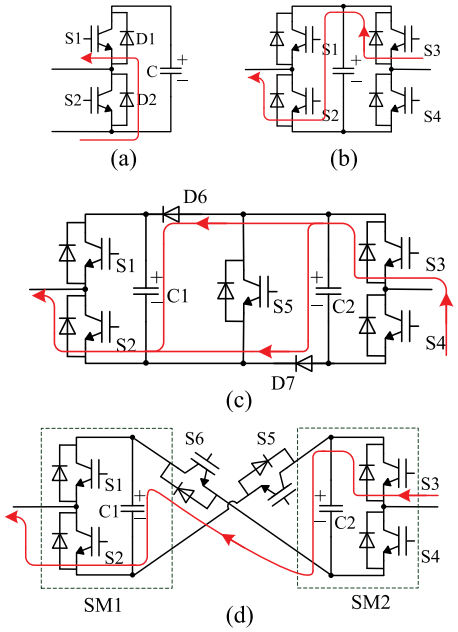

Fig. 6. DC-side short-circuit fault current path for: (a) a half-bridge, (b) a full-bridge, (c) a clamp-double, and (d) a five-level cross-connected SM.

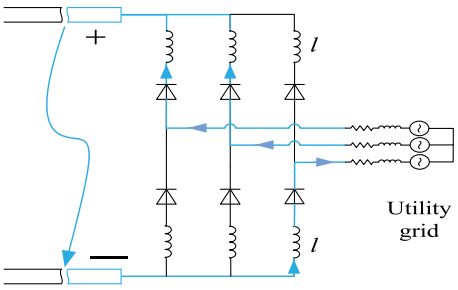

Fig. 7. Equivalent circuit of the MMC system during a dc-side short-circuit fault.

the fault current, i.e., $di_{\rm dc}/dt$. The equivalent circuit of the MMC of Fig. 1 during a dc-side short-circuit fault when all the switches are blocked is shown in Fig. 7. In case of a full-bridge MMC–HVDC system, subsequent to a dc-side short-circuit fault, when all of the IGBTs of the SMs are blocked, the capacitor voltages can generate reversed voltages to block the ac-side currents, as shown in Fig. 6(b). Thus, the full-bridge SMs can provide dc-side short-circuit fault handling capability. In case of a clamp-double MMC–HVDC system, during a dc-side short-circuit fault, when all of the IGBTs are blocked, the two capacitors of the clamp-double SM connected in parallel can generate an opposing voltage to block the short-circuit current, as shown in Fig. 6(c). In case of a five-level cross-connected MMC–HVDC system, after a fault occurrence, when all of the IGBTs are blocked, the two capacitors of the five-level cross-connected SM connected in series can produce an opposing voltage to drive the short-circuit current to zero, as shown in Fig. 6(d). In the MMC–HVDC system based on the clamp-double SMs, although the SMs have the capability to block the dc-side short-circuit current, they can only generate $nv_C/2$ or $V_{\rm dc}/2$ reversed voltage per arm, which is half of the reversed voltage

produced by the full-bridge/the five-level cross-connected SMs per arm. The MMC topology with full-bridge, double-clamp, or five-level cross-connected SMs eliminates the current path of the freewheeling diodes and can potentially interrupt the fault current within a fraction of a second. However, compared to the MMC with half-bridge SMs, this solution sacrifices the cost and power losses [4], [13], [19], [62].

B. Variable-Speed Drives

Application of the MMC to medium-voltage variable-speed drives has been shown to be advantageous over other multilevel converters such as the NPC and series connected H-bridge converter, with respect to the installed silicon area and dc-link energy [100]. However, this application has its own unique control challenges. The main challenge is the large ripple magnitude of the SM capacitor voltages at low frequencies.

The peak-to-peak ripple magnitude of the SM capacitor voltages is given by [83]

$$\delta v_{c,pp} = \frac{I_o}{2C_{\rm SM}\omega}\left(1-\left(\frac{m\cos\phi}{2}\right)^2\right)^{\frac{3}{2}} \tag{16}$$

where $i_{{\rm circ},j} \approx 0$, I_o is the ac-side phase current (i_j) magnitude, m is the magnitude of m_j (the phase-j reference waveform), ω is the ac-side angular frequency, and ϕ is the ac-side power factor angle. As shown in (16), the ripple magnitude of the SM capacitor voltages is inversely proportional to the ac-side frequency and directly proportional to the ac-side phase current magnitude. Consequently, in constant-torque applications, the ripple magnitude of the SM capacitor voltages at low frequencies becomes pronounced. This issue is less pronounced in quadrature torque applications since the current magnitude is proportional to the frequency. Therefore, there is a need to actively mitigate the low-frequency ripple components of the SM capacitor voltages when the MMC is used in variable-frequency constant-torque applications.

The existing capacitor voltage ripple reduction techniques are based on the removal of low-frequency components in the capacitor voltage ripple by introducing a common-mode voltage at the ac-side voltage and a circulating current in the phase-legs of the MMC [101]–[104]. The techniques include:

1) A sine-wave technique: A sinusoidal common-mode phase voltage and circulating current injection technique is proposed in [101], [103], and [104]. The common-mode phase voltage reference and the circulating current are given by

$$m_{\rm cm} = M_{\rm cm}\sin\omega_{\rm cm}t \tag{17a}$$

$$i_{{\rm circ},j} = i_j\left(\frac{1-m_j^2}{M_{\rm cm}}\right)\sin\omega_{\rm cm}t + \frac{m_j i_j}{2} - \frac{i_{\rm dc}}{3} \tag{17b}$$

where $M_{\rm cm}$ and $\omega_{\rm cm}$ are the magnitude and the angular frequency of the common-mode voltage, respectively. The reference waveforms of the SPWM technique, which are used to control the upper and lower arms of phase-j to generate the common-mode voltage are given by

$$m_{p,j} = \frac{1-m_j-m_{\rm cm}}{2} - m_{{\rm circ},j} \tag{18a}$$

$$m_{n,j} = \frac{1+m_j+m_{\rm cm}}{2} - m_{{\rm circ},j} \tag{18b}$$

where $m_{{\rm circ},j}$ is used to control the circulating currents. Based on the PWM strategy, the low-frequency components (averaged over the switching period) in $n_{p,j}$ and $n_{n,j}$ are given by

$$\tilde{n}_{p,j} = N\tilde{m}_{p,j} = N\left(\frac{1-m_j-m_{\rm cm}}{2} - m_{{\rm circ},j}\right) \tag{19a}$$

$$\tilde{n}_{n,j} = N\tilde{m}_{n,j} = N\left(\frac{1+m_j+m_{\rm cm}}{2} - m_{{\rm circ},j}\right) \tag{19b}$$

where $\tilde{x}$ represents the low-frequency components in x. Considering the low-frequency components, (14) becomes

$$\frac{d\tilde{v}_{cp,j}}{dt} = \frac{1}{NC_{\rm SM}}\left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} + \frac{i_j}{2}\right)\tilde{n}_{p,j} \tag{20a}$$

$$\frac{d\tilde{v}_{cn,j}}{dt} = \frac{1}{NC_{\rm SM}}\left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} - \frac{i_j}{2}\right)\tilde{n}_{n,j}. \tag{20b}$$

Due to the attenuating effects of the SM capacitor, the high-frequency (switching frequency and higher) components of the SM capacitor voltages are negligible. Therefore

$$v_{cp,j} \approx \tilde{v}_{cp,j} \tag{22a}$$

$$v_{cn,j} \approx \tilde{v}_{cn,j}. \tag{22b}$$

Substituting for $m_{\rm cm}$ from (17a), $i_{{\rm circ},j}$ from (17b), $\tilde{n}_{p,j}$ from (19a), and $\tilde{v}_{cp,j}$ from (22a) in (20a), the upper-arm phase-j SM capacitor voltages are deduced as

$$\begin{aligned}\frac{dv_{cp,j}}{dt} &\approx \left(\frac{i_{\rm dc}}{3} + i_{{\rm circ},j} + \frac{i_j}{2}\right)\frac{1}{C_{\rm SM}} \\ &\quad\times\left(\frac{1-m_j-m_{\rm cm}}{2} - m_{{\rm circ},j}\right) \\ &= \frac{1}{C_{\rm SM}}\left[\left(-\frac{m_j M_{\rm cm}}{4} - \frac{M_{\rm cm}}{4}\right.\right. \\ &\quad\left.+\frac{\left(1-m_j-m_j^2+m_j^3\right)}{2M_{\rm cm}}\right) i_j\sin\omega_{\rm cm}t \\ &\quad\left.+\frac{\left(1-m_j^2\right)}{4} i_j\cos 2\omega_{\rm cm}t\right].\end{aligned} \tag{23}$$

Assuming a sufficiently fast closed-loop circulating current controller, $i_{{\rm circ},j} = i_{{\rm circ},j,{\rm ref}}$. Considering appropriate phase shifts, similar expressions can be concluded for voltage ripple of the SM capacitors in the lower arm of phase-j. As shown in (23), the SM capacitor voltages do not contain low-frequency components. This contributes to reducing the magnitude of the voltage ripple.

Although by the sine-wave technique, the ripple magnitude of the SM capacitor voltages is reduced, the large magnitude of the circulating current increases the converter power losses and rating values of the components. To resolve this problem, a square-wave technique has been proposed in [102].

2) A square-wave technique: As opposed to the sinusoidal common-mode voltage and circulating current injection, to reduce the peak and rms values of the circulating current, a square-wave common-mode voltage and circulating current injection technique is proposed in [102]. The main drawback of the square-wave injection technique lies in the control of the circulating currents. The circulating current in phase-j, $i_{\mathrm{circ},j}$, of the MMC is controlled by the voltage across the arm inductor, which is given by $v_{\mathrm{circ},j} = L_o \frac{di_{\mathrm{circ},j}}{dt}$. To inject a square-wave circulating current, at certain instances $v_{\mathrm{circ},j} \to \infty$, which is impossible to attain. In reality, the maximum attainable $v_{\mathrm{circ},j}$ is limited and depends on the MMC circuit parameters. This limitation, consequently, impacts the control of the circulating current and the ripple magnitude of the SM capacitor voltages. Furthermore, because of the finite rise/fall time of the square-wave circulating current, additional harmonic components are introduced into the circulating current that would further impact the results.
3) A hybrid technique: A square-wave common-mode voltage and a sinusoidal circulating current (with or without a third harmonic component) is proposed in [105]. The advantage of this technique over the sine-wave technique is the reduction in peak/rms value of circulating currents and the SM capacitor voltage ripple. The common-mode reference voltage waveform and the circulating current are given by

$$m_{\mathrm{cm}} = \begin{cases} M_{\mathrm{cm}} & \text{if } 0 < t \le \dfrac{1}{2f_{\mathrm{cm}}} \\ -M_{\mathrm{cm}} & \text{if } \dfrac{1}{2f_{\mathrm{cm}}} < t \le \dfrac{1}{f_{\mathrm{cm}}} \end{cases}, \quad (24a)$$

$$i_{\mathrm{circ},j} = i_j \left(m_1 \sin\omega_{\mathrm{cm}} t + m_3 \sin 3\omega_{\mathrm{cm}} t\right) \times \left(\frac{1-m_j^2}{\frac{4}{\pi}M_{\mathrm{cm}}}\right) + \frac{m_j i_j}{2} - \frac{i_{\mathrm{dc}}}{3} \quad (24b)$$

where f_{cm} is the common-mode frequency. m_1 and m_3 in (24b) are determined to minimize the rms value of $i_{\mathrm{circ},j}$ and to mitigate the low-frequency components of the SM capacitor voltage ripple. Substituting for m_{cm} from (24a), $i_{\mathrm{circ},j}$ from (24b), $\tilde{n}_{p,j}$ from (19a), and $\tilde{v}_{cp,j}$ from (22a) in (20a), the upper-arm phase-j SM capacitor voltages are deduced as (21). To mitigate the low-frequency components of the SM capacitor voltage ripple, the last term in (21) should be enforced to zero, i.e.,

$$1 - m_1 - \frac{m_3}{3} = 0. \quad (25)$$

Two of the solutions for (25) include: i) $m_1 = 1, m_3 = 0$, and ii) $m_1 = 0.9, m_3 = 0.3$ [105]. While the former solution uses less voltage across the arm inductor to control its circulating current and may use a higher common-mode voltage, the latter minimizes the peak/rms value of the circulating current for a given common-mode voltage peak. That is, the two solutions provide a trade-off in terms of the performance parameters like peak/rms value of circulating current and SM capacitor voltage ripple. Therefore, the solution and the common-mode frequency chosen for a particular application is based on a Pareto optimal front of the performance parameters.

The application of the MMC in quadrature torque motor drives has been investigated in [106] and [107]. An inner current control strategy, comprising the arm current control through the control of the individual SM capacitor voltages as well as the control of the average SM capacitor voltage in each phase, along with a motor control to limit the inrush current during startup is presented in [106]. In [107], a startup technique for an induction machine with fan/blower-type load is presented where the SM capacitor voltages are slowly increased from a small value to their nominal value as the speed of the machine is built. This strategy assists in maintaining the capacitor voltages within the voltage limits. However, it is assumed that the synchronous frequency at startup is sufficiently high to have a small capacitor voltage ripple which may not be the case in all variable-speed drives. An optimized pulse pattern modulation for high-speed drives is implemented in [36]. The advantages of this technique have been explained in Section III-A. Energy balancing control strategies at low-frequency and normal mode of operation are proposed in [108] for the application of MMC in variable-speed drives. The strategies include a low-frequency mode based on the technique proposed in [101], a normal mode at other frequencies, and a switchover mode between the two modes of operation. Dimensioning of the MMC for propulsion system of electric ships, considering the induction machine and load characteristics, is presented in [109], in which the control

$$\frac{dv_{cp,j}}{dt} \approx -\frac{1}{C_{\mathrm{SM}}}\left[\frac{i_j\left(1-m_j^2\right)}{2}\left(\left(\frac{m_1}{3}-\frac{m_3}{2}\right)\cos 2\omega_{\mathrm{cm}}t + \left(\frac{m_1}{6}+\frac{m_3}{2}\right)\cos 4\omega_{\mathrm{cm}}t\right) + \frac{i_j\left(1-m_j^2\right)}{2}\frac{m_3}{6}\cos 6\omega_{\mathrm{cm}}t \right.$$
$$- \frac{i_j}{4}\left(1+m_j\right)\sum_{k=0}^{\infty}\frac{4M_{\mathrm{cm}}}{\pi\left(2k+1\right)}\sin\left\{\left(2k+1\right)\omega_{\mathrm{cm}}t\right\} + \left(1-m_j\right)\frac{\pi i_j\left(1-m_j^2\right)}{8M_{\mathrm{cm}}}\left(m_1\sin\omega_{\mathrm{cm}}t + m_3\sin 3\omega_{\mathrm{cm}}t\right)$$
$$\left. - \frac{i_j\left(1-m_j^2\right)}{2}\left(m_1\sin\omega_{\mathrm{cm}}t + m_3\sin 3\omega_{\mathrm{cm}}t\right)\sum_{k=2}^{\infty}\frac{1}{\left(2k+1\right)}\sin\left\{\left(2k+1\right)\omega_{\mathrm{cm}}t\right\}\right] + \frac{i_j\left(1-m_j^2\right)}{4}\left(1-m_1-\frac{m_3}{3}\right) \quad (21)$$

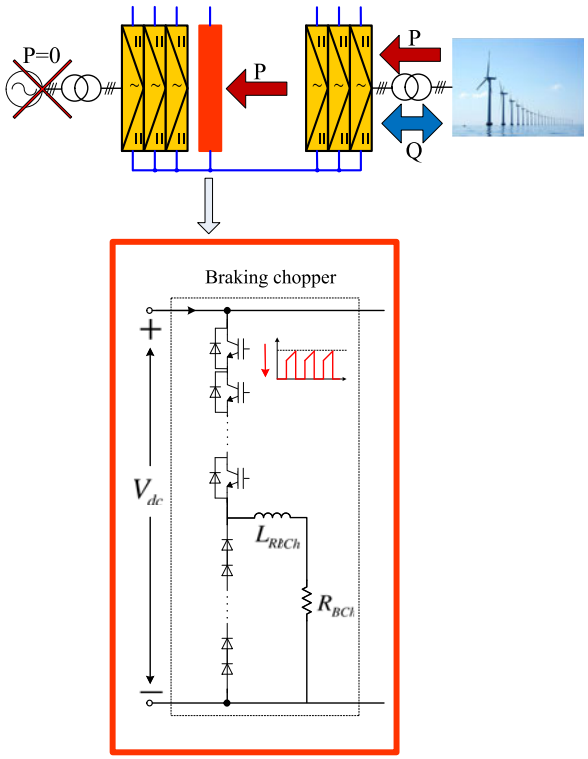

Fig. 8. Conventional braking chopper circuit.

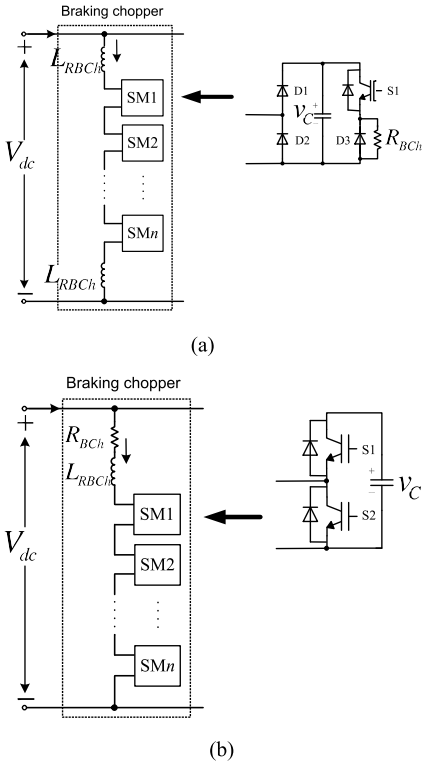

Fig. 9. Modular braking chopper circuits based on the MMC concept.

strategy proposed in [101] is adopted to control the ripple magnitude of SM capacitor voltages at startup and low frequencies. Dimensioning of the MMC for drive applications, including the calculation of the current/voltage rating and the size of the SM capacitors and arm inductances based on the strategy in [101], has been investigated in [110].

Antonopoulos *et al.* [111] present an analysis to select the average SM capacitor voltage within the mid-frequency operating range (one-third of the base speed to the base speed) of MMC-based variable-speed drives. The objective of the analysis is to optimize the difference between the total arm energy and the inserted arm energy and to improve the efficiency and the quality of the output voltages.

C. Dynamic Braking Chopper

In many applications, a dc braking chopper is required to absorb and dissipate the energy. One example is the MMC-based HVDC transmission system of an offshore wind farm. In case of inability of the receiving end (onshore station) of the MMC–HVDC system to accept the power in-feed from the wind farm, e.g., a nonpermanent fault on the onshore grid, the grid code does not tolerate any influence on the operation of the offshore station. Therefore, as shown in Fig. 8, the onshore station needs to absorb and dissipate the rated power of the wind farm without interrupting the operation of the wind farm during onshore faults. Conventionally, this is handled by installing a braking resistor connected to the dc side of the offshore VSC–HVDC converter station in the arrangement shown in Fig. 8. The circuit of Fig. 8 acts like a dc–dc buck converter, which is realized by series connection of a large number of devices to meet the high voltage rating of the switches. The conventional braking chopper of Fig. 8 cannot be applied to the MMC–HVDC converters because of the inductive current flowing through the MMC phase-legs. Alternatively, a modular design with series connected SMs, as shown in Fig. 9, which enables installation of a modular chopper configuration on the onshore side with minimal requirement for cost and space has been proposed and investigated [112], [113].

D. Other Applications

Benefits and salient features of the MMC for HVDC systems make it a prominent choice for flexible ac transmission system (FACTS) applications as well [6], [114]–[119]. The investigation and installation of the MMC-based STATCOM have been reported in [6], in which, based upon the half-bridge SMs, the MMC–STATCOM performs active filtering as well. Guying *et al.* [119] present an MMC-based unified power-flow controller. A shunt active power filter based on the MMC has been presented and discussed in [120].

One of the other potential applications of the MMC is in railway electric traction systems, in which the MMC, as a medium-voltage transformerless converter, is used to supply the traction motors [76], [121]. The application of the MMC for the propulsion system of electric ships has also been reported in [109] and [122].

In [123] and [124], the MMC topology has been investigated for grid connection of energy storage systems. Trintis *et al.* in [123] introduce a modular converter with integrated energy storage based on the MMC to interface low/medium-voltage batteries to the grid. Hillers and Biela in [124] study the optimal

design of the MMC for transformerless grid connection of a standalone high-power energy storage system.

In [125], a power electronic transformer based on an MMC followed by an isolated dual-active-bridge dc–dc converter and an inverter is proposed. Mei *et al.* [126] and Iannuzzi *et al.* [127] discuss the possibility of using MMC as an interface between the grid and photovoltaic panels.

On the subject of dc–dc converters, a family of medium/high voltage dc–dc converters based on the MMC topology has been recently introduced and investigated in [128]–[131]. Norrga *et al.* in [131] propose a methodology to optimize the design of the dc–dc converter based on MMC with regard to silicon area.

VI. Conclusion

The salient features of the MMC, i.e., its modularity and scalability enable it to conceptually meet any voltage level requirements with superior harmonic performance reduced rating values of the converter components and improved efficiency. Over the past few years, the MMC has become a subject of interest for various medium to high voltage/power systems and industrial applications including HVDC transmission systems, FACTS, medium-voltage variable-speed drives, and medium/high voltage dc–dc converters.

For power system applications, e.g., HVDC systems and FACTS, the MMC has reached a certain level of maturity and seems to stand as the most promising technology as a number of MMC–HVDC systems and STATCOMs has been successfully implemented and installed.

For medium-voltage variable-speed drives, there is still a plenty of room for further development to address the operational and control issues of the MMC, specifically under constant-torque low-speed operation. One major problem that needs to be addressed is to minimize the magnitude of the capacitor voltage ripple of the converter SMs at low frequencies without sacrificing the converter efficiency, thereby making a reasonable tradeoff between the converter size/volume/cost and efficiency.

The introduction of a family of modular multilevel dc–dc converters, originated from the MMC topology, has opened up a new avenue on research and development of medium/high voltage dc–dc converters. To take the full advantage of these converters for various applications, advanced modulation strategies that enable high-voltage conversion ratio, high efficiency and reduced component stresses are required.

With a significant amount of MMC-derived converter topologies and applications, it is concluded that development of novel modulation and control strategies will be a major driving factor to shape the future of MMC applications.

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2.2 中文翻译译稿

模块化多电平换流器的运行、控制和应用

摘要： 模块化多电平换流器（MMC）对于中高压电力换流系统来说正在变成一个越来越重要的课题。在过去的几年里，重要的研究指出了伴随着 MMC 运行和控制所产生的技术挑战。在这篇文章里，我们综述了 MMC 运行基础并讨论了控制所面临的挑战和先进的控制策略和趋势。最后，强调了 MMC 的应用和挑战。

关键词： 电容电压平衡，环流控制，高压直流 HVDC 输电，模块化多电平换流器 MMC，模块化技术，冗余，变速传动系统

2.2.1 导言

模块化多电平换流器（MMC）正成为中高级电压应用中最有吸引力的多电平换流器拓扑，特别是对电压源换流器高压直流输电系统。和其他多电平换流器拓扑相比，MMC 的显著特点包括：1）、模块化和可测量性满足任何电压等级需要；2）、高效，对高压应用有特别重要性；3）、优秀的谐波表现，特别是在高压应用当中，在这种应用中通过组合大量相同的低压子模块，减小了被动滤波器的大小；4）、不需要直流连接电容。

在过去几年中，有大量的研究致力于找到 MMC 控制和运行所带来的技术挑战并扩展其应用。这篇综述的主要目的是为 MMC 提供一个更好的理解和针对各种应用的技术命题。这篇文章全面总结了关于 MMC 运行、建模、控制和模块化技术最近的成果，同时强调了 MMC 的广泛应用和伴随的挑战。

文章的其余部分按如下方式展开。第二部分介绍 MMC 电路拓扑和能应用于换流器设计的各种子模块。接下来是关于 MMC 模块化技术、设计局限和各种运行问题最新成果的综述，包括电容器电压平衡和环路电流控制都在第三章中呈现。第四章包括 MMC 在特殊环境下运行和控制的最新发展，例如不平衡电网条件下的运行和容错运行。第五章介绍 MMC 的广泛应用和随之而来的技术挑战。第六章总结了全文。

2.2.2 MMC 拓扑

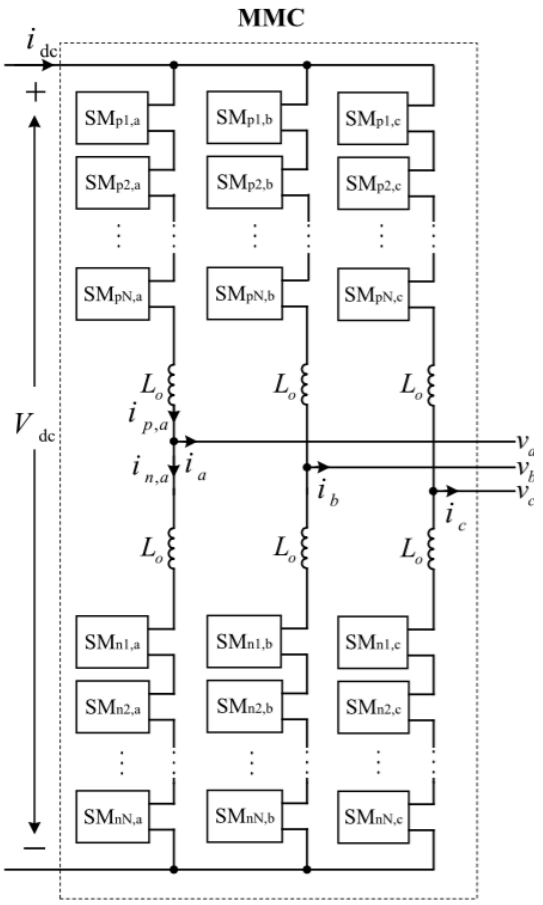

图 2.1 MMC 示意图

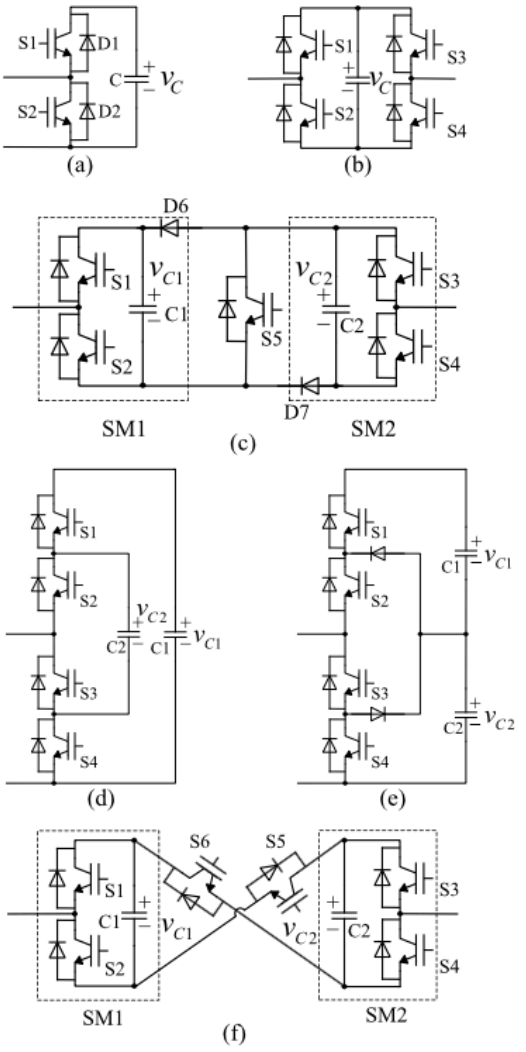

图 2.2 不同 SM 拓扑：(a) 半桥 (b) 全桥 (c) 双钳制 (d) 三级 FC (e) 三级 NPC 和 (f) 五级跨接 SM

图 3.1 所示是三相 MMC 的示意图，这个 MMC 由每相两臂组成，每臂由 N 个序列连接、名义上独立的 SM 和一个序列电感 L_0 组成。尽管控制每一臂中的 SM 长生需要的交流相电压，臂电感器抑制了臂电流中的高频分量。三相臂中的上（下）臂表示成 "p"("n")。

图 3.1 中 MMC 的 SM 可以从如下回路来理解：

1) 半桥回路或斩波单元（chopper-cell）：如图 3.2(a) 所示，半桥 SM 的输出电压或等

于其电容电压 v_c（开/接入状态），或等于 0（关/旁路状态），取决于开关对的开关状态，例如 $S1$ 和 $S2$。

2) 全桥回路或桥臂单元（bridge-cell）：如图 3.2(b) 所示，全桥 SM 的输出电压或等于其电容电压 v_c（开/接入状态），或等于 0（关/旁路状态），取决于四个开关 $S1$ 到 $S4$ 的状态。因为全桥 SM 的半导体数是半桥 SM 半导体数的两倍，基于全桥 SM 的 MMC 的能耗和费用都高于基于半桥 SM 的 MMC。

3) 双钳制回路（clamp-double）：如图 3.2(c) 所示，双钳制回路 SM 由两个半桥 SM、两个额外的二极管和一个与有反向二极管并联的绝缘栅双极型晶体管（IGBT）组成，正常操作中，开关 $S5$ 一直开启，双钳制回路 SM 等价于两个串联的半桥 SM，与同电压等级数量的半桥和全桥 MMC 相比，双钳制回路 MMC 的半导体能耗比半桥 MMC 高但比全桥 MMC 少。

4) 三级换流器回路：如图 3.2(d) 和 (e) 所示，三级 SM 由三级中性点钳制（neutral-point-clamped: NPC）或三级飞跨电容（flying capacitor: FC）换流器。三级 FC MMC 和半桥 MMC 半导体能耗相同。相比之下，三级 NPC MMC 的半导体能耗比半桥 MMC 高但比全桥 MMC 低。从制造和控制的角度，这种 SM 回路吸引力不大。

5) 五级跨接回路（cross-connected）：如图 3.2(f) 所示，一个五级跨接回路由两个半桥 SM 背靠背连接两个有反向并联二极管的 IGBT 组成。它的半导体能耗与双钳制回路相同。

表 3.1 展示了有关不同 SM 回路电压等级、直流侧短路容错能力和电能损耗的比较。直流侧短路问题是 MMC-HVDC 系统的主要挑战之一，这部分会在第五章 A 中讨论。在这所有 SM 回路中，半桥 SM 是适用于 MMC 最受欢迎的 SM。因为其中只有两个开关器件，所以减少了元件数并且提高了效率。在此之后，基于半桥 SM 的 MMC 开始被人们关注。需要注意的是，只有很少的换流器结构源自 MMC 拓扑。本文着重讨论图 3.1 所示的称为双星（double-star）的 MMC 结构。

SM 回路	电压等级	直流容错	能耗
半桥	$0, v_c$	否	低
全桥	$0, +v_c$	是	高
双钳制	$0, v_{C1}, v_{C2}, (v_{C1} + v_{C2})$	是	中
三级 FC	$0, v_{C1}, v_{C2}, (v_{C1} - v_{C2})$	否	低
三级 NPC	$0, v_{C2}, (v_{C1} + v_{C2})$	否	中
五级跨接	$0, v_{C1}, v_{C2}, +(v_{C1} + v_{C2})$	是	中

表 2.1 不同 SM 回路比较

2.2.3 MMC 的模块化、设计、控制和建模

2.2.3.1 模块化技术

针对 MMC 开发/提出的基于单个参考波形的不同的脉宽调制（PWM）技术包括：

1) 载波层叠 PWM 技术（CD-PWM）：这种技术需要 N 个独立三角载波波形关于 0 坐标轴对称出现。相电压参考波形和载波的比较产生了所需的开关输出相电压等级。对应于三角形载波的电压变换由一个特定 SM 的开启/旁路状态决定。基于载波波形的相变换，这一技术被进一步划分为：a) 同相层叠（PD）；b) 正负反向层叠（POD）；c) 交替反向层叠（APOD），分别如图 3.3(a)-(c) 所示。使用这些技术的不足之处包括 SM 电容上电压波动的不等分布和大量环流。为了提高交流侧电压的谐波失真，使用简单载波旋转技术、修正载波旋转技术或信号旋转技术来所有 SM 电容器的电压平衡。尽管采用了 SM 电容器电压平衡技术，输出电压有一个相对较高的总谐波失真（THD）。为了提高这些技术的表现，提出了一种有关 SM 电容电压平衡技术的 PD PWM 技术。在这种基于 PD 载波波形的技术中，有关三角形载波的电压变换不再针对某个特定的 SM。在这种技术中，参考波形和载波波形的比较产生出 $(N + 1) - level$ 波形，进而分别决定了插入上下桥臂中 SM 的数量。取决于桥臂中的电流方向河 SM 电容器的电压状态，在上（下）桥臂中插入除 N 个 SM 之外特定数量的 SM 来最小化 SM 电容器电压间的差异。Mei 等人提出了一种带选择性回路偏置映射法的 PD PWM 技术来平衡 SMSM 电容器。这种方法实现了使用下列反馈的载波旋转：a) 最大/最小 SM 电容电压和 b) 桥臂电流方向。这种技术的优点包括：a) 不需要额外参考信号来控制 SM 电容器和 b) 即便在大量 SM 情况下易于用简单的现场可编程门阵列（FPGA）实现。

2) 次谐波技术：在这种技术中，每相有 $2N$ 个独立的载波，锯齿波或三角波，之间有 $\theta = 360°/2N$ 相位差，如图 3.3(d) 和 (e) 所示。假设对 PD PWM 和次谐波技术有相同数量的开关变换，PD PWM 技术产生更好地线到线电压 THD。

另外，基于使用多参考波形有几种模块化技术。这些模块化技术包括：

1) 直接模块化：在这种模块化技术中，j 相的上下桥臂电压由两个互补的正弦参考曲线控制，如下所示：

$$n_{p,j,ref} = N\frac{\frac{V_{dc}}{2} - v_{j,ref}}{V_{dc}} \tag{1a}$$

$$n_{p,j,ref} = N\frac{\frac{V_{dc}}{2} + v_{j,ref}}{V_{dc}} \tag{1b}$$

其中 $v_{j,ref}$ 代表参考输出电压，$n_{p,j,ref}$ 和 $n_{n,j,ref}$ 是上下桥臂中开启 SM 数量的参考波形。(1) 中的参考波形和 PD 载波波形比较，在 0 到 N 中波动，来决定上下桥臂中需要开启的 SM 数量。直接模块化技术的主要缺点在于存在环路电流，增加了换流器能耗和组件的额定值。

2) 间接模块化：在这种技术中，j 相上下桥臂的参考波形如下给出：

$$n_{p,j,ref} = N\frac{\frac{V_{dc}}{2} - v_{j,ref} - v^{\Sigma}_{reg,j} - v^{circ}_{reg,j}}{\sum_{i=0}^{N} v_{cp,i,j}} \tag{2a}$$

$$n_{p,j,ref} = N\frac{\frac{V_{dc}}{2} + v_{j,ref} - v^{\Sigma}_{reg,j} - v^{circ}_{reg,j}}{\sum_{i=0}^{N} v_{cn,i,j}} \tag{2b}$$

其中 $v_{cx,i,j}$ 表示 j 相桥臂 x 中 $SM-i$ 的电容电压，$v^{\Sigma}_{reg,j}$ 和 $v^{circ}_{reg,j}$ 用来控制 j 相的总能量并分别平衡桥臂之间的能量。类似于直接模块化技术，参考波形和 PD 载波波形比较，在 0 到 N 中波动，来决定上下桥臂中需要开启的 SM 数量。这种技术可以进一步细分成：

a) 闭环控制：闭环控制中，(2) 中的 $\sum_{i=0}^{N} v_{cp,i,j}$ 项基于实际测量电容电压计算，进一步，$v^{\Sigma}_{reg,j}$ 和 $v^{circ}_{reg,j}$ 从 j 相桥臂电容储存的闭环控制总能量和桥臂间能量平衡分别获得。每个桥臂间储存能量的平衡暂时取决于基频正弦环路电流。这种

技术的优点在于 i) 平均 SM 电容电压的控制，使得能在高电压等级和低输出电压下运行，和 ii) 上下桥臂间能量平衡的控制。

b) 开环控制：开环控制中，(2) 中的 $\sum_{i=0}^{N} v_{cp,i,j}$ 项基于估计测量电容电压计算。另外，$v_{reg,j}^{\Sigma} = 0$ 并且估计 $v_{reg,j}^{circ}$ 来降低环路电流的谐波并保证换流器的稳定控制。这种估计由求解描述换流器动态的方程获得，使用测量得到的输出电流和直流连接电压。这种技术的优点在于不需要电压传感器，控制简单迅速。尽管如此，主要缺点在于难以准确估计描述系统动态所需要的真实参数。

3) 相变换载波 PWM 技术（PSC PWM）：在这种技术中，MMC 的每个 SM 独立控制，Sm 的电压平衡任务分为平均控制和平衡控制。每一个 SM 上下桥臂中的的参考波形如下给出：

$$m_{p,i,j} = N\frac{\frac{V_{dc}}{2} - \frac{v_{j,ref}}{N} + v_{a,j} + v_{b,i,j}}{v_{cp,i,j}} \tag{3a}$$

$$m_{p,i,j} = N\frac{\frac{V_{dc}}{2} + \frac{v_{j,ref}}{N} + v_{a,j} + v_{b,i,j}}{v_{cn,i,j}} \tag{3b}$$

其中 $v_{a,j}$ 和 $v_{b,i,j}$ 分别是平均和平衡控制器输出。平均和平衡技术分别控制每一相桥的平均 SM 电容器电压。每一个 SM 电压参考波形和三角载波的比较产生相应 SM 的开关信号。每一个桥臂的三角形载波波形基于次谐波技术实现。这项技术的主要缺点在于随着 SM 数量的增加实现难度加大并且在特定运行情况下存在不稳定性。通过基于上下桥臂中电容电压的不同在参考电压中引入另一个概念，桥臂平衡控制，可以改善后一种缺点。

性质	改进 PD-PWM	直接模块化	间接模块化	PSC-PWM
参考波形数	1	2	2	$2N$
稳定所需额外控制器数	否	否	是	是
是否存在环路电流	是	是	否	否
实现难度	中	中	低（开环）-中（闭环）	高（随着 $N\uparrow$）

表 2.2 模块化策略比较

表 3.2 给出了前述模块化策略的简单比较，MMC 控制策略在图 3.4 的表格中总结。除了前述的 PWM 技术，还提出了一种 SHE-PWM 技术，其中限定开关模式来减

少输出电压波形的低次谐波。开关模式被计算并储存在各种模块化索引和输出电压相角的查询表中。

基于基频开关的模块化技术被提出和研究。提出了一种最近层控制（NLC）模块化技术，其中选择离所需电压波形最近的电压等级。相比于 SHE-PWM，NLC 技术易于实现，所需计算能力更少，相比于 PWM 技术使用的开关频率更低。文献 [35] 中提到的技术基于给定 SM 的固定脉冲形式来保持每一个 SM 中存储能量的稳定性，而不用测量电容器电压或任何反馈控制，去除任何强制模块化索引和输出电压相角的特定的输出电压谐波。[36] 提出的技术最优化了脉冲形式来减小输出电压的谐波失真。基频开关技术的主要优势在于减小开关频率并减小输出电压的 THD 的同时对输出电压频率没有任何限制。这点和 PWM 技术不同，其载波频率限制了输出电压的频率。

2.2.3.2 SM 电容电压平衡

类似于其他多级换流器技术，MMC 需要有功电压平衡策略来平衡和保持 SM 电容器电压在 V_{dc}/N。Deng 和 Zhen 在 [37] 中提出一种电压平衡策略，使用相变换载波 PWM（PSC-PWM）来控制 MMC 桥臂电流中的高频分量。给 SM 每个桥臂加载合适的 PWM 脉冲来平衡电容器电压。这增加了控制的简单性并减少了传感器数量。Hagiwara 和 Akagi 在 [30] 中提出一种电压平衡策略，针对每个 SM 的闭环控制。在 [11] 中，开发了一种 MMC 控制的预测性策略，其中 SM 电容器电压基于预先定义好的损耗方程平衡。最广泛接受的电压平衡策略是基于排序法（sorting method）[8], [38]-[40]。为了实现基于排序法的电容电压平衡，需要测量和排序 SM 每一个桥臂的电容器电压。如果 N 个 SM 对应的桥臂 $n_{p,j}(n_n, j)$ 中上（下）桥臂电压为正，有最低电压的 SM 被选出开启。结果，对应开启的 SM 电容器充电，电压升高。如果 N 个 SM 对应的桥臂 $n_{p,j}(n_n, j)$ 中上（下）桥臂电压为负，有最高电压的 SM 被选出开启。结果，对应开启的 SM 电容器放电，电压下降。不考虑上（下）桥臂的电流方向，如果一个桥臂中的 Sm 被旁路，对应的电容器电压保持不变。尽管排序法保证电容电压平衡在 MMC 运行要求之下，却在 SM 中带来了不必要的开关变换。尽管在两个连续控制期中所需运行的 SM 数保持不变，可能会发生 SM 的开启或旁路。这个结果不是很

理想，因为增加了开关频率相应的增加了能耗，特别是对于高压系统来说。提出/研究的用来减小 MMC 开关频率的方法主要基于：

1) 结合相变换载波 PWM 策略的闭环修正排序法，SM 的开启/旁路状态基于电容电压测量 [39], [41]。在这种方法中，每个控制环中只有有限数量的 SM 参加排序，即在每个控制环并基于需要的电压等级，如果需要在每个桥臂中开启（关断）额外的 SM，只有关状态（开状态）的 Sm 需要被考虑排序和开关。

2) 结合选择性谐波消除 PWM 技术的开环控制 [35]。

3) 混合平衡策略，结合预测误差排序法和传统的电压排序算法 [42]。这种策略基于排序向前一步预测电容电压和其有名值之间的绝对误差来排序。每一个控制期内，有最小预测电压误差的 SM 被选择开启。

4) 基频平衡策略，在预先制定的相角下基于传统方法排序。

5) 一种最优化电容电压平衡策略，排序之前先调整测量之后的 SM 电容电压。这种策略关注电容电压超过特定电压限制的 SM，其他 SM 的开关状态保持相同。引入保持因子并和关闭状态的电容器电压相乘，这些电容器电压超过电压限增加了在下一个控制环内被开通/旁路的概率。

6) 一种预测算法来计算和分配储存在 SM 电容器中的电量 [44]。

2.2.3.3 数学模型

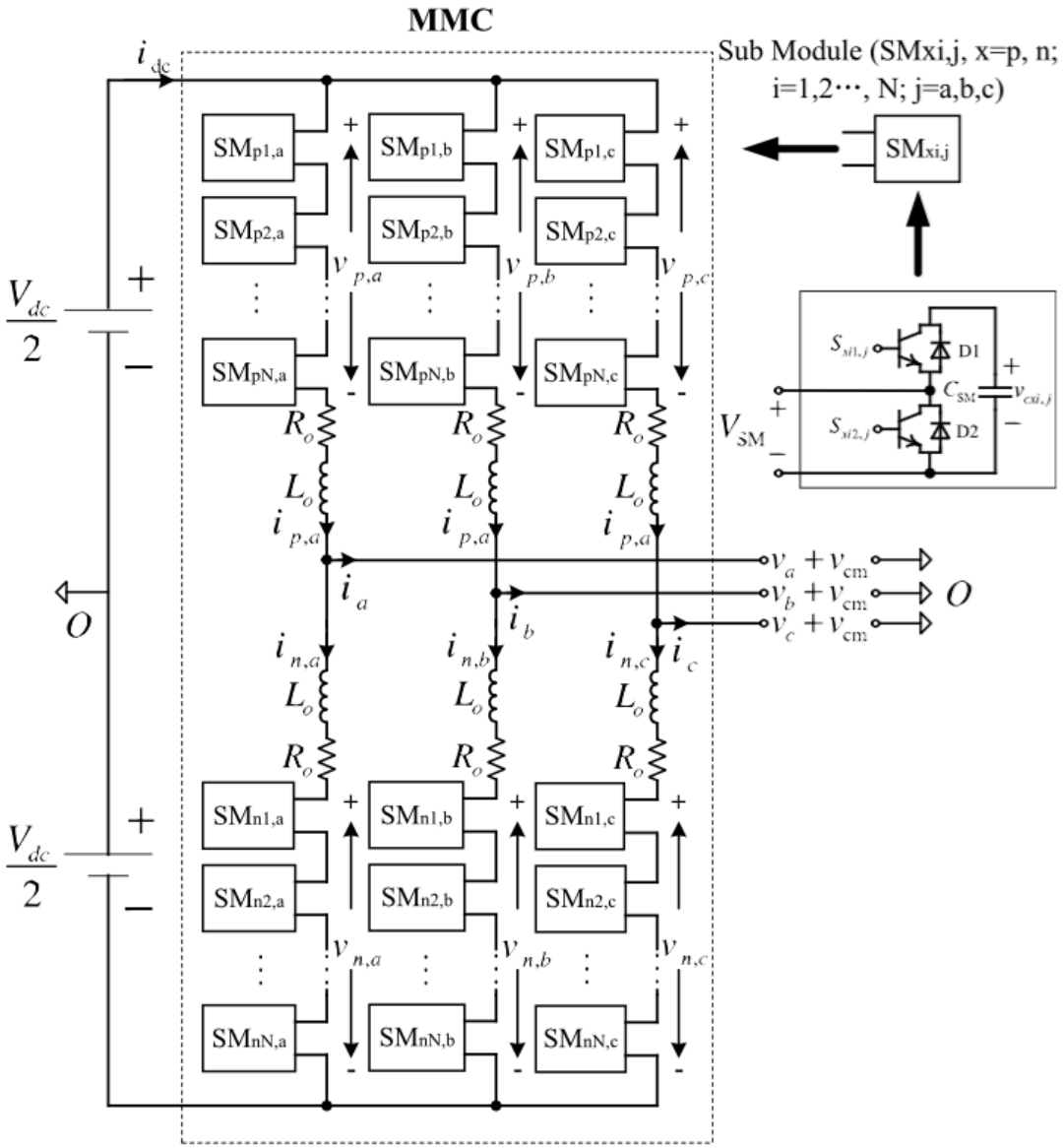

图 2.5 MMC 电路图

图 3.5 所示为一个基于半桥 SM 的三相 MMC 电路图。与图 3.1 相比，有一个额外的桥臂电阻 R_0，用来模拟 MMC 每个桥臂的能耗。

本章建立的 MMC 数学模型基于文献 [8], [11], [45-47] 中使用最广泛的模型。

在图 3.5 中的 MMC 中，j 相上下桥臂电流，$j = a, b, c, i.e, i_{p,j}andi_{n,j}$ 表示为：

$$i_{p,j} = \frac{i_{dc}}{3} + i_{circ,j} + \frac{i_j}{2} \tag{4a}$$

$$i_{n,j} = \frac{i_{dc}}{3} + i_{circ,j} - \frac{i_j}{2} \tag{4b}$$

其中 $i_{circ,j}$ 表示 j 相环路电流，i_j 是交流侧 j 相电流，i_{dc} 是直流侧电流。基于 (4)，环路电流为：

$$i_{circ,j} = \frac{i_{p,j} + i_{n,j}}{2} - \frac{i_{dc}}{3} \tag{5}$$

由 j 相 MMC 动态行为给出的数学公式为：

$$V_{dc} - v_{p,j} = L_0 \frac{di_{p,j}}{dt} + R_0 i_{p,j} + v_j + v_{cm} \tag{6a}$$

$$V_{dc} - v_{n,j} = L_0 \frac{di_{n,j}}{dt} + R_0 i_{n,j} - v_j - v_{cm} \tag{6b}$$

其中 $v_{p,j}$ 和 $v_{n,j}$ 表示 MMCj 相上下桥臂电压，v_j 和 v_{cm} 分别表示基本和共模电压分量。从 (6a) 中减去 (6b) 并从 (4) 中替换出 $i_{p,j}$ 和 $i_{n,j}$，MMC 相电压表示为：

$$v_j + v_{cm} = \frac{v_{n,j} - v_{p,j}}{2} - \frac{R_0}{2} i_j - \frac{L_0}{2} \frac{di_j}{dt} \tag{7}$$

进一步，将 (6a) 和 (6b) 相加并从 (5) 中减去 $i_{circ,j}$，MMC 环流内部动态表达为：

$$L_0 \frac{di_{circ,j}}{dt} + R_0 i_{circ,j} = \frac{V_{dc}}{2} - \frac{v_{n,j} + v_{p,j}}{2} - R_0 \frac{i_{dc}}{3} \tag{8}$$

MMC 的 j 相上下桥臂电压也可以描述为：

$$v_{p,j} = n_{p,j} v_{cp,j} \tag{9a}$$

$$v_{n,j} = n_{n,j} v_{cn,j} \tag{9b}$$

其中 $v_{cp,j}$ 和 $v_{cn,j}$ 分别是上下桥臂独立 SM 电容器电压。方程 (9) 基于有功电容

器电压策略平衡的假设并保持 MMC 每个桥臂中所有 SM 的电容器电压相等，例如 $v_{cxi,j,k} = v_{cx,j,k}$ 对 $\forall i \in 1, 2, ..., N$。将 (9) 中的 $v_{p,j}$ 和 $v_{n,j}$ 带入 (7) 和 (8)，得到下列表达式：

$$v_j + v_{cm} = \frac{n_{n,j}v_{cn,j} - n_{p,j}v_{cp,j}}{2} - \frac{R_0}{2}i_j - \frac{L_0}{2}\frac{di_j}{dt} \tag{10a}$$

$$L_o\frac{di_{circ,j}}{dt} + R_0 i_{circ,j} = \frac{V_{dc}}{2} - \frac{n_{n,j}v_{cn,j} - n_{p,j}v_{cp,j}}{2} - R_0\frac{i_{dc}}{3} \tag{10b}$$

另外，

$$P_{dc} = P_{ac} + P_{loss} \quad \Rightarrow \quad V_{dc}i_{dc} = \sum_{j=a,b,c} v_j i_j + P_{loss} \tag{11}$$

其中 P_{loss} 表示换流器的能耗。

MMC 每一个 SM 电容电压由每臂的功率建模。每臂的功率由下式给出：

$$p_{p,j} = v_{p,j}i_{p,j} = n_{p,j}v_{cp,j}i_{p,j} \tag{12a}$$

$$p_{n,j} = v_{n,j}i_{n,j} = n_{n,j}v_{cn,j}i_{n,j} \tag{12b}$$

MMC 每相桥臂上的功率也可以表示为：

$$\begin{aligned} p_{p,j} = \frac{dW_{p,j}}{dt} &= \frac{d(\frac{N}{2}C_{SM}v_{cp,j}^2)}{dt} \\ &= v_{cp,j}NC_{SM}\frac{dv_{cp,j}}{dt} \end{aligned} \tag{13a}$$

$$\begin{aligned} p_{n,j} = \frac{dW_{n,j}}{dt} &= \frac{d(\frac{N}{2}C_{SM}v_{cn,j}^2)}{dt} \\ &= v_{cn,j}NC_{SM}\frac{dv_{cn,j}}{dt} \end{aligned} \tag{13b}$$

其中 C_{SM} 表示 SM 电容量。基于 (12) 和 (13)，每个 SM 电容器电压波动的动态可以

表示为：

$$\begin{aligned}\frac{dv_{cp,j}}{dt} &= \frac{i_{p,j}}{NC_{SM}}n_{p,j} \\ &= \frac{1}{NC_{SM}}(\frac{i_{dc}}{3}+i_{circ,j}+\frac{i_j}{2})n_{p,j} \qquad (14a)\\ \frac{dv_{cn,j}}{dt} &= \frac{i_{n,j}}{NC_{SM}}n_{n,j} \\ &= \frac{1}{NC_{SM}}(\frac{i_{dc}}{3}+i_{circ,j}+\frac{i_j}{2})n_{n,j} \qquad (14b)\end{aligned}$$

(4), (5), (11) 和 (14) 式提供了一个 MMC 一般化的动态模型，可以用于控制目的。类似于 MMC 的这种一般化动态模型，参考文献 [27] 和 [28] 将每个桥臂中电容电压的累加组成的 MMC 动态模型看成是一个静态变量，而不是独立的 SM 电容电压。

2.2.3.4 MMC 设计限制

MMC 的设计包括选择电容、电感和 SM 的数量，基于一些性能指标包括桥臂电流波动、短路电流、电容电压波动、可靠性和能耗。

1) 电容电感选型：桥臂电感 L_0 作为滤波器来减小桥臂电流中的高频谐波同时也限制了直流侧短路电流。因此，桥臂电感的大小取决于滤波选择和短路电流限制 [5], [51], [52]。

   SM 电容的选型基于对大小/能耗和电压震荡的权衡。在很大范围的运行环境中，SM 电容电压震荡在 [55]-[59] 中得到分析。对于 SM 电容电压 $\delta v_{c,pp}$ 考虑一个许可的峰峰谐波等级，基于 [55] 的元电容取决于：

$$C_{SM} = \frac{P}{3NmV_c\delta c_{c,pp}\omega cos\theta}(1-(\frac{mcos\theta}{2})^2)^{\frac{3}{2}} \qquad (15)$$

   其中 C_{SM} 是 SM 电容，P 是有功功率，V_c 是 SM 电容器的标么电压，m 是调节指数，而 $cos\theta$ 是功率因数。

   基于存储能量和功率流动的关系，[61] 提出一个 SM 电容器选型方法。

2) 功率损耗计算：相比于二级 VSC 系统，半导体损耗大于 1%[13]，MMC 的半导体损耗可以潜在地降低到低于 1%。

主要有两种方法来评估 MMC 的半导体损耗。第一种取决于仿真模型和实时仿真数据 [40], [63]-[67]。尽管这种方法的计算压力很大，却可以提供精确的结果而不用考虑模块化/控制策略，电压等级和 SM 电路拓扑。[62] 和 [63] 介绍的另一种方法，基于分析性模型可以潜在地降低计算时间。可是，保证精度方面是一个挑战因为这种方法基于理想假设和特殊的模块化/控制策略。

3) 可靠性：MMC 因为其模块化的结构，可以提升冗余 SM 结构中的容错限 [12], [68]，进而提升其可靠性。可是，在特定的容错限之下，控制硬件限制了换流器的稳定性。

2.2.3.5 环路电流控制

流经 MMC 三相桥臂的环路电流源自三相桥臂中的电压差异 [53], [70] 并且包含频率是基频两倍的负序分量 [70]。环路电流对于交流侧电压电流没有任何影响。可是，如果不正确地控制，他们会增加相电流的峰值结果将增加换流器的能耗和 SM 电容电压的震荡大小。环路电流在 [70]-[72] 中被建模和分析。[71 提出一种环路电流模型基于控制环路电流为电流控制电压源。这可以接着被用于控制电压来降低环路电流分量的影响。

为了控制环路电流，文献 [11], [28]-[30], [41], [45], [46], [57], [73], [74] 中提出了各种各样的技术。[28]-[30] 中的间接建模技术在前述章节中已经介绍。Harmefors 等人使用有功电阻（合适的控制器）来控制环路电流，包括对桥臂电阻的估计。基于双线频 $acb-dp$ 变压器，Tu 等人 [41] 通过控制他们一对 PI 控制器的的 dp 部分来减小环路电流。Debnath 和 Saeedifard[45] 等人致力于降低通过比例共鸣（PR）控制器的环路电流的交流分量。Yang[57] 等人提出一种改进的开关函数来消除用于 STATic 和 COMpensator（STATCOM）中的 MMC 环路电流。[11] 提出一种基于模型的预测控制（MPC）来降低环路电流分量。主要缺点在于计算量大，尤其对于有大量 SM 的 MMC 来说。

2.2.3.6 SM 电容电压震荡消除技术

[55] 深入研究了 SM 电容电压震荡, [57]-[59] 主要研究基频和二次谐波分量。基于桥臂功率，[76] 提出使用合适的二次谐波分量来降低 SM 电容电压的震荡大小。使用二次和四次谐波分量 [56] 中的方法最优化了每个桥臂中的能量变化。Debnath 和 Saeedifard[45] 提出一种闭环控制策略来减小电容电压波动的二次谐波分量并且数学地证明了所提出的方法简介见底了电容电压的震荡大小。

Engel 和 Doncker[56] 提出最优化方法通过保持桥臂电流的 rms 值来降低电容电压波动，进而限制了换流器的功率损失。

除了 SM 电容电压波动的减小策略，文献 [49] 和 [79] 变形电容电压波动来最大化运行区域（有功率极限定义）。

2.2.3.7 SM 电容预充电和启动过程

MMC 启动时，在正常工作之前需要提前充电到相等的特定电压等级。为了减小冲击电流和启动时间，最好是一种快速平滑启动。[55], [80]-[86] 从去能量化的角度研究了 MMC 中 SM 电容器的预充电和启动过程。启动过程经两步进行：1) 分别充电直流侧电容器和经过二极管桥整流器的 SM 电容器至 V_{dc} 和 $\frac{V_{dc}}{2N}$，假设所有 SM 电容器插入直流侧并且涌入电流被交流侧的串联电阻限制，2) 旁路交流测电阻接着从 $2N$ 到 N 逐渐减少开通 SM 的数量，进而让电容从 $\frac{V_{dc}}{2N}$ 到 $\frac{V_{dc}}{N}$。

2.2.4 特殊情况下 MMC 的运行

2.2.4.1 非平衡电网条件

建模和仿真 MMC 的主要技术文献假设系统处于平衡状态 [1]-[7], [9], [10], [12]。非平衡条件下 MMC 的控制在文献 [8], [9], [87]-[89] 中有讨论。在非平衡电网条件下，主要的控制目标是：i) 通过限制负序分量来平衡交流侧电压，ii) 调节电网直流总线电压，iii) 控制环路电流和 SM 电容器电压。

Saeedifard 和 Iravani[8] 提出了一种普遍的 PWM 策略来在非平衡电网条件下控制 MMC，这种情况下，MMC 动态可以被视为两个解耦的子系统，正序和负序子系统；每个子系统可以被分别控制。

Tu 等人 [87] 提出一种直流电压波动限制的控制器来去除非平衡电网条件下直流侧零序分量并保持电网直流总线电压恒定。可是，在非平衡电网电压条件下，在实际功率器件中有双线频率波动。Guan 和 Xu 在 [9] 中提出零序交流电压控制器，和正负序交流电压控制器，来在非平衡电网条件下运行 MMC-HVDC 系统通过/不通过接口变压器。

2.2.4.2 容错运行

如前面所提到的，MMC 的模块化设计提高了其冗余和容错。在任何原件/SM 失效的前提下，失效的 SM 需要被检测出来并旁路。当一个开环错误出现时，MMC 的输出电压和电流紊乱。进一步，失效的 SM 电容器电压升高，导致更大的破坏。

2.2.5 应用

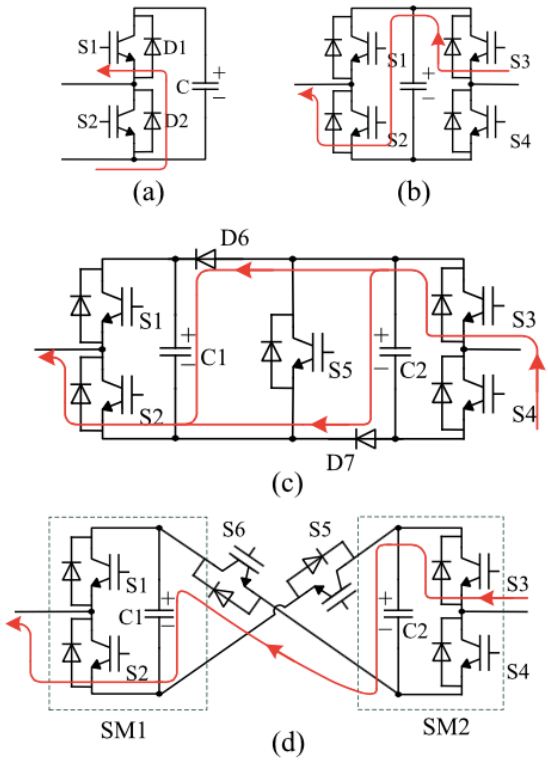

图 2.6 直流侧短路错误电流路径：(a) 半桥；(b) 全桥；(c) 双钳制；(d) 五级跨接 SM

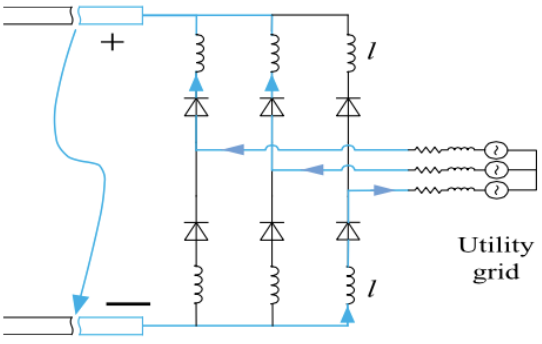

图 2.7 直流短路时 MMC 系统的等效电路

2.2.5.1 HVDC 系统

MMC 最初是为了 HVDC 系统而提出，变成了 HVDC 系统最可靠的 VSC 形式。采用传统半桥 SM 的 MMC-HVDC 系统的一个主要挑战之一是缺少直流侧电流错误处理能力。这个问题非常严重，尤其是对于没有过载能力的 HVDC 系统来说。现有的干预和处理 MMC-HVDC 系统直流侧短路故障的方法总结如下：

1) 打开交流侧 CB。这种方案并不是很快速因为它需要几个循环，比如两到三个循环。结果是，组成非控制整流器的 MMC 惯性二极管需要忍受几个循环高故障电流。

2) 采用直流侧 CB。尽管用于 HVDC 的固态直流 CB 怎年来得到开发，但这项技术并不是很成熟费用也比较高。

3) 在 HVDC 换流器结构中嵌入直流故障处理能力。

2.2.5.2 变速伺服

MMC 在中压变速伺服中的应用比其他多级换流器例如 NPC 和串联 H 桥换流器有更大的优势。可是，这种应用有其自身独有的控制挑战。主要的挑战在于在低频情况下 SM 电容器电压有很大的波动量。

SM 电容电压的峰峰波动量由下式给出 [83]：

$$\delta v_{c,pp} = \frac{I_0}{2C_{SM}\omega}(1 - (\frac{mcos\theta}{2})^2)^{\frac{3}{2}} \tag{16}$$

其中 $i_{circ,j} \approx 0$，I_0 是交流侧相电流 (i_j) 大小，m 是 m_j 的幅值，ω 是交流侧相角频率，θ 是交流侧功率因数角。如式（6）所示，SM 电容电压的波动幅值反比例于交流频率并且正比例与交流侧相电流幅值。结果，在恒转矩应用中，SM 电容器电压的波动幅值在低频时变得很大。这种情况在正交转矩应用时不那么明显因为电流幅值正比于频率。因此，有必要减小 SM 电容器电压的低频波动分量当 MMC 应用在变频恒转矩情况下时。

2.2.5.3 动态制动斩波器

在很多应用中，直流制动斩波器需要吸收和分解能量。一个例子是离岸风电场中的基于 MMC 的 HVDC 变换系统。因为 MMC-HVDC 末端无法接收风电场的功率，例如按上电网的非永久性故障，电网无法忍受离岸电站的任何故障。因此，如图 3.8 所示，岸上电站需要吸收和分解风电场的功率而在出现故障时不干扰风电场的运行。这就需要在 VSC-HVDC 换流站离岸直流侧安装由如图 3.8 所示的制动电阻来实现。

另外，图 3.9 所示为串联连接 SM 的模块化设计，使模块化斩波器能够满足最小费用和空间的情况下被安装到岸上。

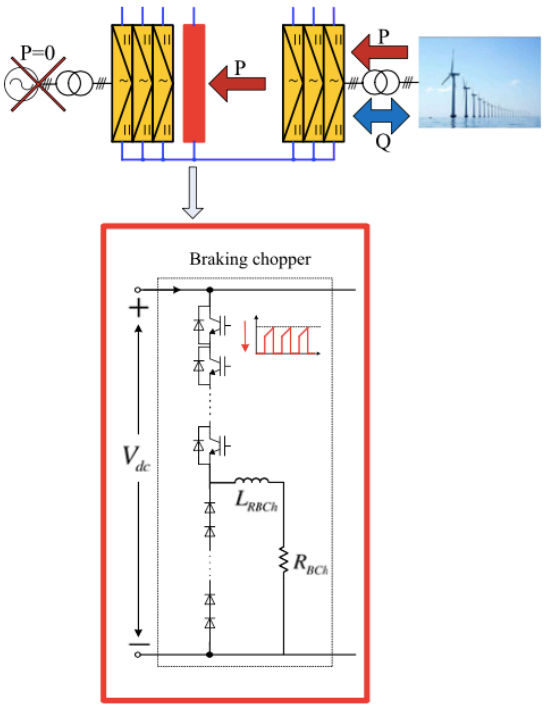

图 2.8 传统制动斩波器电路

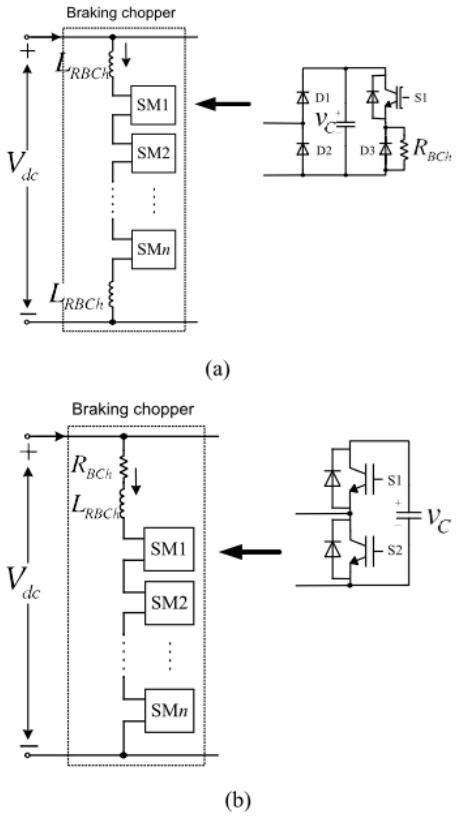

图 2.9 基于 MMC 概念的模块化制动斩波器

2.2.6 结论

MMC 的主要特征，例如其模块化和可测量性使其理论上满足任何电压等级的需求，有非常好的谐波性能和很高的效率。在过去几年中，对各种中/高压电压/功率系统和包括 HVDC 转换系统、FACTS、中压变速伺服和中/高压 dc-dc 换流器在内的工业应用，MMC 变成了一个热点问题。

对电力系统应用来说，例如 HVDC 系统和 FACTS，MMC 有一定的成熟度，并且似乎是最主流的技术，因为很多 MMC-HVDC 系统和 STATCOMs 被成功地完成和安装起来。

对于中压变速伺服，有关 MMC 的运行和控制未来还有很多发展空间，尤其是在常转速低速的情况下。需要注意的一个主要问题是在低频情况下减小电容器电压波动的大小同时不牺牲换流器效率，因此需要在换流器大小/容量/费用和效率之间做一个权衡。

源自 MMC 拓扑的一类模块化舵机 dc-dc 换流器的引入打开了中/高压 dc-dc 换流器领域研究和发展的一个新方向。为了更好的应用在各种应用中去，需要有高压换流器比率、高效率和器件压力较小的的高级模块化策略。

随着大量出现的源自 MMC 的换流器拓扑和应用，可以得出结论，新的模块化和控制策略的发展会是未来 MMC 应用的主要推动力。

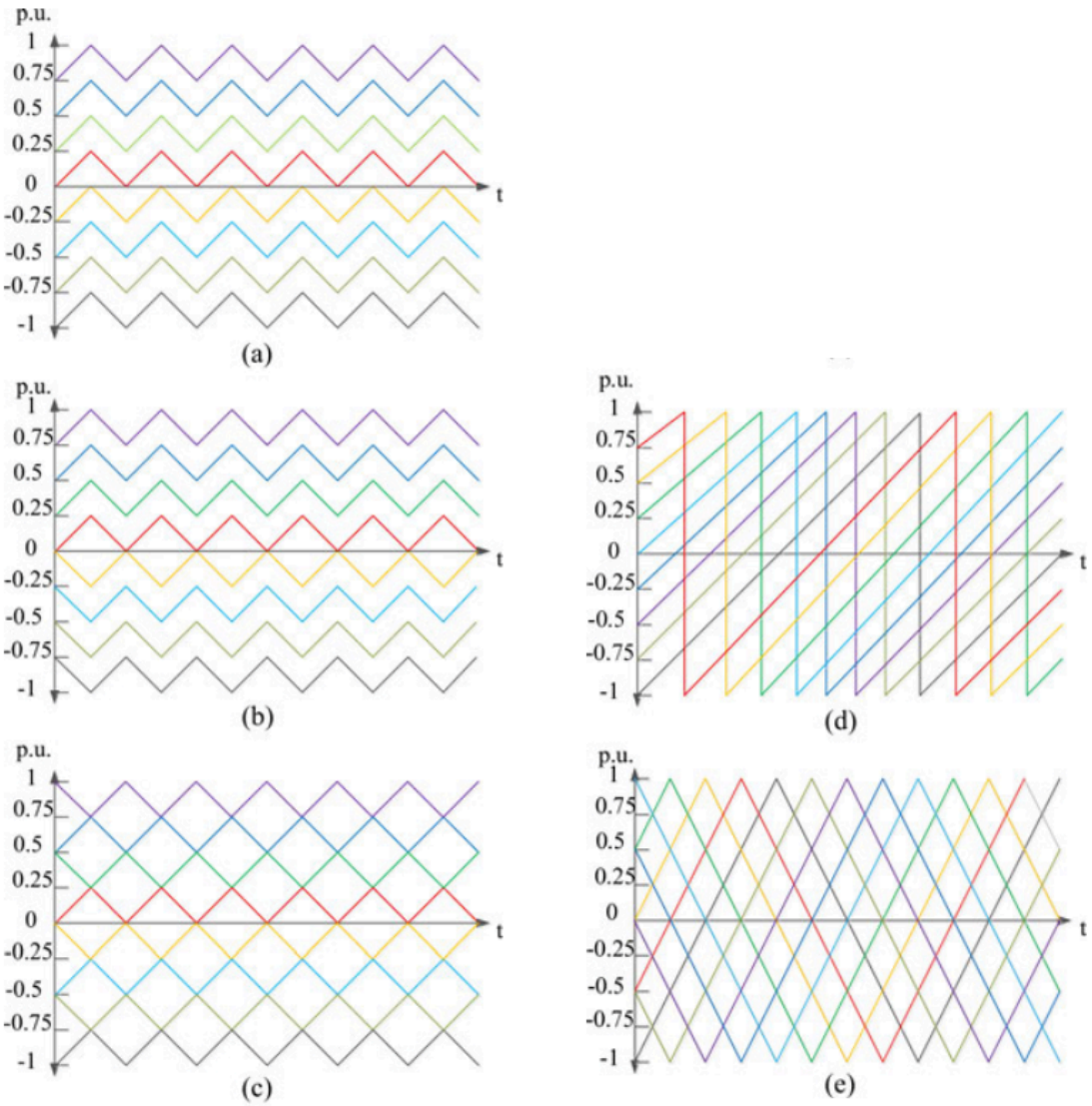

图 2.3 多电平载波： (a) PD, (b) POD, (c) APOD, (d) saw-tooth, and (e) 相变换载波

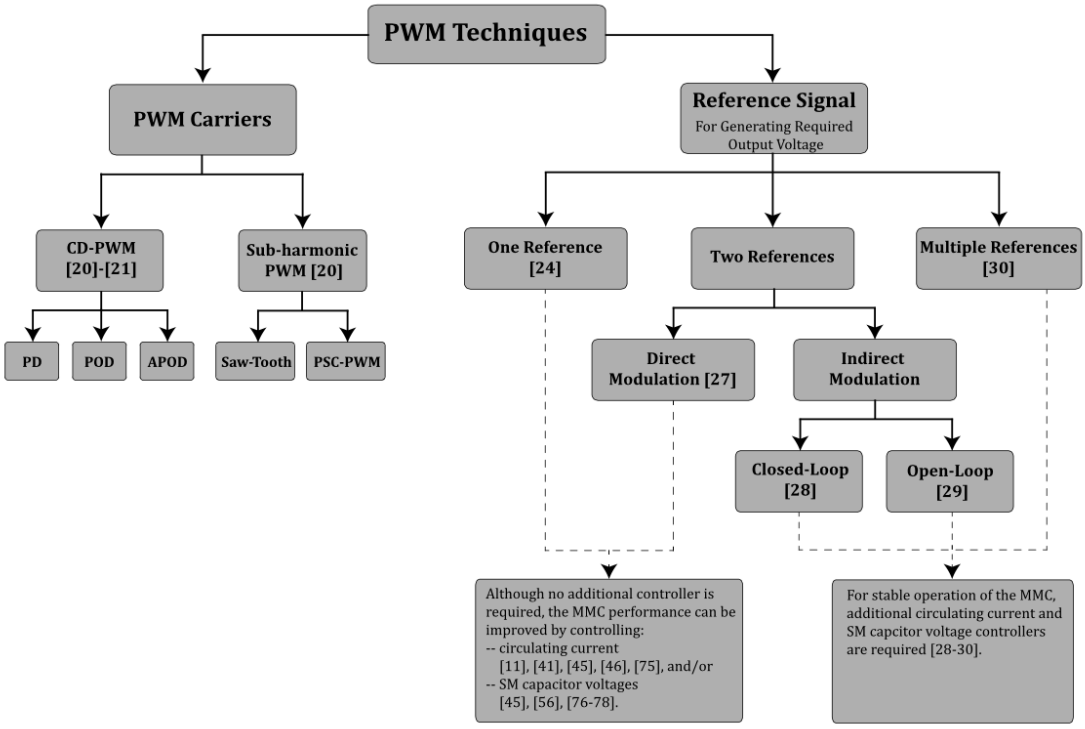

图 2.4 MMC 使用的不同 PWM 技术概览

第 3 章　开题报告

3.1　项目研究目的

现在电力系统常用的数据格式是基于 BPA 文本文件，其缺陷是不易于实现自定义等高级操作，在研究新能源或新设备并网问题时, 需要在现有的大电网模型基础上建立新元件模型, 但 BPA 不能修改和自定义元件模型。相比之下，DIgSILENT 具有可靠灵活的系统建模能力，该软件不仅包含了其他电力系统仿真软件中的潮流、短路、机电暂态、电磁暂态等分析功能, 还具有很多独特而实用的优点。它是以图形化操作和数据管理技术为支撑, 便于调试和结果分析; 具有风力发电、光伏发电等元件模型, 也可由用户自定义各种与那件模型。

针对电力系统不同的问题，采用较优的电力系统商业软件，可以使得科研分析等工作具有事半功倍的效果。因此需要数据转换程序，以便能够选择需要的仿真软件进行仿真。

3.2　研究内容和研究步骤

研究内容主要分为以下几个方面：

- 复习潮流计算中所使用的主要数据类型和数据格式。
- 学习 BPA 的主要功能和数据格式，BPA 数据是基于卡片格式的, 主要的潮流数据卡片可以分为五类, 分别为区域控制数据卡、节点数据卡、支路数据卡、变压器卡及数据修改卡。进而学习 DIgSILENT 的数据格式和相关操作，DIgSILENT 采用的是分层的面向对象的数据库, 潮流数据填入各个代表元件的图形中储存为对象。
- 阅读、学习由 BPA 到 PSS/E 的实现程序和董炜学长编写的 BPA 到 DIgSILENT 转换程序，在这个过程中形成自己对 BPA 到 DIgSILENT 程序转换的思路，着重理解相关参数的对应和转化，发现方法。

- 完成程序的编写，对比分析几个软件的潮流计算结果。
- 带入相关的算例进行测试，对比 BPA 和 DIgSILENT 的动态计算结果。

3.3 程序运行流程

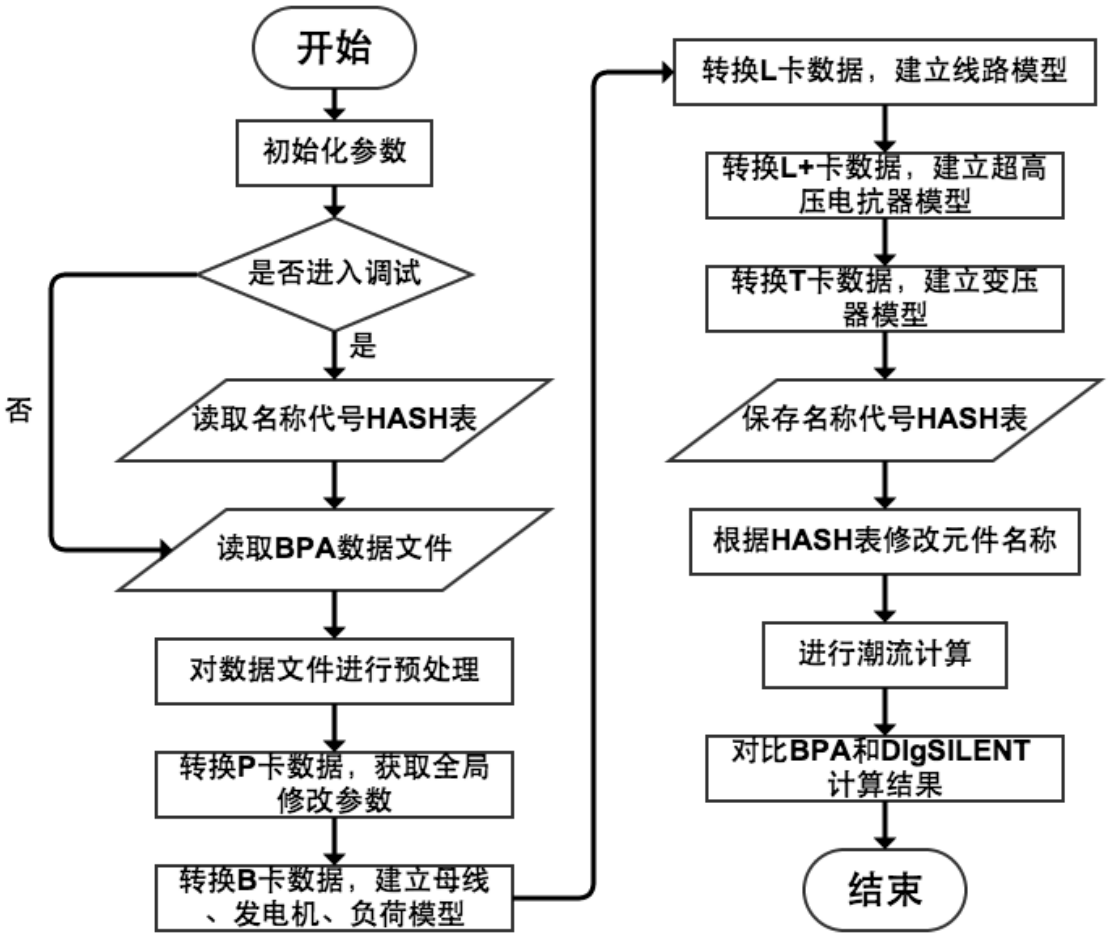

图 3.1 BPA 至 DIgSILENT 数据转换程序流程图

如图 3.1 所示为程序的运行流程图，BPA 模型导入 DIgSILENT 主要需要以下步骤：

1) 首先读取潮流修改卡片 P 卡，获取全网或部分网络发电出力或负荷的修改百分数。

2) 建立母线、发电机和负荷节点的 DIgSILENT 模型，读取节点数据卡 B 卡，根据不同情况处理填入数据。

3) 通过读取对称线路数据卡 L 卡和线路高抗参数数据卡 L+ 卡，建立普通线路模型和超高压电抗器模型。

4) 读取变压器数据卡 T 卡建立变压器模型。

5) 在 DIgSILENT 和 BPA 中分别进行潮流计算，比较相关运行结果。

3.4 论文的进度安排

本文的主要内容是通过文献资料的阅读整理，学习数据转换的基础理论知识，了解有关的常规算法以及新提出的改进算法，研究这些算法的理论并且对目前常用的算法进行收集整理，分析各种算法的优缺点以及适用条件。认识并熟悉 BPA 和 DIgSILENT 的基本使用技巧，了解他们的数据格式，编程语言，并能有一定应用。

进度安排

3 月 23 日 -4 月 20 日：进行文献资料的阅读学习，学习软件编程语言和仿真软件，研究由 BPA 到 PSS/E 的实现程序和董炜学长编写的 BPA 到 DIgSILENT 转换程序，熟悉软件使用；

4 月 21 日 -5 月 10 日：进行程序的开发和调试；

5 月 11 日 -5 月 21 日：结合算例对比程序运行结果，改进程序；

5 月 22 日 -结题：完成毕业论文的撰写。

第 4 章 DIgSILENT 的 Python 接口简介

4.1 Python 脚本语言的优势

本章主要介绍在 *PowerFactory* 中整合 Python 脚本语言的接口，并解释了在 DIgSILENT 中开发 Python 脚本的相关步骤。在 *PowerFactory* 中，Python 脚本语言主要实现以下功能：

- 任务自动化执行
- 创建用户自定义的运算指令
- 将 *PowerFactory* 整合到其他应用程序之中

DIgSILENT 自带的 DPL 程序在可以快速实现 DIgSILENT 内部数据的导入和导出，并且易于访问或更改 DIgSILENT 内部对象。但是，DPL 存在以下明显缺点：

- DPL 不能像 Python 语言那样实现比较灵活和通用的功能
- DPL 的开发环境不能像 Python 语言那样提供调试功能

因此,DPL 适用于程序代码较短的功能，并不适于开发大型或复杂的功能。相比于 DPL，Python 脚本语言有以下明显的优势：

- Python 适用性强，并不是为 DIgSILENT 专门设计，属于高级编程语言
- 语法简单，逻辑清晰，程序可读性强
- 免费，适用于开源协议
- 用途极其广泛
- 有大量的标准运行库和第三方接口模块
  - 对外部数据库和类似于 Microsoft Office 应用程序的接口

- 网络互联服务等等

对 Python 的整合使得 *PowerFactory* 可以实现以上提到的种种优势，要在 *PowerFactory* 中使用 Python，需要遵循以下步骤：

1. 安装 Python 脚本解释器
2. 使用 *PowerFactory* 中的 Python 模块*'power factory.pyd'* 编写 Python 脚本程序
3. 通过 *PowerFactory* 中的 Python 命令对象 (*ComPython*) 执行 Python 脚本

4.2 *PowerFactory* 中的 Python 模块

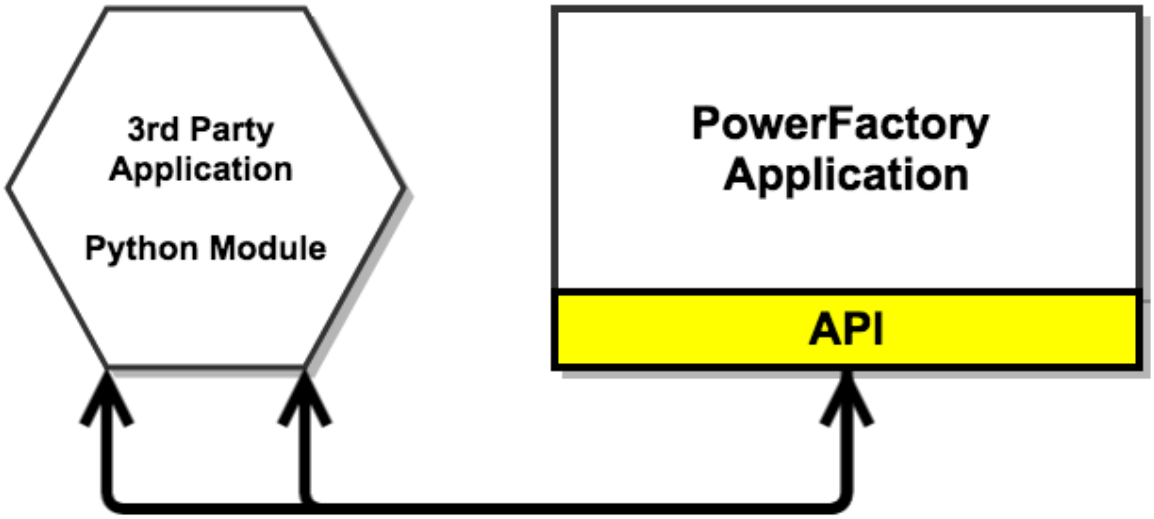

图 4.1 Python Module 通过 API 与 *PowerFactory* 交互示意图

如图 4.2 所示，Python 脚本主要通过一个和 *PowerFactory API* 交互的动态 Python 模块 (*'power factory.pyd'*) 来实现 *PowerFactory* 的相关功能。这种方法使得 Python 脚本可以使用 *PowerFactory* 中的大量数据，包括：

- 所有对象
- 所有属性 (元件数据，类型数据，结果)

- 所有命令 (潮流计算等等)
- 大部分特殊内建函数 (DPL 函数)

导入这个动态模块的 Python 脚本可以通过 *PowerFactory* 内部命令行对象 *ComPython* 来运行，或者通过外部引擎使用。

4.3 Python 命令行对象 (*ComPython*)

Python 命令行对象 (*ComPython*) 如图 4.2 将 Python 脚本链接到 *PowerFactory*。它仅仅保存文件的路径而不是具体文件。

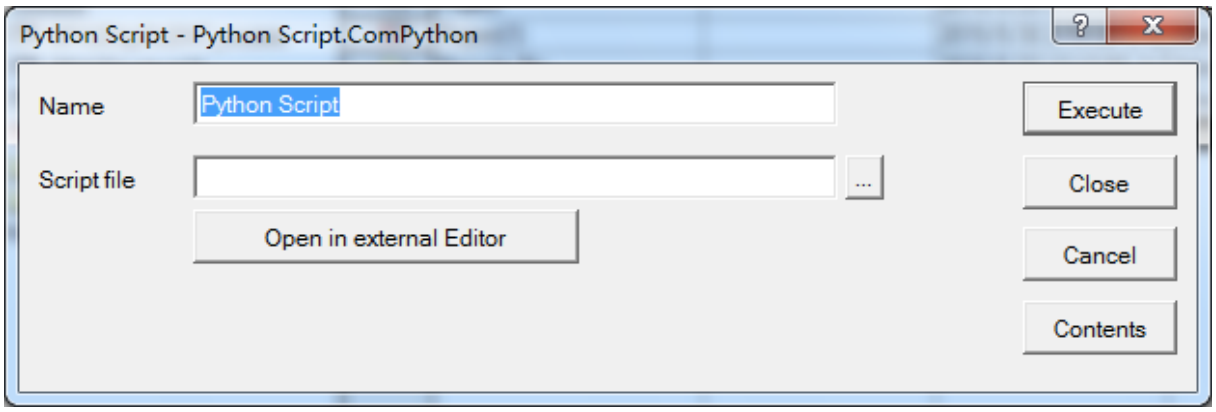

图 4.2 Python 命令行对象 (*ComPython*) 对话框

脚本可以通过点击 **Execute** 按键来执行，可以通过点击 **Open in external Editor** 来比编辑脚本，脚本的编码需采用 UTF-8 编码格式。

要新建一个 Python 命令对象，需点击 *New Object* 按钮，并选择如图 4.3 所示 *DPL Command and more* 选项，在下拉菜单中选择 *Python Script*。

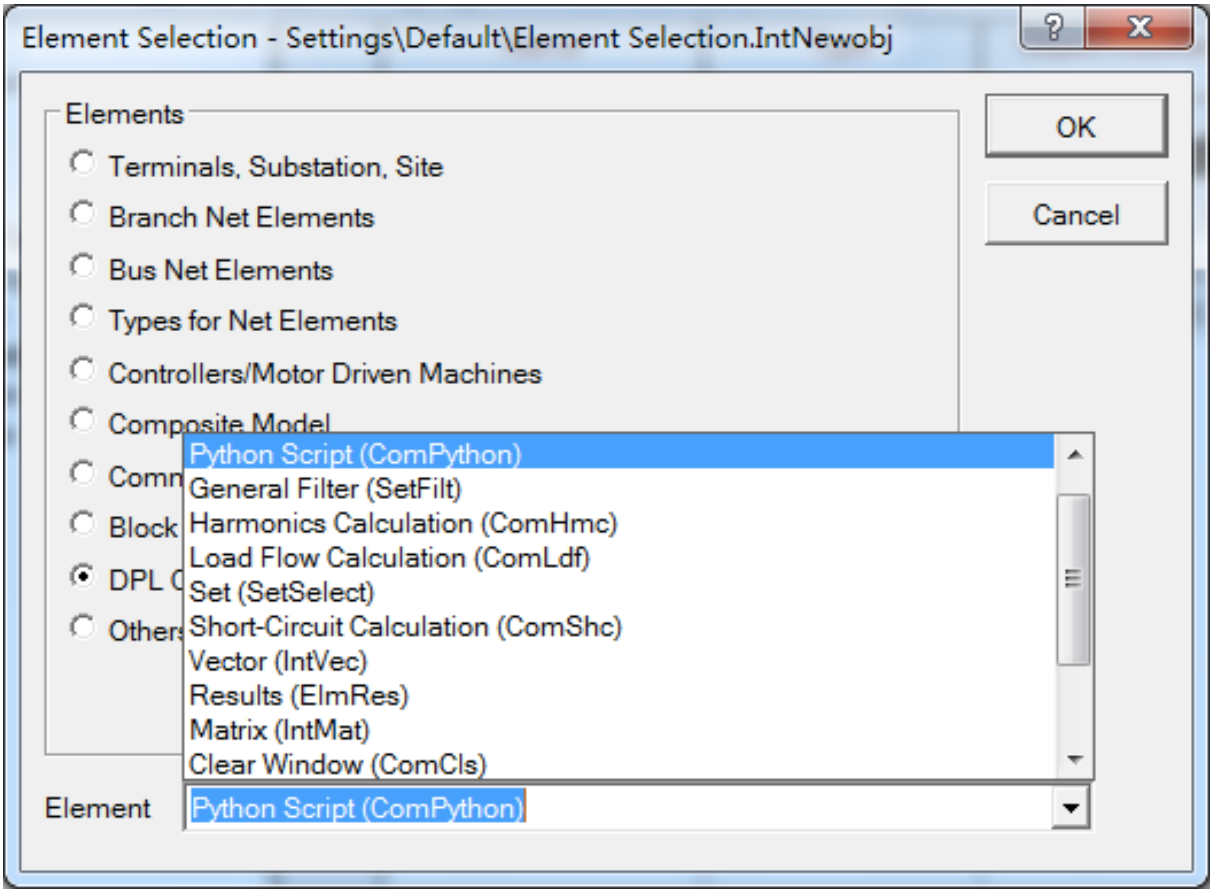

图 4.3 新建一个 Python 命令行对象 (*ComPython*)

4.4 调试 Python 脚本

与其他 Python 脚本一样，*PowerFactory* 也可以通过特殊应用程序来调试。

4.4.1 准备条件

推荐使用 Eclipse IDE 来调试 Python 甲苯，需要安装 Python 插件 *PyDev*。

1. 从 *www.eclipse.org/downloads/* 安装 Eclipse Standard
2. 点击 *help* 菜单中的*"Install New Software ..."*，添加目录 *http://pydev.org/updates* 并安装 *PyDev*

4.4.2 为 *PowerFactory* 调试 Python 脚本

如下所示是一个通过 *PyDev* 远程调试 Python 脚本的介绍。

1. 启动 Eclipse 并打开 *Debug* 视图
2. 通过点击 *PyDev* 菜单中的*"Start Debug Server ..."* 启动远程调试服务
3. 准备待调试的 Python 脚本：
   - 在 *sys.path* 中添加*"pydevd.py"*
   - 导入 PyDev 调试模块*"pydevd"*
   - 通过启动 *pydevd.settrace()* 开始调试

   Example:

```
#prepare debug
import sys
sys.path.append \
("C:\\Program Files\\eclipse\\plugins\\org.python.pydev\\pysrc")
import pydevd
#start debug
pydevd.settrace()
```

4. 运行该脚本的 Python 命令行对象 (*ComPython*)
5. 进入 Eclipse 使用远程调试服务调试

第 5 章 BPA 数据读取与转换

5.1 BPA 数据卡片的分类

主要的数据卡片可分为四类, 分别为区域控制、节点数据、支路数据及节点数据修改卡。

卡片分类	卡片描述
区域控制数据卡	AC、A，指定参与区域功率交换的分区及安排交换功率量 AO，按区域分类输出 I，指定区域交换功率
节点数据卡	B，交流节点卡 BD，两端直流节点卡 BM，多端直流节点卡 +，延续节点卡 X，可切换电抗、电容器卡
支路数据卡	L，对称线路卡 LD，两端直流线路卡 LM，多端直流线路卡 T，变压器和移相器卡 R，带负荷调压变压器调节数据卡 E，不对称等值支路卡 RZ，可快速调整的线路串补数据卡
数据修改卡	P，系统中发电出力和负荷按百分数修改卡 Z，分区重新命名卡 DZ，分区删除卡

表 5.1 主要数据卡片分类

在 BPA 到 DIgSILENT 的数据转换程序中，我们需要处理的主要是一下这些卡片：B，交流节点卡；L，对称线路卡；T，变压器和移相器卡；P，系统中发电出力和负荷按百分数修改卡。下面来详细介绍各个卡片的数据格式和模型。

5.2 B 卡

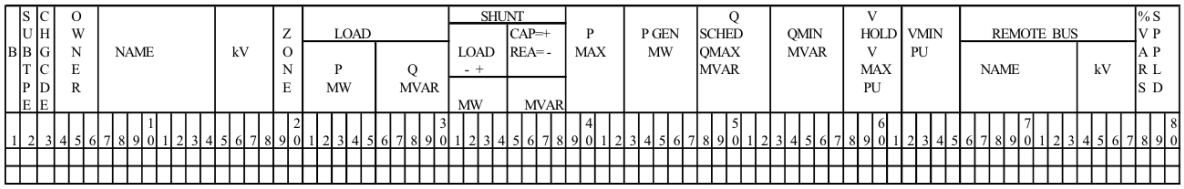

图 5.1 B 卡数据

列	格式	内容
1	A1	卡片类型－B
	A1	卡片子型 -各子型如下： 空白－PQ 节点 T －PQ 节点，但节点电压受带负荷调压变压器控制 C －PQ 节点，但节点电压受某发电机控制 V －PQ 节点，但节点电压有限制值：$V_{min} < V < V_{max}$，当电压越界时，自动转换为 PV 节点，这时 Q 起变化，以保证电压在限制值内，由此产生的未安排无功，将由程序自动装上电容器（电抗器）来平衡 E －PV 节点，无功出力没有限制，但为达到控制电压，无功出力超过上下限时，超过部分无功称为未安排无功，程序自动装上电容器或电抗器 Q －PV 节点，但节点无功功率有限制值：$Q_{min} < Q < Q_{max}$，当越界时，自动转换为 PQ 节点 G －PV 节点（其为发电机节点），缺省电压在 0.95 ～ 1.15 之间变化，并去控制 BC 节点的电压。其无功 Q 也有限制，当 Q 越限时，中止电压控制。被控节点不可以是 Vθ 节点、BG 节点或者其它已处于被控状态下的节点 F －在计算中先作为 PV 节点，待有功功率 P 收敛后再自动转换为 B（PQ）节点 S －Vθ 节点，为交流同步网的缓冲机 J －在采用改进的牛顿 -拉夫逊法时作为 BS 节点，当解法转化为牛顿 -拉夫逊法以后，该节点自动转换为 B（PQ）节点 K －在采用改进的牛顿 -拉夫逊法时作为 BS 节点，当解法转化为牛顿 -拉夫逊法以后，该节点自动转换为 BE（PV）节点 L －在采用改进的牛顿 -拉夫逊法时作为 BS 节点，当解法转为牛顿 - 拉夫逊法以后，该节点自动转换为 BQ（PV 节点，$Q_{min} \leqslant Q \leqslant Q_{max}$）节点 X －在该节点装有电抗器或者电容器，由程序自动控制投切电抗器或者电容器，以维持该节点或者其它节点的电压为给定值。

其中 S 节点的判断比较重要，需要特殊处理。需在同步电机卡中选定为 reference machine，如图 5.1 所示。

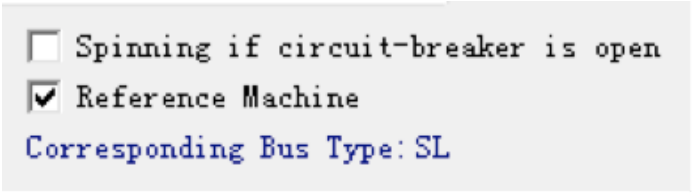

图 5.2 reference machine 选择

5.2.1 DIgSILENT 负载模型介绍及数据转换

列	格式	内容
2	A1	修改码，在程序中不做处理
4-6	A3	所有者代码－用于确定区域功率交换中联络线的测点和输出表中按所有者分类的分析报告，可不填，当不填时在 DIgSILENT 中选取为 0 号 owner。
7-18	A8, F4.0	节点名称（7-14），此节点名称直接设这为 DIgSILENT 节点 ElmTerm 项的 NAME，而基准电压（kV）（15-18）则直接设定为 DIgSILENT 的 Nominal Voltage（标准电压）。
19-20	A2	节点所在的分区名称，在区域功率交换中用于确定区域的分区，在系统合并和按分区分类输出时也有用。在转换到 DIgSILENT 的过程中作为网络数据的大框架，使所有节点，线路，变压器等元器件都转换在这项之下。
21-30	**2F5.0**	**以 MW 和 Mvar 表示的恒定负荷，无功正值为感性、负值为容性。这两项数据正是该节点负载的数据信息。**

如上表所示，第 21-30 列为描述恒定负荷所需要的有功、无功信息，在 DIgSILENT 中对应的是负载模型。

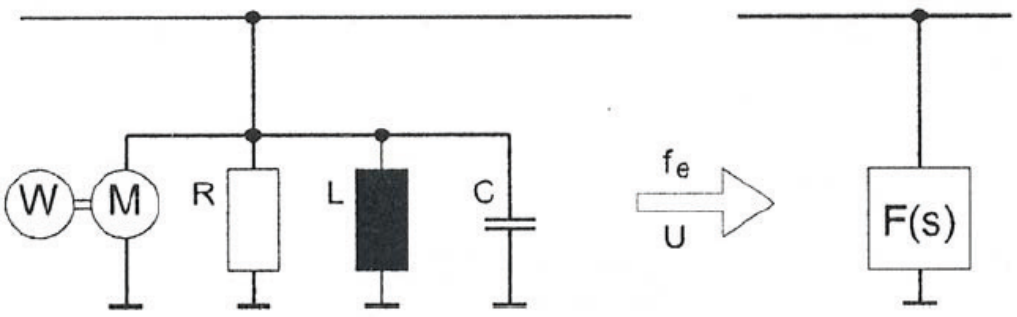

图 5.3 DIgSILENT 普通负载模型

DIgSILENT 中采用的负荷模型是一种动态负荷、静态负荷与用户自定义“特殊”负荷的综合，在 DIgSILENT 中负载模型描述如图 5.3.

通常情况下选择为 3 项平衡负载，切数据输入模式（Input Mode）选择为 Default 模式。在平衡负载情况之下，负载的潮流分析可不用专门将其专门设为单相或双相负载。其潮流模型如下：

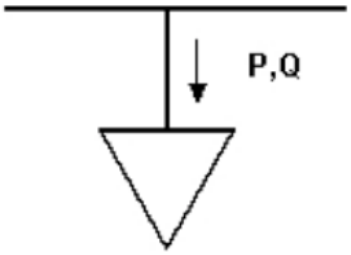

图 5.4 DIgSILENT 平衡负载的潮流模型

负荷电压依赖性可以如下述方程建模：

$$P = P_0 \left[aP * (\frac{v}{v_0})^{e\_ap} + bP * (\frac{v}{v_0})^{e\_bp} + cP * (\frac{v}{v_0})^{e\_cp} \right] \tag{5.1}$$

其中

$$1 - aP - bP = cP \tag{5.2}$$

$$Q = Q_0 \left[aP * (\frac{v}{Q} v_0)^{e\_aQ} + bQ * (\frac{v}{v_0})^{e\_bQ} + cQ * (\frac{v}{v_0})^{e\_cQ} \right] \tag{5.3}$$

其中

$$1 - aQ - bQ = cQ \tag{5.4}$$

指数	常量
0	功率
1	电流
2	电阻

表 5.4 为实现不同负载功效的指数选取

通过对上述公式的几项指数经行赋值，就可以对固有的负载建模。表 5.4 提供了分别实现恒功率，恒电流以及恒定电阻特性的负载模型所需要的指数参数。但是相应的每个系数（aP, bP, cP, aQ, bQ, cQ）则可以任意定义如图：

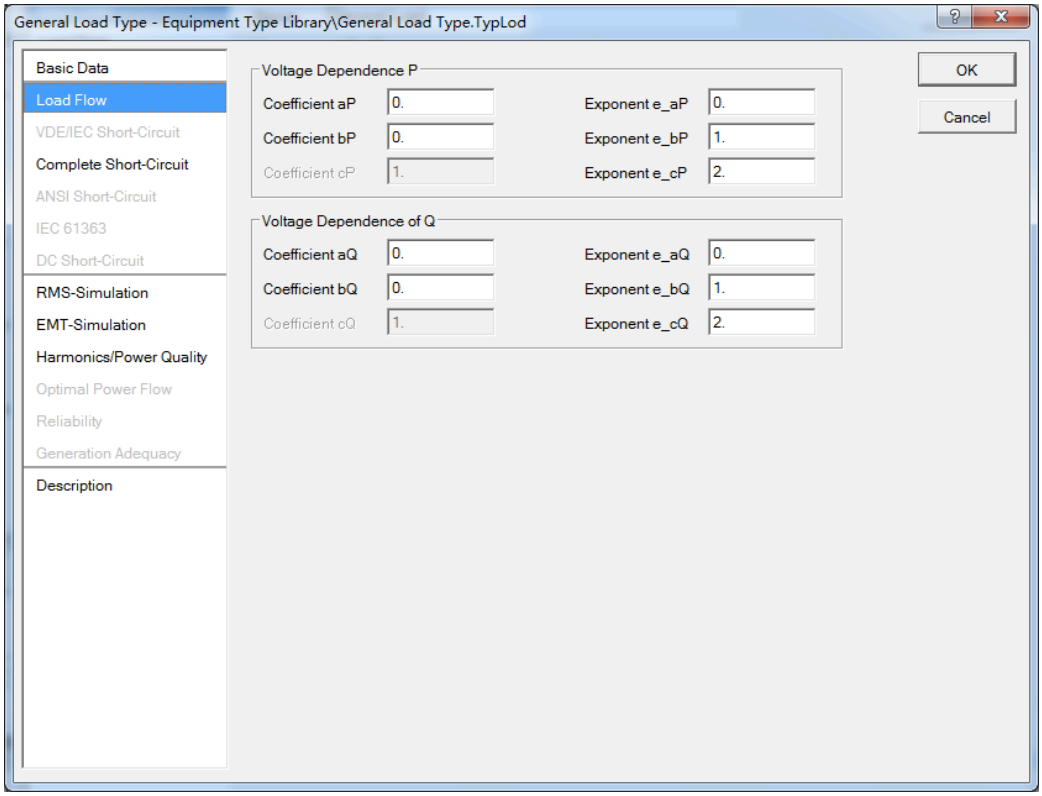

图 5.5　不同功能负载实现的系数表格图

如图 5.5 所示，以有功功率为例，图中的参数使得有功负载的最后方程形式为 $P = P_0 \left[aP * (\frac{v}{v_0})^0 + bP * (\frac{v}{v_0})^1 + cP * (\frac{v}{v_0})^2 \right]$，可见负载有功不仅与恒定功率 P_0 有关，还与负载电压平方有关，而且负载功率受电压控制，这正好与 $P = \frac{U^2}{R}$ 公式一致，所以当取 $aP = bP = aQ = bQ = 0, cP = cQ = 1$ 时可以表示为一恒阻抗负荷，即可以作为一个阻抗使用。

同理，当取 $aP = aQ = 1, bP = bQ = 0, cP = cQ = 0$ 时，则是恒功率负载。

通过负荷调节因子，负载可以单独被放大或者缩小如下：

$$P = scale * P_0 \tag{5.5}$$

$$Q = scale * Q_0 \tag{5.6}$$

$$P = scale * P_0 \left[aP * (\frac{v}{v_0})^{e\_ap} + bP * (\frac{v}{v_0})^{e\_bp} + cP * (\frac{v}{v_0})^{e\_cp} \right] \tag{5.7}$$

$$Q = scale * Q_0 \left[aP * (\frac{v}{Q} v_0)^{e\_aQ} + bQ * (\frac{v}{v_0})^{e\_bQ} + cQ * (\frac{v}{v_0})^{e\_cQ} \right] \tag{5.8}$$

公式 5.7 和 5.8 是考虑到有电压依赖的情况下的特性。

当考虑到馈线负荷调节过程中的负载，则在 DIgSILENT 的 *ElmLod* 数据卡中需要选定“*Adjusted by Load Scaling*”，这种情况下潮流计算时数据卡中本身的范围因素将不被使用而是被 feeder-scaling 因素给替换，如图 5.6 显示了负荷调节因子用以维持 feeder 设置的方式。

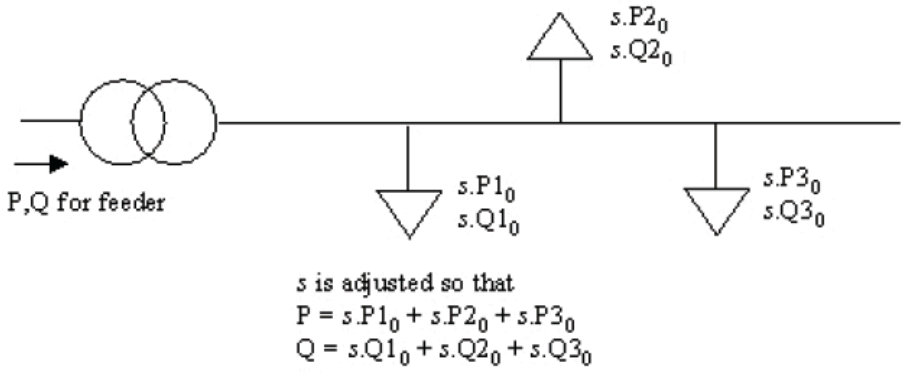

图 5.6 负荷调节因子用以维持 feeder 设置的方式

以上是 DIgSILENT 负载潮流特性的参数介绍，对于数据的转换由于 BPA 只给出了负载的有功和无功所以最主要的是将有功和无功分别准确的转化 DIgSILENT 有功无功的输入项 P_0, Q_0。对应的 DIgsILENT 数据位置如图 5.7 所示。

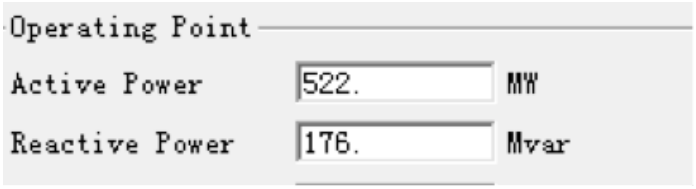

图 5.7 负载有功，无功的转换

5.2.2 DIgSILENT 电抗器模型介绍及数据转换

列	格式	内容
31-38	2F4.0	以 MW 和 Mvar 表示的、在基准电压下的节点并联导纳负荷, 无功: (+)= 容性,(-)= 感性。注意: 对于 BX 节点, 此项忽略

R-L 型电抗器：此种电抗器是电阻与电感串联构成的。为了定义电感以及电阻需要两种输入模式：

- 设计参数：参数通过额定无功功率，额定电流和品质因数确定。

- 布线参数：参数通过感抗和电阻确定。

式 5.9 给出了电感 L 与感抗的一般关系：

$$L_{rea} = \frac{X_{rea}}{2\pi f_{nom}} \cdot 1000 \tag{5.9}$$

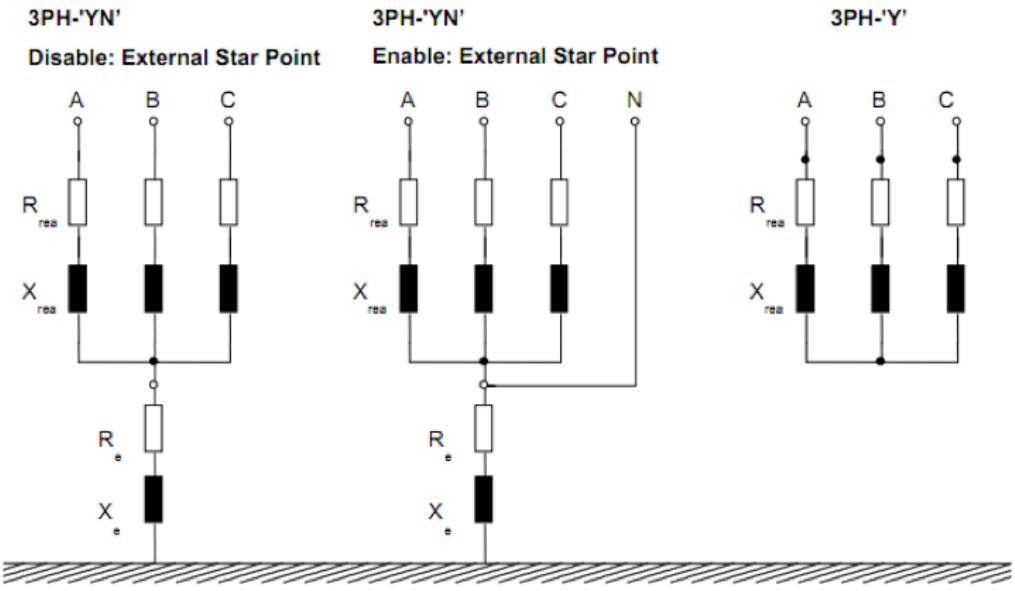

图 5.8 *3PH-'YN'，3PH-'Y'* 技术模型

如图 5.8 所示为 *3PH-'YN'，3PH-'Y'* 技术，如果内部接地阻抗星型点已经*'connected'*，可以将星型接法的接线点连接到中性线路（建立方式：*External Star Point*）来建立*'connected'*（如图 2-12 的二图情况）。对于中心点连接的情况，接地电阻和接地感抗

需要考虑（如图 2-12 的一图情况），对于*'disconnected'* 情况，接地电阻和感抗可以忽略。

$X_{rea}, R_{rea}, Q_{rea}$ 的关系如式 5.10 和 5.11 所示，其中 qf_{rea} 是额定频率下的品质因数。

$$X_{rea} = \frac{U_{nom}^2}{Q_{rea}} \tag{5.10}$$

$$R_{rea} = \frac{X_{nom}}{qf_{rea}} \tag{5.11}$$

电抗器无功功率与额定电流关系如下：

$$Q_{rea} = \frac{I_{rea} \cdot \sqrt{3} \cdot U_{nom}}{1000} \tag{5.12}$$

$$\Delta S = \Delta P + j\Delta Q = 3I^2(R + jX) = \frac{P^2 + Q^2}{U_j^2}(R + jX) \tag{5.13}$$

另一种电抗器是 C 型电抗器：此种电抗器是纯电容型的。有两种模式可以定义 C 型电容器：

- 设计参数：参数通过额定电容功率，额定电流。
- 布线参数：参数通过容抗和电容确定。

电容和电抗的关系如式 5.14 所示：

$$C_{rea} = \frac{B_{rea}}{2 \cdot \pi \cdot f_{rea}} \tag{5.14}$$

如图 5.9 所示，在 *ABC-'YN'*，*ABC-'Y'* 技术中，如果内部接地阻抗星型点已经*'connected'*，可以将星型接法的接线点连接到中性线路（建立方式：*External Star Point*）来建立*'connected'*（如图 2-13 的二图情况）。对于中心点连接的情况，接地电阻和接地感抗需要考虑（如图 2-13 的一图情况），对于*'disconnected'* 情况，接地电阻和感抗可以忽略。

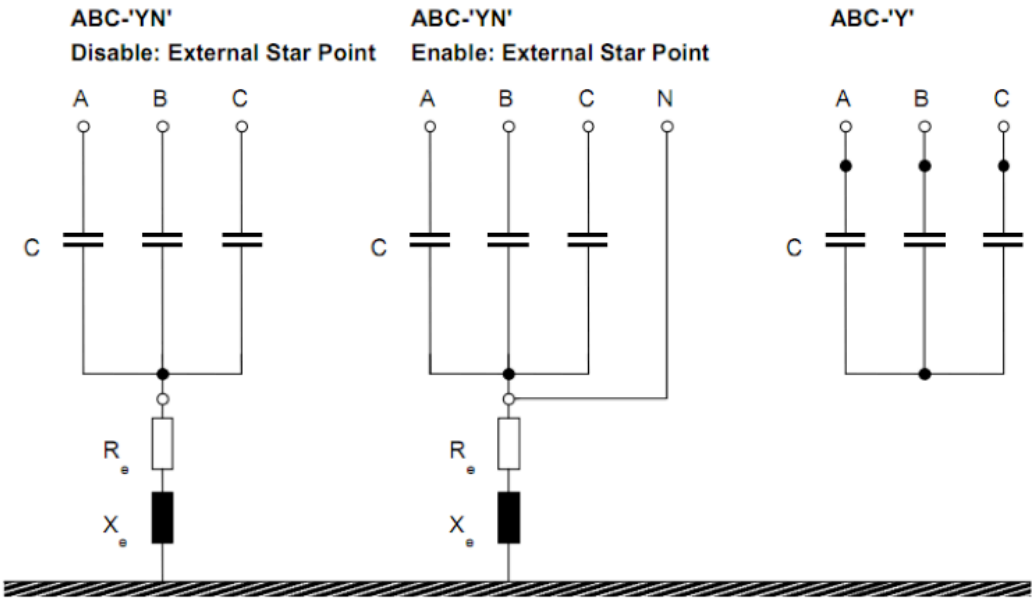

图 5.9 *ABC-'YN'*,*ABC-'Y'* 技术模型

B_{cap} 和 Q_{cap} 的关系以及 Q_{cap} 和 I_{cap} 的关系分别如式 5.15 和 5.16 所示：

$$B_{cap} = \frac{Q_{cap}}{U_{nom}^2} \cdot 10^6 \tag{5.15}$$

$$Q_{cap} = \frac{I_{cap} \cdot \sqrt{3} \cdot U_{nom}}{1000} \tag{5.16}$$

R-L-C 型电抗器：它由感抗，电阻，容抗串联构成。为了定义其感抗，电阻以及容抗，有两种输入模式：

- a）设计参数：参数通过额定有功功率（L-C），额定电流（L-C），电感等级或共振频率或者调谐顺序以及额定频率下的品质因数或者共振频率下的品质因数。

- 布线参数：参数通过感抗或者电感，容抗或者电容大小以及电阻确定。

容抗 B_{cap} 和电容 C_{cap} 的关系如式 5.17 所示。

$$C_{cap} = \frac{B_{cap}}{2 \cdot \pi \cdot f_{nom}} \tag{5.17}$$

感抗 X_{rea} 和电感 L_{rea} 的关系如式 5.18 所示。

$$L_{rea} = \frac{X_{rea}}{2 \cdot \pi \cdot f_{nom}} \cdot 1000 \tag{5.18}$$

电感等级，共振频率以及调谐顺序关系如下式所示，其中 P_{grad} 是电感度。

$$f_{res} = \frac{f_{nom}}{\sqrt{P_{grad}/100}} \tag{5.19}$$

$$n_{res} = \frac{f_{res}}{f_{nom}} \tag{5.20}$$

如式 5.21 所示为额定频率下的品质因数与共振频率下品质因数的关系。

$$g_{reaf_0} = g_{rea} \cdot n_{res} = g_{rea} \cdot \frac{f_{res}}{f_{nom}} \tag{5.21}$$

g_{rea} 为额定频率下的品质因数，g_{reaf_0} 为共振频率下的品质因数。

电容额定功率和额定无功功率，$L-CQ_{tot}$ 之间的关系如下：

$$Q_{cap} = Q_{tot} \cdot (1 - P_{grad}/100) = Q_{tot} \cdot \left(1 - \left(\frac{f_{nom}}{f_{res}}\right)^2\right) \tag{5.22}$$

Q_{cap} 为额定电容功率，Q_{tot} 为额定无功功率。

额定电感功率与额定无功功率，$L-CQ_{tot}$ 之间的关系如下：

$$Q_{cap} = Q_{tot} \cdot (100/P_{grad} - 1) = Q_{tot} \cdot (n^2 - 1) = Q_{tot} \cdot \left(\left(\frac{f_{nom}}{f_{res}}\right)^2 - 1\right) \tag{5.23}$$

共振频率 f_{res} 由下式给出：

$$f_{res} = \frac{1}{2\pi\sqrt{L_{rea} \cdot 10^{-3} \cdot C_{cap} \cdot 10^{-6}}} \tag{5.24}$$

电感，共振频率及电感之间的关系如下：

$$L_{rea} = \frac{10^3}{(2\pi f_{res}) \cdot C_{cap} \cdot 10^{-6}} \tag{5.25}$$

Q_{cap} 和 B_{cap} 之间的关系以及 $X_{rea}, R_{rea}, Q_{rea}$ 三者之间的关系如下：

$$B_{cap} = \frac{Q_{cap}}{U_{nom}^2} \cdot 10^6 \tag{5.26}$$

$$X_{rea} = \frac{U_{nom}^2}{Q_{rea}} \tag{5.27}$$

$$R_{rea} = \frac{X_{rea}}{qf_{rea}} \tag{5.28}$$

其中 qf_{rea} 是电阻设定为零的零的品质因数的品质因数。

以上就是对于 DigSILENT 中电抗器的介绍，但是上述的关键信息 qf_{rea} 在 B 卡中并没有给出，因此需要通过下述方法求出 qf_{rea}。

$$I_{rea} = \frac{Q_{[}rea]}{\sqrt{2} \cdot U_{nom}} \cdot 1000 \tag{5.29}$$

$$R_{rea} = \frac{P_{rea}}{I_{rea}^2} \cdot 1000 \tag{5.30}$$

$$qf_{rea} = \frac{X_{rea}}{R_{rea}} \tag{5.31}$$

而且由于 B 卡只提供了电抗器的无功及有功功率，无法判别其到底是 R-L 还是 R-L-C 模型，所以一般情况下只区分 B 卡的电抗器是 C 还是 R-L 型。（另外值得注意的是，软件中的电压都是线电压）

5.2.3 DIgSILENT 同步发电机模型介绍及数据转换

列	格式	内容
39-42	F4.0	P_{max}: 最大有功出力 (MW)
43-47	F5.0	P_{gen}: 实际有功出力 (MW)

48-52	F5.0	对于 PQ 节点 (即 B、BC、BT、BV 节点) 此项填所安排的无功出力值 QSCHED(Mvar); 对于其它节点此项填无功出力最大值 Q_{max}(Mvar): (+)= 容性,(-)= 感性
53-57	F5.0	无功出力最小值 Q_{min}(Mvar)
58-61	F4.3	所安排的电压值或者 V_{max}(标么值)
62-65	F4.3	所安排的 V_{min} 值 (标么值), 对于 Vθ(即 BS 型) 节点, 此项填角度值, 注意此时省缺的格式为 F4.1, 单位度

对于上面的 39-65 列，他们都实际上是 DIgSILENT 中 ElmSym 同步电机的数据，以下是对 DIgSILENT 同步电机模型的介绍。

通常情况下有两种典型的同步发电机：

- 轮转子发电机以及涡轮转子发电机

- 突轴转子发电机

轮转子发电机模型使用在转轴以接近 1500-3000 转每分钟旋转。这种类型发电机通常运用于热电厂以及核电厂。转速在 60 到 750 转每分钟的低转速的同步发电机通常使用突轴转子发电机的模式，这种发电机通常使用在柴油和水能发电站。

如图 5.10 和 5.11 所示是这两种模式发电机的截面图，同时也展现了 d 轴和 q 轴的方向。

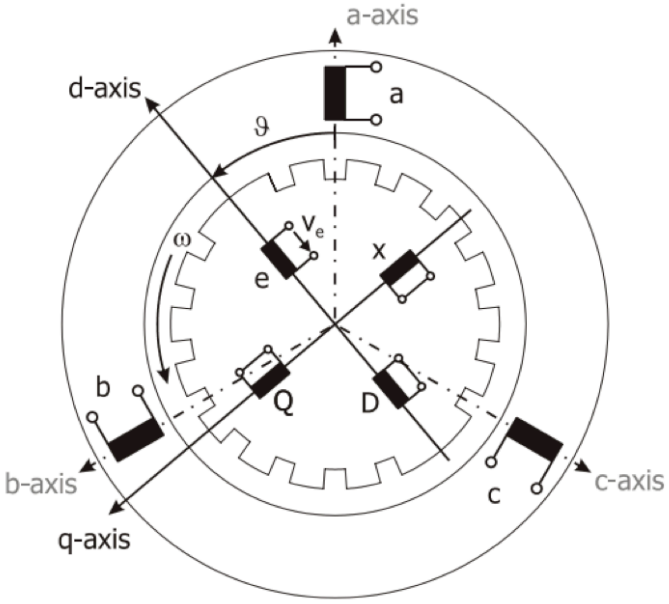

图 5.10 轮转子同步发电机截面图

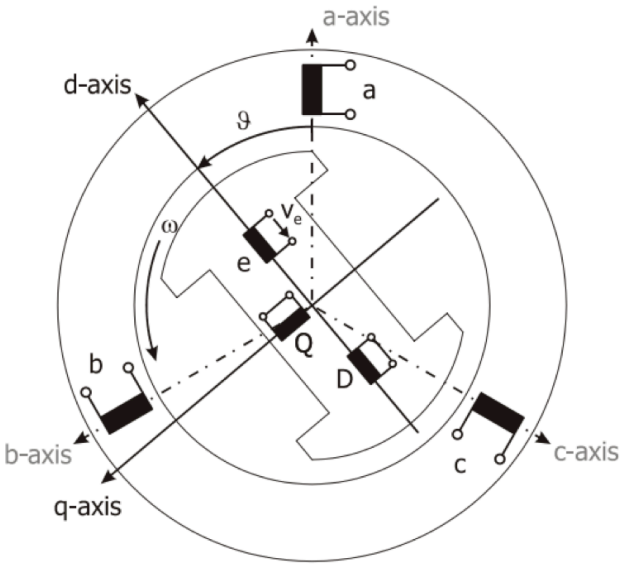

图 5.11 突轴转子同步发电机截面图

它们分别对应于同步电机的最大用功出力，实际有功出力，最小无功出力和最大无功出力。

DIgSILENT 中同步电机模型的建立与韩祯祥院士《电力系统分析》中介绍的一样，在此处不再赘述。建立电机特性所需要的参数如下：

DIgSILENT 参数	对应电机参数	单位	参数范围
tds	Td	$'s$	$x > 0$
tqs	Tq	$'s$	$x \geqslant 0$
$tdss$	Td	$''s$	$x > 0$
$tqss$	Tq	$''s$	$x > 0$
xd	xd	$p.u.$	$x > 0$
xds	xd	$'p.u.$	$x > 0$
$xdss$	xd	$''p.u.$	$x > 0$
xq	xq	$p.u.$	$x > 0$
xqs	xq	$'p.u.$	$x \geqslant 0$
$xqss$	xq	$''p.u.$	$x > 0$
$xdsat$	短路电流比	$p.u.$	$x \geqslant 0$
$xdsss$	xd'' 饱和值	$p.u.$	$x > 0$

表 5.7 同步电机建模阻抗参数

图 5.12 展示了互感间的磁链。线性直线代表着指示需要克服气隙磁阻的励磁电流的气隙。饱和程度来源于气隙线的开环特性。

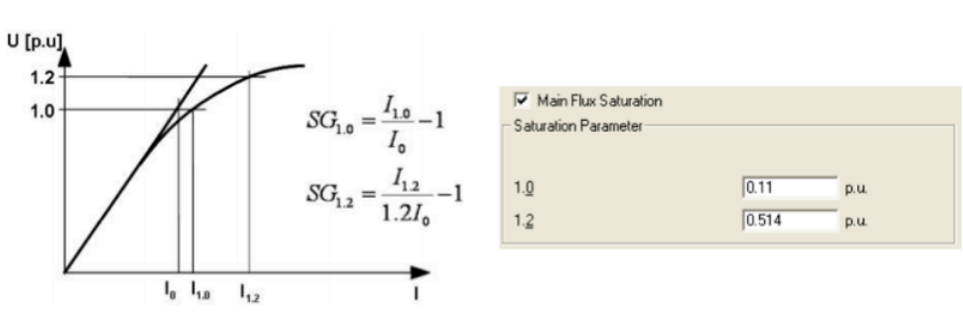

图 5.12 开环饱和

通过指定获得无负载情况下的 $1p.u$ 和 $1.2p.u$ 额定发电机电压的励磁电流 $I_{1.0pu}$ 和 $I_{1.2pu}$。这样可以计算参数 $s_{g1.0}(= C_{sat}(1.0pu))$ 和 $s_{g1.2}(= C_{sat}(1.2pu))$。

它们的计算如下：

$$s_{g1.0} = \frac{i_g(1.0p.u.)}{i_0} - 1 \tag{5.32}$$

$$s_{g1.2} = \frac{i_g(1.2p.u.)}{1.2i_0} - 1 \tag{5.33}$$

对于二次饱和函数：

$$A_g = \frac{1.2 - \sqrt{1.2\frac{s_{g1.2}}{s_{g1.0}}}}{1 - \sqrt{1.2\frac{s_{g1.2}}{s_{g1.0}}}} \tag{5.34}$$

$$B_g = \frac{s_{g1.0}}{(1 - A_g)^2} \tag{5.35}$$

以上数据主要用于暂态的计算，对于潮流计算则考虑下面几项转换数据：

BPA 的 B 卡 43-47 列 *Pgen* 项对应的就是发电机的实际有功输出及下图中 DIgSILENT 的 *Active Power* 一项。

图 5.13 实际有功转换

BPA 的 B 卡的 48 57 列分别是发电机无功出力的最大与最小值，它们分别于 DIgSILENT 的 *Reactive Power Limits* 中两项对应，如下图

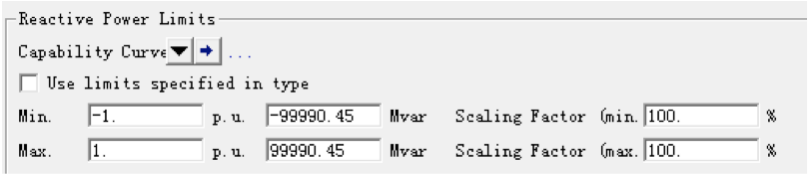

图 5.14 无功范围转换

注意 DPL 中只有标幺值才能填写，只要将 BPA 中的有名值数据转换成标幺值填进去后，DIgSILENT 会自动计算出有名值。上图中计算出来最小是 -1，最大是 1，那是因为改发电机的视在功率是 99990.45。

对于发电机的基准功率 BPA 没有直接给出，在转换过程中这一项应该取 BPA 的基准功率。

同理 B 卡的 39-42 项则是定义发电机的最大有功出力，他对应转换的是 DIgSILENT 的 *Active Power*：*Operational Limits Max* 一项，如下图。

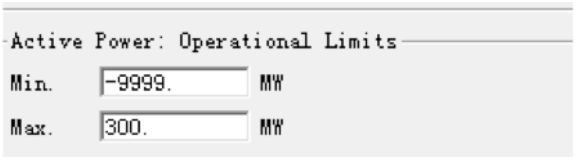

图 5.15 有功限制

上图中 *Active Power*：*Operational Limits* 中 *Min* 一项由于 BPA 没有给出，一般填为 -9999，这并不会影响潮流运算。

BPA 的 B 卡 58-61 项则是定义了发电机的输出电压，此数据对应 DIgSILENT 的 *Dispatch* 下的 *Voltage* 一项，如下图。

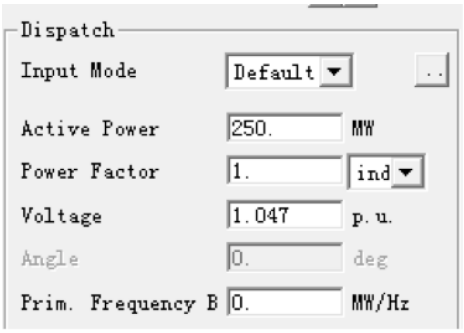

图 5.16 发电机运行电压的转换

但是需要注意，BPA 中此项数据是有名值而 DIgSILENT 中则是标幺值，所以需要在程序转换过程中对其数据类型进行转换。

以上即为 DIgSILENT 中同步发电机模型的介绍以及 BPA 转换为 DIgSILENT 数据的思路。

列	格式	内容
66-77	A8,F4.0	对于 BG 和 BX 节点有用, 填写其所要控制的节点名 (66- 73) 和基准电压 (74-77)。要控制的电压值填在被控节点记录卡 58-61 列
78-80	F3.0	发电机在对远方节点作电压控制时, 提供的无功功率的百分数

5.3 L 卡，E 卡

该卡用于模拟对称的 π 型支路。

在模拟母线之间连接线或者母线的常闭分段断路器时，可使用电抗值 X=0.0001（标幺值）的一条线路。要注意的是一般情况下支路 X 之最小值取为 0.0001。

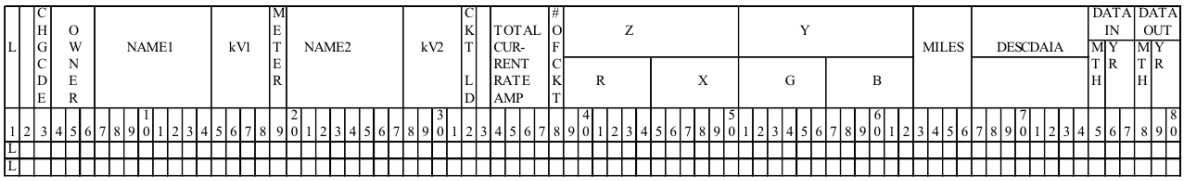

图 5.17 L 卡数据

列	格式	内容
1	A1	卡片类型－ L
2	A1	空白
3	A1	修改码
4-6	A3	所有者代码
7-18	A8, F4.0	节点名 1（7-14）和基准电压（kV）（15-18）
19	I1	区域联络线测点标记（在作区域交换功率控制时有用） 填 1 －表示在节点 1 测量 填 2 －表示在节点 2 测量 空白－允许程序按如下原则处理 1）在线路两端节点中，节点所有者与线路所有者不同的节点为测点； 2）当线路两端节点所有者相同时，节点 1 为测量点
20-31	A8, F4.0	节点名 2（20-27）和基准电压（kV）（28-31）
32	A1	并联线路的回路标志，即回路号。
34-37	F4.0	线路额定电流值，供检验线路过负荷和（$N-1$）开断校核过负荷用，单位安培

38	I1	并联线路数目，仅作信息用
39-50	2F6.5	在系统基准电压和基准容量下的阻抗标么值：$R(39-44)$,$X(45-50)$
51-62	2F6.5	线路对地导纳标么值（对称支路只需填一侧值）：$G/2(51-56)$,$B/2(57-62)$。
63-66	F4.1	线路（或段）的长度（英里），可不填
67-74	A8	线路说明数据（字符数字型），可不填
75-77	A1，I2	投运日期：月—75 列（1、2、3、4、5、6、7、8、9、0、N、D）；年号—（76-77）。可不填
78-80	A1，I2	停运日期，可不填

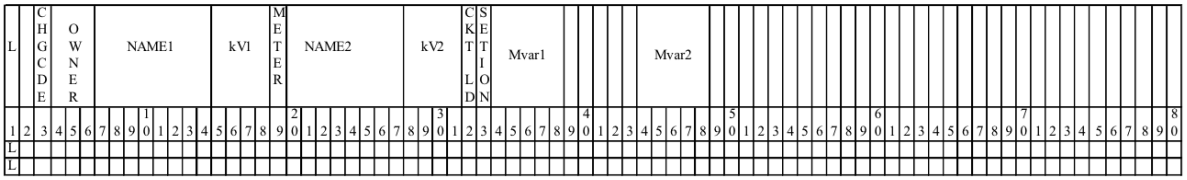

图 5.18 E 卡数据

列	格式	内容
1	A1	卡片类型－E
2	A1	空白
3	A1	修改码
4-6	A3	所有者代码
7-18	A8, F4.0	节点名 1（7-14）和基准电压（kV）（15-18）
19	I1	在区域联络线功率控制时用的联络线测点标记，其填写规则见 L 卡第 19 列的说明
20-31	A8, F4.0	节点名 2（20-27）和基准电压（kV）（28-31）
32	A1	并联线路的回路标志，即回路号。
34-37	F4.0	线路额定电流值，供检验线路过负荷和（$N-1$）开断校核过负荷用，单位安培
38	I1	并联线路数目，仅作信息用，可不填
39-50	2F6.5	在系统基准电压和基准容量下的阻抗标么值：$R(39-44)$,$X(45-50)$
51-62	2F6.5	线路对地导纳标么值（对称支路只需填一侧值）：$G/2(51-56)$,$B/2(57-62)$。
63-74	2F6.5	在线路节点 2 端的对地导纳标么值：$G2\text{-}(63-68)$,$B2\text{-}(69-74)$
75-77	A1，I2	投运日期：月—75 列（1、2、3、4、5、6、7、8、9、0、N、D）；年号—（76-77）。可不填
78-80	A1，I2	停运日期，可不填

BPA 的 L 卡数据对应 DIgSILENT 里的数据类型有四种：输电线路（$*.ElmLne$），电容器（$*.ElmScap$），理想变压器的阻抗（$*.ElmZpu$）。

这三种数据类型的区分方式：若线路两端的电压值不一致，即 I 端电压与 J 端电压不相等，则说明不是普通线路类型，需要将此元件建立为理想变压器的阻抗

(∗.$ElmZpu$)类型。在线路电压一致的前提下,若线路的电抗值(X)小于零,此时将元件建立为电容器模型(∗.$ElmScap$)。若前面两个条件皆不符合,说明是普通的输电线路,则建立输电线路模型(∗.$ElmLne$)。以下对 DIgSILENT 的这几种线路模型进行介绍。

5.3.1 DIgSILENT 线路模型介绍及数据转换

5.3.1.1 架空线路模型

在 DIgSILENT 中,架空线路共有两种模型:

1. 集总参数 这种模型用于短传输线或者低频率下相对较长的线路中有一定的可接受精度

2. 分布式参数 由于考虑了传输线中的电波方程,这种模型比集总参数模型更加精确,它用于长线以及高频线路模型中

下面就对这两种参数做进一步介绍。

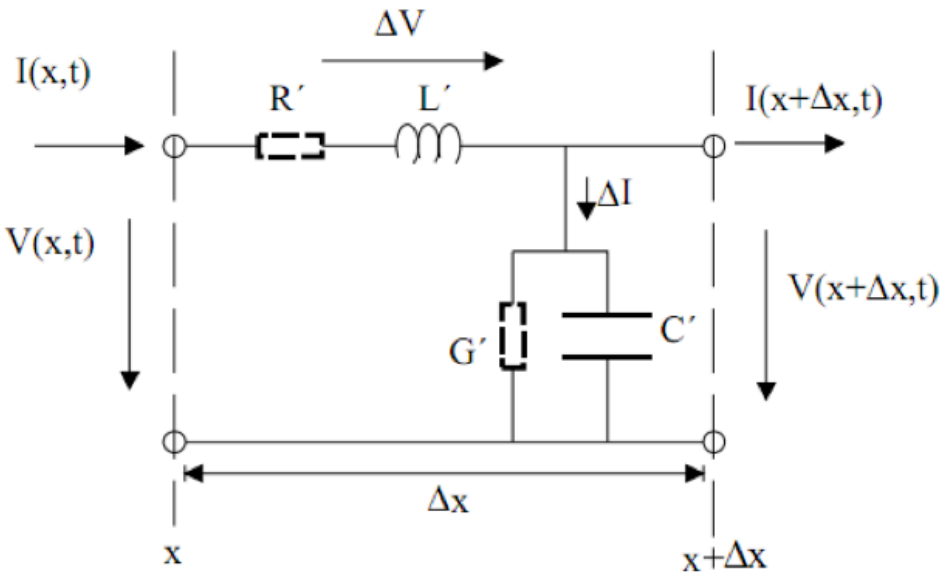

图 5.19 DIgSILENT 线路模型

依靠这个模型可以推导出下面的分布式和集总式两种简化模型，而推导过程需要的参数就是上图中的 R', Z', B', G'。

如图 5.20 所示，线路模型的参数实际上都是依赖于此模型经行推导的。

其中：

$$Z_\pi = Z_c \cdot sinh\gamma \cdot l = Z' \cdot l \cdot \frac{sinh\gamma \cdot l}{\gamma \cdot l} \tag{5.36}$$

$$Y_\pi = \frac{cosh\gamma \cdot l - 1}{Z_c \cdot sinh\gamma \cdot l} = \frac{1}{2} \cdot \gamma' \cdot l \cdot \frac{thg\left(\frac{\gamma \cdot l}{2}\right)}{\frac{\gamma \cdot l}{2}} \tag{5.37}$$

γ 是传播系数 $\gamma = \sqrt{Z' \cdot \gamma'}$。

Z' 和 Y' 是单位长度等值阻抗和导纳。

图 5.20 中的 Z_π 和 Y_π 是频率依赖参数。

使用分布参数模型需要在 *ElmLne* 的 *basic page* 中选定“*Distributed Parameter*”，如下图：

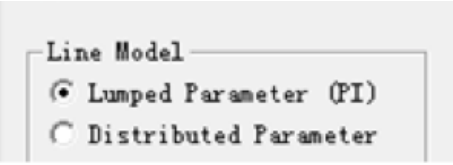

图 5.20　分布参数模型的选择

集总式分布参数模型表达式如下：

$$Z_\pi = B = Z' \cdot l = R' \cdot l + j\omega \cdot L' \cdot l \tag{5.38}$$

$$Y_\pi = \frac{A-1}{B} = \frac{1 + \frac{1}{2} \cdot Z' \cdot Y' \cdot l^2}{Z' \cdot l} = \frac{1}{2} \cdot Y' \cdot l = \frac{1}{2} \cdot (G' \cdot l + j\omega \cdot C' \cdot l) \tag{5.39}$$

电路模型图如下图。与分布式参数模型不同，这个模型有离散 R,L,G 以及 C。因此此模型不仅适用于稳定状态计算也可以用于暂态仿真计算。

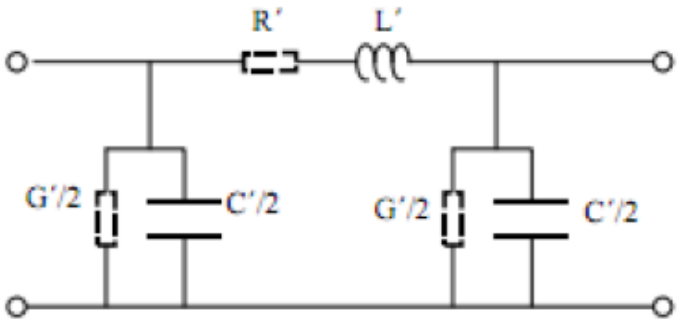

图 5.21 传输线集总模型

使用集总参数模型需要在 *ElmLne* 的 *basic page* 中选定“*Lumped Parameter*”如下图：

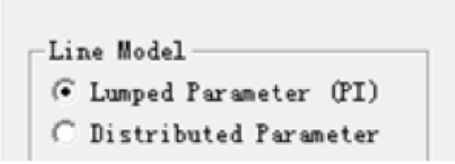

图 5.22 集总参数模型的选择

模型的精准性依赖于因子 $f \cdot l$。对于架空线在小于 250km 以及电力系统频率下，等效是很有效的，其产生的误差可以忽略。

对于 BPA 到 DIgSILENT 数据的转换过程中，BPA 提供的是的 π 模型参数 X,R,B,G，所以需要逆推导图 5.19 中的。但是以 DIgSILENT 的 DPL 提供的运算功能，实现这个逆推导的过程基本不可行，而且由于 BPA 中还存在有不对称电路，此时是无法等效为 π 模型电路的，因此我换了一种方法处理这个问题。

下图中的部分实际上可以看为一个电容与电阻的并联，这正好与 DIgSILENT 的 SHUNT 元件的 C 型电抗相似，所以可以用两个 C 型电抗去代替 $Y\pi$，而线路只需要知道其单位阻抗 Z'，线路的 B', G' 直接填为 0。下面我会证明 Z' 可以使用 BPA 中 X,R 求出的阻抗去替换。

证明：

$$Z = \frac{sinh\gamma l}{\gamma l} Z' l \tag{5.40}$$

由于 l 一般取 1，所以上式又可写为：

$$Z = \frac{sinh\gamma}{\gamma} Z'l \tag{5.41}$$

$$\gamma = \sqrt{Z' \cdot Y'}$$

由于计算处理过程 B', G' 实际上是给 B', G' 赋予一个无穷趋于 0 的值，所以可以看为 $\gamma \to 0$。

由级数展开：

$$sinh\gamma l = \gamma l + \frac{(\gamma l)^3}{3!} + \frac{(\gamma l)^5}{5!} + \frac{(\gamma l)^7}{7!} + ... \tag{5.43}$$

$$\lim_{\gamma \to 0} \frac{sinh\gamma}{\gamma} = \lim_{\gamma \to 0} \frac{\gamma + \frac{(\gamma)^3}{3!} + \frac{(\gamma)^5}{5!} + \frac{(\gamma)^7}{7!} + ...}{\gamma} = 1 \tag{5.44}$$

所以可得

$$Z = Z'$$

这样，可以直接用 BPA 求出的 Z 去替换 DIgSILENT 线路参数中的 Z'。

DIgSILENT 中 C 型电抗的模型如图 5.23：

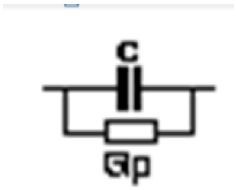

图 5.23 DIgSILENT 中 C 型电抗的模型

而现在知道 BPA 中的 $Y\pi$ 参数，而 DIgSILENT 中 C 型电抗的模型参数则是有其电容和电阻上的有功与无功推导的，所以这里需要经行一个逆推导，过程如下：

$$Q_c = YB \cdot U_B^2 \tag{5.46}$$

$$P_r = YG \cdot U_B^2 \tag{5.47}$$

通过上述模型的建立就可以完成 DIgSILENT 对 BPA 中对称电路与不对称电路的转换建模了。

DIgSILENT 中电容器模型如图 5.24 所示。

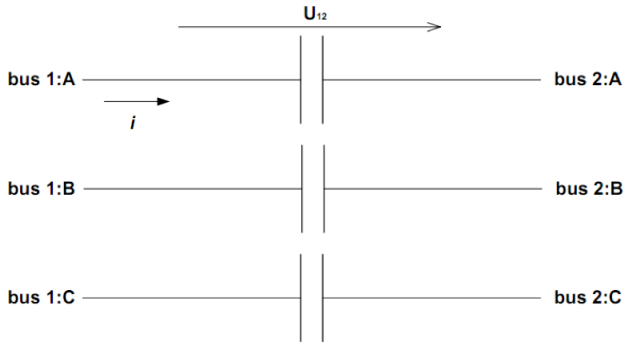

图 5.24 DIgSILENT 中电容器模型

交流模型中

$$I = j\omega_{\pi} CU \tag{5.48}$$

直流模型中，由于纯电容是隔直流的，所以模型可以看为一无穷大电阻，即

$$I = 0 \tag{5.49}$$

变压器的阻抗模型中，包含理想变压器的感抗模型。

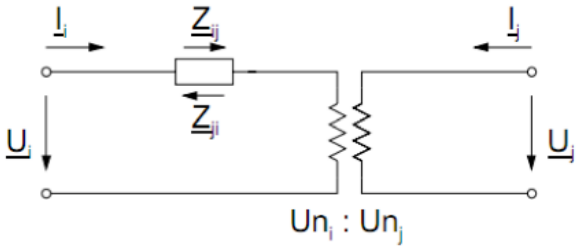

图 5.25 公共阻抗正，负，零序绝对值模型

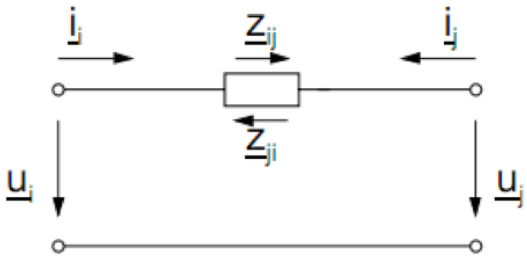

图 5.26 公共阻抗正，负，零序标幺值模型

此模型在潮流分析需要注意的参数如下表：

DIgSILENT 参数	对应电机参数	单位
Sn	额定功率	MVA
nphase	相数（三相或一相模型）	1 或 3
iequalz	等阻抗 $z_{ij} = z_{ji}$	使能/不使能
r_pu, x_pu	$'i - j'$ 正序阻抗	$p.u.$
r_pu_ji, x_pu_ji	$'j - i'$ 正序阻抗	$p.u.$
r0_pu, x0_pu	$'i - j'$ 零序阻抗	$'p.u.$
r0_pu_ji, x0_pu_ji	$'j - i'$ 零序阻抗	$''p.u.$
iz2eqz1	阻抗 $z_2 = z_1$	使能/不使能
r2_pu, x2_pu	$'i - j'$ 负序阻抗	$'p.u.$
r2_pu_ji, x2_pu_ji	$'j - i'$ 负序阻抗	$''p.u.$

表 5.11 公共阻抗输入参数

5.3.1.2 线路数据转换

线路的名称是以 BPA 线路两端节点名命名。

比如在 039BPA 数据中，BUS-10 与 BUS-11 之间的线路则命名为 *lne_BUS-11_BUS-12_1*，其中最后一位数字 1 是用于区别是否这两个节点有并联母线的，转换如下图：

图 5.27 线路数据转换

正如前面对 BPA 的 L 卡介绍中提到的第 19 项数据 METER 用于判断基准节点。在转换过程中我也是通过此项选择基准节点的，而选择的思想就如 L 卡中对 METER 功能介绍的方法一样。

对于线路的长度则参照 BPA 中数据转换，如果 BPA 数据没填，则 DIgSILENT 中使用默认的 1km，转换如下图：

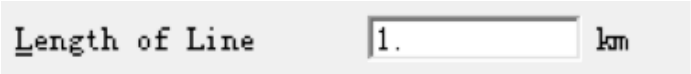

图 5.28 线路长度

在建立好输电线路模型（*.*ElmLne*）以后，由于 DIgSILENT 对这种数据的储存用了两个数据块，所以需要建立它的 Type 文件，输电线路类型（*.*TypLne*），这两个文件同时储存一条输电线路的数据。

在 *TypLne* 中额定电流就是指定参考节点的电压，额定电流就是 L 卡中额定电流一项数据卡数据。

在数据转换过程中，需要注意的是 DIgSILENT 采用的是有名值，BPA 采用的是标幺值。需要进行转换。有名值与标幺值之间的转换公式为（其中有上标的为有名值）：

$$R = R' \cdot l \cdot \frac{100}{U_R^2}, X = X' \cdot l \cdot \frac{100}{U_N^2}, B = B' \cdot l \cdot \frac{U_N^2}{100} \tag{5.50}$$

由于正序网络结构的各元件参数与正常运行的等值网络相同。因此只需要将元件转换好的有名电阻直接转换到上述正负序项中即可。

5.3.2 L+ 卡

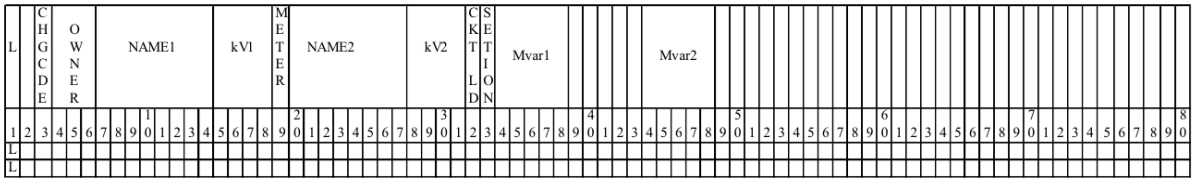

图 5.29 L+ 卡数据

列	格式	内容
1	A1	卡片类型－ L
2	A1	空白
3	A1	修改码
4-6	A3	所有者代码

7-18	A8, F4.0	节点名 1（7-14）和基准电压（kV）（15-18）
20-31	A8, F4.0	节点名 2（20-27）和基准电压（kV）（28-31）
32	A1	并联线路的回路标志，即回路号。
34-38	F5.0	线路前侧高抗容量（Mvar，填正值）
44-48	F5.0	线路后侧高抗容量（Mvar，填正值）

我国电力系统正在向大容量、远距离、超（特）高的方向发展。超高压输电压系统由于其电压等级提高，可传输更大的容量，更远的距离，但是线路的电容效应限制了传输容量，降低了系统静态和动态稳性，增加了工频过电压幅值，所以超高压输电线路往装设并联高压电抗器（下文简称高抗）解决无功平衡和过电压问题。

而 L+ 卡的目的实际上就是为了模拟超高电压下的电抗器，起到抵消电容效应的作用。而 DIgSILENT 电抗器在前文有详细介绍，这里就不赘述了。

5.3.3 T 卡

致　谢

附　录

本科生毕业论文(设计)任务书

一、题目：_____

二、指导教师对毕业论文(设计)的进度安排及任务要求：

起讫日期 200　年　月　日至 200　年　月　日

指导教师(签名)_____　职称 _____

三、系或研究所审核意见：

负责人(签名)_____

年　月　日

毕 业 论 文(设计)考 核

一、指导教师对毕业论文(设计)的评语：

指导教师(签名) _____

年　月　日

二、答辩小组对毕业论文(设计)的答辩评语及总评成绩：

成绩比例	文献综述占 **(10%)**	开题报告占 **(20%)**	外文翻译占 **(10%)**	毕业论文 **(**设计**)** 质量及答辩占 **(60%)**	总评成绩
分值					

答辩小组负责人(签名) _____

年　月　日