# JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA

## DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING


A PRACTICAL WORK BOOK
OF
COMPUTER ORGANIZATION & ARCHITECTURE LAB
(18B17CI414)

SUBMITTED
TO
DR. RAHUL PACHAURI

NAME OF STUDENT: TANISHQ AGARWAL ENRL NO. 211B326

CLASS: BTECH-3RD YEAR BATCH: B9

BRANCH: CSE SESSION: 2023-2024

# ***INDEX***

| S. NO. | AIM OF THE EXPERIMENT | DATE OF SUBMISSION | SIGNATURE | REMARKS |
|---|---|---|---|---|
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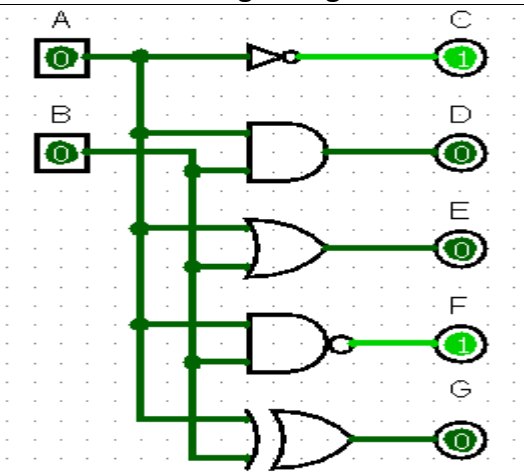
# EXPERIMENT#1

**Aim: Designing of basic digital circuits using logic gates.**

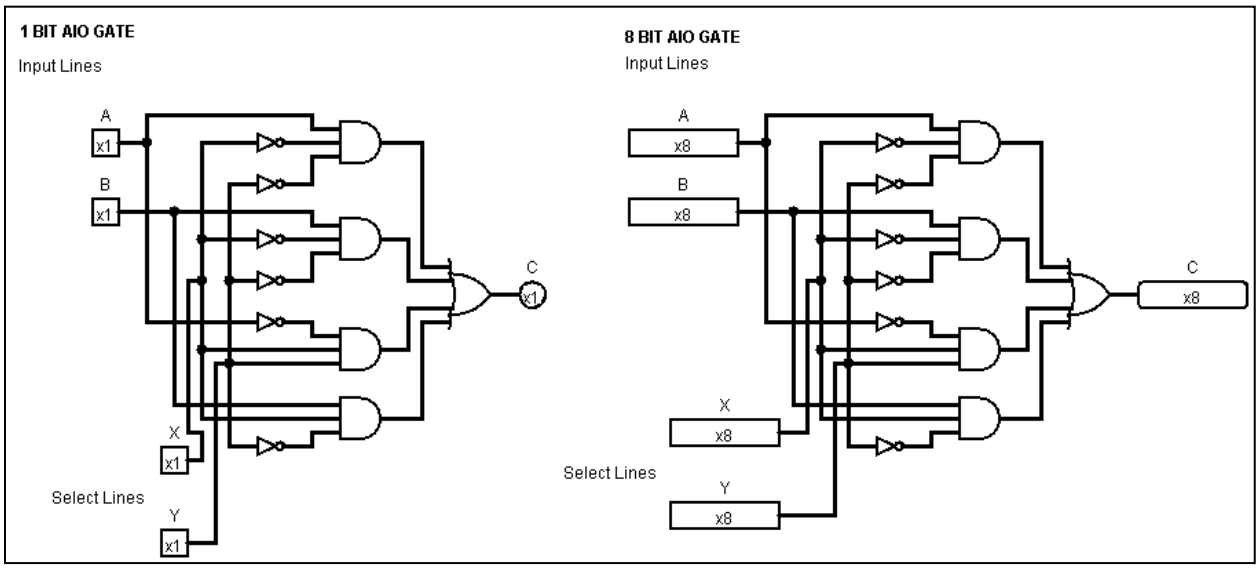
**Exercise#1:** Design two inputs and five outputs All-in-One logic gate circuit shown in Fig.1 using Logisim simulator with (i) data width 1 (ii) data width 4.

| Boolean Expressions | Logic Diagram |
|---|---|
| C = not A<br>D = A.B<br>E = A+B<br>F = ~(A.B)<br>G = A⊕B |  |
| **Truth Table or Karnaugh (K) Map** | |

| A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |

**Exercise#2:** Design two inputs and one output All-in-One logic gate diagram shown in Fig.2 using Logisim simulator with (i) data width 1 (ii) data width 8.

**Logic Diagram :**



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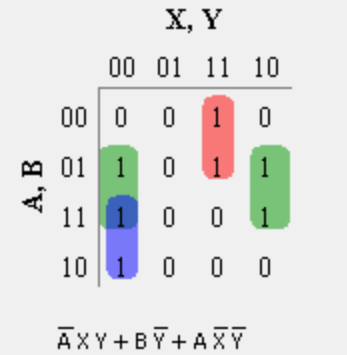
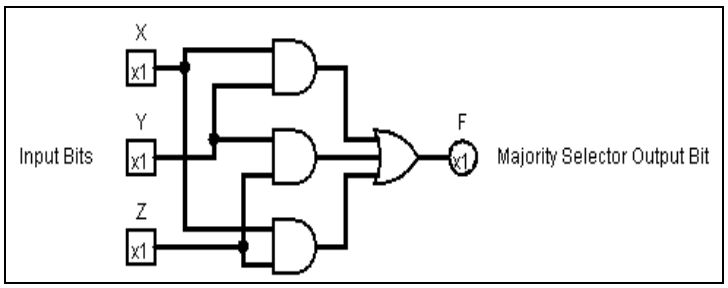
**Boolean expression and K-Map :**

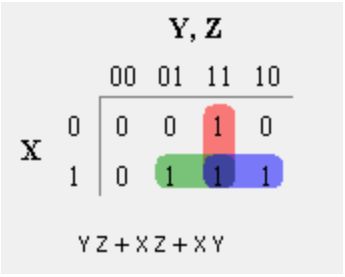



**Exercise#3:** Design a three-input majority detector combinational digital circuit using Logisim simulator which shows output equal to 1 if the input variables have more 1's than 0's, the output is 0 otherwise.

**Logic Diagram:**

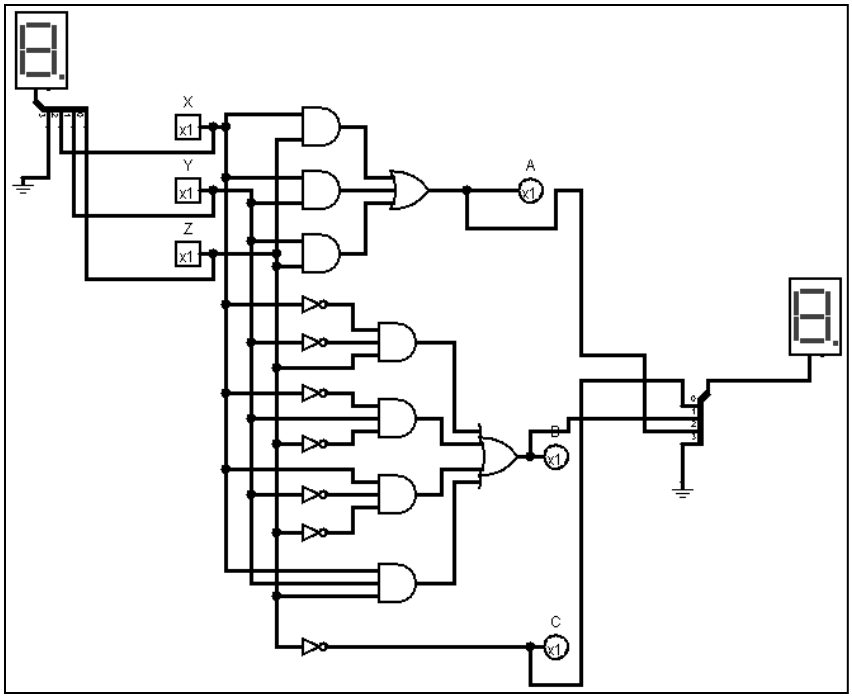



**Boolean Expression and K-Map:**




**Exercise#4:** Design a combinational circuit with three inputs and three outputs. When the input is 0, 1, 2, or 3, the output is one greater than the input and when the input is 4, 5, 6, or 7, the output is one less than the input. Display the input and output digits using Hex digit display with splitter.

**Logic Diagram:**




**Boolean Expressions & Truth Table :**

| X | Y | Z | A | B | C |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

A= Y Z + X Z + X Y

B= ~X ~Y Z + ~X Y ~Z + X ~Y ~Z + X Y Z

C= ~Z

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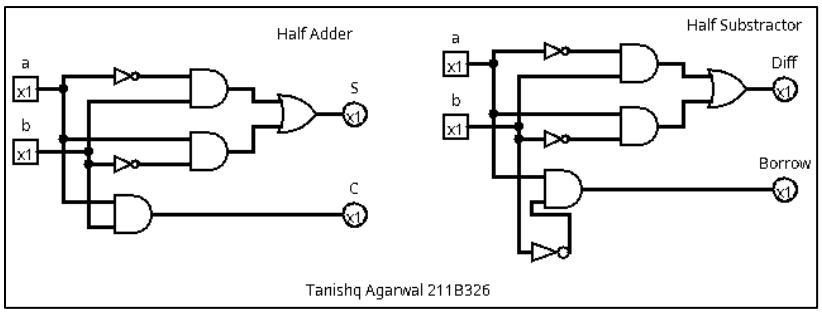
# EXPERIMENT#2

**Aim: Design of binary adders and subtractors.**

**Exercise#1:** Design half adder and half subtractor shown in Fig. 1 and Fig. 2 using logisim simulator.

**Logic Diagram :**




**Boolean expression and Truth Table :**

S: ~a b + a ~b

C: a b

Diff: ~a b + a ~b

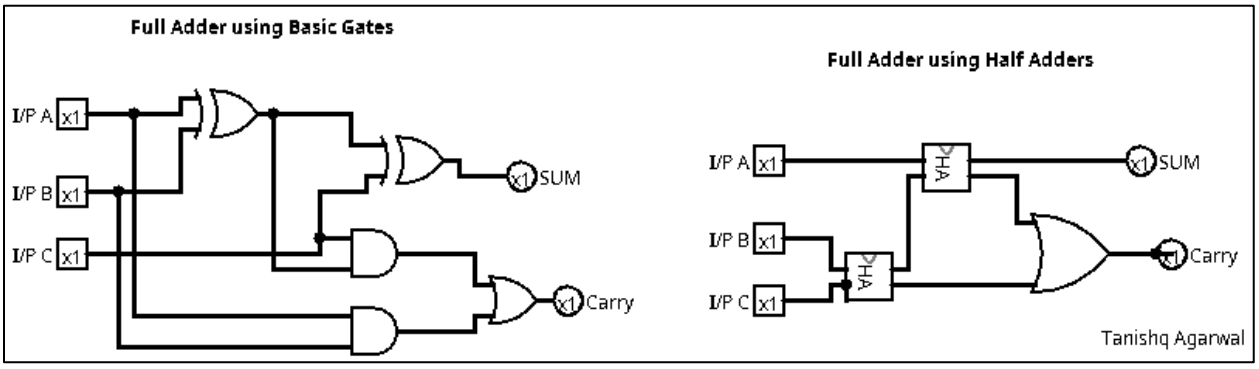
Borrow: a ~b

| a | b | Diff | Borrow |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

| a | b | S | C |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**Exercise#2:** Design full adder using (i) basic gates only (ii) by adding half adder as sub circuit using logisim.

**Logic Diagram :**




**Boolean expressions and K-Maps :**

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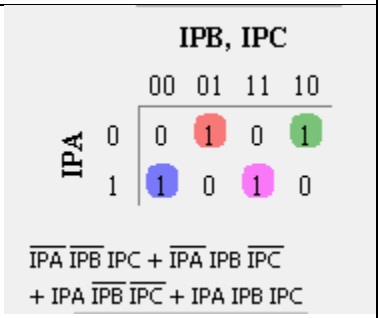
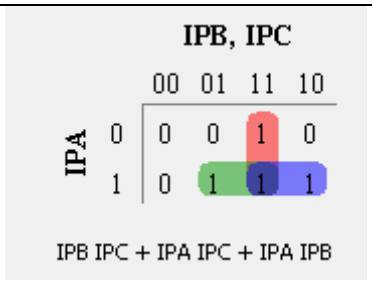
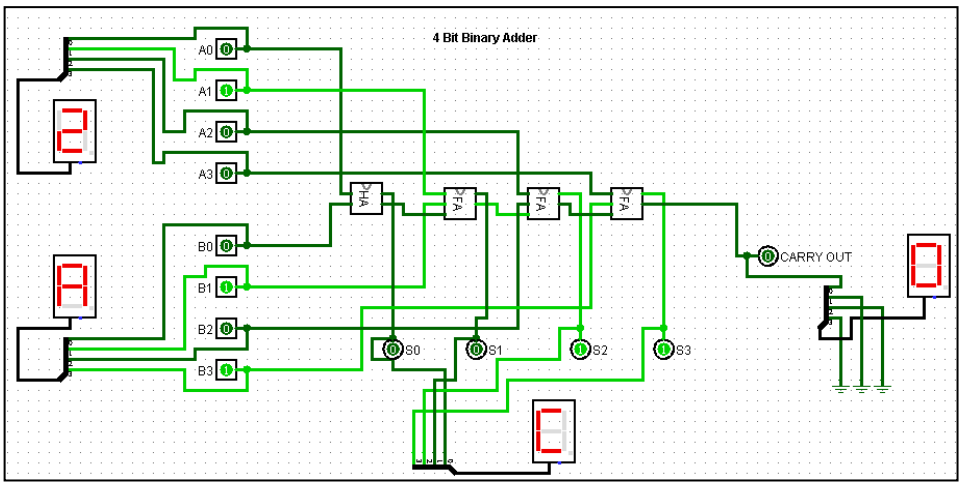
| Sum | Carry |
|---|---|
|  |  |

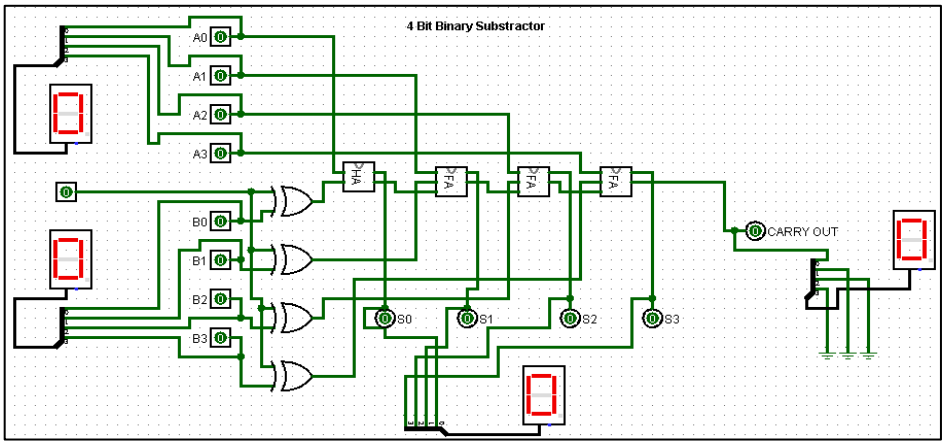
**Exercise#3:** Design 4-bit binary adder using one half adder and 3-full adders as shown in Fig. 5. Use half adder and full adders as sub circuits in the design. Display both the input digits; output digit and end carry digit using Hex digit display with splitter available in logisim simulator.

**Logic Diagram:**




**Exercise#4:** Design 4-bit binary adder-subtractor using full adders as shown in Fig. 6. Use full adders as sub-circuits in the design. Display both the input digits, initial carry digit; output digit, and end carry digit usingHex digit display with splitter available in logisim simulator.

**Logic Diagram:**



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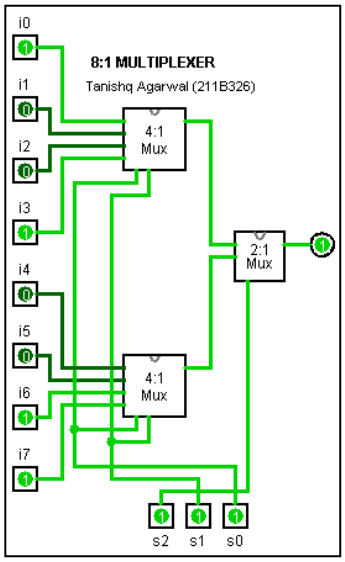
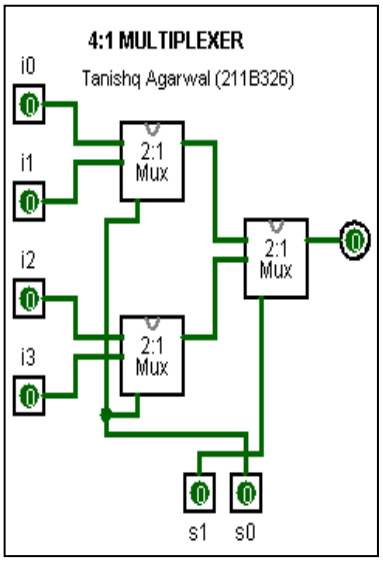
# EXPERIMENT#3

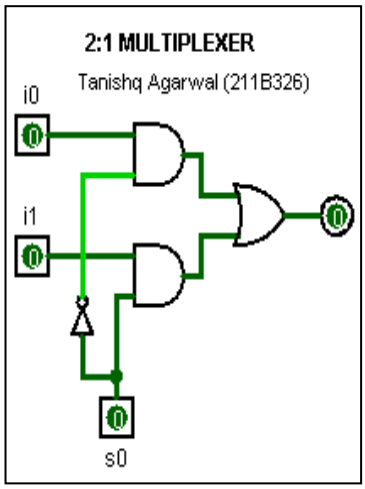
**Aim: Design of basic combinational logic circuits. (MUX, DEMUX,ENCODER, DECODER)**

**Exercise#1:** Design an 8:1 multiplexer using two 4:1 multiplexers and one 2:1 multiplexer (shown in Fig.1) Use both types of multiplexers as sub circuits in the design.

**Logic Diagram & SubCircuits:**

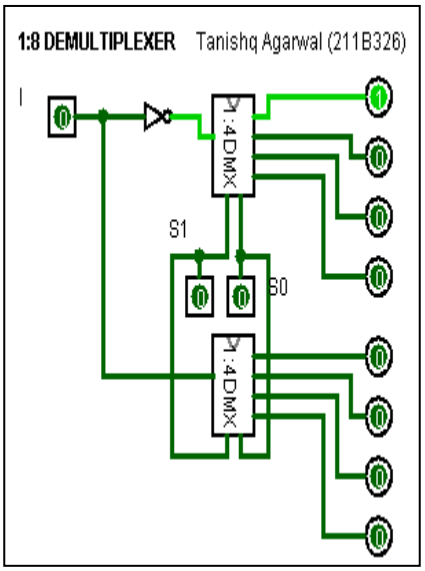


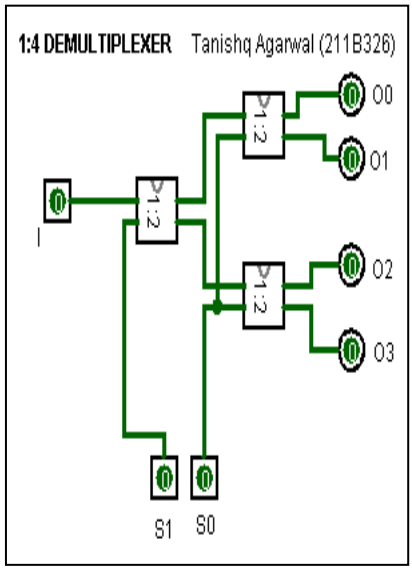



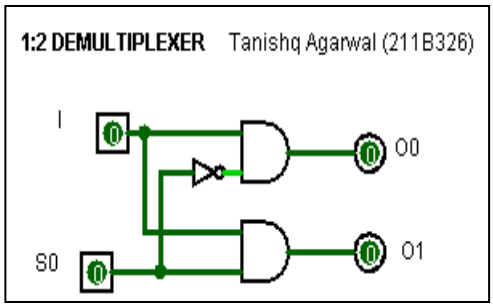




**Exercise#2:** Design a 1:8 de-multiplexer using three 1:4 de-multiplexers. Use 1:4 de-multiplexers as sub circuits in the design.

**Logic Diagram & SubCircuits:**



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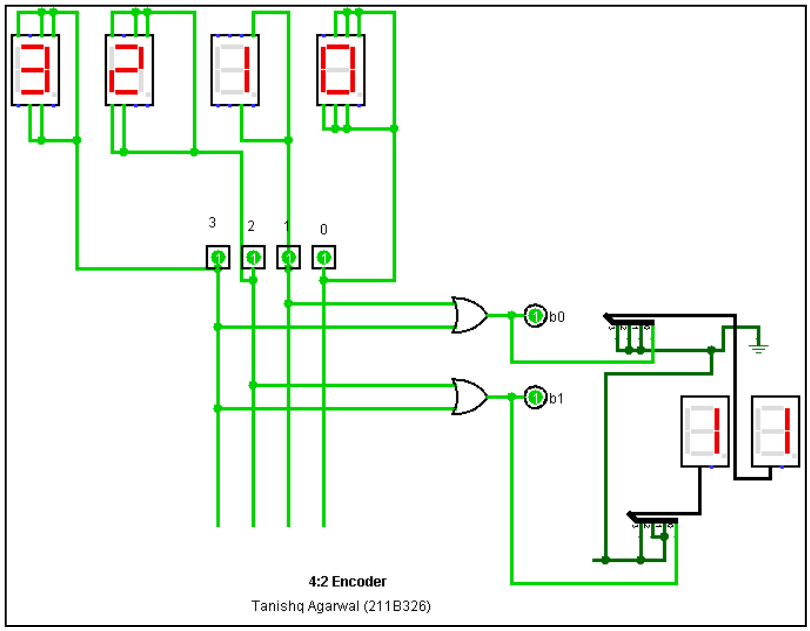
**Exercise#3:** Design quad to binary (4-to-2) encoder using logic gates. Display all four input digits using seven segment displays and two output binary bits using hex displays available in logisim simulator

**Logic Diagram:**




**Exercise#4:** Design 3-to-8 decoder using two 2-to-4 decoders with enable (E) line shown in Fig. 2. Use 2:4 decoder as sub circuits in the design.

**Logic Diagram & SubCircuits:**