

Full\_Adder\_design

Proj-003.1

By Isaias M Ramirez



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imramirez.engineering@gmail.com

Chapel Hill NC

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# Introduction

Any good computer needs an adder. This documentation describes my design for a full adder.

# Full Adder Design

This design is derived from [1] as it relates to the equations used in the implementation. An abstract version of the HDL is shown in Fig. 1.

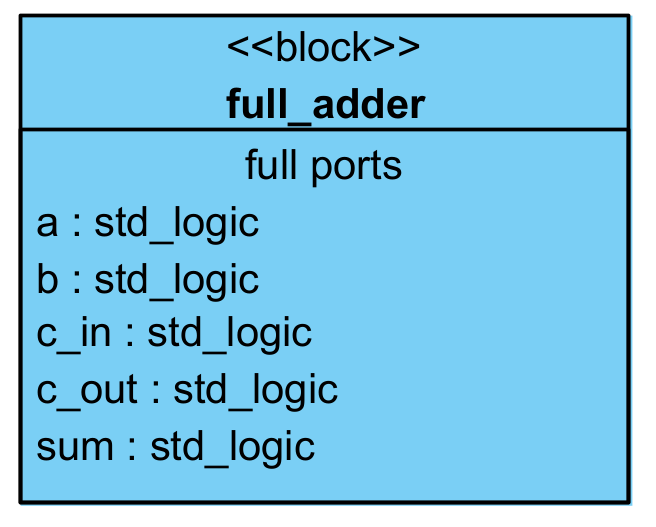


Figure Full Adder Block

As can be seen from Fig. 1, the full adder has 5 ports all of type std\_logic. For this design each can be treated as a single bit. The equations that describe the behavior of these ports are illustrated with Equation 1 and 2 below.

The truth table is left out of this documentation and the VHDL implementation can be found within the repository where this documentation is stored.

# Sources

[1] S. L. Harris and D. Harris, *Digital Design and Computer Architecture, RISC-V Edition*. Morgan Kaufmann, 2021.