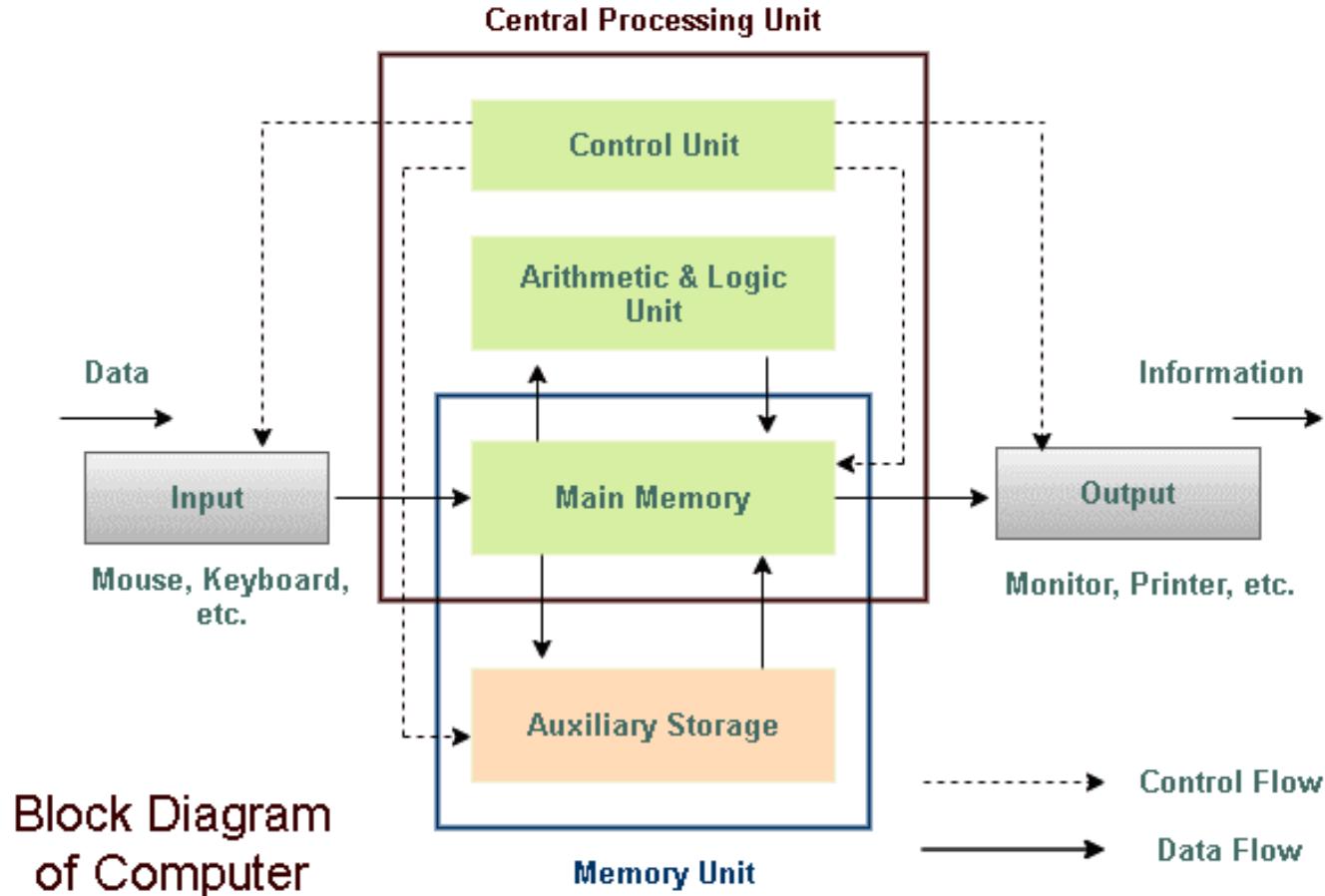


Fundamental of Microprocessor

UNIT – 1

Block Diagram of Computer



8085 Microprocessor Architecture





Definition

- ▶ Microprocessor is
 - Multipurpose
 - Programmable
 - Clock driven
 - Register based
 - Electronic device
 - Reads binary instructions from storage device called memory
 - Accepts data as binary input
 - Processes data according to instructions
 - Provides results as output

- ▶ Microprocessor is multipurpose, programmable, Clock driven, Register based Electronic device that reads binary instructions from storage device called memory and accepts data as binary input, processes data according to instructions provides results as output.

- ▶ Microprocessor operates in binary 0 or 1
- ▶ Each processor recognizes and processes a group of bits called word
- ▶ Microprocessor are classified according to their **word length** such as 8 bits, 16 bits etc

Applications

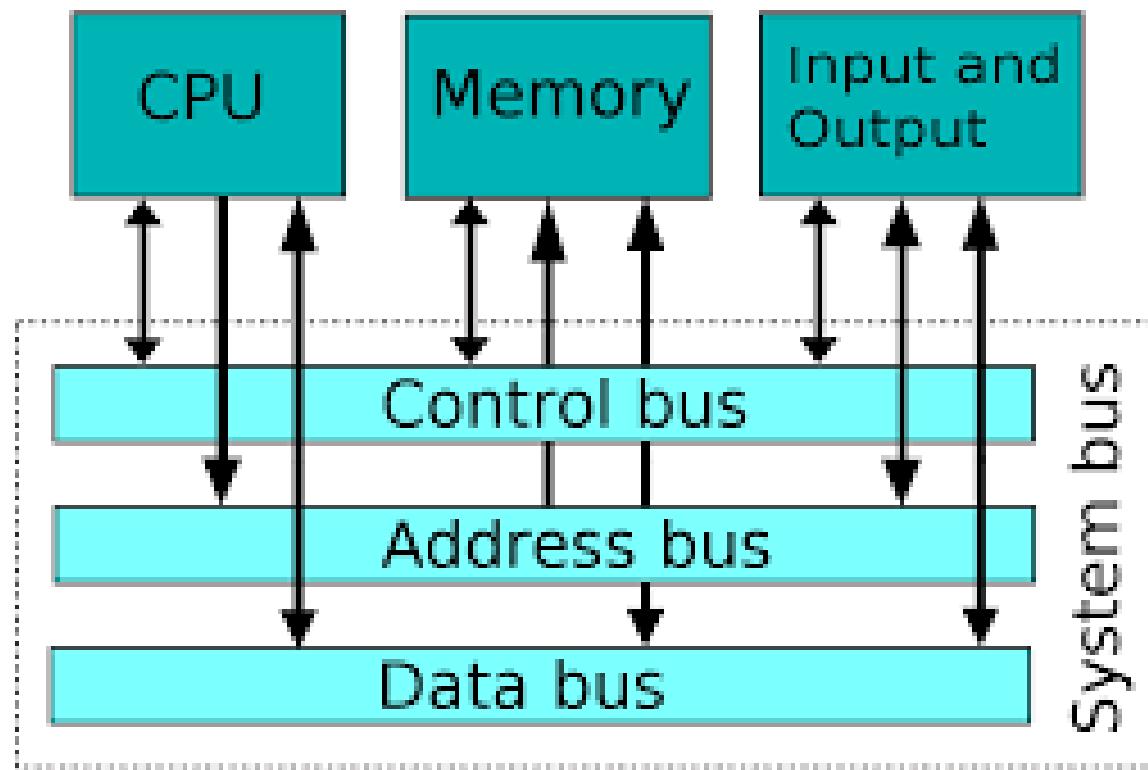
- ▶ Microcontrollers
- ▶ Measurement and testing equipment
 - Blood group analyzers
 - X-ray analyzer
 - Signal generators
- ▶ Washing machine
- ▶ Microwave oven
- ▶ Scientific and engineering research
- ▶ Industry
- ▶ Security system: smart cameras, CCTV, smart door
- ▶ Traffic light control

Advantage of microprocessor

- ▶ Computational speed is high
- ▶ Intelligence has been brought to system
- ▶ Automation of industrial process and office automation
- ▶ Flexible
- ▶ Compact in size
- ▶ Maintenance is easier

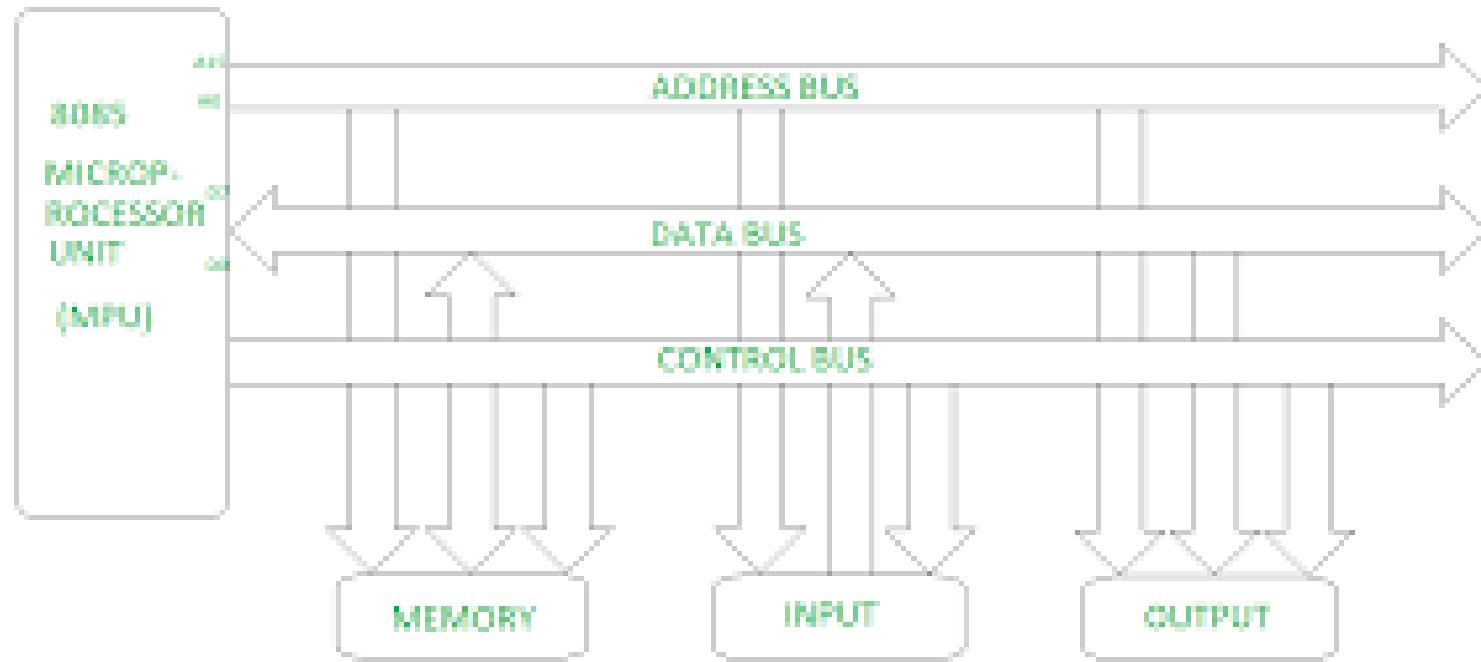
System Bus

- ▶ A bus is a subsystem that is used to **connect computer component** and transfer data between them.
- ▶ A **system bus** is single computer bus that connects the major components of a computer system combining the functions of a **Data bus** to carry information, an **Address bus** to determine where it should be sent and **Control bus** to determine its operation.



- ▶ Design of the system bus **varies from system to system** and can be specific to particular computer design.
- ▶ System bus **characteristics** are dependent on need of the processor, the speed, and the wordlength of data and instructions.
- ▶ **Size of bus** :- known as width, determines how much data can be transferred at a time and indicates the number of available wires.
- ▶ 32 bit bus refers 32 parallel wires that can simultaneously transfer 32 bits.

Microprocessor with bus organization



Bus organization system of 8085 Microprocessor

Microprocessor with Bus organization

- ▶ Bus is a group of conducting wires which carries information.
- ▶ All peripherals are connected to microprocessor through bus.
- ▶ Three types of buses
- ▶ Address bus
- ▶ Control Bus
- ▶ Data Bus

▶ Address Bus

- It is group of conducting wires which carries address only.
- Address bus is unidirectional because data flow in one direction, from microprocessor to memory or from microprocessor to input /output devices.
- Length of address bus of 8085 is 16 bit or 4 hexa digits, from 0000 H to FFFF H.
- It can address 65536 different memory locations

▶ Data Bus

- Group of conducting wires which carries data only.
- Data bus is bidirectional because data flow both way from microprocessor to memory or I/O devices and from memory or Input/output devices to microprocessor.
- 8085 have 8 bit data bus means 2 hexadecimal ranging from 00 H to FF H.
- ***Write operation:*** processor will put data to be written in the data bus.
- ***Read operation:*** memory controller will put data into data bus from specific memory location.

- ▶ Width of data bus is directly related to largest number that the bus can carry, such as 8 bit can carry from 0 to 255.

▶ Control bus

- It is group of conducting wires which is used to generate timing and control signals to all associated peripherals.
- Some control signals are:
 - Memory Read
 - Memory write
 - I/O read
 - I/O write
 - Opcode fetch

Microprocessor Architecture and operations

- ▶ Microprocessor is programmable digital device, designed with registers, flip-flops and timing elements.
- ▶ The microprocessor has set of instructions designed internally to manipulate data and communicate with peripherals.
- ▶ The process of data manipulation and communication is determined by the logic design of the microprocessor, called architecture.

- ▶ Microprocessor can be programmed to perform functions on given data by selecting necessary instructions from its set.
- ▶ These instructions are given to the microprocessor by writing them into memory.
- ▶ Writing or entering instructions and data are given by input device.

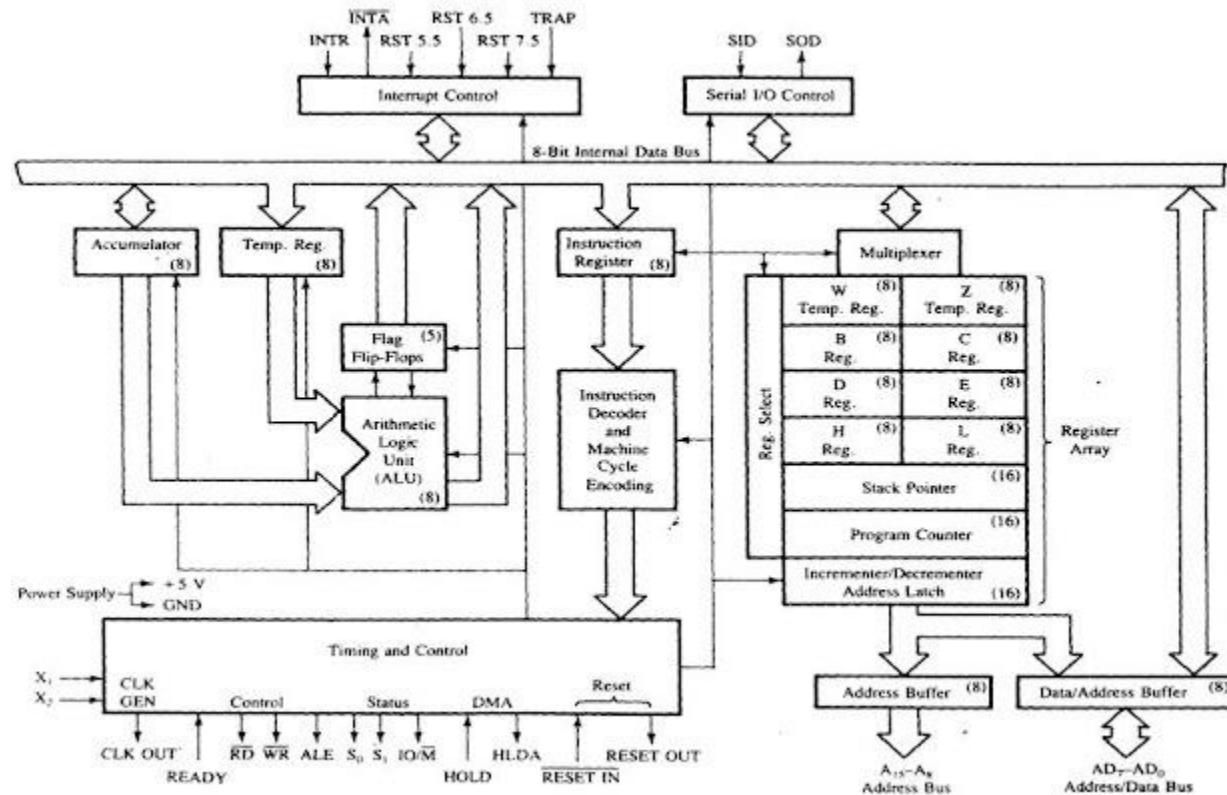
- ▶ The microprocessor reads or transfer one instructions at time, matches it with its instructions set and performs data manipulation indicated by instructions.
- ▶ The result can be store into the memory or send to output device.

- ▶ Microprocessor can respond to external signals.
- ▶ It can be interrupted ,reset, or asked to wait to synchronize with slower peripherals.

8085

- ▶ 8085 is complete 8 bit parallel CPU.
- ▶ Main components are:-
 - Array of registers
 - ALU
 - Encoder/Decoder
 - Timing and control circuits
- ▶ All components are linked by internal data bus.

8085 microprocessor functional block diagram



▶ ALU

- Performs computing functions
- Includes accumulator, temporary registers, arithmetic and logic circuits and five flags.
- Temporary registers hold data during Arithmetic and logic operations.
- Result is stored in accumulator.
- Flag (flip-flops) are set or reset according to the result of operations.

- ▶ **Accumulator(register A):**
 - 8 bit register which is part of ALU
 - stores 8 bit data
 - 8085 is accumulator based microprocessor
 - When data is read from input port it is moved to accumulator and when data is send to output port, it must be first place in accumulator.

- ▶ **Temporary Register(W and Z)**
 - 8 bit registers not accessible to the programmer
 - During program execution 8085 places the data for short period
- ▶ **Instruction Register(IR)**
 - 8 bit register not accessible to the programmer
 - It receive the operation code from internal data bus and passes to the instruction decoder which decodes so that microprocessor knows which type of operation to perform.

▶ Registers Array

- General Purpose Registers
 - B, C, D, E, H & L (8 bit registers)
 - Can be used singly
 - Or can be used as 16 bit register pairs
 - BC, DE, HL
 - H & L can be used as a data pointer (holds memory address)
- Data can be directly added or transferred from one to another.
- Contain can be incremented or decremented or combined logically with the contain of the accumulator
-

- ▶ **Stack Pointer**
 - It is 16 bit register known as memory pointer
 - It points to the memory location in RAM called stack
 - The beginning of the stack is defined by loading a 16 bit address in the stack pointer.
- ▶ **Program Counter**
 - This is a register that is used to control the sequencing of the execution of instructions.
 - This register always holds the address of the next instruction.
 - PC is incremented by 1 to point next memory location.

▶ Flag register

- Registers consists of five flip-flops, each holding the status of different states separately.
- Known as flag registers or flags
- 8085 set or reset one or more flags.
- S (sign flag), Z (zero flag), AC (auxillary carry flag), P (parity flag) & CY (carry flag)

- **Carry(CY)**- If the last operation generates a carry, its status will be 1 otherwise 0
 - It can handle the carry or borrow from one word to another
- **Zero(Z)**-If the result of last operation is zero, Its status will be 1 otherwise 0
 - It is often used in loop control and in searching for particular data value
- **Sign(S)**-If the MSB of the result of the last operation is 1(negative) then its status will be 1 otherwise 0
- **Parity (P)**-If the result of last operation has even number of 1's its status will be 1 otherwise 0
- **Auxillary Carry(AC)**- If the last operation generates carry from the lower half word its status will be 1 otherwise 0. Used for performing BCD arithmetic.

D7

D6

D5

D4

D3

D2

D1

D0

S

Z

X

AC

X

P

X

CY

- ▶ **Timing and control unit**
 - This unit synchronizes all the microprocessor operations with the clock and generates necessary control signals for communications between microprocessor and peripherals.
- ▶ **Interrupt controls**
 - The various interrupt control signals are used to interrupt microprocessor.
 - INTR, RST 5.5, RST 6.5, RST 7.5 and TRAP
- ▶ **Serial I/O control**
 - Two serial I/O control SID and SOD are used for serial data transmission.

Microprocessor operations

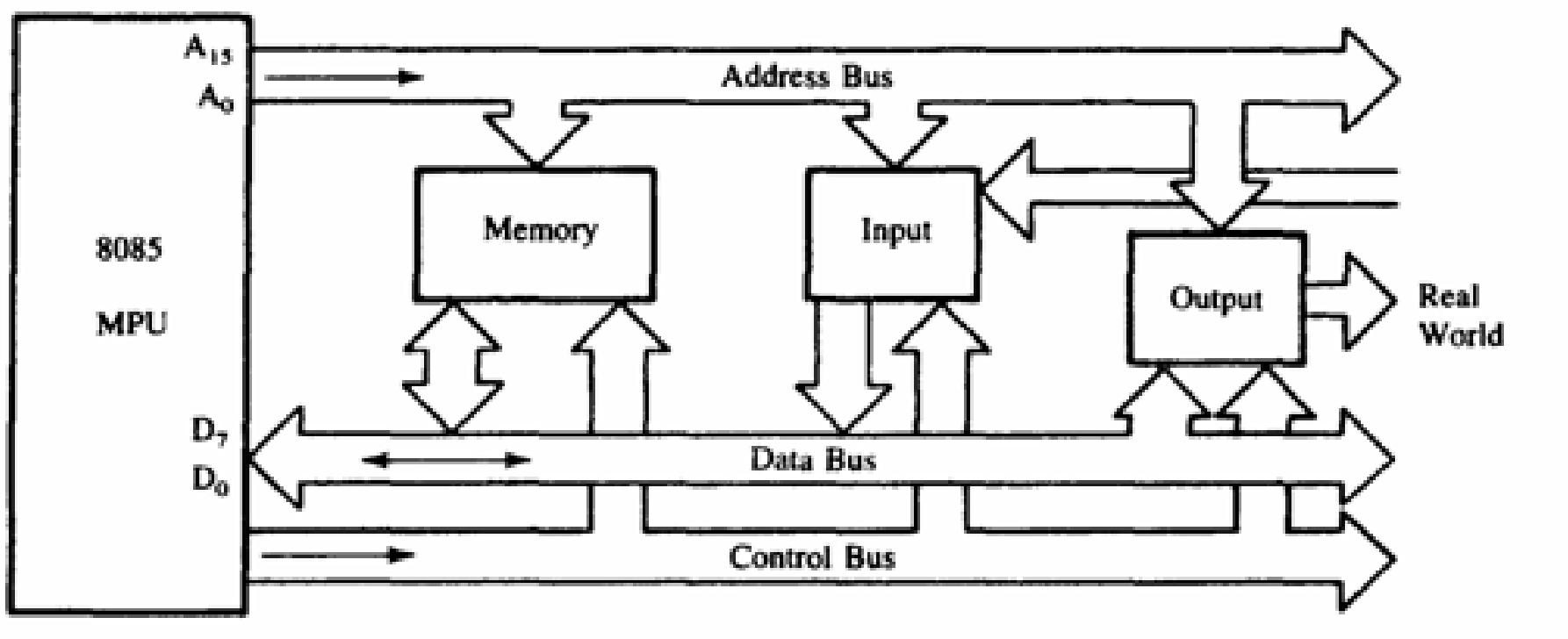
- ▶ Functions performed by microprocessor can be classified in three general category.
 - Microprocessor initiated operations
 - Internal operations
 - Peripheral(or externally initiated) operations

Microprocessor initiated operations

- ▶ Microprocessor performs primarily four operations:
 - **Memory Read**:–Read data or instructions from memory
 - **Memory Write**:–Write data or instructions to memory
 - **I/O read** :–Accepts data from input devices
 - **I/O write**:–sends data to output devices
- ▶ To communicate with a peripherals or a memory microprocessor needs to perform following steps:-
 - Step1 identify the peripherals or memory location with its address
 - Step2 transfer binary information(data or instructions)
 - Step 3 provide timing or synchronization signals

- ▶ 8085 perform this using set of communications lines called buses.
- ▶ Address bus, data bus and control bus.

8085 Bus structure



▶ Address Bus

- 8085 Microprocessor has 16 bit address bus.
- The bus over which the CPU sends out the address of the memory location is known as Address bus.
- The address bus carries the address of memory location or peripherals devices to be written or to be read from.
- The address bus is ***unidirectional***. It means bits flowing occurs only in one direction, only from microprocessor to peripheral devices.

NOTE:-We can find that how much memory location is needed ,by using the formula 2^N . where N is the number of bits used for address lines.

In 8085 the memory size is $2^{16} = 65536$ bytes or 64Kb,
So it can access upto 64 kb memory location.

► Q.>If a processor has 4 GB memory then how many address lines are required to access this memory?

► Ans: $4\text{GB} = 4 * 1\text{GB}$

$$4 = 2^2$$

$$1\text{GB} = 2^{30}$$

$$\text{So, } 4\text{GB} = 2^2 * 2^{30} = 2^{32}$$

So 32 address lines are required to access the 4 GB memory.



► Data bus

- 8085 Microprocessor has 8 bit data bus.
- So it can be used to carry the 8 bit data starting from 00000000H(00H) to 11111111H(FFH). Here 'H' tells the Hexadecimal Number.
- It is bidirectional. These lines are used for data flowing in both direction means data can be transferred or can be received through these lines.
- The data bus also connects the I/O ports and processor.
- The largest number that can appear on the data bus is 11111111.
- It has 8 parallel lines of data bus. So it can access upto $2^8 = 256$ data

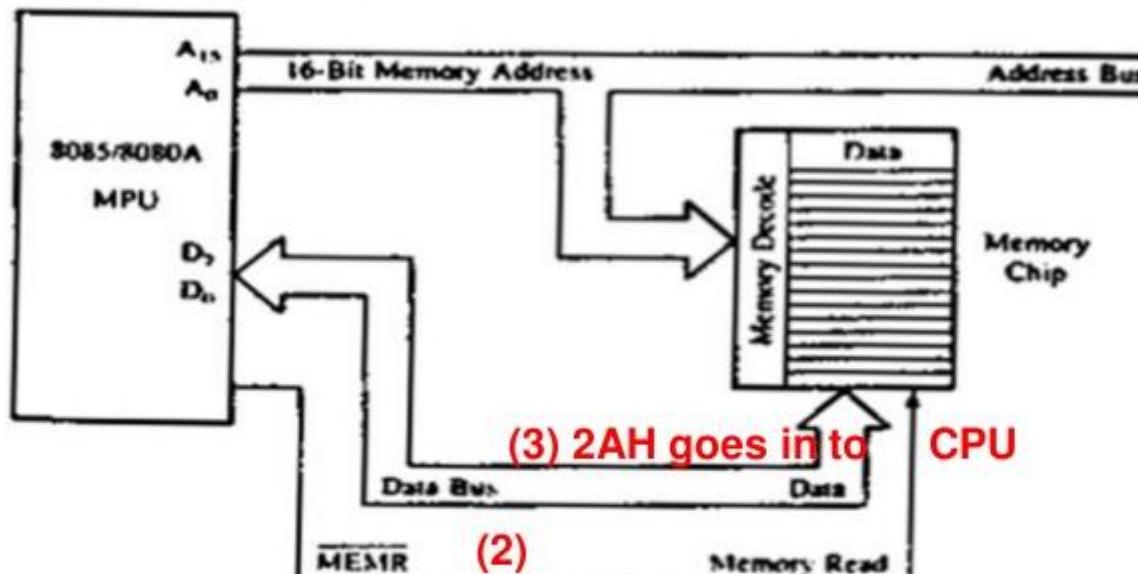
▶ Control Bus

- Control bus is comprised of various single lines that carry synchronization signals.
- These are not group of lines as in data bus and address bus, it is a individual line that provides a pulse to indicate microprocessor operations.
- The microprocessor generates specific control signals for every operations.

Memory read operation

Read Operation:

(1): 0010 0000 0101 0000 = 2050H



Memory Read Operation

Internal Data operations

- ▶ Internal architecture of microprocessor define what and how the operations can be performed with the data. These operations are:
 - Store 8 bit data
 - Perform arithmetic and logical operations
 - Test for conditions
 - Sequence the execution of instructions
 - Store data temporarily during execution in the defined R/W memory locations called stack

- ▶ To perform all operations the microprocessor requires registers , ALU and control unit, and internal buses.

Peripherals or Externally initiated operations

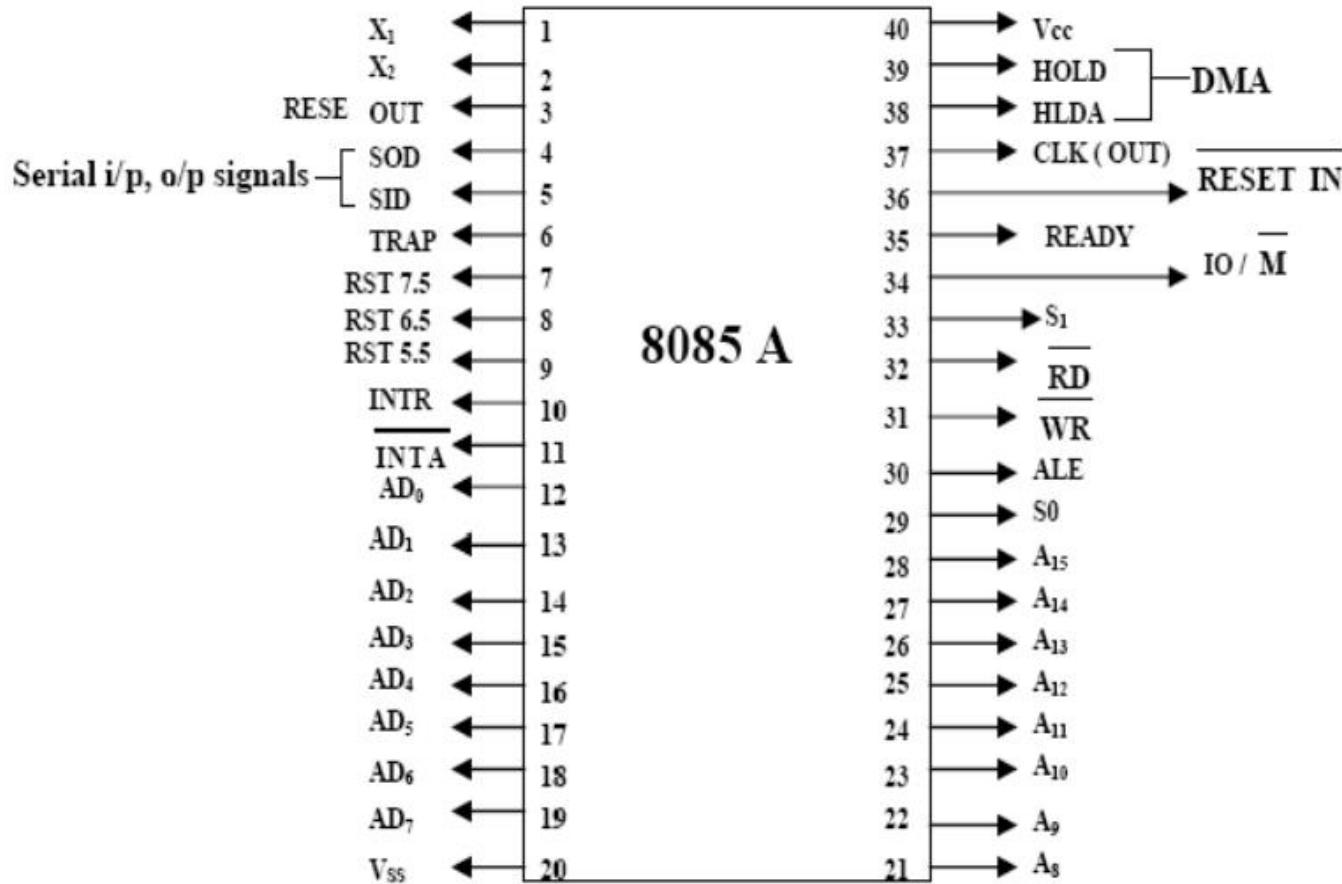
- ▶ External devices can initiate the following operations, for which individual pins on the microprocessor chip are assigned: Reset, Interrupt, Ready, Hold.
- ▶ **Reset:**
 - When reset pin is activated by an external key, all internal operations are suspended and the program counter is cleared to 0000H. Now the program execution can again begin at the zero memory address.
- ▶ **Interrupt:**
 - The microprocessor can be interrupted from the normal execution of instructions and asked to execute some other instructions called service routine. The microprocessor resumes its operation after completing the service routine.

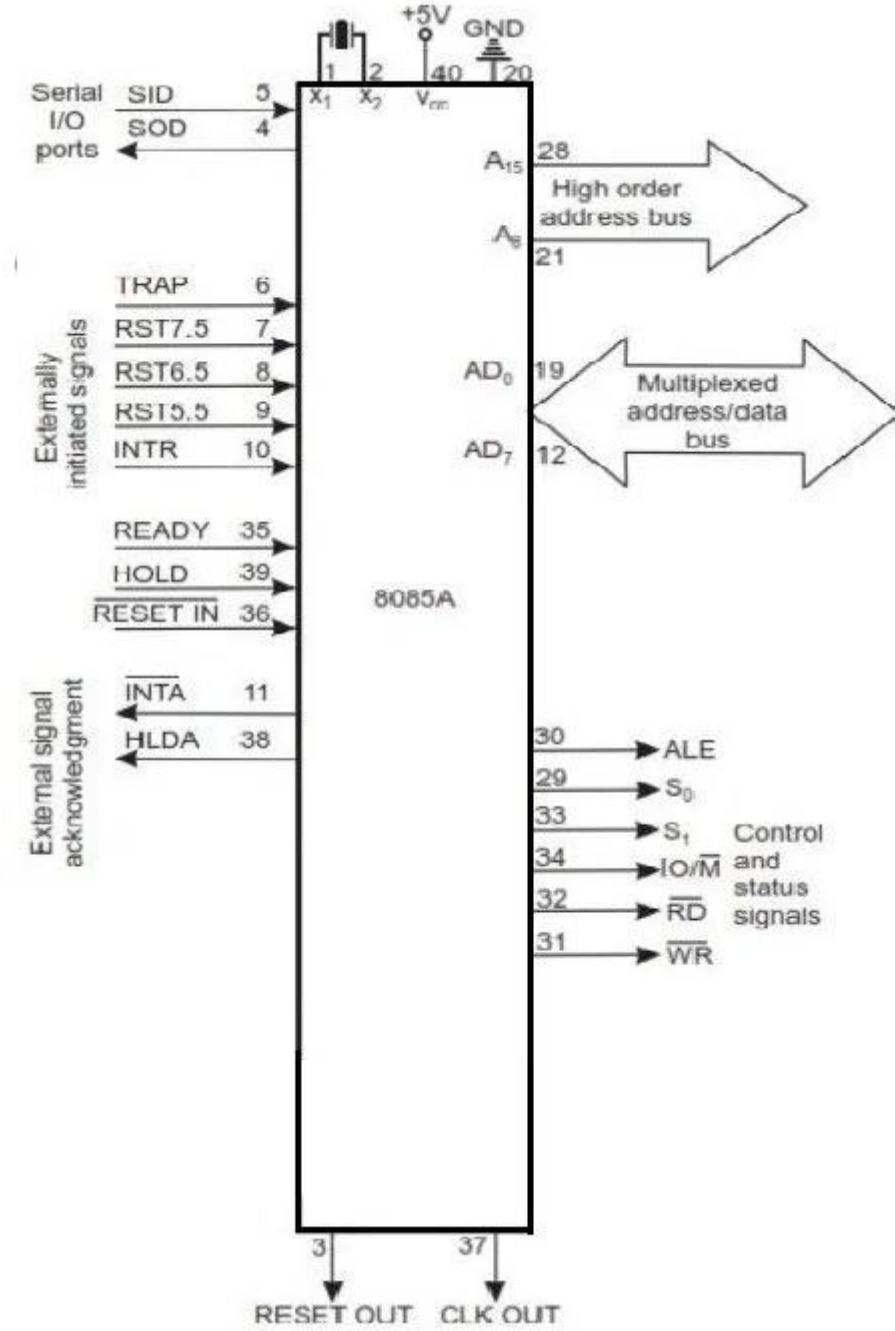
- ▶ Ready:
 - 8085 has pin called ready. When this ready pin is low, the microprocessor enters into Wait state. This signal is used primarily to synchronize slower peripherals with microprocessor.
- ▶ Hold:
 - When the HOLD pin is activated by an external signals, the microprocessor relinquishes control of buses and allows the external peripheral to use them.

8085 Pin configuration

- ▶ 8085 is 8 bit microprocessor.
- ▶ It has 16 bit address bus with 64 KB addressing capabilities.
- ▶ 8085 is 40 pin DIP package.
- ▶ The pins can be grouped as
 - 1. power supply and clock signals
 - 2. Address bus
 - 3. Data Bus
 - 4. Control and status bus
 - 5. Interrupt and externally initiated signals
 - 6. Serial I/O port

8085 Pin configuration





1. Power supply and clock frequency

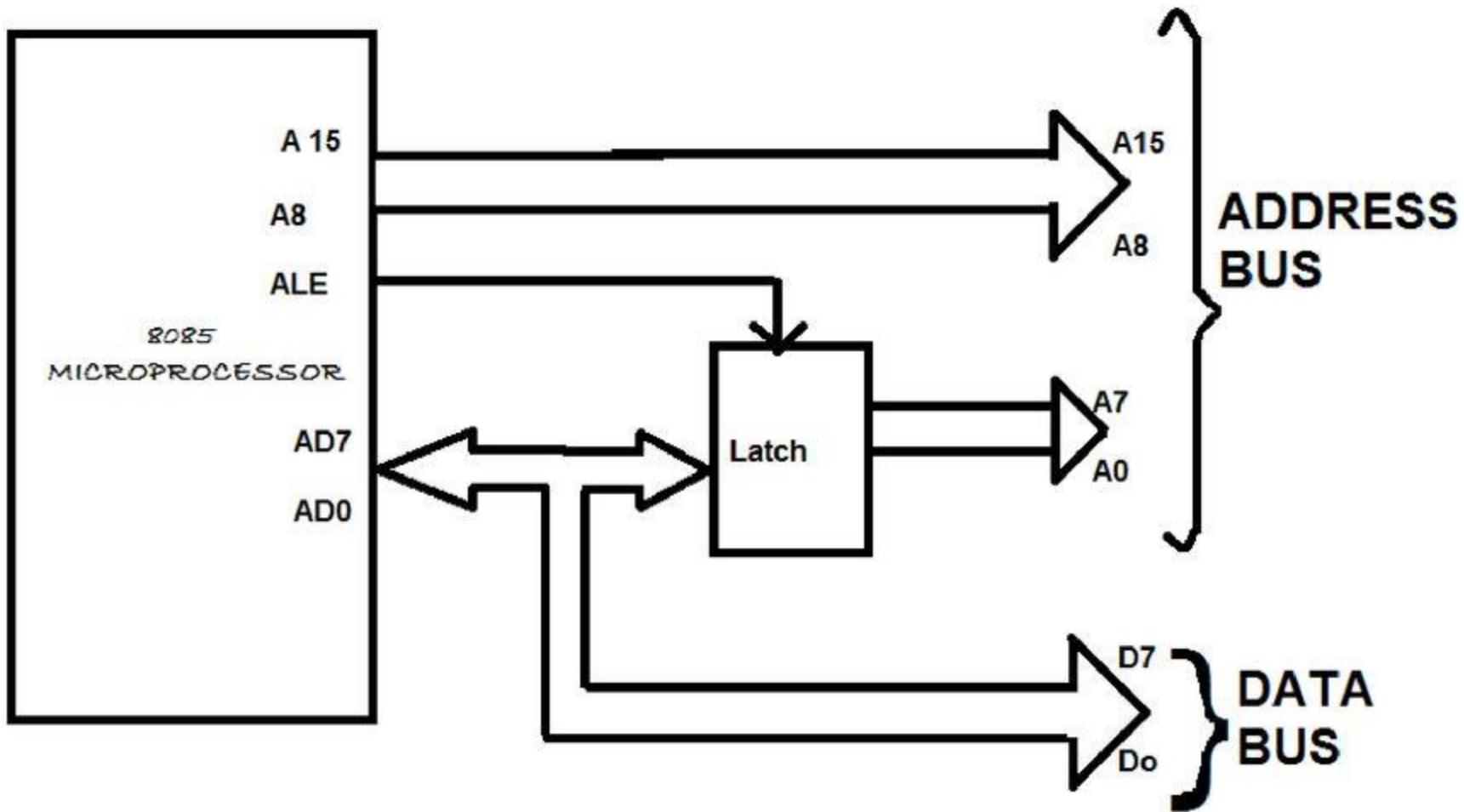
- ▶ $V_{cc} = +5$ volt power supply
- ▶ $V_{ss} = \text{Ground}$
- ▶ X1,X2: crystal or R/C network or LC network connections to set the frequency of internal clock generator.
- ▶ Frequency 3 MHz
- ▶ CLK (output)– clock output is used as system clock for peripherals and devices interfaced with the microprocessor.

2. Address Bus

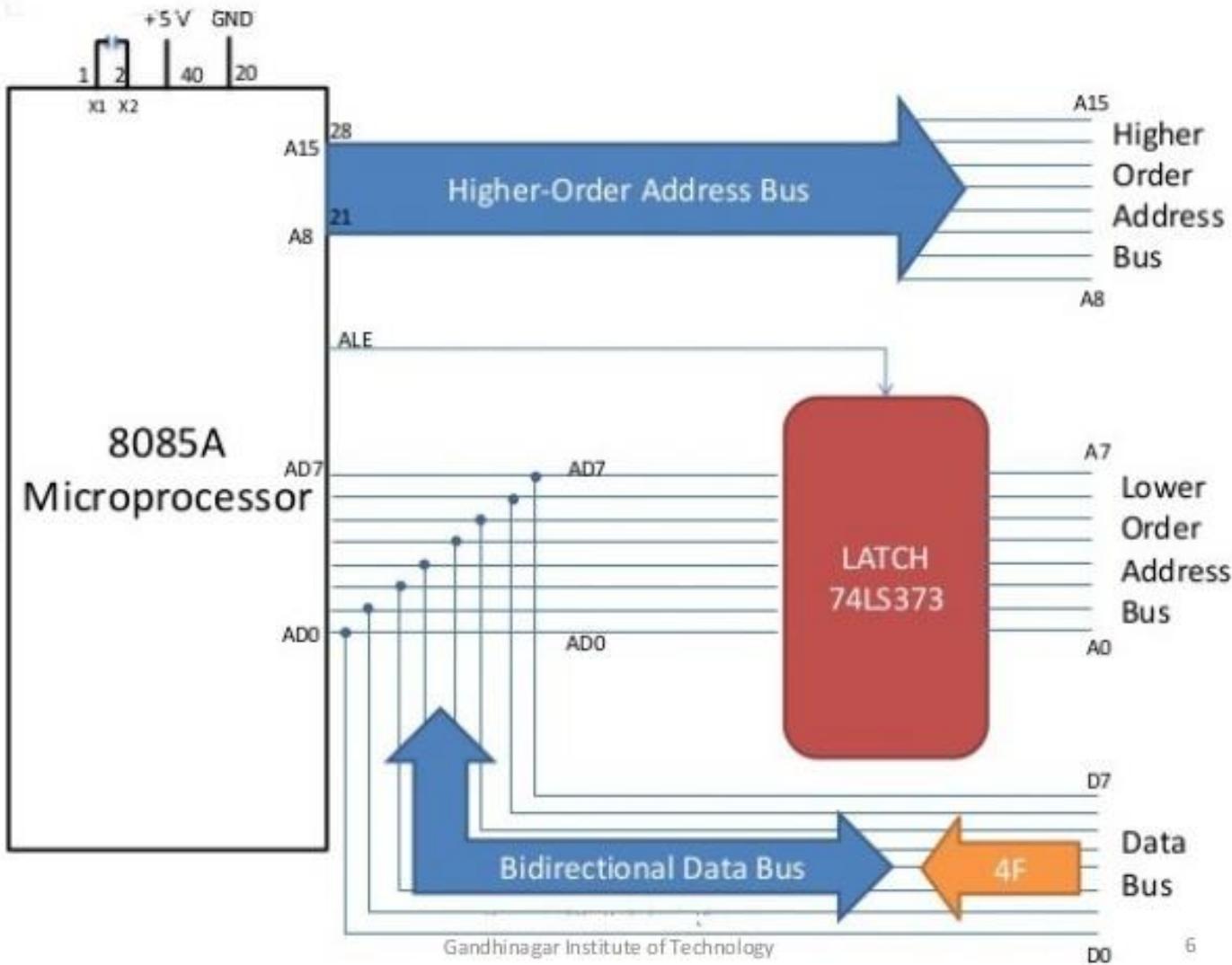
- ▶ A8-A15
- ▶ It carries most significant bits of memory address or the 8 bits of the I/O address.

3. Multiplexed Address /Data Bus

- ▶ AD0–AD7
- ▶ These multiplexed set of lines used to carry the lower order 8 bit address as well as data.
- ▶ During the opcode fetch operation, in the first clock cycle, the lines deliver the lower order address A0–A7.
- ▶ In subsequent IO/Memory, Read/Write clock cycle the lines are used as data bus.
- ▶ The CPU may read or write out data through this lines.



[FIG : DE MULTIPLEXING OF MULTIPLEXED ADDRESS DATA BUS.]



4. Control and status signal

- ▶ These signals contains two control signal (RD and WR) , three status signal(IO/M,S1 and S0) to identify the nature of operations and one special signal (ALE) to indicate the beginning of operations.
 - **ALE (Output):– Address Latch Enable**
 - The signal helps to capture the lower order address presented on the multiplexed address/ data bus.
 - **RD(Active Low):–Read memory or IO device**
 - It means that the selected memory location or I/O device is to be read and that the data bus is ready to accept data from memory or I/O device.

- **WR (Active Low):– Write memory or I/O device**
 - This indicates that the data on the data bus is to be written into the selected memory location or I/O device.
- **IO/M(output):– Select memory or I/O device**
 - The status signal indicates that the read/ write operation relates to whether the memory or I/O device. It goes high to indicate an I/O operation and low for ,memory operation.

IO/ \bar{M}	S_1	S_0	States
0	0	1	Memory Write
0	1	0	Memory Read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch

5. Interrupt and externally initiated signals

- ▶ Interrupt are the signals generated by external devices to request the microprocessor to perform a task. There are 5 interrupt TRAP, RST 7.5,RST6.5,RST5.5 and INTR.
 - **INTA**:–It is interrupt acknowledgement signal.
 - **RESET IN**:–When the signal on this pin is low, the PC is set to 0, and microprocessor is reset.
 - **RESET OUT**:– This signal indicates that the processor is being reset. The signal can be used to reset other connected devices.

- **READY**:- This means device is ready to send and receive data. When this signal is low, the processor waits for an integral number of clock cycles until it goes high.
- **HOLD**:-this signal indicates that other master is requesting the use of address and data buses.
- **HLDA(HOLD Acknowledge)**:-It indicates that CPU has received HOLD request and it will relinquish the bus in next clock cycle. HLDA is set to low after HOLD signal is removed.

6. Serial I/O signals

- ▶ SOD and SID:- These lines are used for serial communication.
 - **SOD(Serial output data line)**:- The output SOD is set/reset as specified by SIM (Set Interrupt Mask) Instructions.
 - **SID(Serial input data line)**:- The data on this line is loaded into accumulator whenever a RIM (Read Interrupt Mask) instruction is executed.

Interrupts in 8085

- ▶ Interrupts are the signals generated by the external devices to request the microprocessor to perform a task. There are five types of interrupt i.e RST5.5,RST6.5,RST7.5, INTR and TRAP. Interrupt are classified into following groups on basis on their parameter:
- ▶ **Vector Interrupt:-**
 - In this type of interrupt, the interrupt address is known to the processor. For example RST7.5, RST6.5,RST5.5 ,TRAP.

▶ **Non vector Interrupt**

- In this type of interrupt the interrupt address is not known to processor. So, address need to be send externally by the device to perform interrupts.
- Example: INTR

▶ **Maskable interrupt**

- In this type of interrupt, interrupt can be disable by writing some instructions in a program. For example RST5.5,RST6.5,RST7.5

▶ **Non maskable Interrupt**

- In this type of interrupt we cant disable the interrupt by writing some instructions in the program. For Example TRAP

► **Software interrupt**

- In this type of interrupt the programmer had to add the instructions into the program to execute the interrupt . There are 8 software interrupt in 8085, i.e RST 0–7

► **Hardware interrupt**

- There are 5 hardware interrupt in 8085 used as hardware interrupt i.e Trap,RST5.5,RST6.5,RST7.5,INTA

Interrupt Service Routine(ISR)

- ▶ A small program or a routine that when executed, services the corresponding interrupting source is called ISR.
- ▶ TRAP
 - Non maskable interrupt
 - Has highest priority among all interrupt
 - By default it is enabled until it get acknowledged
 - This transfers control to 0024H

- ▶ RST 7.5
 - Maskable interrupt
 - Have second priority
 - When interrupt is executed, the processor saves the content of the PC register into the stack and branches to 003CH
- ▶ RST 6.5
 - Maskable interrupt
 - Have third priority
 - When interrupt is executed, the processor saves the content of the PC register into the stack and branches to 0034H

- ▶ RST 5.5
 - Maskable interrupt
 - When interrupt is executed, the processor saves the content of the PC register into the stack and branches to 002CH

▶ INTR

- Maskable interrupt
- Have lowest priority
- It can be disable by resetting microprocessor
- When INTR goes high following event occurs:
 - The microprocessor checks the status of INTR signal during the execution of each instruction.
 - When INTR signal is high then microprocessor completes its current instruction and sends active low interrupt acknowledge signal.
 - When instructions are received then microprocessor saves the address of the next instruction on stack and executes the received instruction.

Addressing modes of 8085

- ▶ The different ways in which a processor can access data are referred as its addressing modes.
- ▶ The addressing mode is indicated in instructions itself.
- ▶ The various addressing modes are:
 - Register Addressing Mode
 - Immediate Addressing Mode
 - Direct Addressing mode
 - Register Indirect Addressing Mode
 - Implied Addressing Mode

- Register Addressing Mode

- It is most common form of data addressing.
- Transfer data from one register to other.
- It is carried out with same size registers.
- *E.g MOVA,B* (move data from source register B to Destination Register A)

- Immediate Addressing Mode
 - Data is specified in instructions itself.
 - Data immediately follows the hexadecimal opcode.
 - *E.g MVI C,3AH* (I implies immediate data and Data 3AH is moved to register C)
- Direct Addressing mode
 - The Address of data is defined in instruction itself.
 - *E.g LDA 2000H*(Load Accumulator with content of 2000H memory.)

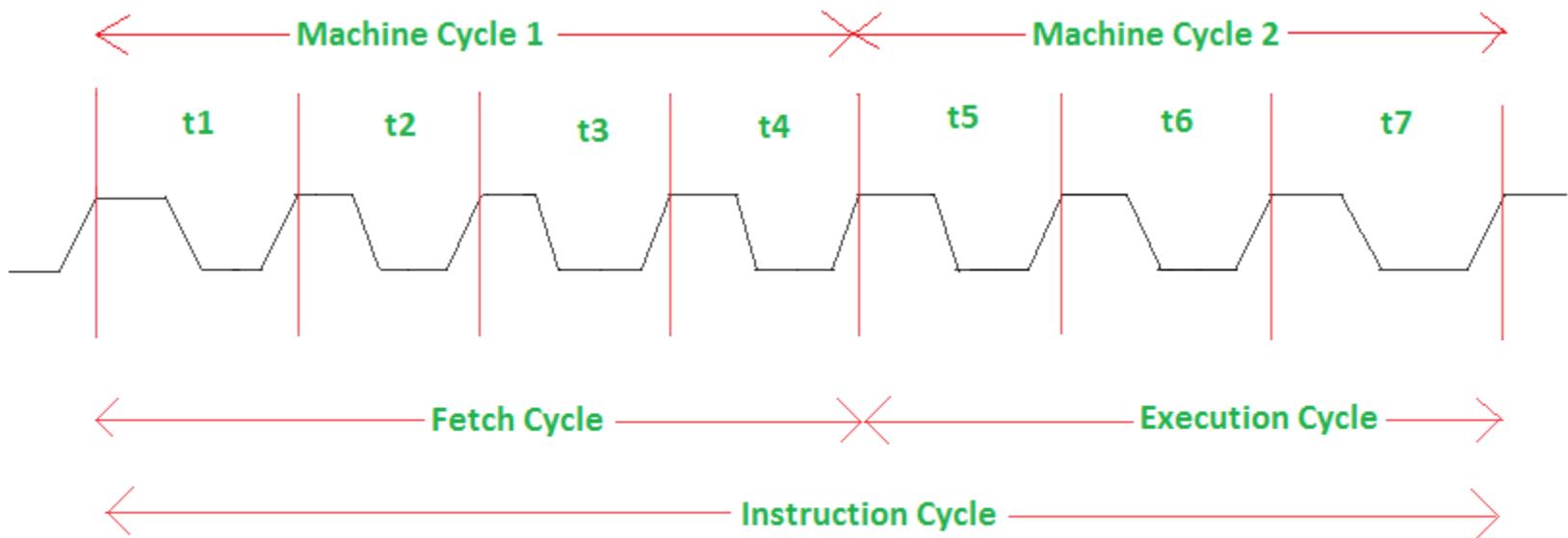
- Register Indirect Addressing Mode
 - In this mode address of operand is specified by register pair.
 - H pair, B pair or D pair.
 - *E.g MOV C,M* (M is memory location specified by H-L pair and address of operand is in H-L pair register)
- Implied Addressing Mode
 - The Addressing mode of certain instructions is implied by the instructions function.
 - *E.g STC* (set carry flag)
 - *CMC* (complement carry flag)

Instruction cycle

- ▶ The necessary steps that the CPU carries out to fetch an instruction and necessary data from memory and to execute it constitute an *instruction cycle*.
- ▶ Instruction cycle is defined as time required to complete the execution of an instruction.
- ▶ An instruction cycle constitute of fetch and execute cycle.
- ▶ The necessary steps which are carried out to fetch an opcode from memory constitute **fetch cycle**.
- ▶ The necessary steps which are carried out to get data if any from memory and to perform the specific operation specified in the instruction constitute of *execute cycle*.

Total time to execute the instruction

► $IC = Fc + Ec$



Instruction cycle in 8085 microprocessor

Fetch cycle

- ▶ First byte of instruction is its opcode.
- ▶ The program counter keeps the memory address of the next instruction to be executed in the beginning of fetch cycle.
- ▶ The content of PC, which is address of instruction to be fetch is send to memory.
- ▶ The memory places opcode to data bus so as to transfer to CPU.
- ▶ The entire process takes 2 clock cycle and in next one cycle instruction is decode.

Execution cycle

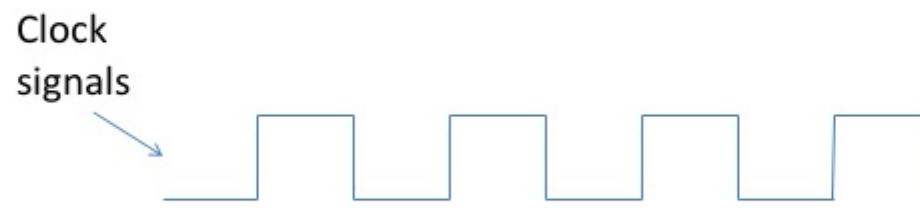
- ▶ The opcode fetch from memory goes to IR from IR it goes to decoder which decodes instruction after instruction is decoded execution begins.
- ▶ If operand is in register, the execution begins immediately and is completed in one clock cycle.
- ▶ If instruction contains data or operand address then CPU has to perform some read operation to get desired data.
- ▶ In some instruction write operation is performed. In write cycle data are send from CPU to memory or o/p device.
- ▶ In some cases execute cycle may involve one or more read or write cycle or both.

Machine Cycle

- ▶ It is defined as time required to complete one operation of accessing memory, I/O or acknowledging external request.
- ▶ This cycle may consist of 3 to 6 T states
- ▶ **T States:** It is defined as one subdivision of operation in one clock period. These subdivisions are internal states synchronized with system clock and each T states precisely equal to one clock period.

T-States

One clock period is called a T-state.



Time period of clock

Machine Cycles of 8085

- ▶ The 8085 has following basic machine cycle
 - opcode Fetch Cycle(4T)
 - Memory Read Cycle(3T)
 - Memory Write Cycle(3T)
 - I/O read Cycle(3T)
 - I/O write Cycle(3T)
 - Interrupt

Machine Cycle	Status			Control Signals		
	$\overline{IO/M}$	S1	S0	\overline{RD}	\overline{WR}	\overline{INTA}
Opcode Fetch	0	1	1	0	1	1
Memory Read	0	1	0	0	1	1
Memory Write	0	0	1	1	0	1
I/O Read	1	1	0	0	1	1
I/O Write	1	0	1	1	0	1
Interrupt Acknowledge	1	1	1	1	1	0
HALT	Z	0	0	Z	Z	1
HOLD	Z	X	X	Z	Z	1
RESET	Z	X	X	Z	Z	1

Where Z is tri state (pin neither connected to supply nor ground. High impedance) and X represents do not care.

8085 machine cycle status and control signals

Timing Diagram of opcode fetch machine cycle

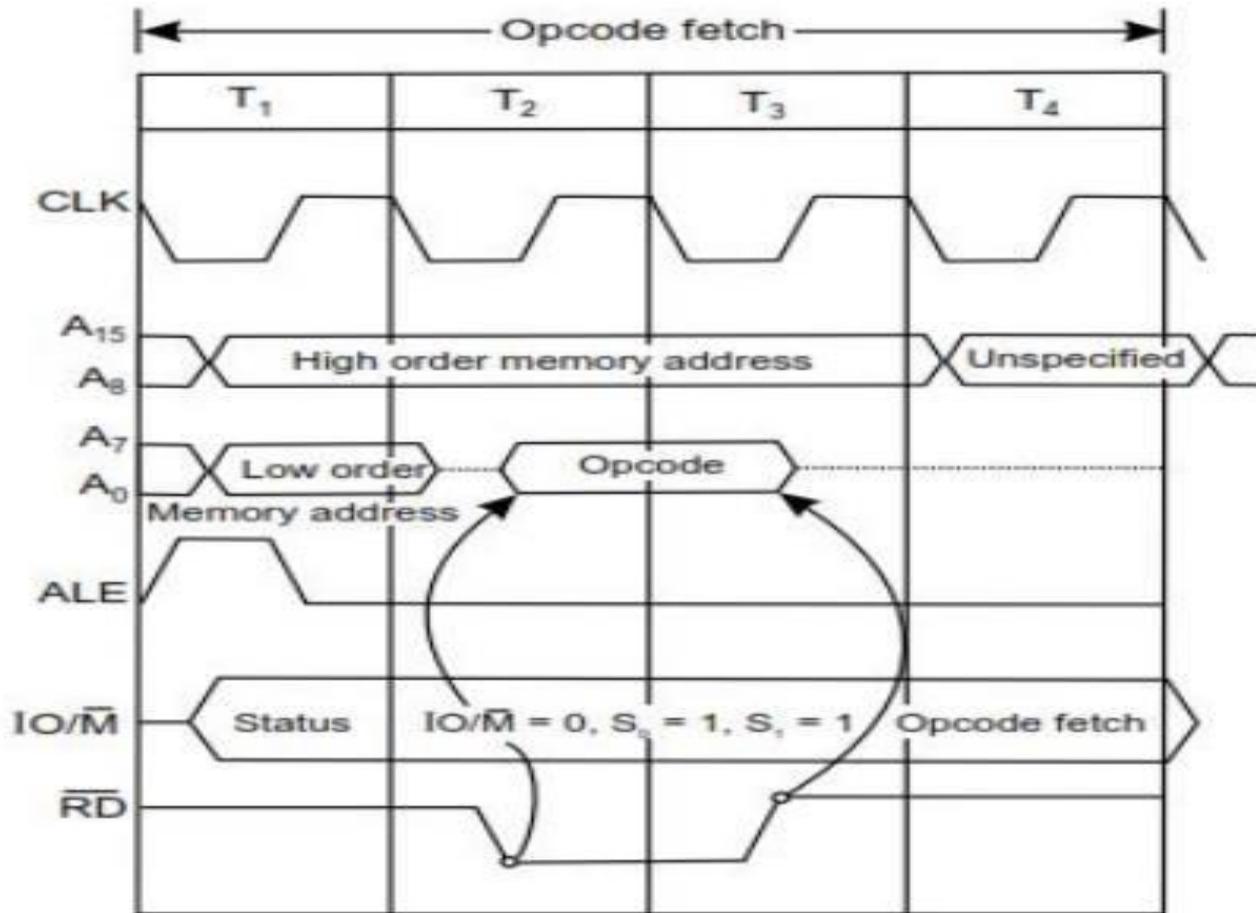


Fig 1.8 Opcode fetch machine cycle

OPCODE FETCH

- The Opcode fetch cycle, fetches the instructions from memory and delivers it to the instruction register of the microprocessor
- Opcode fetch machine cycle consists of **4 T-states**.

T1 State:

During the T1 state, the contents of the program counter are placed on the 16 bit address bus. The **higher order 8 bits** are transferred to address bus (**A8-A15**) and **lower order 8 bits** are transferred to multiplexed A/D (**AD0-AD7**) bus.

ALE (address latch enable) signal goes **high**. As soon as ALE goes high, the memory latches the AD0-AD7 bus. At the middle of the T state the **ALE goes low**

T2 State:

During the beginning of this state, the **RD' signal goes low** to enable memory. It is during this state, the selected memory location is placed on D0-D7 of the Address/Data multiplexed bus.

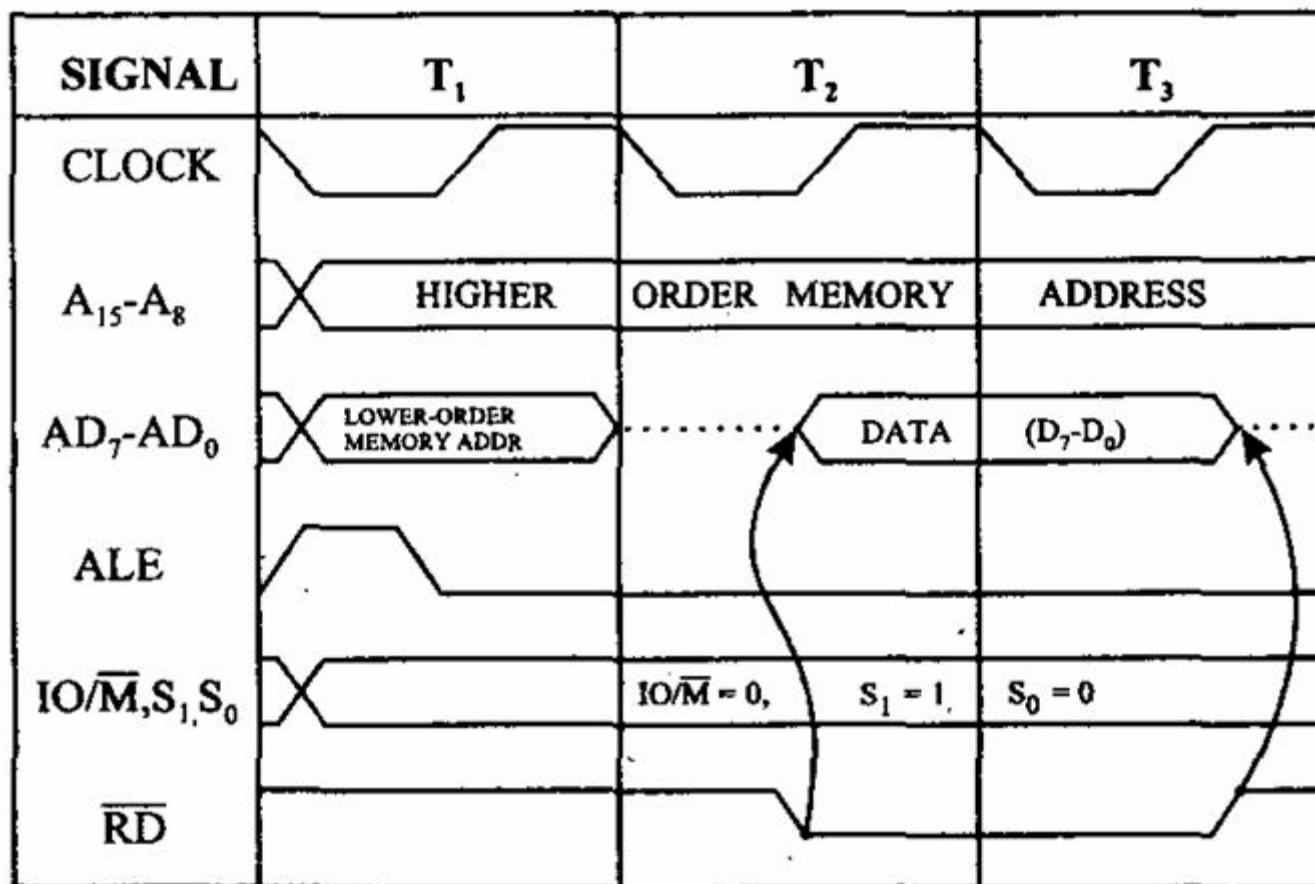
T3 State:

In the previous state the Opcode is placed in D0-D7 of the A/D bus. In this state of the cycle, the Opcode of the A/D bus is transferred to the instruction register of the microprocessor. Now the **RD' goes high** after this action and thus disables the memory from A/D bus.

T4 State:

In this state the Opcode which was fetched from the memory is decoded.

Timing Diagram of memory read cycle



- These machine cycles have 3 T-states.

T1 state:

- The higher order address bus (**A8-A15**) and lower order address and data multiplexed (**AD0-AD7**) bus. **ALE goes high** so that the memory latches the (**AD0-AD7**) so that complete 16-bit address are available.

The mp identifies the memory read machine cycle from the status signals **IO/M'=0, S1=1, S0=0**. This condition indicates the memory read cycle.

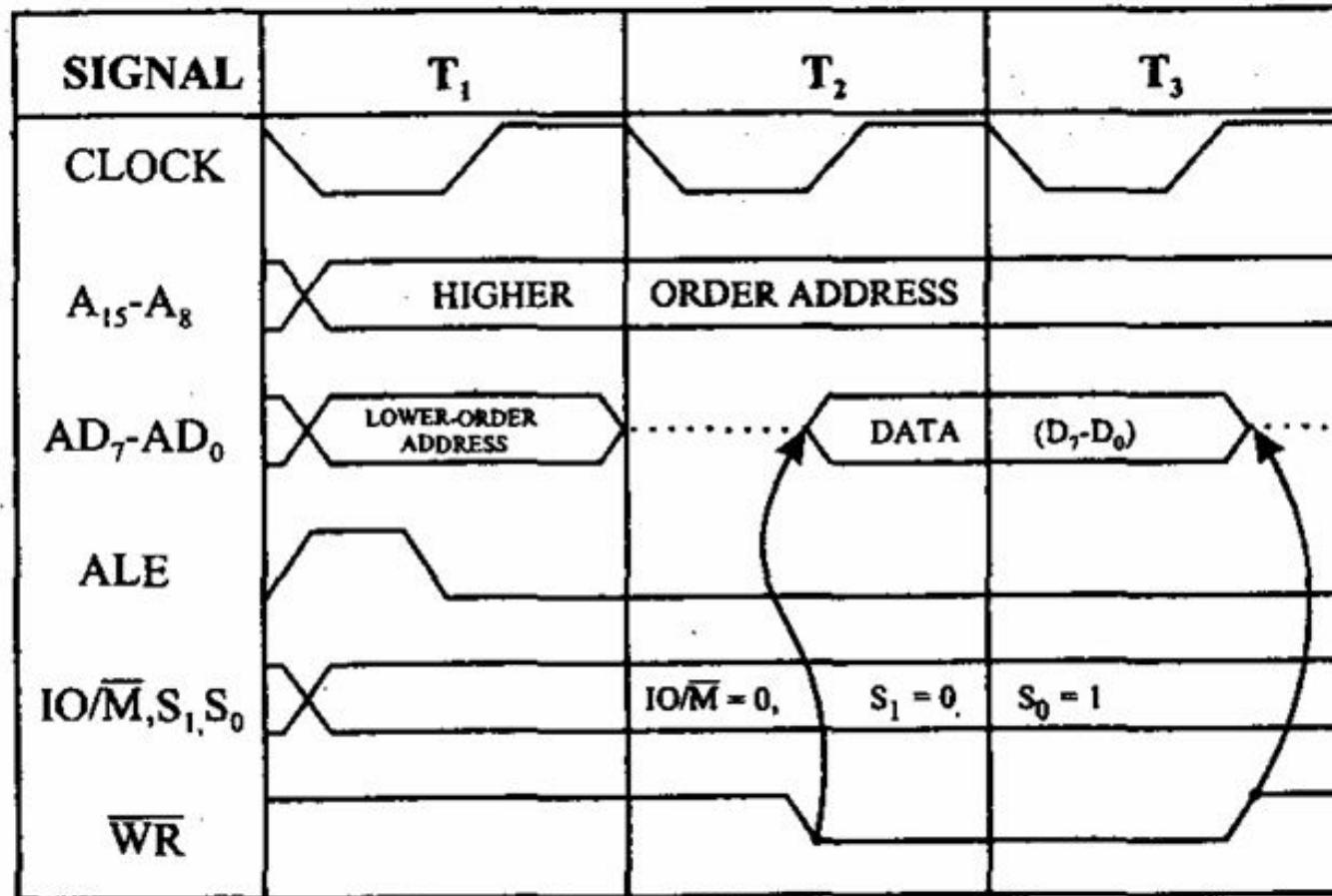
T2 state:

- Selected memory location is placed on the (**D0-D7**) of the A/D multiplexed bus. **RD'** goes **LOW**

T3 State:

- The data which was loaded on the previous state is transferred to the microprocessor. In the middle of the T3 state **RD'** goes high and disables the memory read operation. The data which was obtained from the memory is then decoded.

Timing Diagram of memory write cycle



- These machine cycles have 3 T-states.

T1 state:

- The higher order address bus (**A8-A15**) and lower order address and data multiplexed (**AD0-AD7**) bus. **ALE goes high** so that the memory latches the (**AD0-AD7**) so that complete 16-bit address are available.

The MP identifies the memory read machine cycle from the status signals **IO/M'=0, S1=0, S0=1**. This condition indicates the memory read cycle.

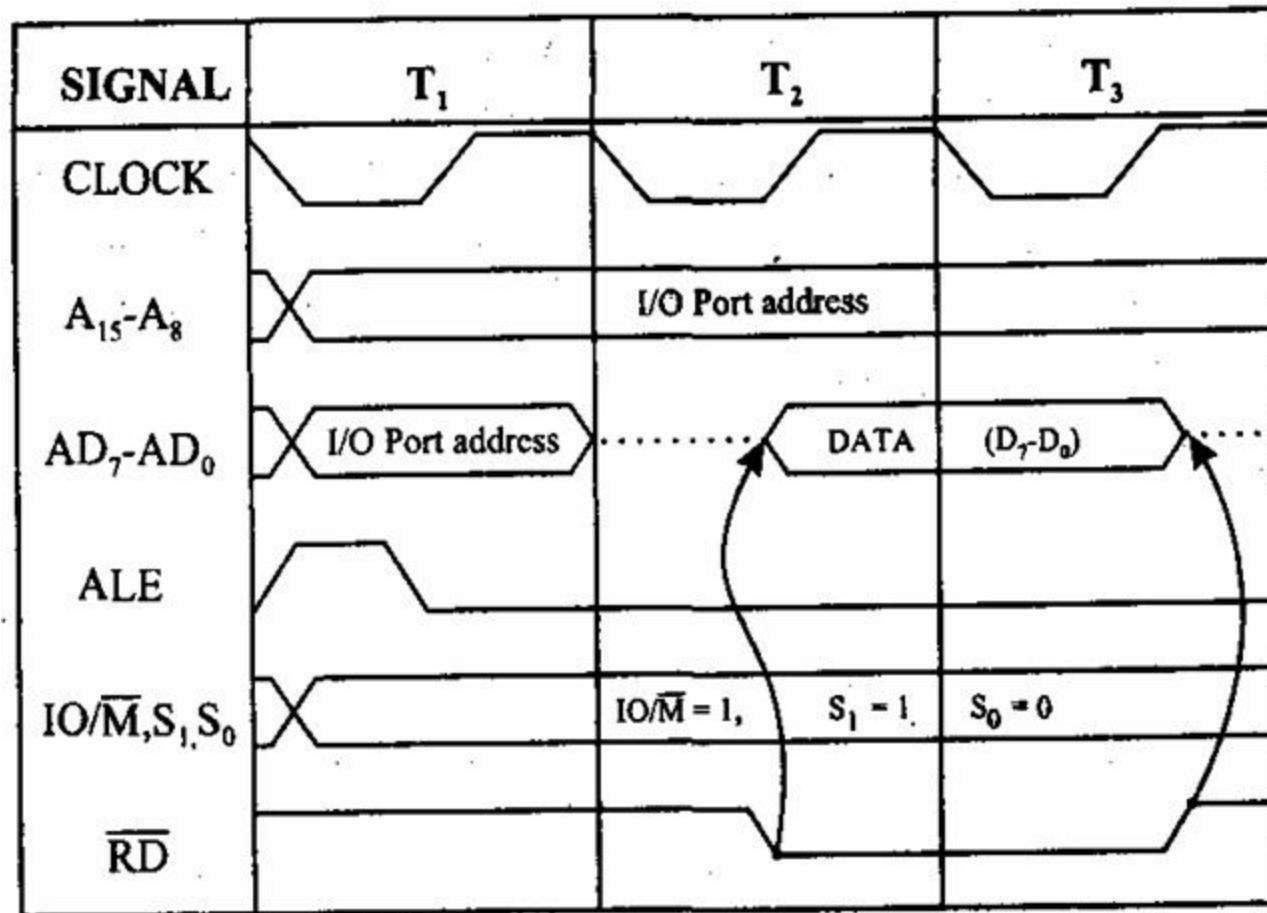
T2 state:

- Selected memory location is placed on the (**D0-D7**) of the A/D multiplexed bus. **WR'** goes **LOW**

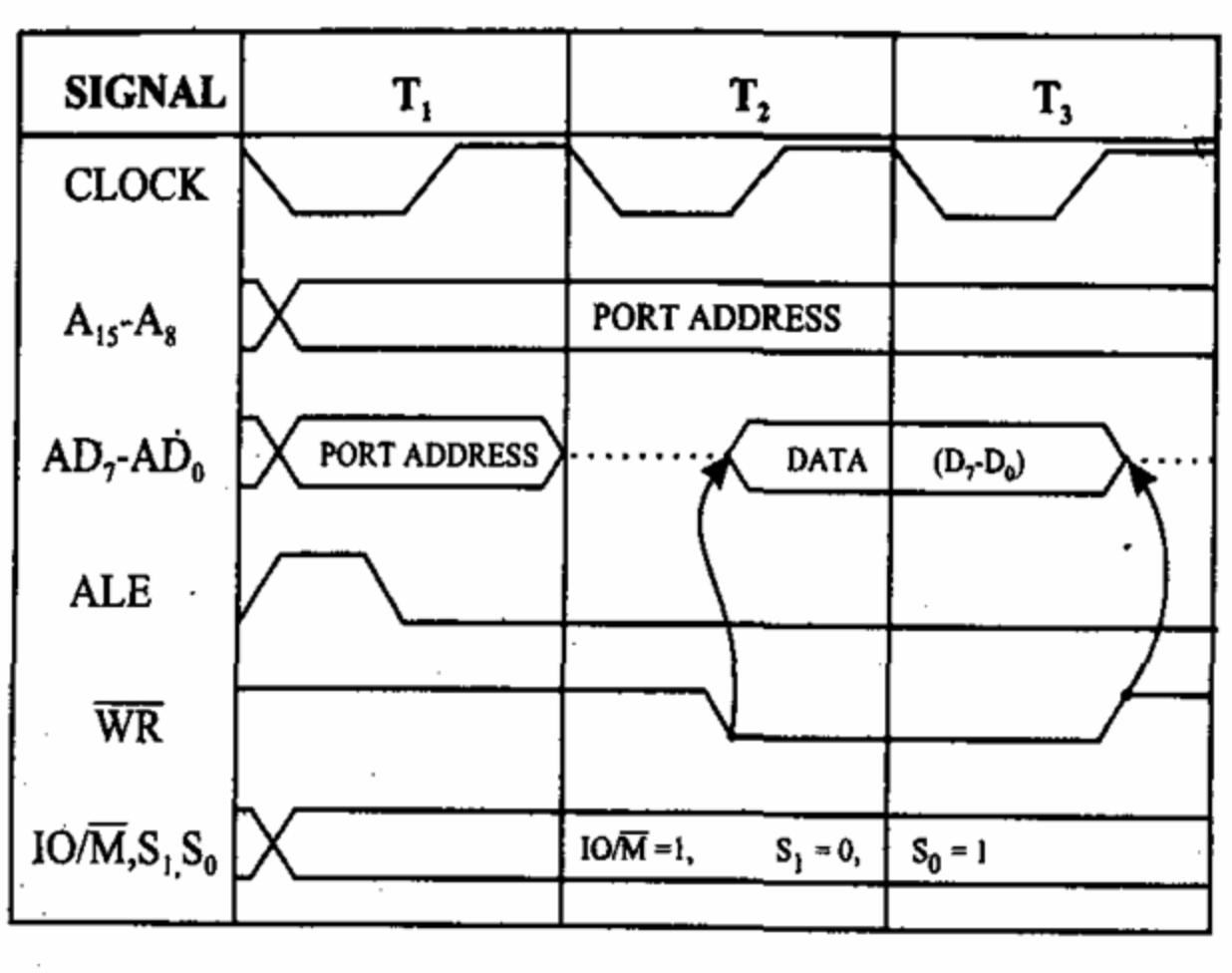
T3 State:

- In the middle of the T3 state **WR'** goes **high** and **disables the memory write operation**. The data which was obtained from the memory is then decoded.

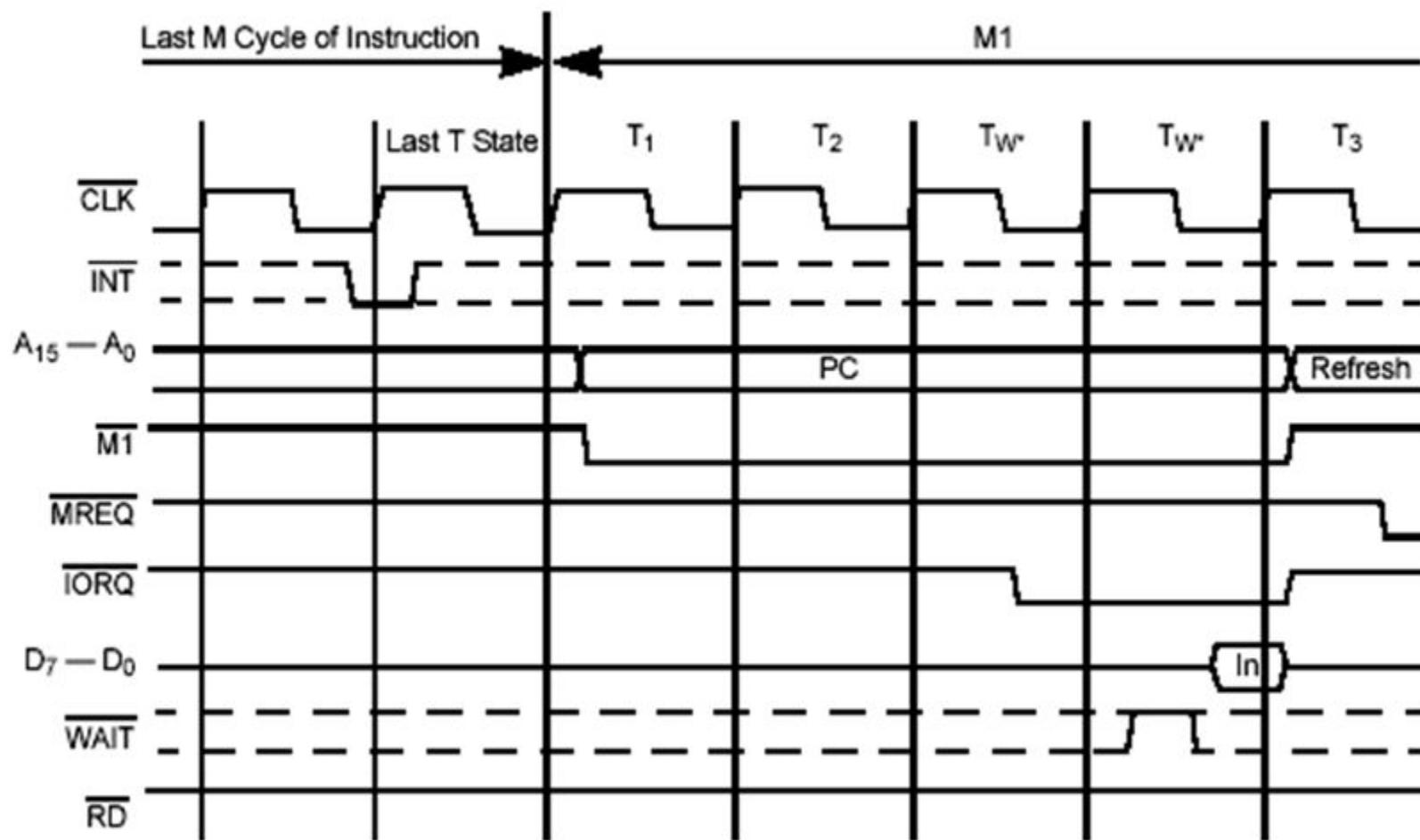
Timing Diagram of I/O read cycle



Timing Diagram of I/O write cycle

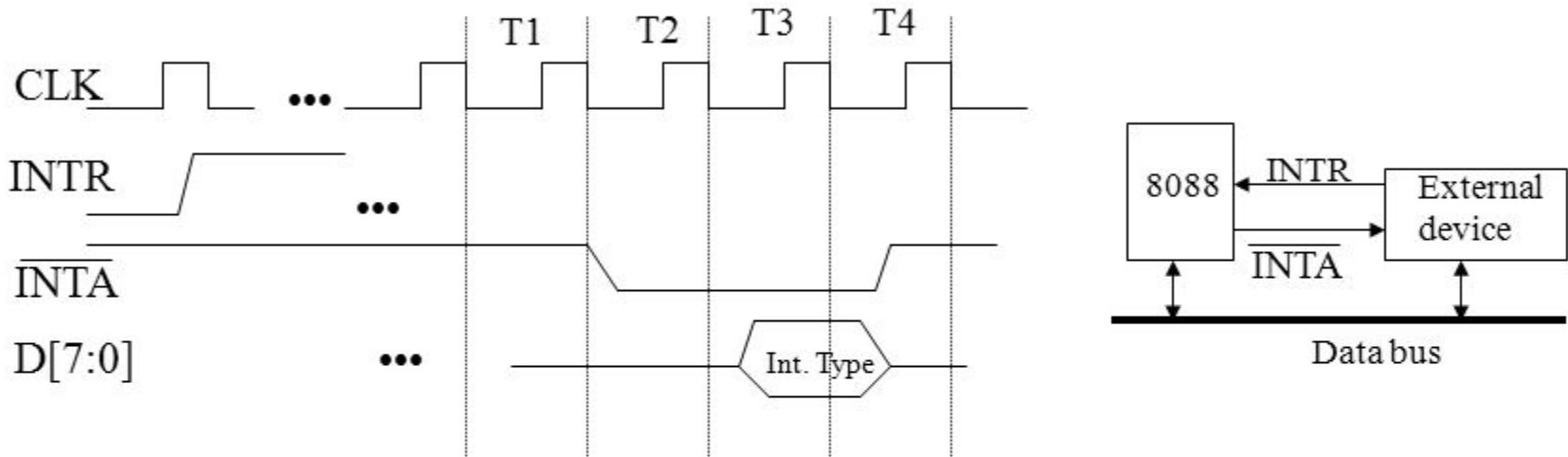


Interrupt Request/Acknowledge Cycle



Two wait states are automatically added to this cycle

Interrupt Acknowledge Timing Diagrams



- ❑ It takes one bus cycle to perform an interrupt acknowledge
- ❑ During T1, the process tri-states the address bus
- ❑ During T2, INTA is pulled low and remains low until it becomes inactive in T4
- ❑ The interrupting devices places an 8-bit interrupt type during $\overline{\text{INTA}}$ is active

Timing Diagram of opcode machine cycle

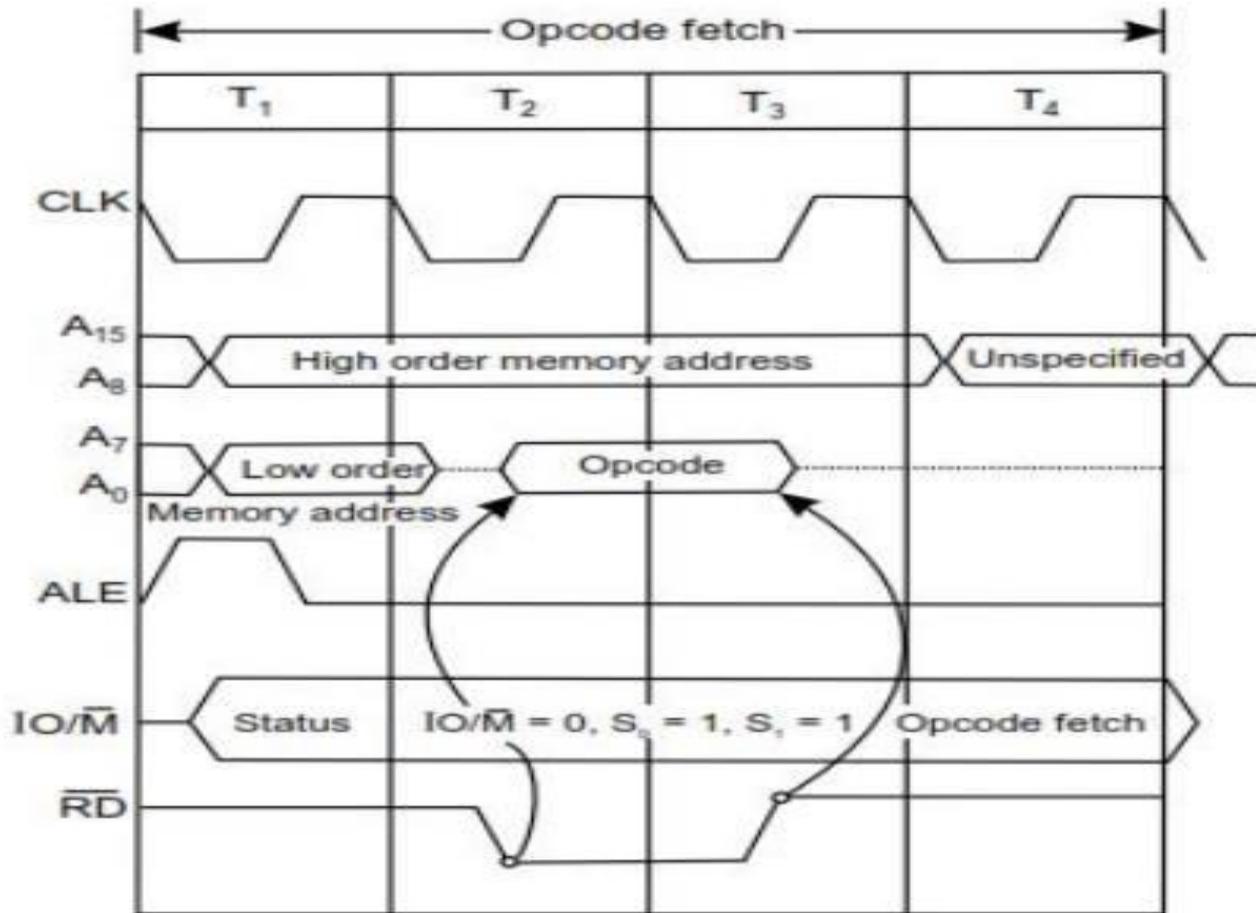


Fig 1.8 Opcode fetch machine cycle

Timing Diagram of memory read cycle

