# CPLD 設計作業

銘傳大學電腦與通訊工程系

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|---|---|
| 班　　級 | 電通二乙 |
| 組　　別 | 第 27 組 |
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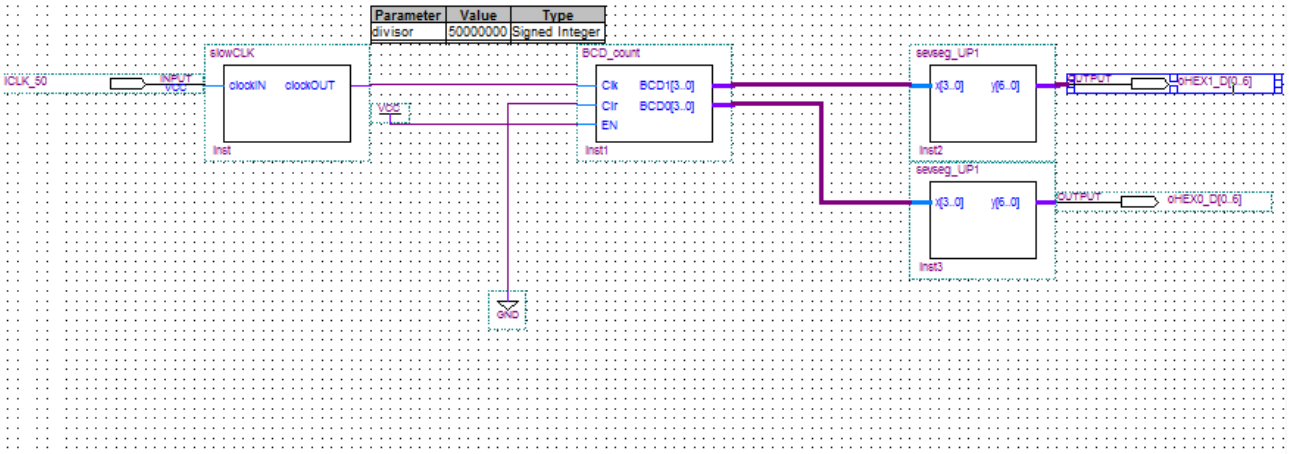
| 實習成果 | 本次應繳作業共 2 題，完成 2 題 |
| 時　　間 | 2017/10/27 |

## 第一題

問題描述: **整合設計: 實現一個兩位數 BCD 計數器**

模擬結果:




https://www.youtube.com/watch?v=g5xlUkuDq84

**第二題**

問題描述: **實現一個四位數 BCD 計數器**

**程式碼:**< BCD_count>

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;

ENTITY BCD_count IS
PORT ( Clk : IN STD_LOGIC ;
        Clr, EN : IN STD_LOGIC ;
        BCD3,BCD2,BCD1, BCD0 : BUFFER STD_LOGIC_VECTOR(3
DOWNTO 0) ) ;
 END BCD_count ;

ARCHITECTURE Behavior OF BCD_count IS
BEGIN
PROCESS (Clk)
BEGIN
  IF Clk'EVENT AND Clk = '1' THEN
      IF Clr = '0' THEN
          BCD1 <= "0000" ; BCD0 <= "0000" ; BCD2 <= "0000" ; BCD3 <=
"0000" ;
      ELSIF EN = '1' THEN
          IF BCD0 = "1001" THEN
              BCD0 <= "0000" ;
              IF BCD1 = "1001" THEN
```

```
                    BCD1 <= "0000";
                    IF BCD2 = "1001" THEN
                        BCD2 <= "0000";
                        IF BCD3 = "1001" THEN
                            BCD3 <= "0000";
                            ELSE
                    BCD3 <= BCD3 + '1' ;
                END IF ;
                ELSE
                    BCD2 <= BCD2 + '1' ;
                END IF ;
                ELSE
                    BCD1 <= BCD1 + '1' ;
                END IF ;
            ELSE
                BCD0 <= BCD0 + '1' ;
            END IF ;
        END IF ;
    END IF;
END PROCESS;
END Behavior ;
```

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```
library ieee;
use ieee.std_logic_1164.all;


entity aaa is
  generic(divisor:integer:=1000000);
port(    clockIN : in    std_logic;
                    clockOUT: out std_logic);
end aaa;
architecture arch of aaa is
signal PULSE : std_logic;
begin
process(clockIN)
variable counter,divisor2 : integer range 0 to divisor;
begin
    divisor2:=divisor/2;
if (clockIN 'event and clockIN ='1') then
            if counter = divisor then
                counter := 1;
            else
                counter := counter + 1;
            end if;
        end if;
if (clockIN 'event and clockIN ='1') then
            if (( counter= divisor2) or (counter = divisor))then
                PULSE <= not PULSE ;
```

```
            end if;
        end if;
        clockOUT <= PULSE ;
    end process;
end arch;
```

<七段顯示器>

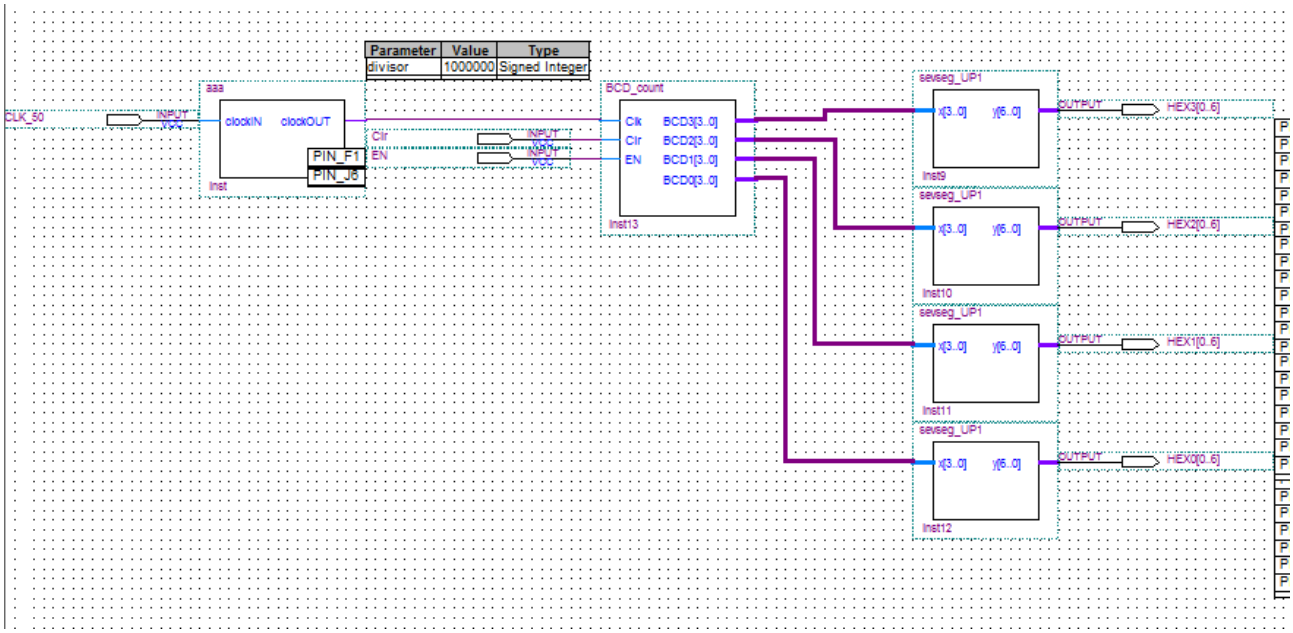
```
library ieee;
use ieee.std_logic_1164.all;

entity sevseg_UP1 is
   port(    x:in std_logic_vector(3 downto 0);
                  y:out std_logic_vector(6 downto 0));
end sevseg_UP1;
architecture a of sevseg_UP1 is
        begin
        with x select
                y <= "0000001" when "0000",
                        "1001111" when "0001",
                        "0010010" when "0010",
                        "0000110" when "0011",
                        "1001100" when "0100",
                        "0100100" when "0101",
                        "0100000" when "0110",
                        "0001111" when "0111",
                        "0000000" when "1000",
                        "0000100" when "1001",
                        "0001000" when "1010",
                        "1100000" when "1011",
                        "0110001" when "1100",
                        "1000010" when "1101",
                        "0110000" when "1110",
```

"0111000" when others;

end a;

模擬結果:




https://www.youtube.com/watch?v=v3XB95RAbdQ