CPLD 設計作業

銘傳大學電腦與通訊工程系

班　　級	電通二乙
組　　別	第 27 組
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組員姓名/學號	陳奕璁 05050536
作業撰寫人	陳韋澔
授課教師	陳慶逸
實習成果	本次應繳作業共 3 題，完成 3 題
時　　間	2017/10/20

第一題

問題描述: **使用 if-then-else 敘述**

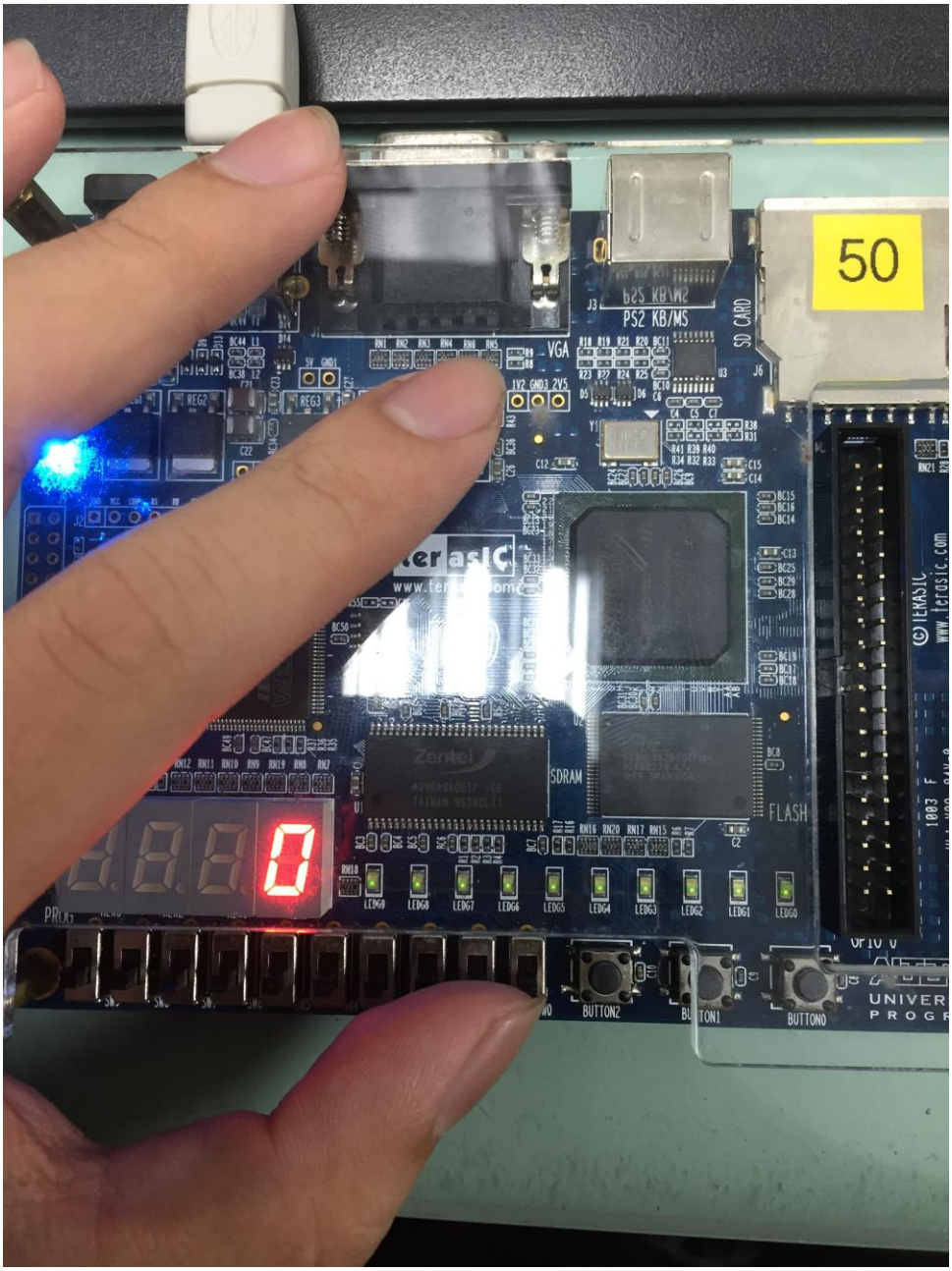
設計一個可以顯示數字 0-9, A 到 F 的七段顯示器解碼電路(共陽極),並在 DE0 實驗板進行驗證

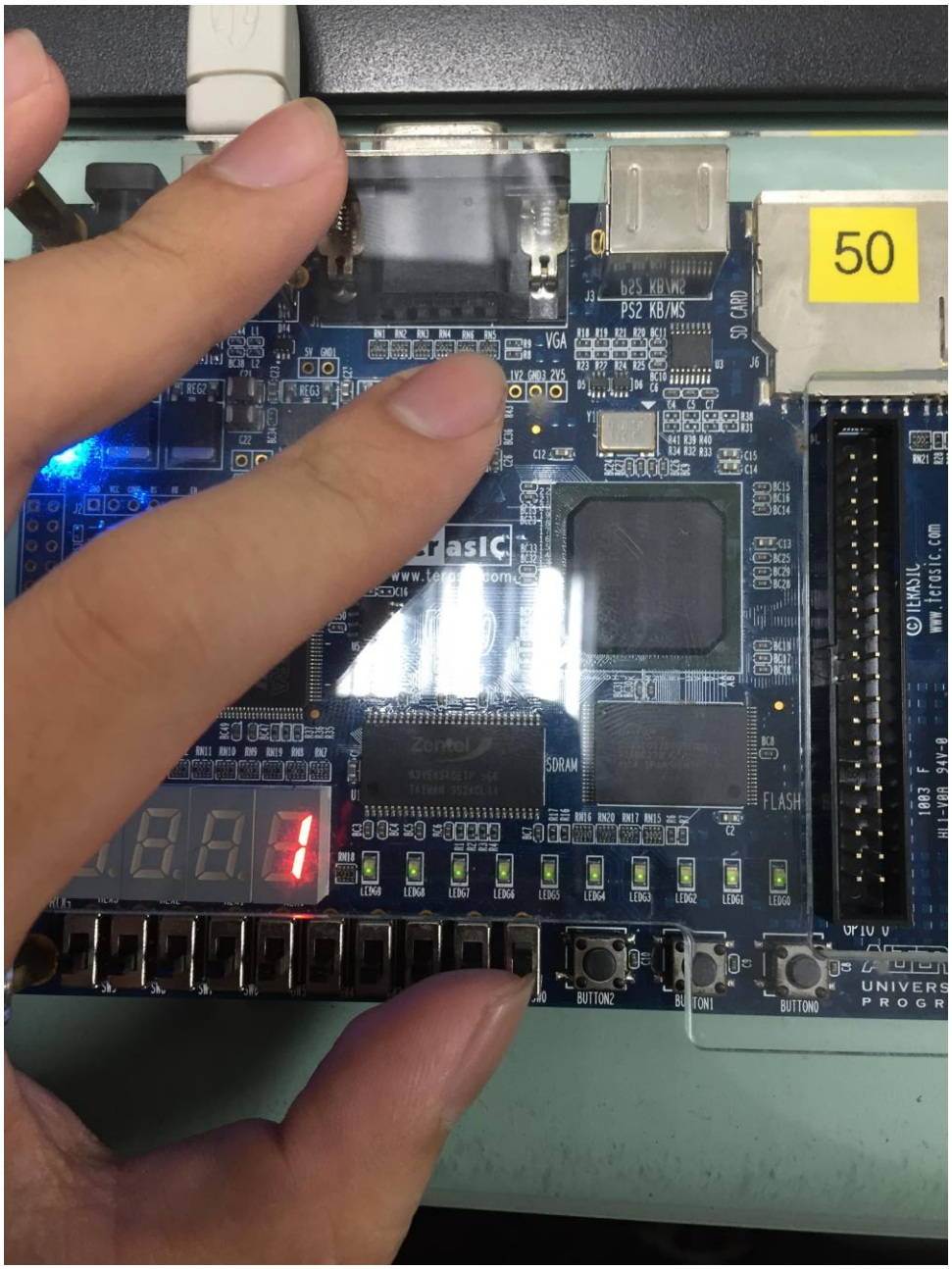
程式碼:

```
library ieee;
use ieee.std_logic_1164.all;
entity sevseg_UP1 is
port(    SW:in std_logic_vector(3 downto 0);
          HEX0_D:out std_logic_vector(0    to 6));
end sevseg_UP1;

architecture a of sevseg_UP1 is
begin
          process(SW)
begin
            if SW= "0000" then HEX0_D<="0000001";
            elsif SW="0001" then HEX0_D<="1001111";
            elsif SW="0010" then HEX0_D<="0010010";
            elsif SW="0011" then HEX0_D<="0000110";
          elsif SW="0100" then HEX0_D<="1001100";
          elsif SW="0101" then HEX0_D<="0100100";
          elsif SW="0110" then HEX0_D<="0100000";
          elsif SW="0111" then HEX0_D<="0001111";
          elsif SW="1000" then HEX0_D<="0000000";
          elsif SW="1001" then HEX0_D<="0000100";
          elsif SW="1010" then HEX0_D<="0001000";
          elsif SW="1011" then HEX0_D<="1100000";
          elsif SW="1100" then HEX0_D<="0110001";
          elsif SW="1101" then HEX0_D<="1000010";
          elsif SW="1110" then HEX0_D<="0110000";
          else HEX0_D<="0111000" ;
          end if;
          end process;
 end a;
```

模 擬 結 果 ：

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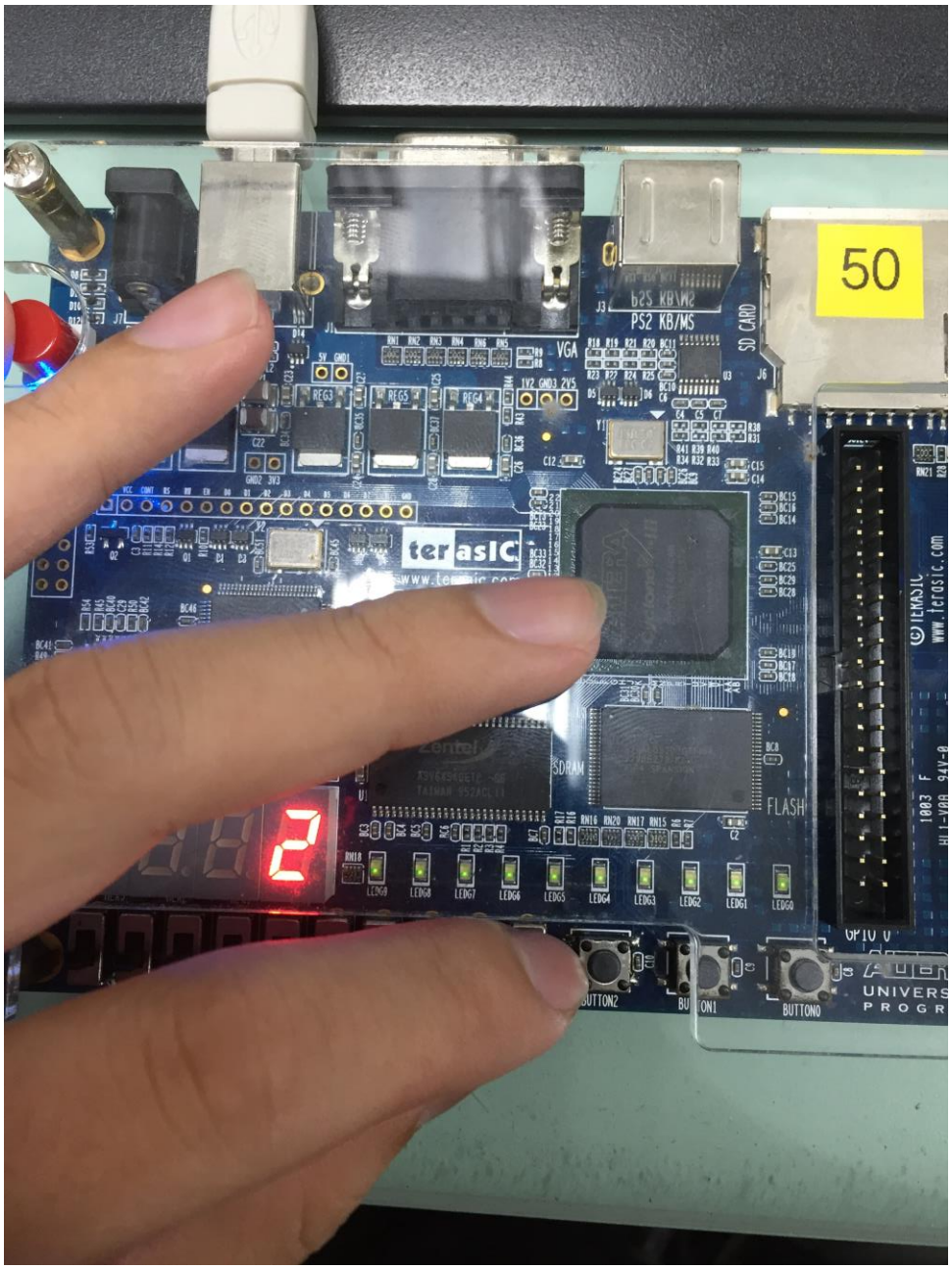
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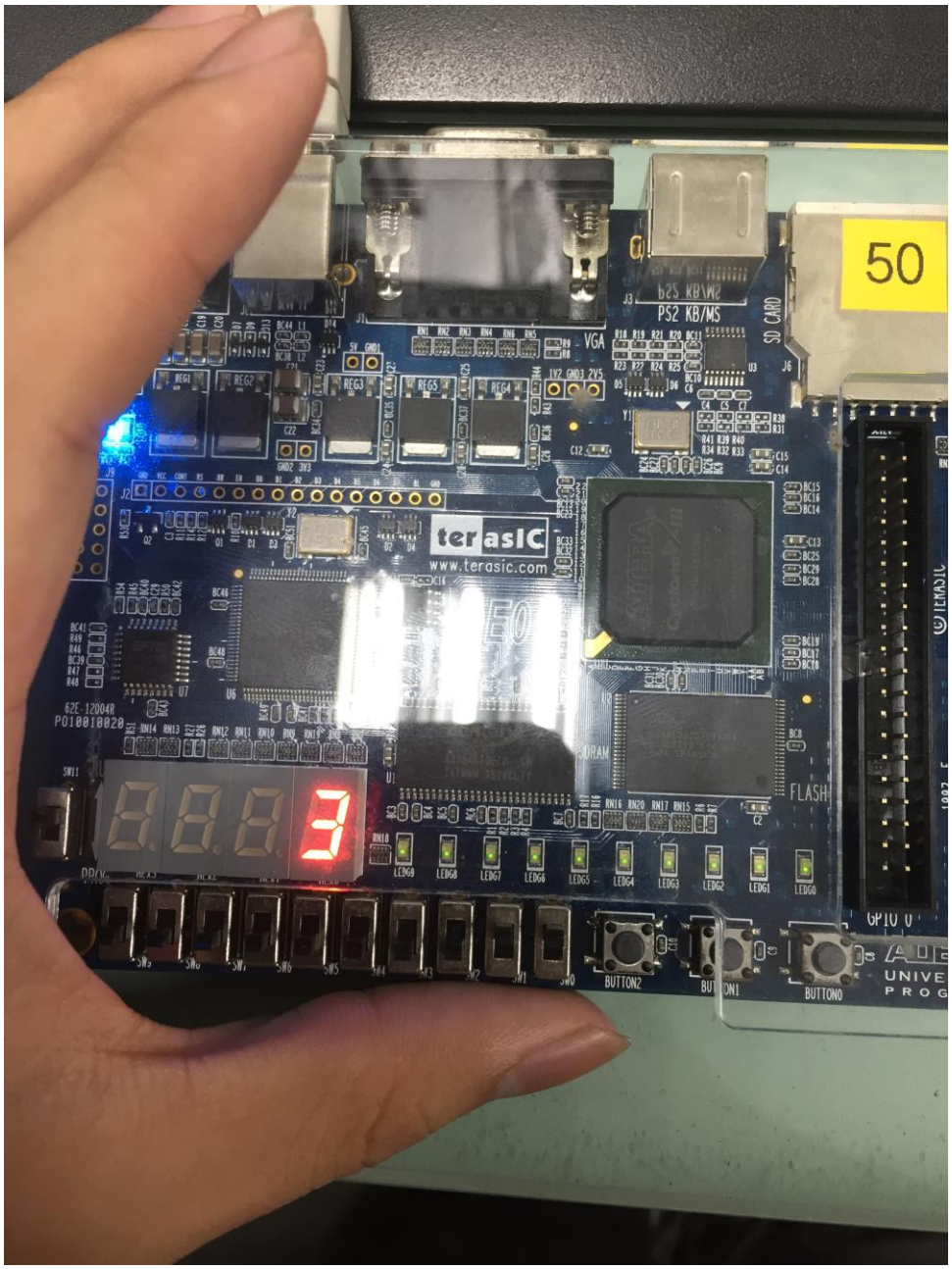
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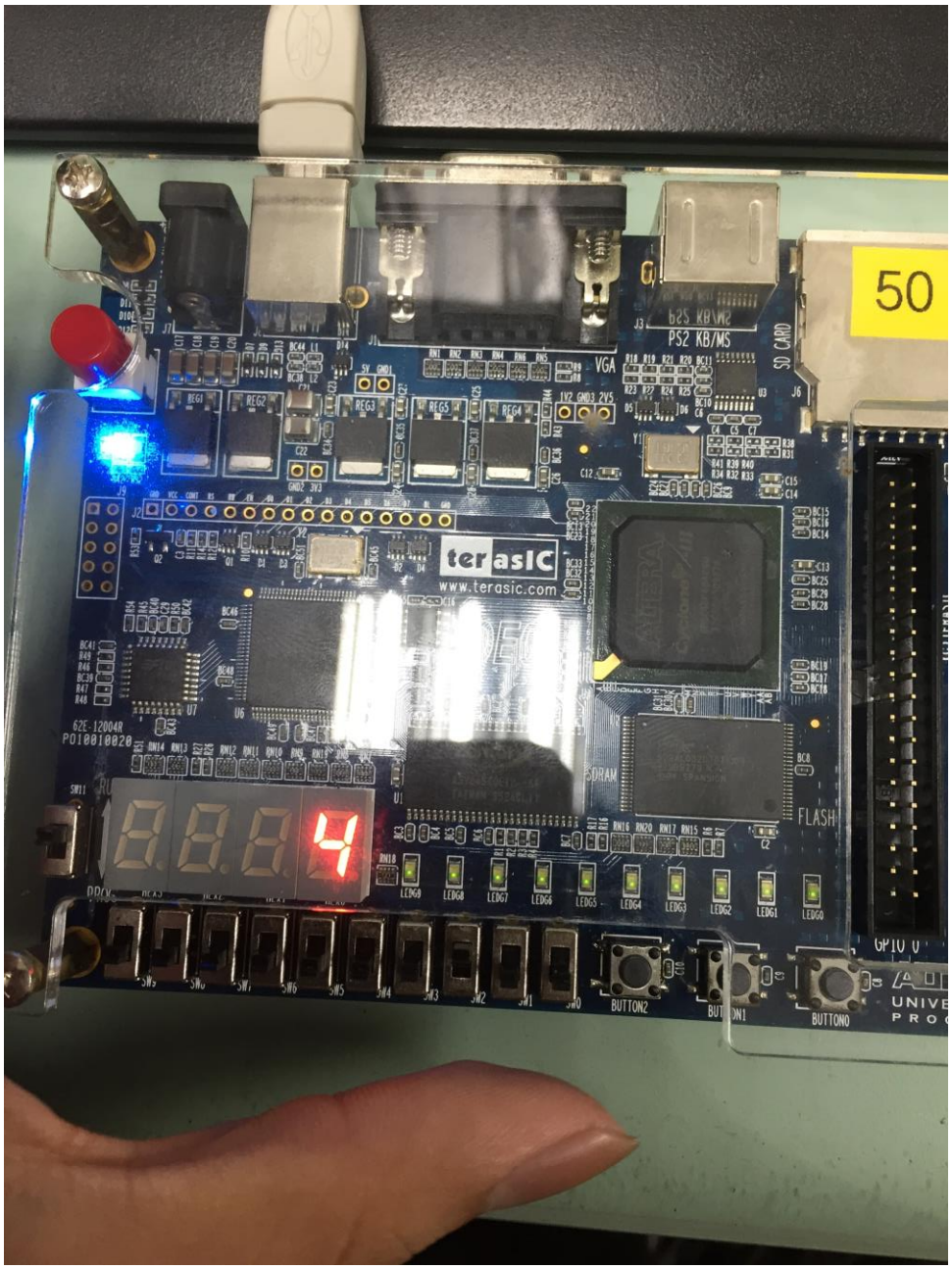
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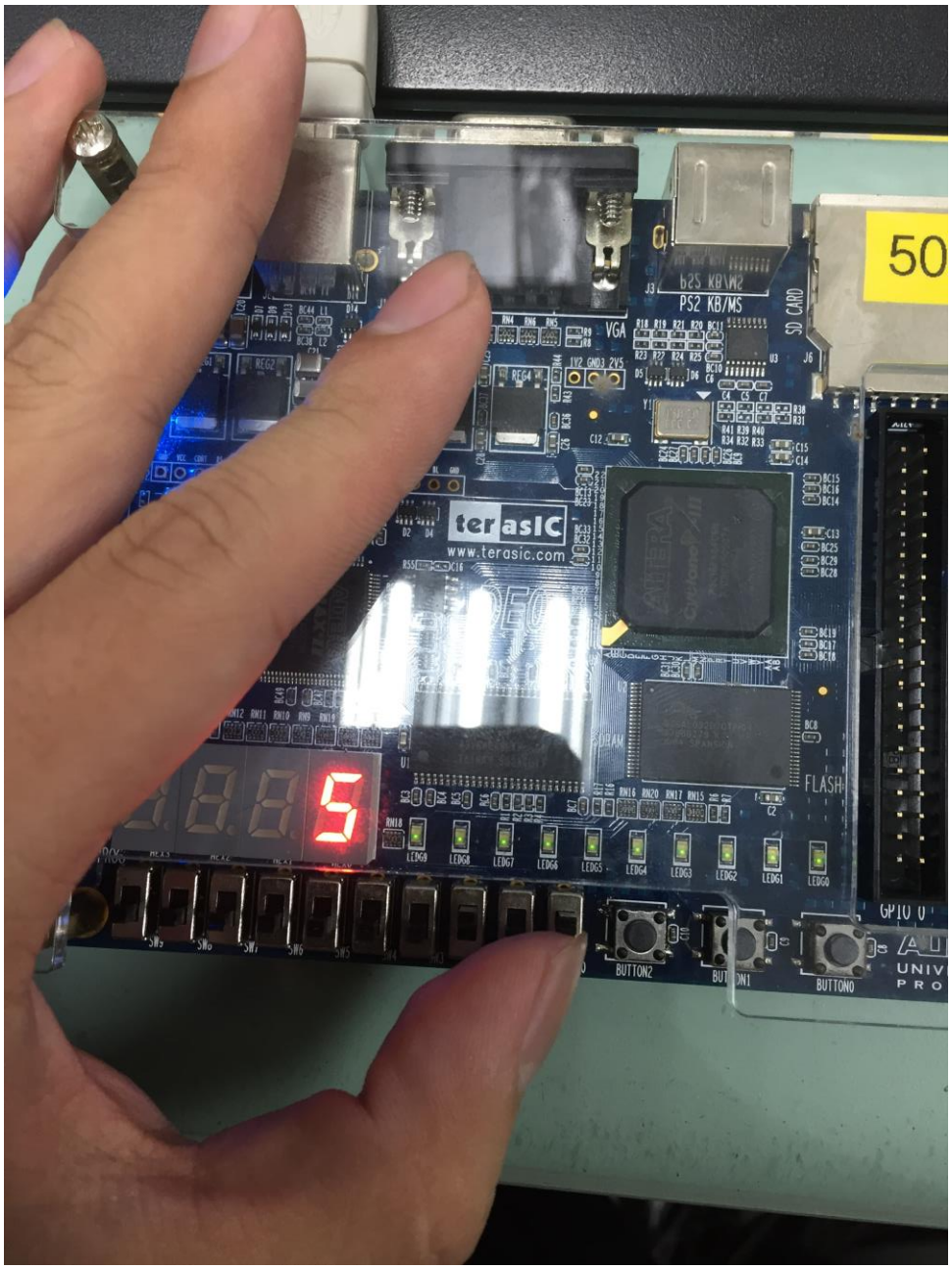
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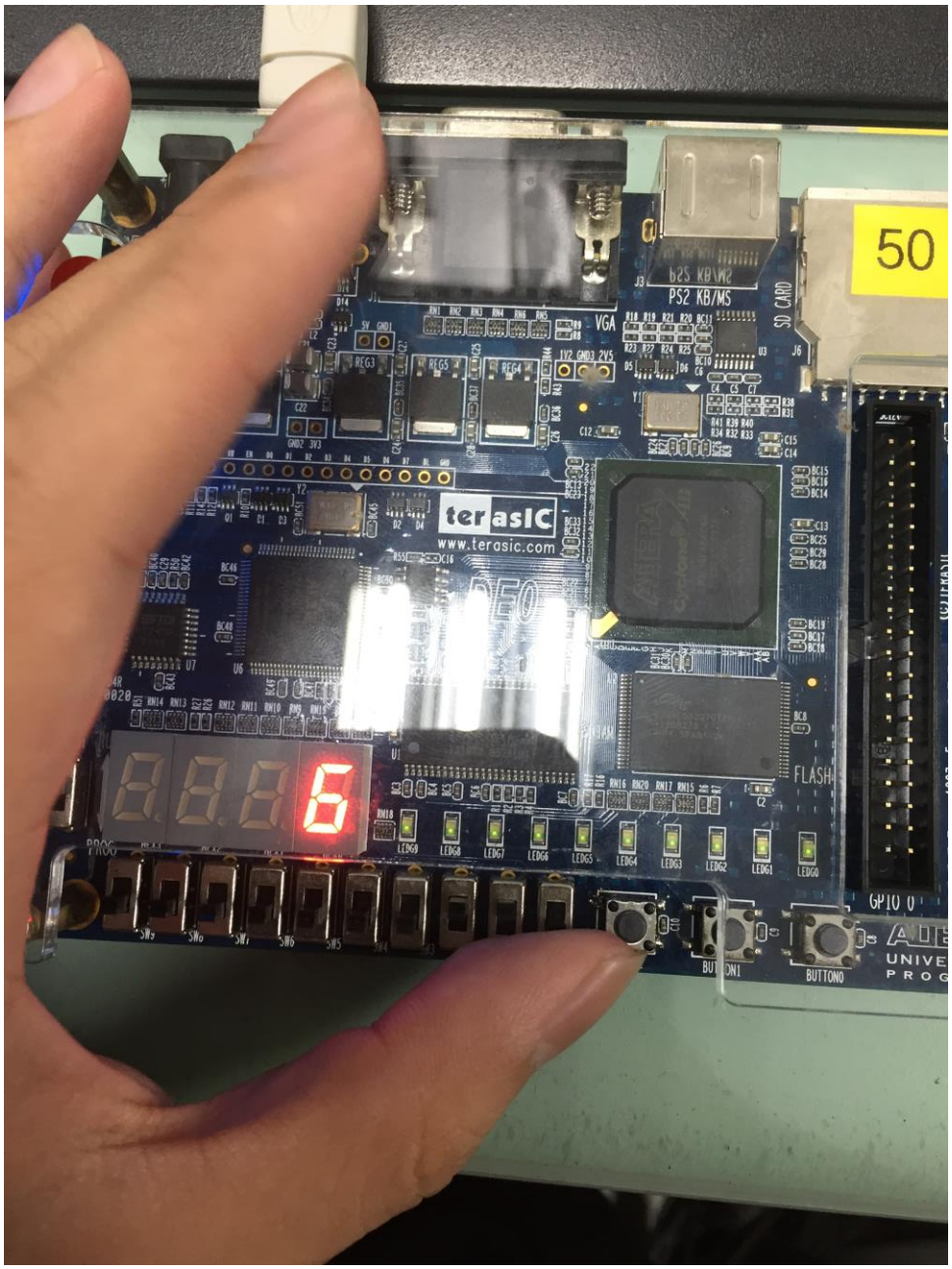
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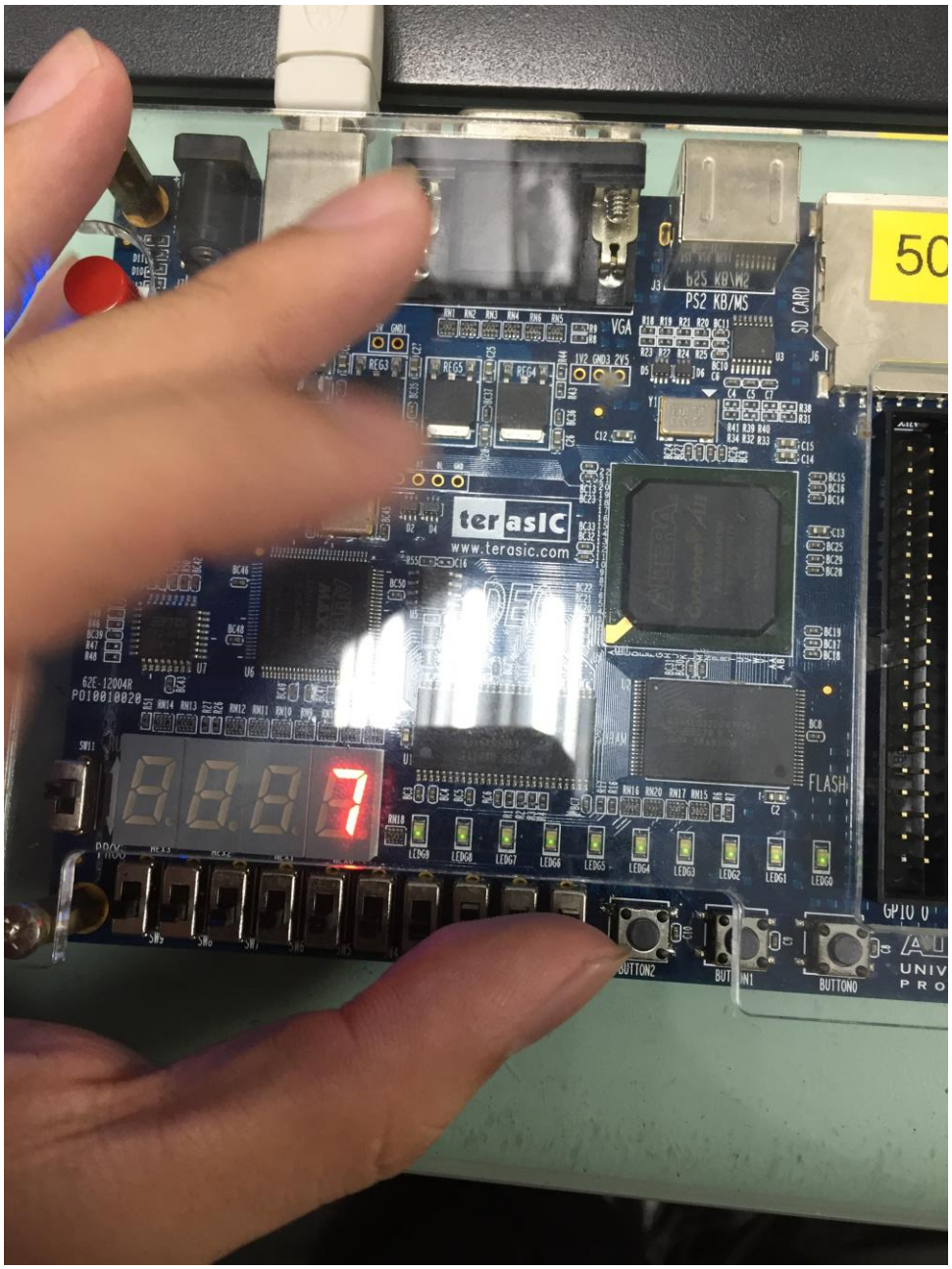
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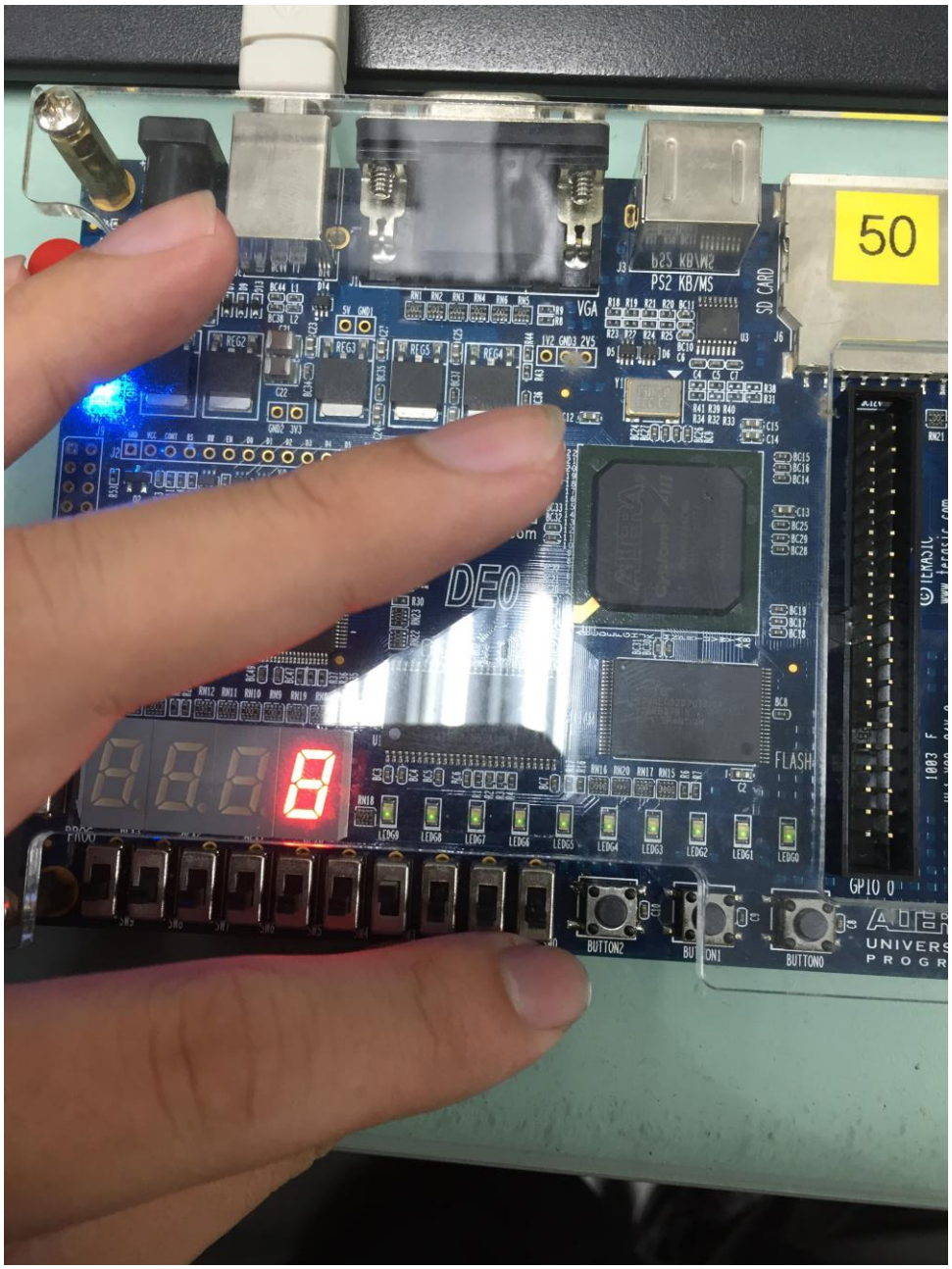
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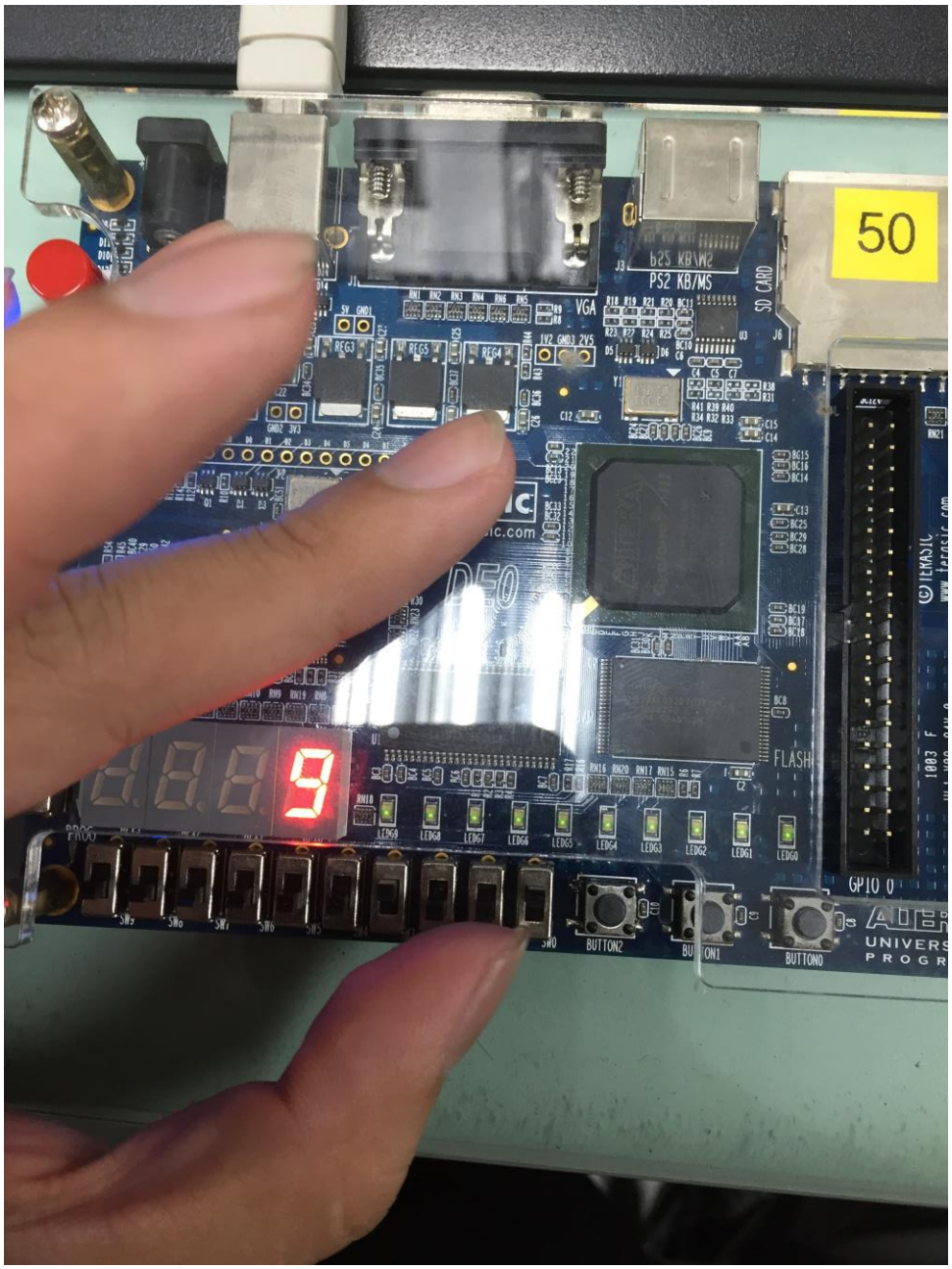
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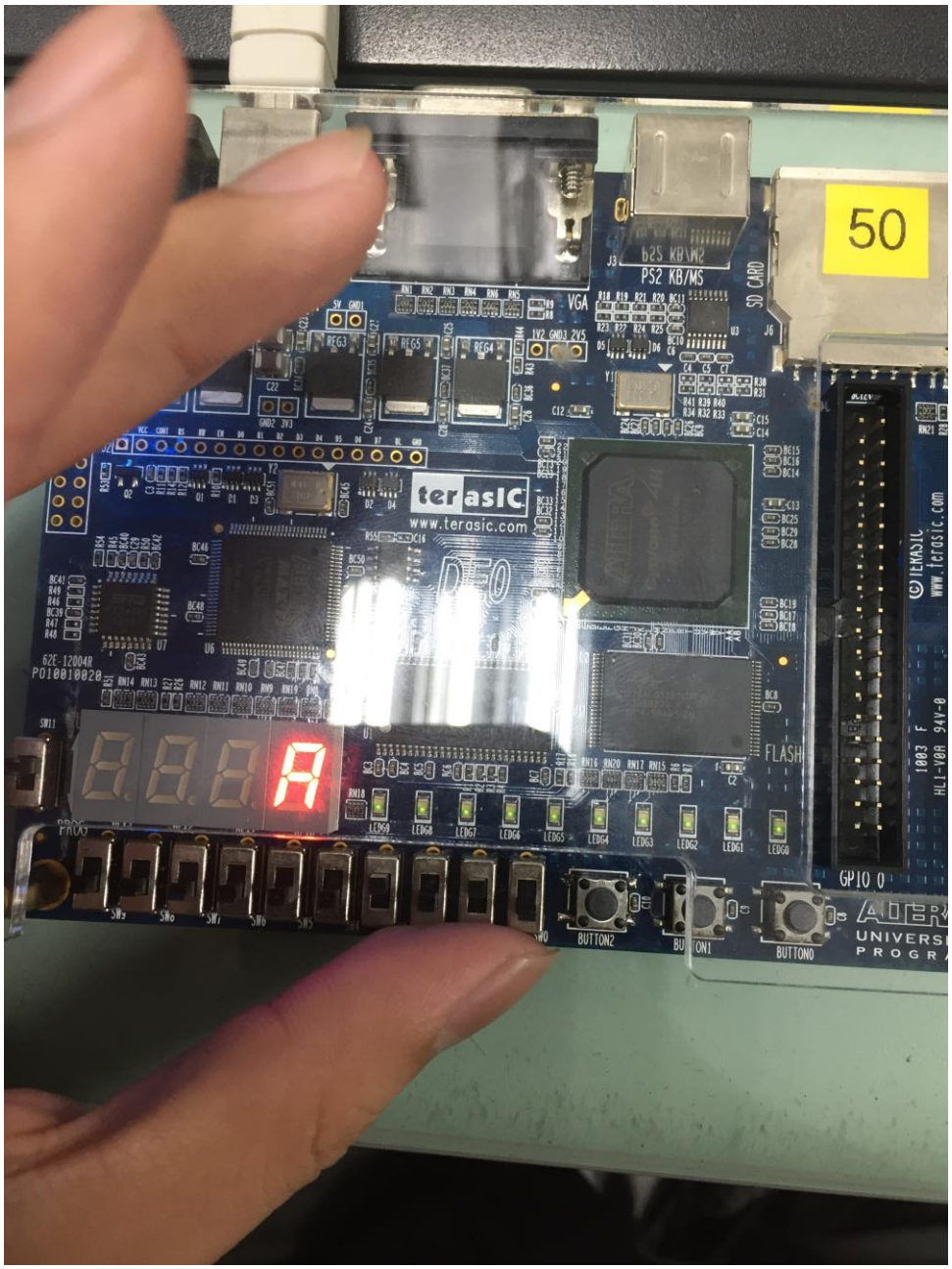
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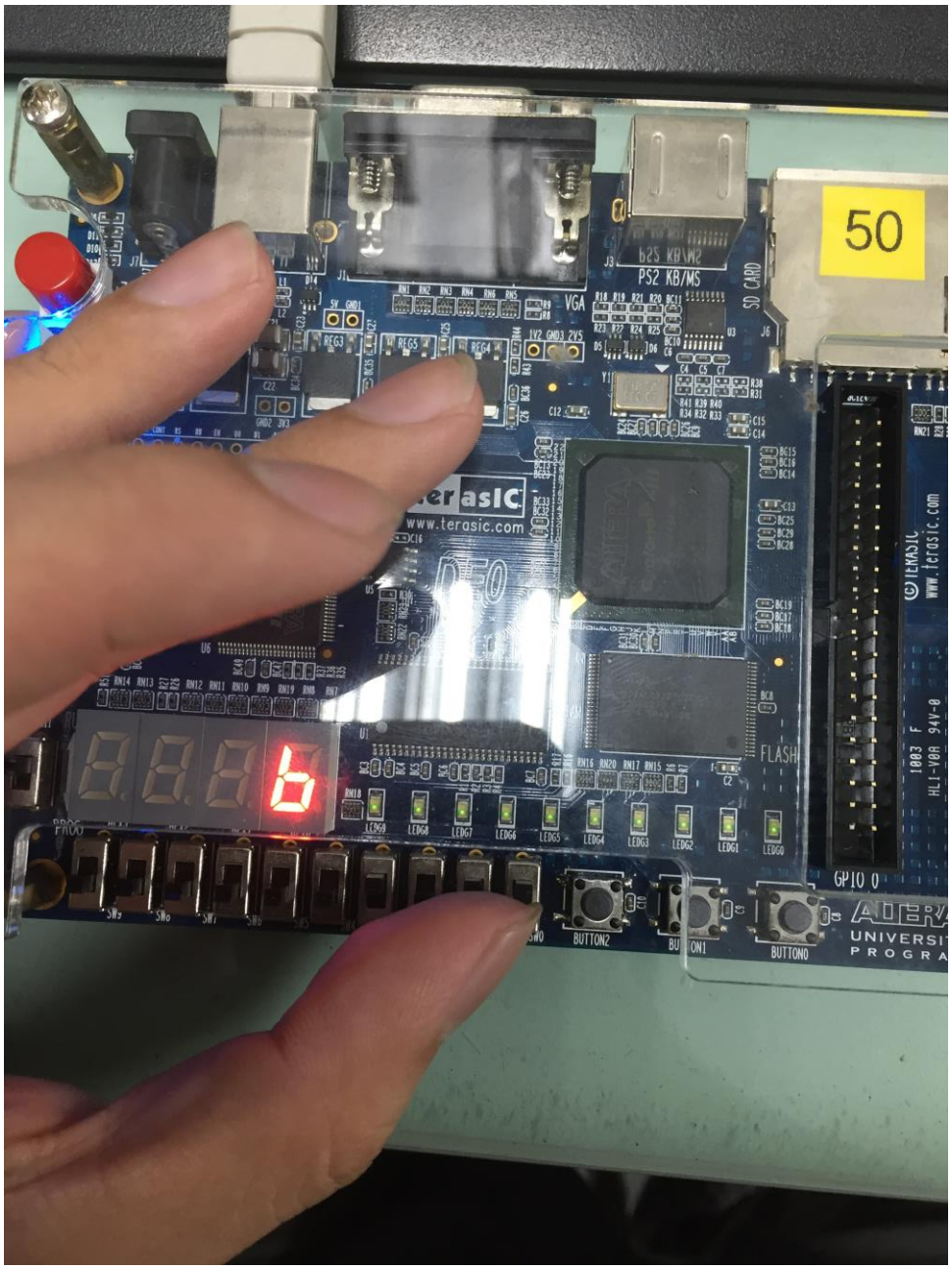
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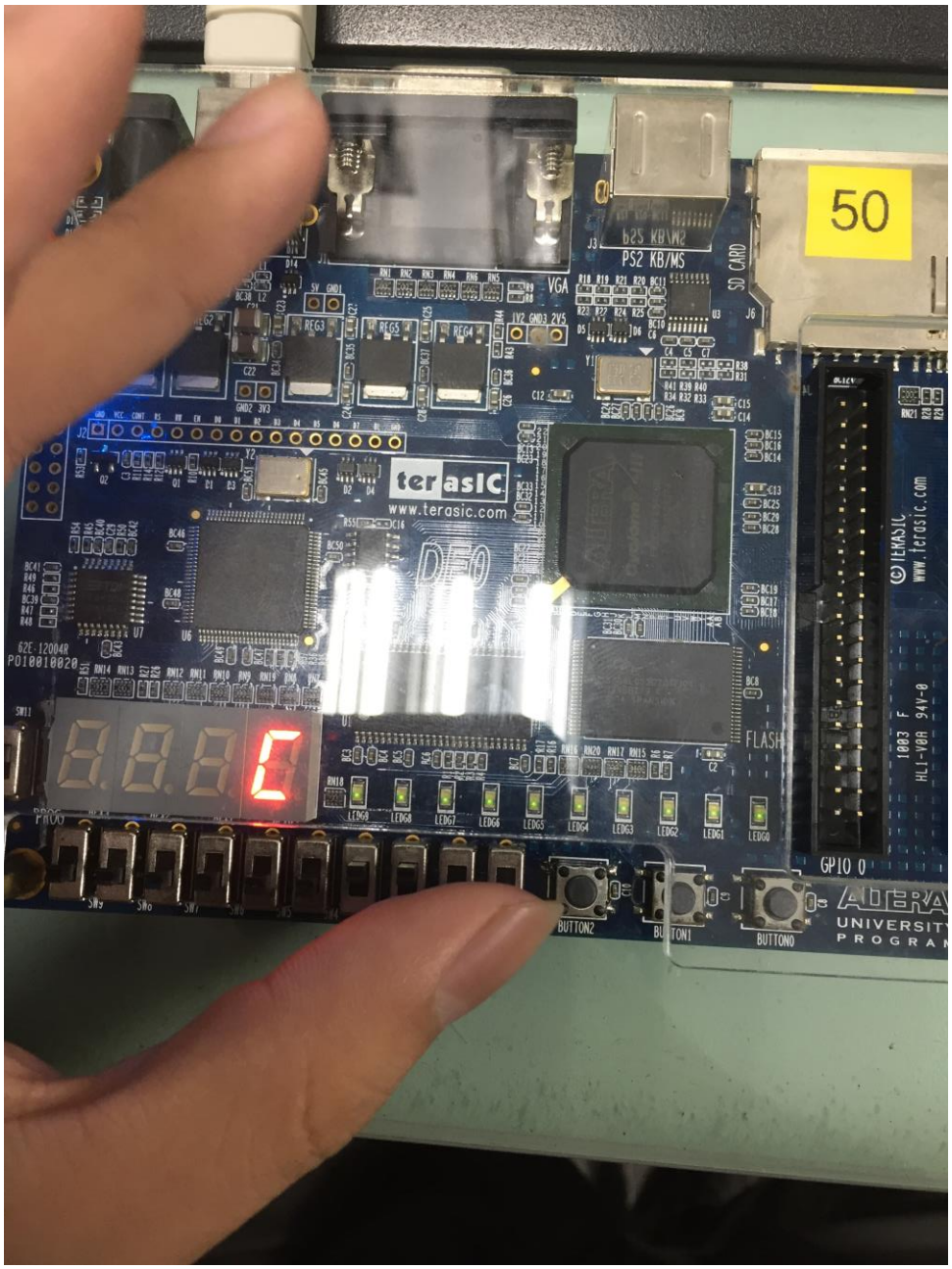
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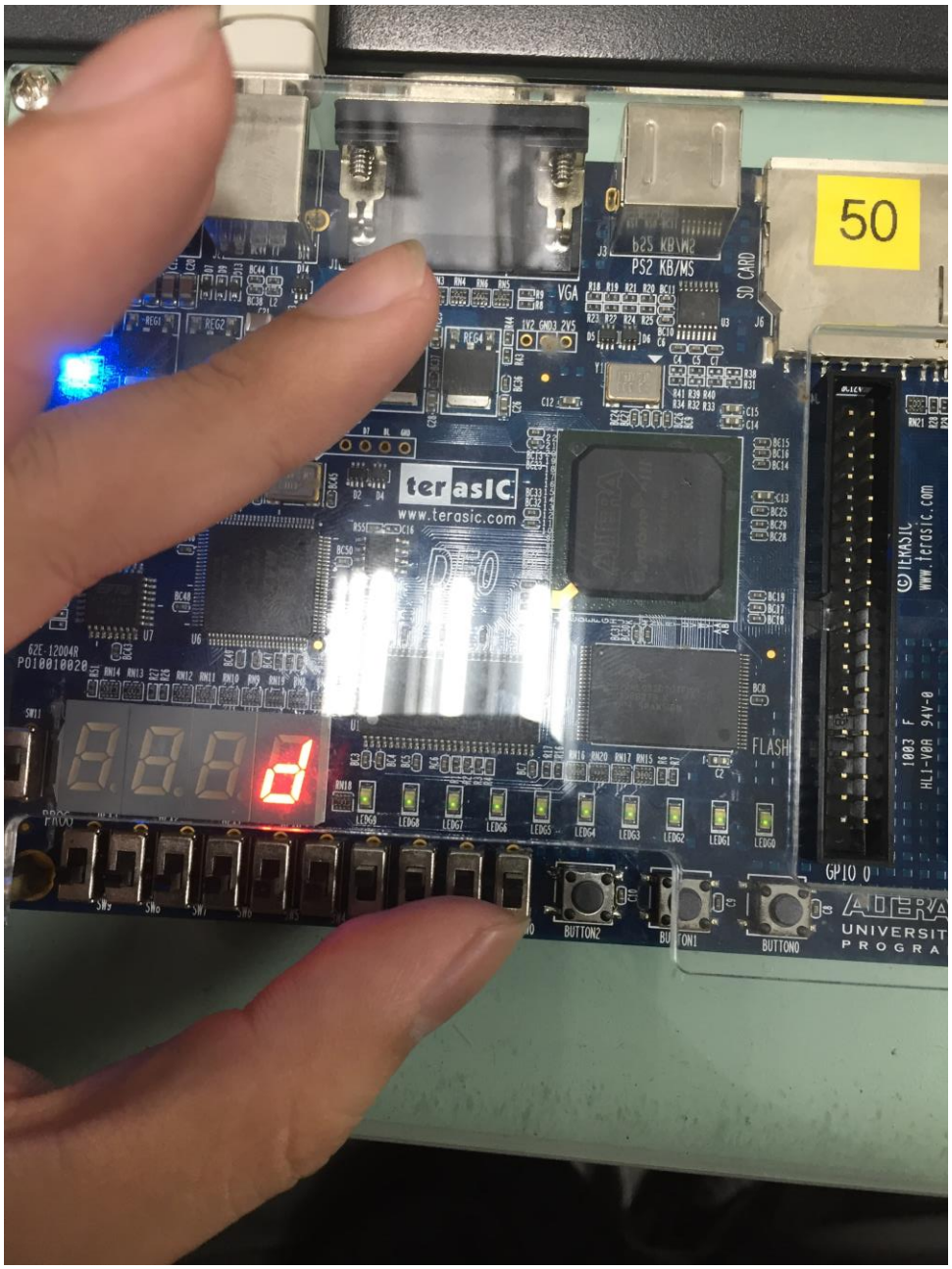
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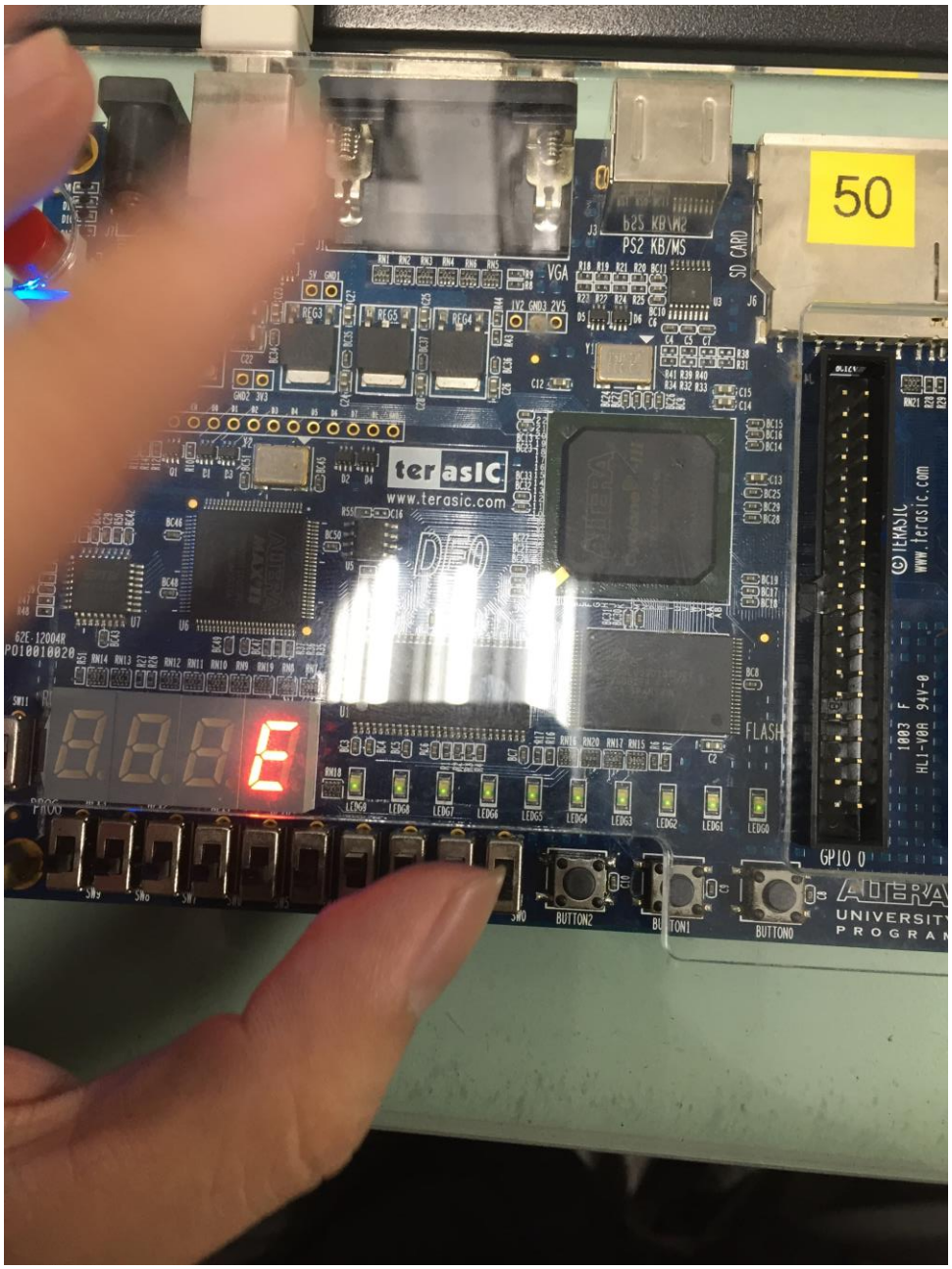
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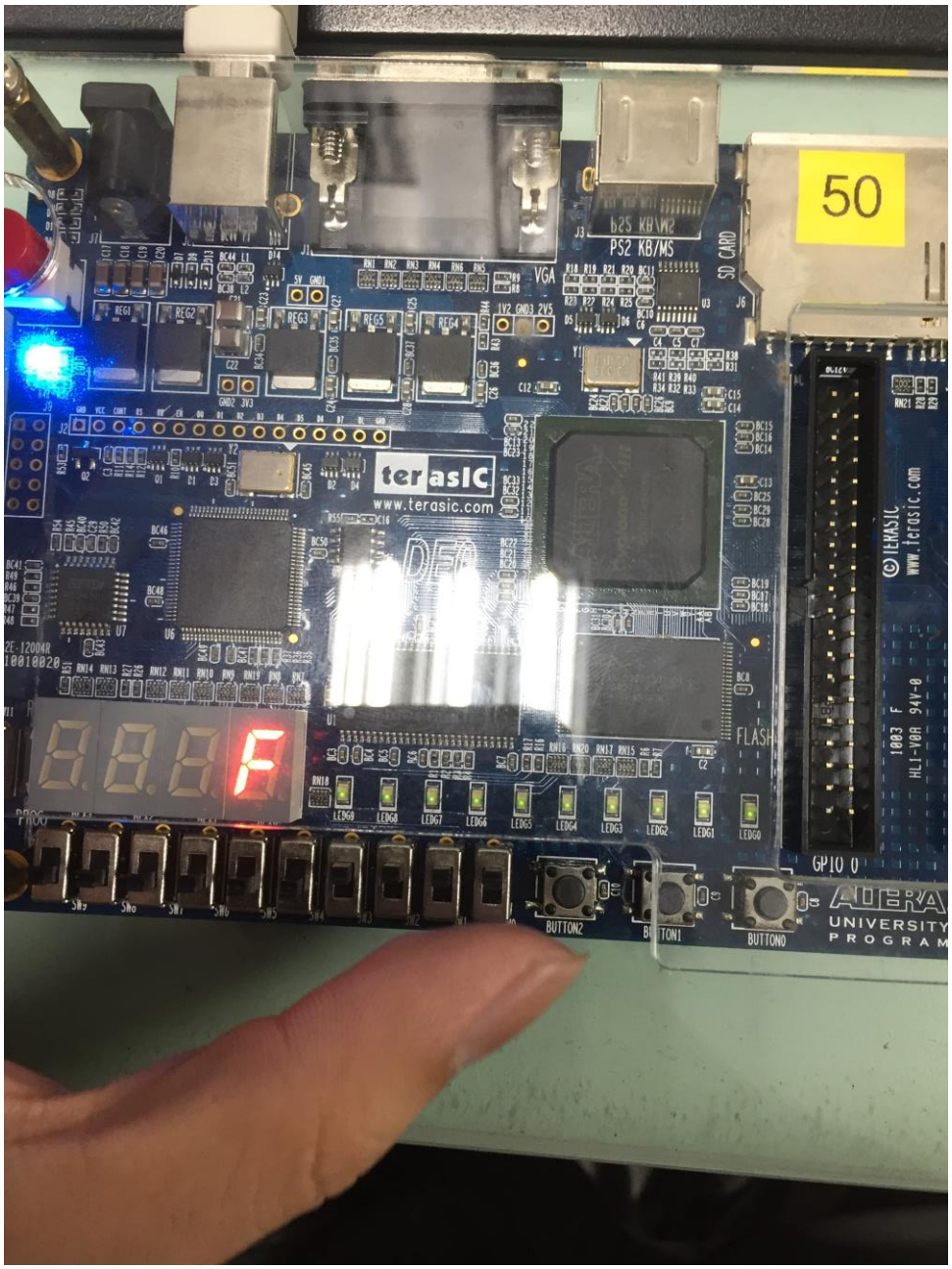
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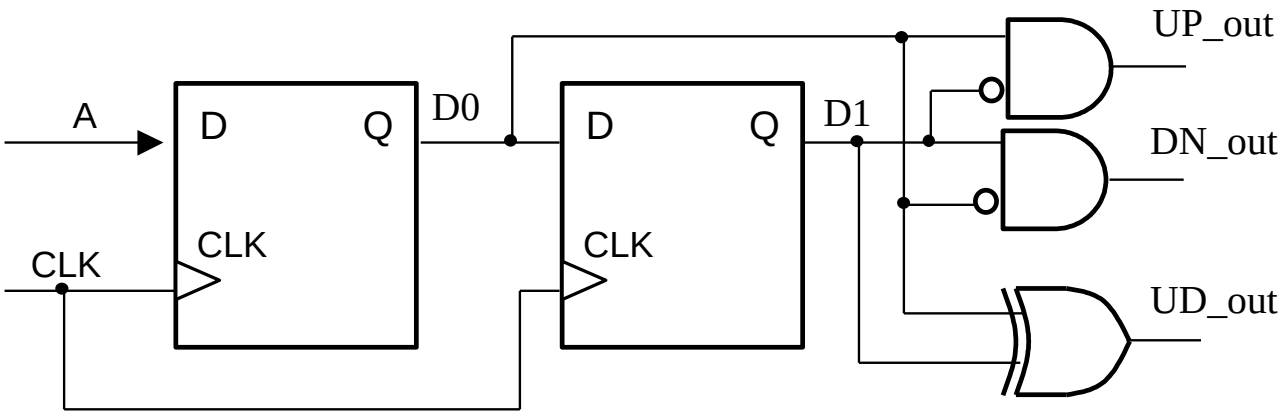
第二題

問題描述: 試完成下面的微分電路；其中 UP_out 為上緣微分，DN_out 為下緣微分，而 UD_out 為上下緣微分。

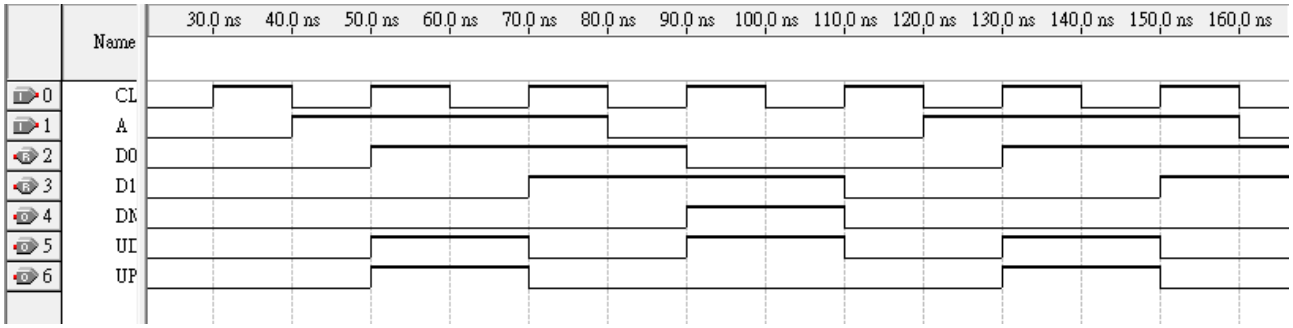


程式碼:

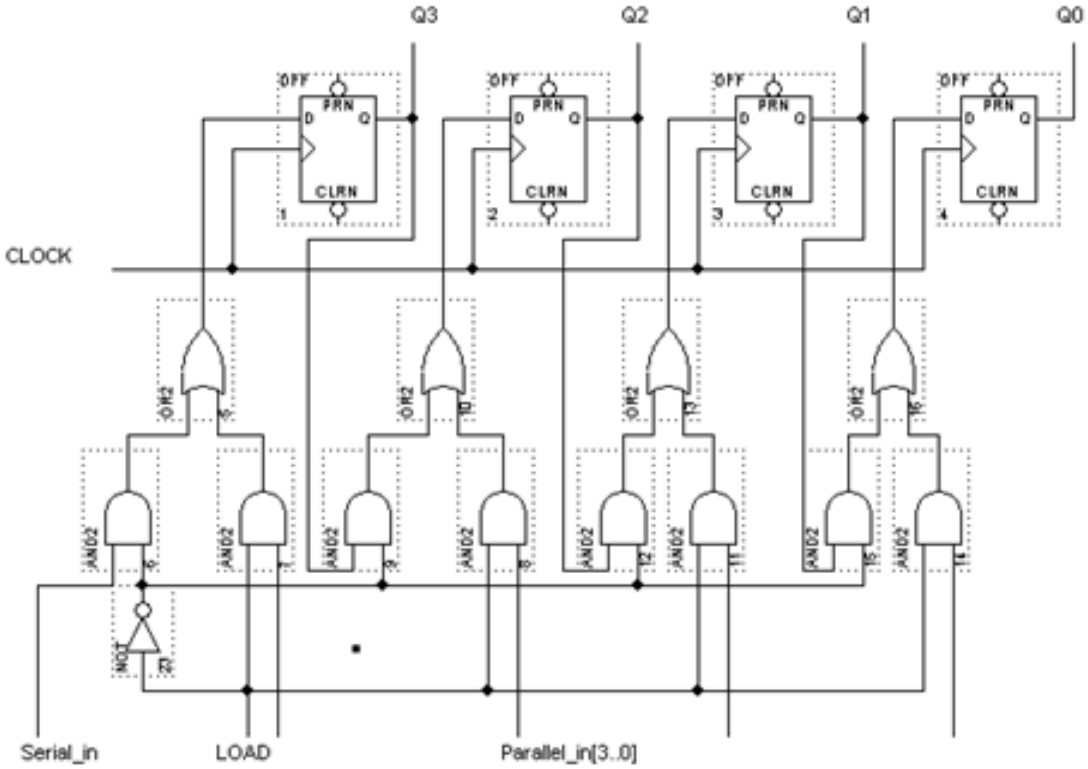
```
library ieee;
use ieee.std_logic_1164.all;

entity dd is
	port(A, CLK : in std_logic;
		UP ,DN ,UD		: out std_logic);
end dd;

architecture behavioral of dd	is
	signal D0, D1: std_logic;
begin
D_ff: process(CLK)
	begin
		if CLK'event and CLK='1' then
			D0 <= A;
			D1 <= D0;
		end if;
	end process D_ff;

		UP <= D0 AND (not D1);
		DN <= D1 and (not D0);
		UD <= D0 xor D1;
```

```
end behavioral;
```

模擬結果:



第三題



問題描述:

程式碼:

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY abc IS
      PORT (Parallel_in : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
      Clock : IN STD_LOGIC;
      Serial_in : IN STD_LOGIC;
      LOAD:IN STD_LOGIC;
      Q : BUFFER    STD_LOGIC_VECTOR(3 DOWNTO 0));
END abc;

ARCHITECTURE a OF abc IS
BEGIN
process
   begin
   wait until Clock'EVENT AND Clock ='1';
    if LOAD ='1' then
         Q <= Parallel_in;
    else
```

```
            Q(0)<=Q(1) ;
            Q(1)<=Q(2) ;
            Q(2)<=Q(3);
            Q(3)<=Serial_in;
      end if;
end process;
END a;
```

模　　擬　　結　　果　　：