CPLD 設計作業

銘傳大學電腦與通訊工程系

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組別	第 27 組
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實習成果	本次應繳作業共 2 題，完成 2 題
時間	2017/12/1

第一題

問題描述: **實現一個 1Hz 頻率計數的 3 bits 計數器**

程式碼:計數器

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.std_logic_unsigned.all;
ENTITY aa IS
PORT(    x,CLK :IN STD_LOGIC;
               OP        :OUT std_logic_vector(2 downto 0));
END aa;

ARCHITECTURE a OF aa IS
BEGIN
PROCESS(clk)
variable present_state: std_logic_vector (2 downto 0);
         BEGIN
IF clk'event and clk='1' then
                   CASE present_state IS
                     WHEN "000" =>
                             if x='1' then    present_state:="001";
                             else present_state:="111";
                             end if;
                     WHEN "001" =>
                             if x='1' then    present_state:="010";
                             else present_state:="000";
                             end if;
                     WHEN "010" =>
                             if x='1' then    present_state:="011";
                             else present_state:="001";
                             end if;
                     WHEN "011" =>
                             if x='1' then    present_state:="100";
                             else present_state:="010";
                             end if;
                   WHEN "100" =>
```

```
            if x='1' then    present_state:="101";
            else present_state:="011";
            end if;
        WHEN "101" =>
            if x='1' then    present_state:="110";
            else present_state:="100";
            end if;
        WHEN "110" =>
            if x='1' then    present_state:="111";
            else present_state:="101";
            end if;
        WHEN "111" =>
            if x='1' then    present_state:="000";
            else present_state:="110";
            end if;
        WHEN others=>
            if x='1' then    present_state:="000";
            else present_state:="000";
            end if;
        END CASE;
    end if;
    op<= present_state;
END PROCESS;
END a;
```

1HZ 除頻

```
library ieee;
use ieee.std_logic_1164.all;


entity slowCLK is
  generic(divisor:integer:=50000000);
port(    clockIN : in    std_logic;
         clockOUT: out std_logic);
end slowCLK;
architecture arch of slowCLK is
```

```
signal PULSE : std_logic;
begin
process(clockIN)
variable counter,divisor2 : integer range 0 to divisor;
begin
    divisor2:=divisor/2;
        if (clockIN 'event and clockIN ='1') then
            if counter = divisor then
                counter := 1;
            else
                counter := counter + 1;
            end if;
        end if;
if (clockIN 'event and clockIN ='1') then
            if (( counter= divisor2) or (counter = divisor))then
                PULSE <= not PULSE ;
            end if;
        end if;
        clockOUT <= PULSE ;
    end process;
end arch;
```

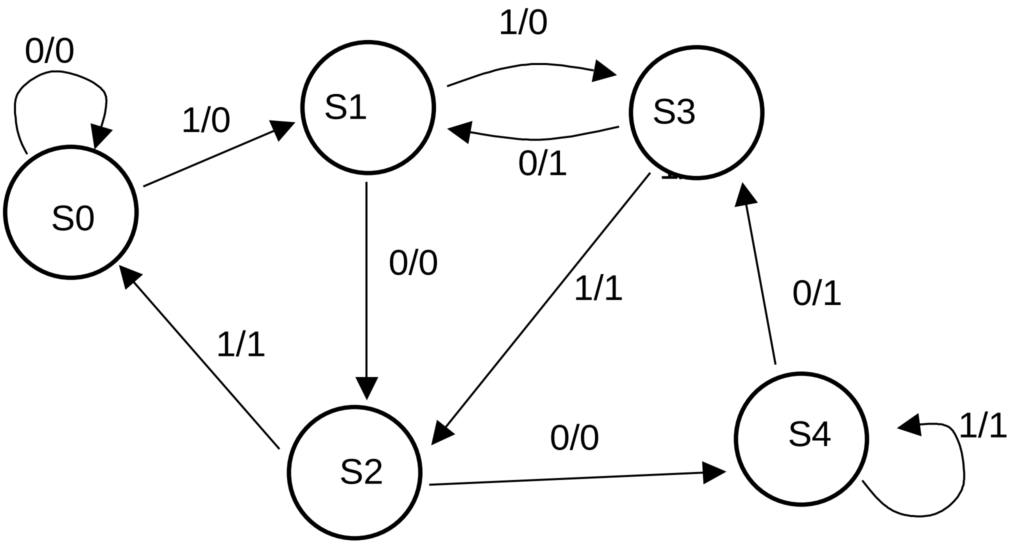
模擬結果:

逆時針:https://www.youtube.com/watch?v=8PIzlaCHh4s

順時針: https://www.youtube.com/watch?v=H_QdpNDrE-U

第二題

題目:　試實現下面之 Mealy 狀態機

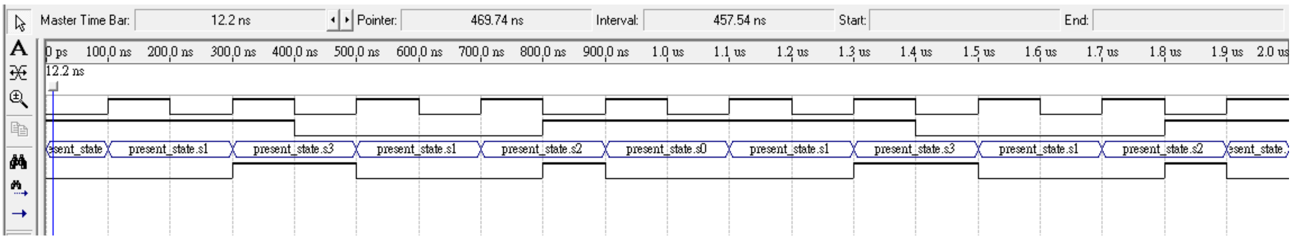


程式碼:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.std_logic_unsigned.all;
ENTITY dd IS
PORT(CLK    :IN STD_LOGIC;
        X       :IN STD_LOGIC;
        op      :OUT STD_LOGIC);
END dd;
ARCHITECTURE a OF dd IS
TYPE State IS (s0,s1,s2,s3,s4);
SIGNAL present_state : State;
SIGNAL next_state: State;
BEGIN
     state_comp: PROCESS(present_state)
```

```
BEGIN
CASE present_state IS
WHEN s0 =>
      IF X = '0' THEN
            next_state <= s0;
      ELSE
            next_state <= s1;
      END IF;
      IF X = '0' THEN
            op <= '0';
      ELSE
            op <= '0';
      END IF;
 WHEN s1 =>
      IF X = '0' THEN
            next_state <= s2;
      ELSE
            next_state <= s3;
      END IF;
      IF X = '0' THEN
            op <= '0';
      ELSE
            op <= '0';
      END IF;
WHEN s2 =>
      IF X = '0' THEN
```

```
            next_state <= s4;
        ELSE
            next_state <= s0;
        END IF;
        IF X = '0' THEN
            op <= '0';
        ELSE
            op <= '1';
        END IF;
    WHEN s3 =>
        IF X = '0' THEN
            next_state <= s1;
        ELSE
            next_state <= s2;
        END IF;
        IF X = '0' THEN
            op <= '1';
        ELSE
            op <= '1';
        END IF;
    WHEN s4 =>
        IF X = '0' THEN
            next_state <= s3;
        ELSE
            next_state <= s4;
        END IF;
        IF X = '0' THEN

            op <= '1';

        ELSE

            op <= '1';

        END IF;

    END CASE;

    END PROCESS state_comp;


        state_clocking: PROCESS (CLK)

    BEGIN

        IF CLK'EVENT AND CLK = '1' THEN

            present_state <= next_state;

        END IF;

    END PROCESS state_clocking;

END a;
```



Master Time Bar: 12.2 ns

Pointer: 469.74 ns

Interval: 457.54 ns

Start:

End: