CPLD 設計作業

銘傳大學電腦與通訊工程系

班　　級	電通二乙
組　　別	第 27 組
組員姓名/學號	陳韋澔/05050032
組員姓名/學號	陳奕璁/05050536
作業撰寫人	陳韋澔
授課教師	陳慶逸
實習成果	本次應繳作業共 3 題，完成 3 題
時　　間	2017/12/08

第一題

■ 問題描述: 利用階層式設計實現一個半加法器(h_adder.vhd)

(互斥或閘: xor_2.vhd, 及閘: and_2.vhd)。

程式碼: h_adder

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

ENTITY h_adder IS
PORT (    A,B : IN STD_LOGIC;
             Sum,Carry : out    STD_LOGIC);
END h_adder;
ARCHITECTURE a OF h_adder IS
    component and_2
       port ( A,B :in std_logic;
                    Carry : out std_logic );
    end component;

    component xor_2
       port ( A,B :in std_logic;
                    Sum      :out std_logic );
    end component;

BEGIN
    U1:and_2 port map(A,B,Carry);
    U2:xor_2 port map(A,B,Sum);
END a;
```

and_2

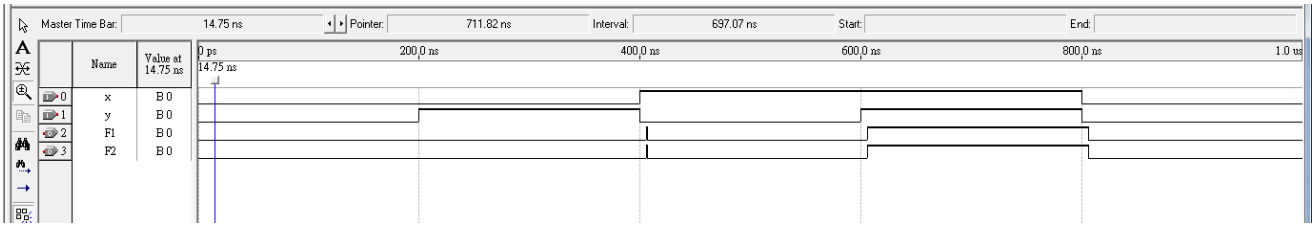
```
library ieee;
    use ieee.std_logic_1164.all;
    entity and_2 is
    port ( A,B    :in std_logic;
                Carry         :out std_logic);
```

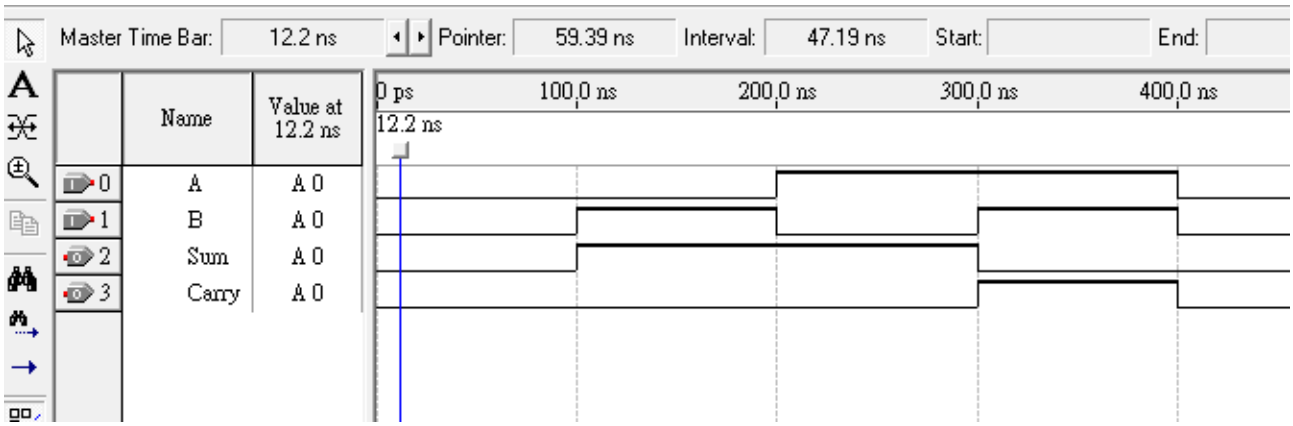
```
end or_2;
ARCHITECTURE a OF or_2 IS
    begin
        Carry <=A and B;
            end a;
```

xor_2

```
library ieee;
    use ieee.std_logic_1164.all;

    entity or_2 is
    port ( A,B    :in std_logic;
                Sum       :out std_logic);
    end or_2;

    ARCHITECTURE a OF or_2 IS
    begin
        Sum<=A xor B;
    end a;
```

模擬結果:




Master Time Bar: 12.2 ns
Pointer: 59.39 ns
Interval: 47.19 ns
Start:
End:
Name
Value at 12.2 ns
0 ps
100.0 ns
200.0 ns
300.0 ns
400.0 ns
12.2 ns
0 A A 0
1 B A 0
2 Sum A 0
3 Carry A 0

第二題

- 問題: 利用階層式設計實現一個 4-bit 加法器(add_4_bits.vhd)

  (1-bit 加法器: add_1_bit.vhd)。

程式碼: add_4_bits

```
library IEEE;
 use IEEE.std_logic_1164.all;


 entity add_4_bits is
 port ( A: in std_logic_vector(3 DOWNTO 0);
          B: in std_logic_vector(3 DOWNto 0);
          C: in std_logic;
          Sum: out std_logic_vector(3 DOWNto 0);
          Carry: out std_logic );
 end add_4_bits;
ARCHITECTURE a OF add_4_bits IS
    component add_1_bit
      port ( A,B,C :in std_logic;
                Sum,Carry : out std_logic );
   end component;

   signal s1,s2,s3 :std_logic;
BEGIN
   U1:add_1_bit port map(C,A(0),B(0),s1,Sum(0));
   U2:add_1_bit port map(s1,A(1),B(1),s2,Sum(1));
   U3:add_1_bit port map(s2,A(2),B(2),s3,Sum(2));
```

```
    U4:add_1_bit port map(s3,A(3),B(3),Carry,Sum(3));
END a;
```

add_1_bit

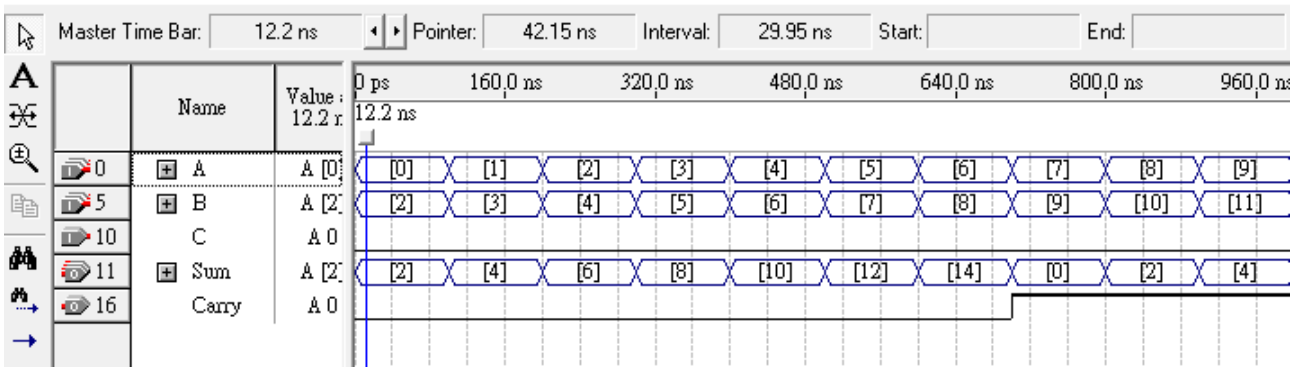
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

ENTITY add_1_bit IS
PORT (    A,B,C : IN STD_LOGIC;
          Sum,carry : out    STD_LOGIC);
END add_1_bit;
ARCHITECTURE a OF add_1_bit IS
    component h_adder
       port ( A,B :in std_logic;
                 Sum,Carry : out std_logic );
    end component;

    component or_2
       port ( A,B :in std_logic;
                 Carry       :out std_logic );
    end component;

signal s1,s2,s3 :std_logic;
BEGIN
    U1:h_adder port map(A,B,s1,s3);
    U2:h_adder port map(s1,C,sum,s2);
    U3:or_2 port map(s2,s3,carry);
```

```
END a;
```

or_2

```
library ieee;
    use ieee.std_logic_1164.all;
    entity or_2 is
    port ( A,B    :in std_logic;
           Carry        :out std_logic);
    end or_2;
    ARCHITECTURE a OF or_2 IS
      begin
          Carry<=A or B;
            end a;
```

實　　驗　　結　　果　　：



第三題

問題: **以 5 個四對一的多工器實現一個十六對一的多工器。**

程式碼: mux16to1c

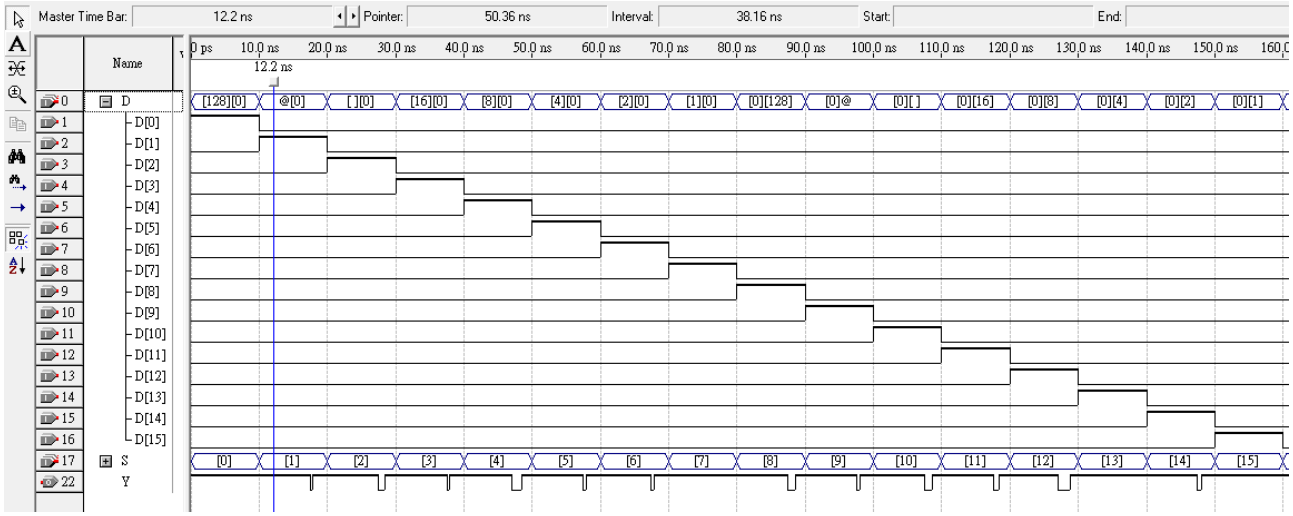
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

ENTITY mux16to1c IS
PORT (    D : IN STD_LOGIC_vector(0 to 15);
          S : IN    STD_LOGIC_vector(3 downto 0);
          Y : OUT STD_LOGIC);
END mux16to1c ;

ARCHITECTURE a OF mux16to1c IS
component mux4_1 is
port ( d0,d1,d2,d3 :in std_logic;
          S1,S0      :in std_logic;
          Y                  :out std_logic );
end component;
signal m :std_logic_vector(0 to 3);
BEGIN

    U1:mux4_1 port map(D(0),D(1),D(2),D(3),S(1),S(0),m(0));
    U2:mux4_1 port map(D(4),D(5),D(6),D(7),S(1),S(0),m(1));
    U3:mux4_1 port map(D(8),D(9),D(10),D(11),S(1),S(0),m(2));
    U4:mux4_1 port map(D(12),D(13),D(14),D(15),S(1),S(0),m(3));
```

```
    U5:mux4_1 port map(m(0),m(1),m(2),M(3),S(3),S(2),Y);
END a;
```

mux4_1

```
library ieee;
    use ieee.std_logic_1164.all;

    entity mux4_1 is
    port ( d0,d1,d2,d3    :in std_logic;
                S1,S0      :in std_logic;
                Y          :out std_logic);
    end mux4_1;

    ARCHITECTURE a OF mux4_1 IS
    begin
        Y <= ((not S1)and (not S0)and d0)
                or((not S1)and S0 and d1)
                or (S1 and (not S0)and d2)
                  or (S1 and S0 and d3);

    end a;
```

實　　驗　　結　　果　　:


Master Time Bar: 12.2 ns
Pointer: 50.36 ns
Interval: 38.16 ns
Start:
End:
Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
110.0 ns
120.0 ns
130.0 ns
140.0 ns
150.0 ns
12.2 ns
0 D
D[0]
D[1]
D[2]
D[3]
D[4]
D[5]
D[6]
D[7]
D[8]
D[9]
D[10]
D[11]
D[12]
D[13]
D[14]
D[15]
17 S
22 Y
[128][0]
@[0]
[ ][0]
[16][0]
[8][0]
[4][0]
[2][0]
[1][0]
[0][128]
[0]@
[0][ ]
[0][16]
[0][8]
[0][4]
[0][2]
[0][1]
[0]
[1]
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