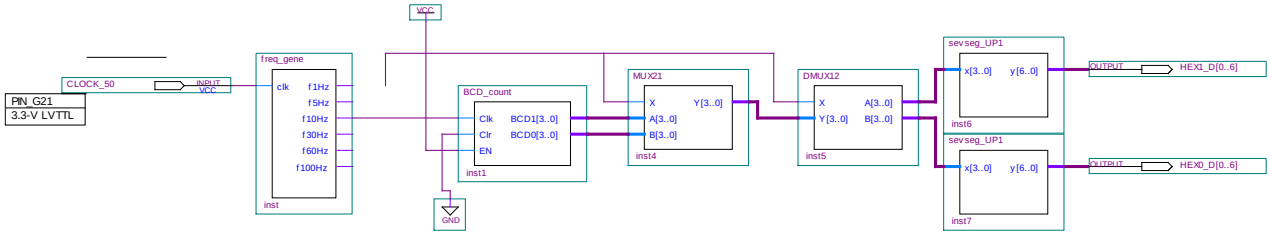
CPLD 設計作業

銘傳大學電腦與通訊工程系

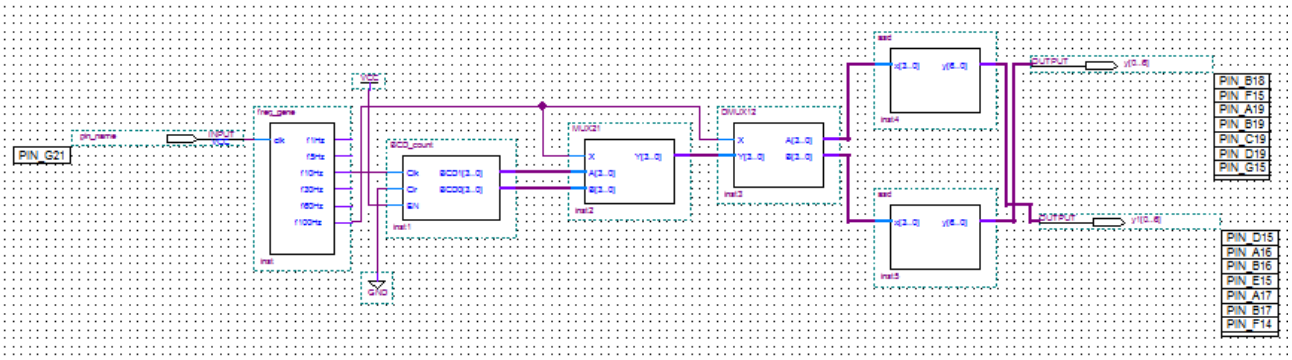
班　　級	電通二乙
組　　別	第 27 組
組員姓名/學號	陳韋澔/05050032
組員姓名/學號	陳奕璁/05050536
作業撰寫人	陳韋澔
授課教師	陳慶逸
實習成果	本次應繳作業共 2 題，完成 2 題
時　　間	2017/12/22

第一題

問題描述: 請分別設定掃瞄頻率為 1Hz, 10Hz, 30Hz, 60Hz, 100Hz, 觀察七段顯示器的計數結果有何不同?



模擬結果:



多工掃描，100Hz 計數器

https://www.youtube.com/watch?v=WaJmMcV2WIs

第二題

問題: 利用 DE0 實現一個多工掃瞄式的 4 位數 BCD 計數器

程式碼:

七段顯示器

```
library ieee;
use ieee.std_logic_1164.all;


entity asd is
   port(    x:in std_logic_vector(3 downto 0);
                    y:out std_logic_vector(6 downto 0));
end asd;
      architecture a of asd is
         begin
         with x select
                  y <= "0000001" when "0000",
                              "1001111" when "0001",
                              "0010010" when "0010",
                              "0000110" when "0011",
                              "1001100" when "0100",
                              "0100100" when "0101",
                              "0100000" when "0110",
                              "0001111" when "0111",
                              "0000000" when "1000",
                              "0000100" when "1001",
                              "0001000" when "1010",
```

```
                    "1100000" when "1011",
                    "0110001" when "1100",
                    "1000010" when "1101",
                    "0110000" when "1110",
                    "1111111" when others;
    end a;
```

除頻

```
library ieee;
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entity asd is
   port(    x:in std_logic_vector(3 downto 0);
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                    "0000110" when "0011",
                    "1001100" when "0100",
                    "0100100" when "0101",
                    "0100000" when "0110",
                    "0001111" when "0111",
                    "0000000" when "1000",
```

```
                    "0000100" when "1001",
                    "0001000" when "1010",
                    "1100000" when "1011",
                    "0110001" when "1100",
                    "1000010" when "1101",
                    "0110000" when "1110",
                    "1111111" when others;
    end a;
```

多功除頻

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity freq_gene is
port(
      clk : in std_logic;
      f1Hz,f5Hz,f10Hz,f30Hz,f60Hz,f200Hz: out std_logic
    );
end freq_gene;

architecture arch of freq_gene is

component slowCLK
  generic(divisor:integer:=8);
port( clockIN : in   std_logic;
```

```
        clockOUT: out std_logic);
end component;

begin

u1: slowCLK
      generic map(50000000)     --1Hz
      port map(clk,f1Hz);
u2: slowCLK
      generic map(10000000)     --5Hz
      port map(clk,f5Hz);
u3: slowCLK
      generic map(5000000)      --10Hz
      port map(clk,f10Hz);
u4: slowCLK
      generic map(1666666)      --30Hz
      port map(clk,f30Hz);
u5: slowCLK
      generic map(833333)       --60Hz
      port map(clk,f60Hz);
u6: slowCLK
      generic map(250000)       --100Hz
      port map(clk,f200Hz);
end arch;
```

BCD_COUNT

```
LIBRARY ieee ;
```

```
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;

ENTITY BCD_count IS
PORT ( Clk : IN STD_LOGIC ;
        Clr, EN : IN STD_LOGIC ;
        BCD3,BCD2,BCD1, BCD0 : BUFFER STD_LOGIC_VECTOR(3
DOWNTO 0) ) ;
  END BCD_count ;

ARCHITECTURE Behavior OF BCD_count IS
BEGIN
PROCESS (Clk)
BEGIN
   IF Clk'EVENT AND Clk = '1' THEN
      IF Clr = '1' THEN
         BCD3 <= "0000" ; BCD2 <= "0000" ; BCD1 <= "0000" ; BCD0 <=
"0000" ;
      ELSIF EN = '1' THEN
          IF BCD0 = "1001" THEN
              BCD0 <= "0000" ;
              IF BCD1 = "1001" THEN
                  BCD1 <= "0000";
                  IF BCD2 = "1001" THEN
                   BCD2 <= "0000" ;
                   IF BCD3 = "1001" THEN
```

```
                    BCD3 <= "0000" ;


                ELSE
                    BCD3 <= BCD3 + '1' ;
                END IF ;
            ELSE
                    BCD2 <= BCD2 + '1' ;
                END IF ;
            ELSE
                BCD1 <= BCD1 + '1' ;
            END IF ;
        ELSE
            BCD0 <= BCD0 + '1' ;
        END IF ;
    END IF ;
  END IF;
END PROCESS;
END Behavior ;
```

1 對 4

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;


ENTITY DMUX14 IS
PORT ( X    : IN    STD_LOGIC_vector(1 downto 0);
       Y: IN STD_LOGIC_vector(3 downto 0);
       A,B,C,D: OUT STD_LOGIC_vector(3 downto 0));
```

```
END DMUX14;


ARCHITECTURE a OF DMUX14 IS
BEGIN


	A <= Y when X="00" else "1111";
	B <= Y when X="01" else "1111";
	C <= Y when X="10" else "1111";
	D <= Y when X="11" else "1111";


END a;
```

4 對 1

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;


ENTITY MUX41 IS
PORT ( X    : IN    STD_LOGIC_vector(1 downto 0);
	A,B,C,D: IN STD_LOGIC_vector(3 downto 0);
	Y: OUT STD_LOGIC_vector(3 downto 0));
END MUX41;


ARCHITECTURE a OF MUX41 IS
BEGIN


	Y <= A when X="00" else
		B when X="01" else
```

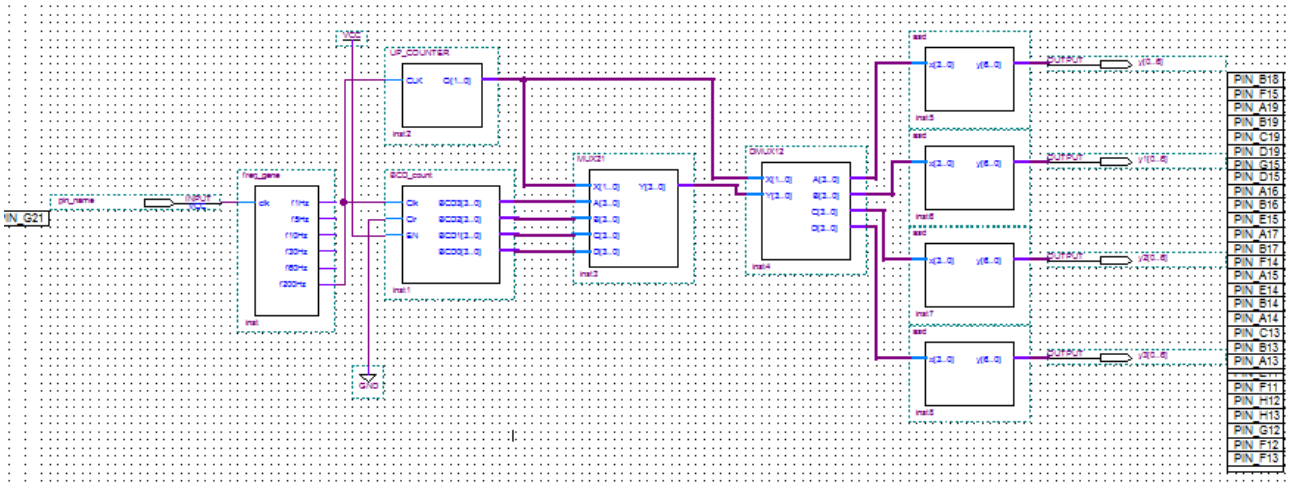
```
            C when X="10" else
            D;
END a;
```

上數器

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY UP_COUNTER is
PORT( CLK: IN STD_LOGIC;
Q   : OUT STD_LOGIC_VECTOR(1 DOWNTO 0));
END UP_COUNTER;
ARCHITECTURE a OF UP_COUNTER IS
SIGNAL QN : STD_LOGIC_VECTOR(1 DOWNTO 0);
BEGIN
    PROCESS (CLK)
    BEGIN
        IF CLK'event AND CLK='1' THEN
                QN <= QN+1;
        END IF;
    END PROCESS;
    Q<=QN;
END a;
```

實驗結果:



多工掃描 4 位數計數器，200Hz

https://youtu.be/7ZNZx-hddG4