CPLD 設計作業

範圍：參數化設計

銘傳大學電腦與通訊工程系

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作業成果	應繳作業共 2 題，每題 50 分 我共完成 2 題，應得 50 分
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■ 請確實填寫自己寫完成題數，填寫不實者(如上傳與作業明顯無關的答案，或是計算題數有誤者)，本次作業先扣 50 分。

第一題

音調產生器: 利用 Genetic map 及 port map 敘述，利用 SW[6..0]來控制輸出頻率，實現一個能產生 Do, Rei, Mi,…, Si 等音調的樂音產生器。

```
Library IEEE;
Use ieee.std_logic_1164.all;

Entity mux4 IS
PORT(d0,d1,d2,d3,d4,d5,d6:IN std_logic;
s:IN STD_LOGIC_VECTOR(6 DOWNTO 0) ;
x:OUT std_logic);
END mux4;

Architecture A of mux4 IS
BEGIN
WITH s SELECT

x <= d0 WHEN "0000001",
d1 WHEN "0000010",
d2 WHEN "0000100",
d3 WHEN "0001000",
d4 WHEN "0010000",
d5 WHEN "0100000",
d6 WHEN "1000000",
'0' WHEN OTHERS ;
```

```
END a;
```

slowCLK

```
library ieee;
use ieee.std_logic_1164.all;
entity slowCLK is
generic(divisor:integer:=50000000);
port( clockIN : in std_logic;
clockOUT: out std_logic);
end slowCLK;
architecture arch of slowCLK is
signal PULSE : std_logic;
begin
---------- clk divider ----------
process(clockIN)
variable counter,divisor2 : integer range 0 to divisor;
begin
divisor2:=divisor/2;
---------- up counter ----------
if (clockIN 'event and clockIN ='1') then
if counter = divisor then
counter := 1;
else
counter := counter + 1;
end if;
end if;
```

```
----- clk generator -----
if (clockIN 'event and clockIN ='1') then
if (( counter= divisor2) or (counter = divisor))then
PULSE <= not PULSE ;
end if;

end if;
clockOUT <= PULSE ;
end process;
end arch;
```

mux4

```
Library IEEE;
Use ieee.std_logic_1164.all;

Entity mux4 IS
PORT(d0,d1,d2,d3,d4,d5,d6:IN std_logic;
s:IN STD_LOGIC_VECTOR(6 DOWNTO 0) ;
x:OUT std_logic);
END mux4;

Architecture A of mux4 IS
BEGIN
WITH s SELECT

x <= d0 WHEN "0000001",
```

```
d1 WHEN "0000010",
d2 WHEN "0000100",
d3 WHEN "0001000",
d4 WHEN "0010000",
d5 WHEN "0100000",
d6 WHEN "1000000",
'0' WHEN OTHERS ;

END a;
```

https://youtu.be/exTYZQWObw4

第二題

設計可以實現一個用 SW[2..0]三個指撥開關選擇不同輸出頻率的功能。

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY music IS
PORT (clkIN : in std_logic;
s : IN STD_LOGIC_VECTOR(2 DOWNTO 0);
y : out std_logic
);
END music;

ARCHITECTURE a OF music IS
component slowCLK
generic(divisor:integer:=50000000);
port ( clockIN : in std_logic ;
clockOUT: out std_logic);
end component;

COMPONENT mux4
PORT(d0,d1,d2,d3,d4,d5,d6: IN STD_LOGIC;
s : IN STD_LOGIC_VECTOR(2 DOWNTO 0 );
x : OUT STD_LOGIC);
end component;

signal clk:std_logic_vector( 6 downto 0 );
BEGIN
```

```
clk1:slowCLK generic map(191571)
port map(clkIN,clk(0));
clk2:slowCLK generic map(170649)
port map(clkIN,clk(1));
clk3:slowCLK generic map(151976)
port map(clkIN,clk(2));
clk4:slowCLK generic map(143267)
port map(clkIN,clk(3));
clk5:slowCLK generic map(127551)
port map(clkIN,clk(4));
clk6:slowCLK generic map(113636)
port map(clkIN,clk(5));
clk7:slowCLK generic map(101420)
port map(clkIN,clk(6));
mu:Mux4 port map(d0=>clk(0),d1=>clk(1),d2=>clk(2),d3=>clk(3),
d4=>clk(4),d5=>clk(5),d6=>clk(6),s=>s,x=>y);
end a;
```

mux4

```
Library IEEE;
Use ieee.std_logic_1164.all;

Entity mux4 IS
PORT(d0,d1,d2,d3,d4,d5,d6:IN std_logic;
s:IN STD_LOGIC_VECTOR(2 DOWNTO 0) ;
```

```
x:OUT std_logic);
END mux4;

Architecture A of mux4 IS
BEGIN
WITH s SELECT

x <= d0 WHEN "000",
d1 WHEN "001",
d2 WHEN "010",
d3 WHEN "011",
d4 WHEN "100",
d5 WHEN "101",
d6 WHEN "110",
'0' WHEN OTHERS ;

END a;
```

slowCLK

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https://youtu.be/6tv_KSiW4dg