CPLD 設計作業

範圍： Data flow description

銘傳大學電腦與通訊工程系

班　　級	電通四甲
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作業成果	應繳作業共 10 題，每題 10 分 我共完成 10 題，應得 100 分
授課教師	陳慶逸

■ 請確實填寫自己寫完成題數，填寫不實者(如上傳與作業明顯無關的答案，或是計算題數有誤者)，本次作業先扣 50 分。

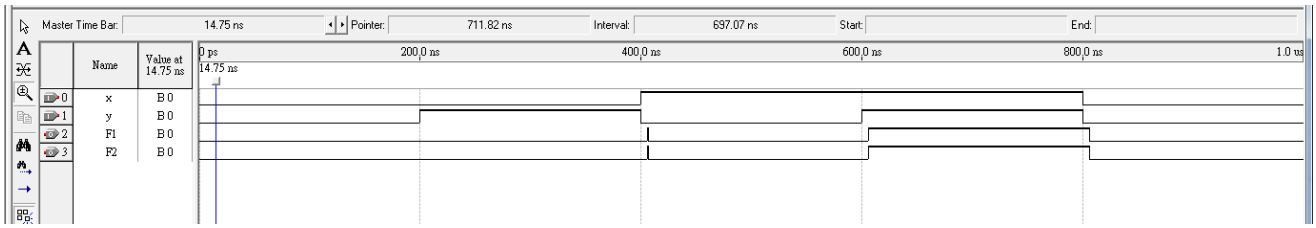
第一題

問題描述: 利用 VHDL 以及時序模擬的結果證明 x(x'+y) = xy

程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y: in STD_LOGIC;
          F1,F2 : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F1<=x and ((not x) or y);
  F2<=x and y;

end arch;
```

模擬結果擷圖:



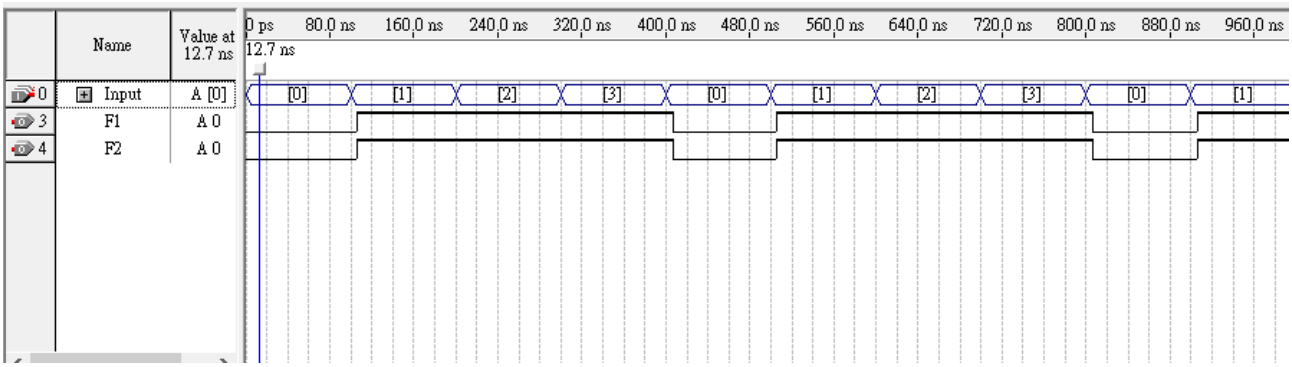
第二題

問題描述: 利用 VHDL 以及時序模擬的結果證明 x+x'y = x+y

程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y: in STD_LOGIC;
          F1,F2 : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F1<=x or (not(x)and y);
  F2<=x or y;

end arch;
```

模擬結果擷圖:



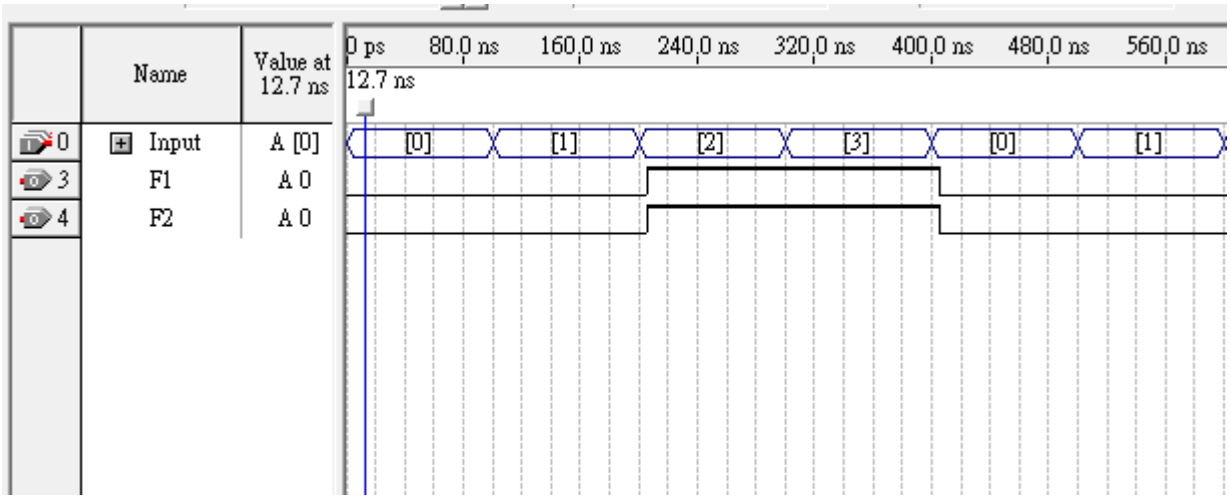
第三題

問題描述: 利用 VHDL 以及時序模擬的結果證明 (x+y)(x+y') = x

程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y: in STD_LOGIC;
          F1,F2 : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F1<=(x or y) and (x or not(y)) ;
  F2<=x ;

end arch;
```

模擬結果擷圖:



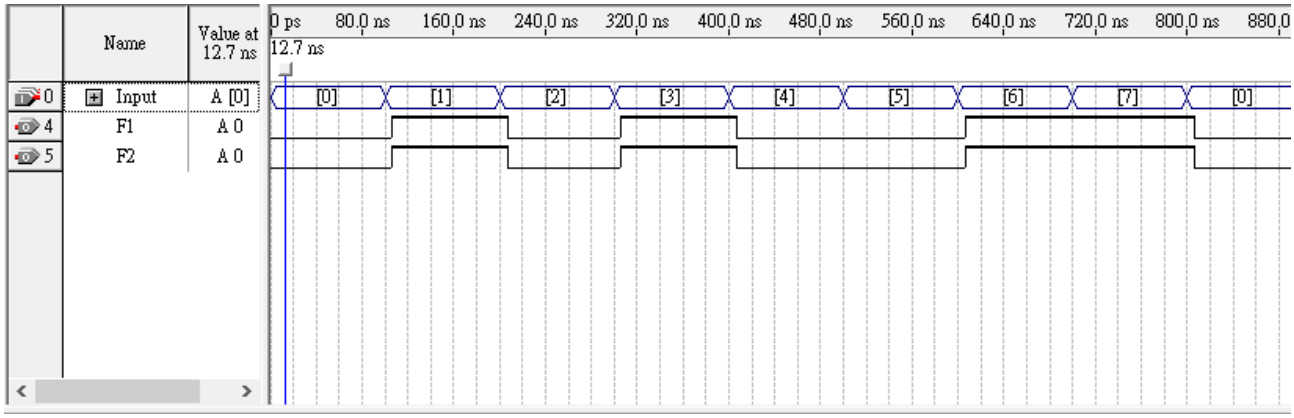
第四題

問題描述: 利用 VHDL 以及時序模擬的結果證明 xy + x'z + yz = xy + x'z

程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y,z: in STD_LOGIC;
          F1,F2 : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F1<=(x and y) or (not(x) and z) or (y and z) ;
  F2<=(x and y) or (not(x) and z);

end arch;
```

模擬結果擷圖:



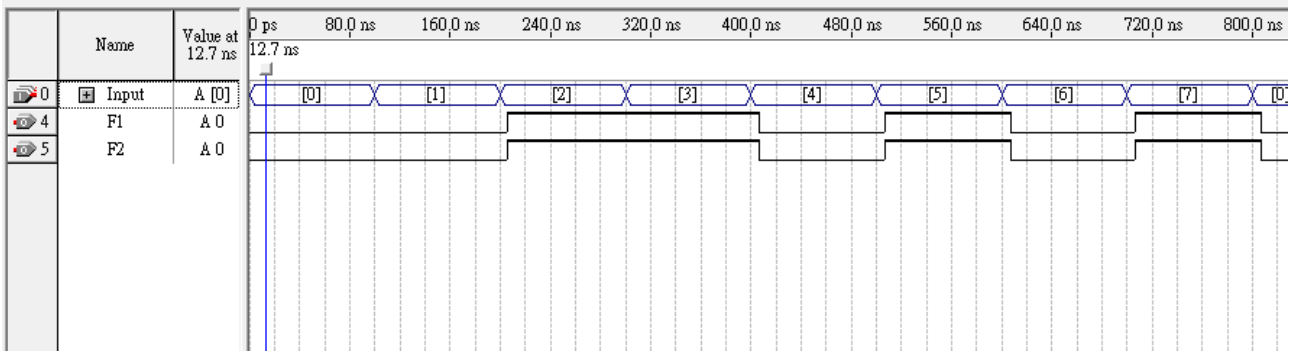
第五題

問題描述: 利用 VHDL 以及時序模擬的結果證明 (x+y)(x'+z)(y+z)=(x+y)(x'+z)

程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y,z: in STD_LOGIC;
          F1,F2 : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F1<=(x or y) and (not(x) or z) and (y or z) ;
  F2<=(x or y) and (not(x) or z);

end arch;
```

模擬結果擷圖:



第六題

問題描述: 利用 VHDL 以及時序模擬的結果證明下面的真值表中，F = ∑(1,4,5,6,7)

和 F = not (∑(0,2,3))的輸出結果是相同的。

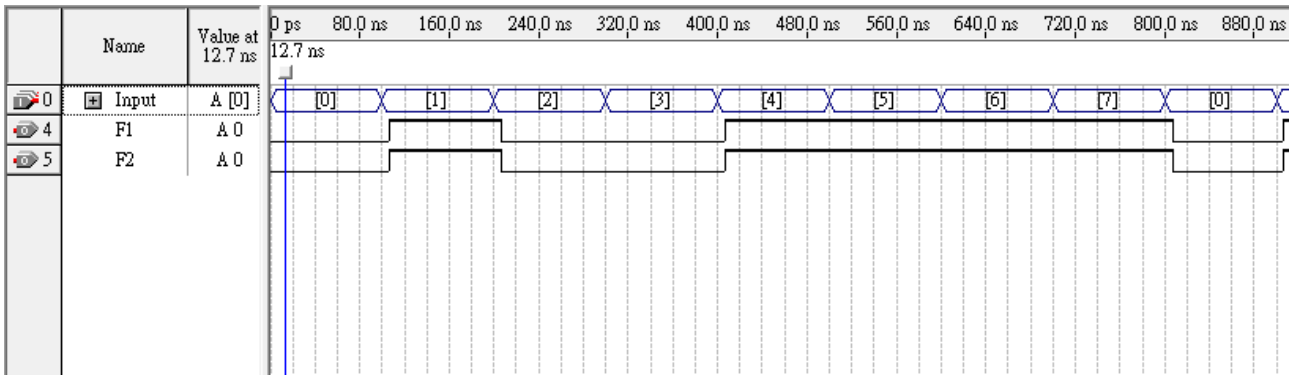
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y,z: in STD_LOGIC;
          F1,F2 : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F1<=(not(x) and not(y) and z )
       or (x and not(y) and not(z) )
       or (x and not(y) and z )
       or (x and y and not(z) )
       or (x and y and z);
  F2<=not((not(x) and not(y) and not(z) )
       or (not(x) and y and not(z) )
       or (not(x) and y and z));
```

```
end arch;
```

模擬結果擷圖:



第七題

問題描述:下面真值表中，請以 product of maxterms 來表示 f_1 的輸出，並以 sum of minterms 來表示 f_2 的輸出。最後，請利用 VHDL 來描述 f_1 和 f_2，並完成時序模擬。

Functions of Three Variables

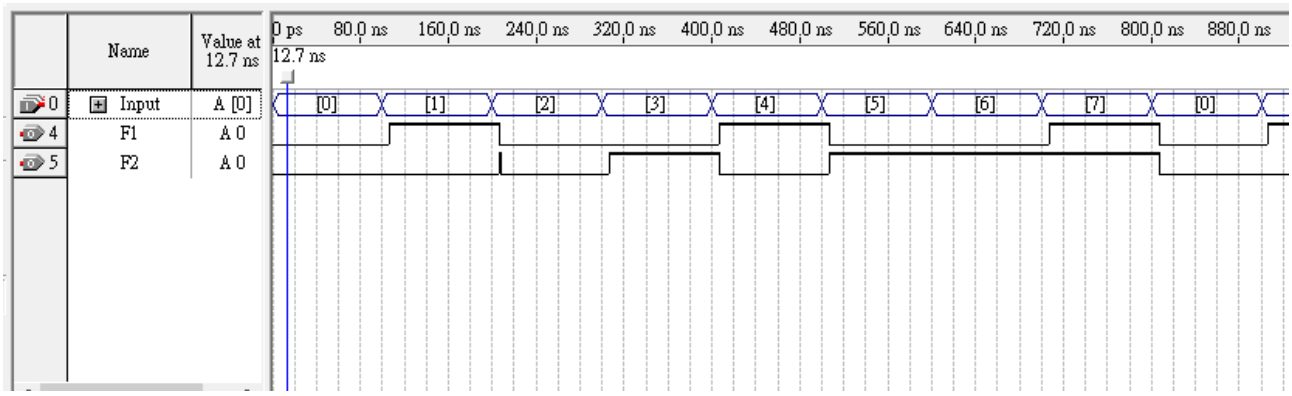
x	y	z	Function f_1	Function f_2
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y,z: in STD_LOGIC;
          F1,F2 : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F1<=(x or y or z )
       and (x or not(y) or z )
       and (x or not(y) or not(z))
       and (not(x) or y or not(z))
       and (not(x) or not(y) or z);
  F2<=(not(x) and y and z )
```

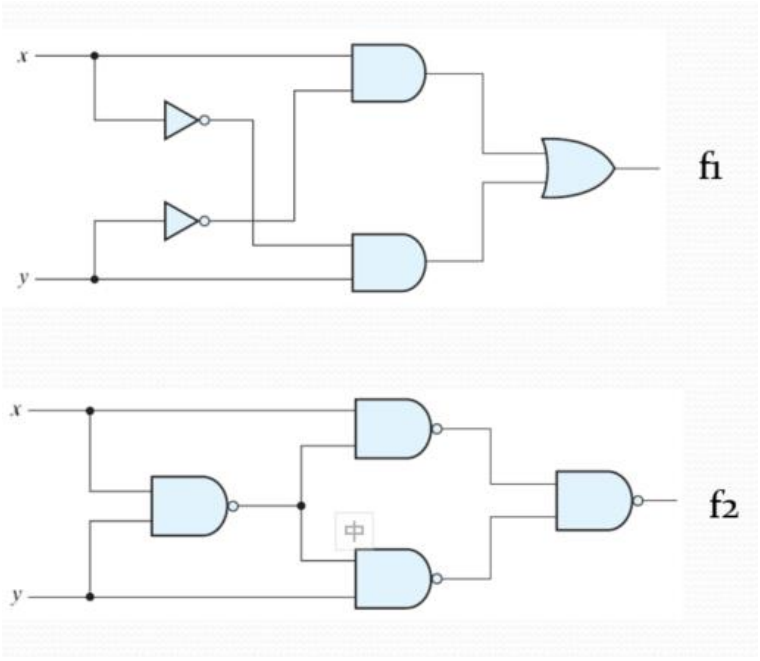
```
        or (x and not(y) and z )
        or (x and y and not(z) )
        or (x and y and z );

end arch;
```

模擬結果擷圖:



第八題

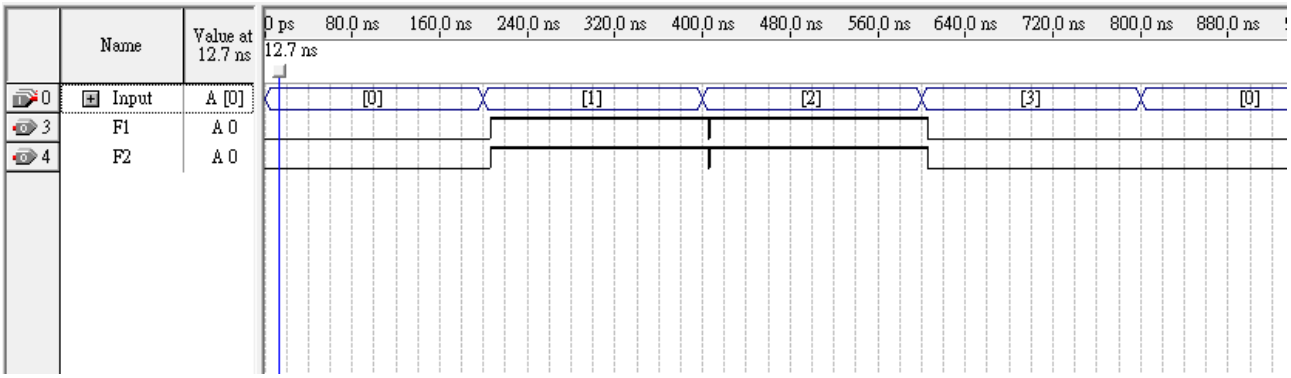
問題描述:請利用 VHDL 來描述下面電路，並完成時序模擬。



程式碼:

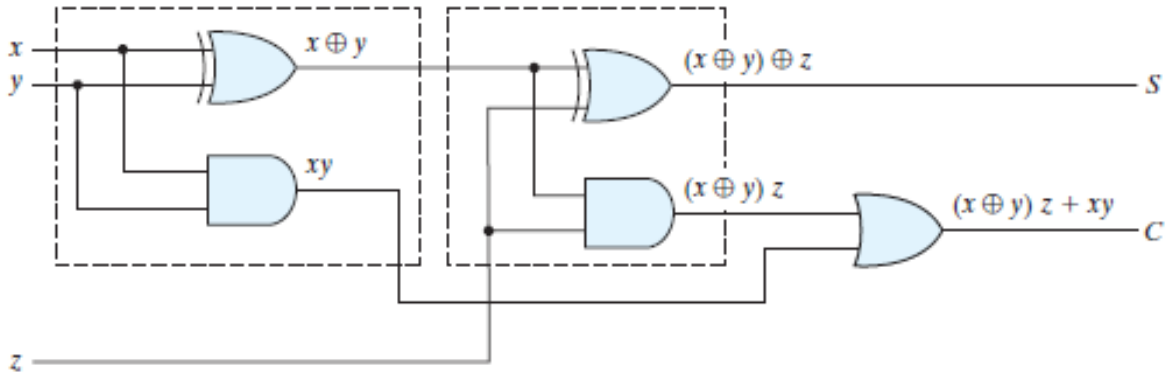
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y: in STD_LOGIC;
          F1,F2 : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F1<=(x and not(y))
       or (not(x) and y);
  F2<=(x nand (x nand y))
        nand((x nand y)nand y);

end arch;
```

模擬結果擷圖:


Name
Value at 12.7 ns
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
12.7 ns
0
Input
A [0]
[0]
[1]
[2]
[3]
[0]
3
F1
A 0
4
F2
A 0

第九題

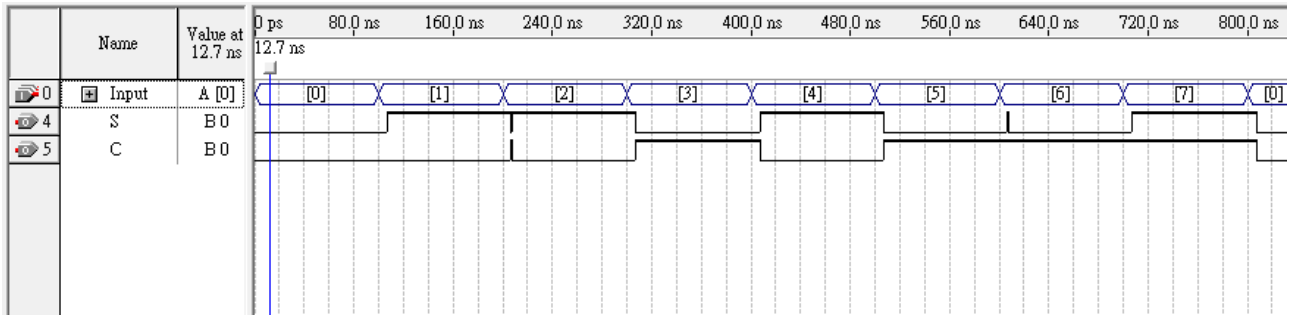
問題描述:請利用 VHDL 來描述下面電路，並完成時序模擬。



程式碼:

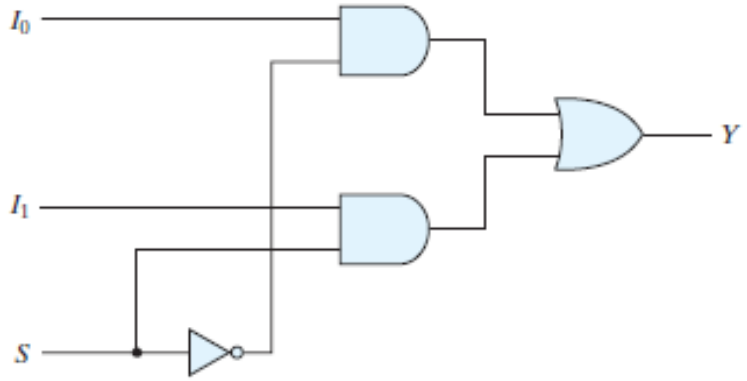
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y,z: in STD_LOGIC;
            S,C : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  S<=(x xor y) xor z;
  C<=((x xor y)and z)
        or(x and y);

end arch;
```

模擬結果擷圖:


Name
Value at 12.7 ns
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
12.7 ns
0
Input
A [0]
4
S
B 0
5
C
B 0
[0]
[1]
[2]
[3]
[4]
[5]
[6]
[7]
[0]

第十題

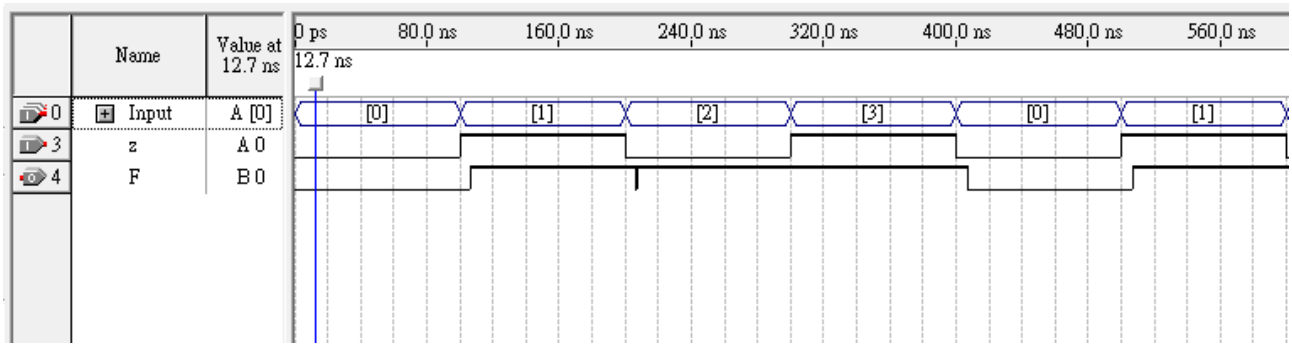
問題描述:請利用 VHDL 來描述下面電路，並完成時序模擬。



程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity abc is
port ( x,y,z: in STD_LOGIC;
            F : out STD_LOGIC);
end abc;

architecture arch of abc is
begin

  F<=(x and not(z)) or (y and z);


end arch;
```

模擬結果擷圖:


Name
Value at 12.7 ns
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
12.7 ns
0
Input
A [0]
[0]
[1]
[2]
[3]
[0]
[1]
3
z
A 0
4
F
B 0