CPLD 設計作業

範圍： State machine

銘傳大學電腦與通訊工程系

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作業成果	應繳作業共 2 題，每題 50 分 我共完成 2 題，應得 100 分
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■ 請確實填寫自己寫完成題數，填寫不實者(如上傳與作業明顯無關的答案，或是計算題數有誤者)，本次作業先扣 50 分。

第一題

實現一個 1Hz 頻率計數的 3 bits 計數器:

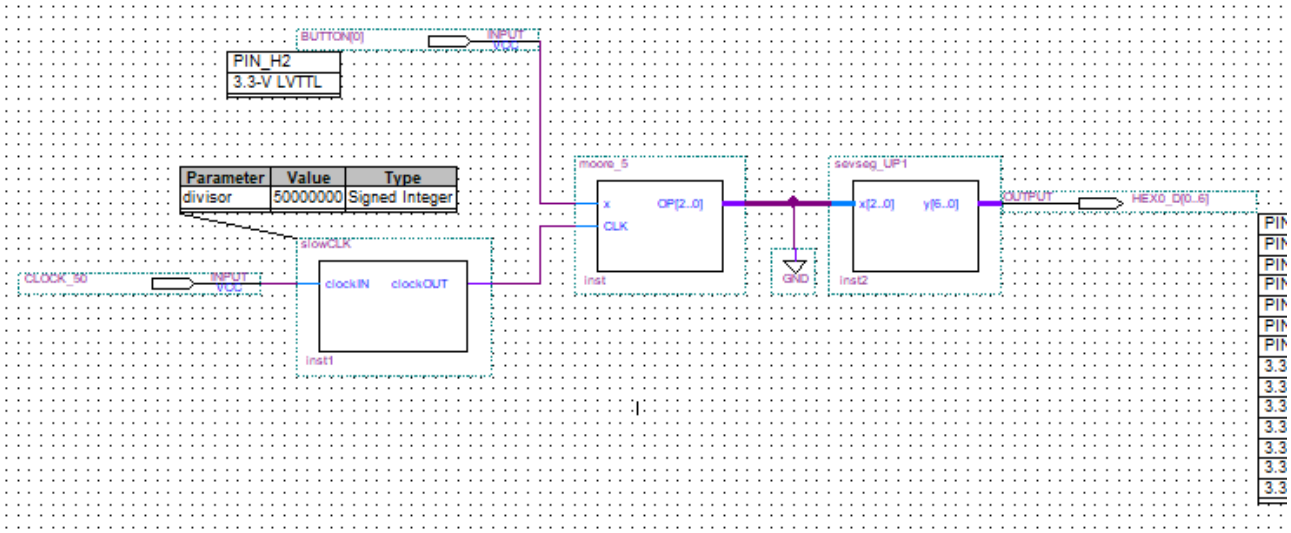
1. 可控制上、下數計數的 3 位元計數器。

2. 計數頻率為 1Hz。

3. 在 DE0 實驗板上實現本電路功能要求。

本題應包含 DE0 實驗板驗證,執行結果請以影片播放方式 Demo(可上傳至 youtube 並設為公開，然後並在實驗報告上提供連結至 youtube 影片的網址)。

最上層設計的電路圖擷圖:




```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.std_logic_unsigned.all;

ENTITY moore_5 IS
PORT(    x,CLK :IN STD_LOGIC;
                    OP       :OUT std_logic_vector(2 downto 0));
END moore_5;

ARCHITECTURE a OF moore_5 IS
BEGIN
PROCESS(clk)
```

```
variable present_state: std_logic_vector (2 downto 0);
        BEGIN
          IF clk'event and clk='1' then
                CASE present_state IS
                WHEN "000" =>
                if x='1' then    present_state:="001";
                else present_state:="111";
                end if;
                WHEN "001" =>
                   if x='1' then    present_state:="010";
                   else present_state:="000";
                   end if;
                WHEN "010" =>
                if x='1' then    present_state:="011";
                else present_state:="001";
                end if;
                WHEN "011" =>
                   if x='1' then    present_state:="100";
                   else present_state:="010";
                   end if;
                WHEN "100" =>
                if x='1' then    present_state:="101";
                else present_state:="011";
                end if;
               WHEN "101" =>
                if x='1' then    present_state:="110";
                else present_state:="100";
                end if;
                WHEN "110" =>
                if x='1' then    present_state:="111";
                else present_state:="101";
                end if;
                WHEN "111" =>
                if x='1' then    present_state:="000";
                else present_state:="110";
                end if;
               WHEN others=>
                if x='1' then    present_state:="000";
                else present_state:="000";
                end if;
```

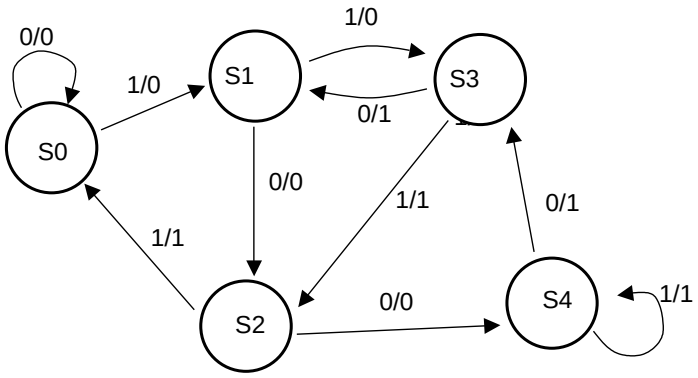
```
        END CASE;
    end if;
    op<= present_state;
END PROCESS;
END a;
```

影片連結網址:

https://youtu.be/Pr7DSpirNC4

第二題

請實現下面的狀態機電路。



程式碼:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.std_logic_unsigned.all;

    ENTITY zxc IS
PORT(CLK    :IN STD_LOGIC;
      X       :IN STD_LOGIC;
        op     :OUT STD_LOGIC);
    END zxc;

ARCHITECTURE a OF zxc IS
TYPE State IS (s0,s1,s2,s3,s4);
SIGNAL present_state : State;
SIGNAL next_state: State;
BEGIN
    state_comp: PROCESS(present_state)
    BEGIN
    CASE present_state IS
    WHEN s0 =>
        IF X = '0' THEN
            next_state <= s0;
        ELSE
            next_state <= s1;
        END IF;
```

```
        IF X = '0' THEN
            op <= '0';
        ELSE
            op <= '0';
        END IF;

    WHEN s1 =>
        IF X = '0' THEN
            next_state <= s2;
        ELSE
            next_state <= s3;
        END IF;
        IF X = '0' THEN
            op <= '0';
        ELSE
            op <= '0';
        END IF;
    WHEN s2 =>
        IF X = '0' THEN
            next_state <= s4;
        ELSE
            next_state <= s0;
        END IF;
        IF X = '0' THEN
            op <= '0';
        ELSE
            op <= '1';
        END IF;

    WHEN s3 =>
        IF X = '0' THEN
            next_state <= s1;
        ELSE
            next_state <= s2;
        END IF;
        IF X = '0' THEN
            op <= '1';
        ELSE
            op <= '1';
        END IF;
```

```
    WHEN s4 =>
        IF X = '0' THEN
            next_state <= s3;
        ELSE
            next_state <= s4;
        END IF;
        IF X = '0' THEN
            op <= '1';
        ELSE
            op <= '1';
        END IF;

    END CASE;
    END PROCESS state_comp;

    state_clocking: PROCESS (CLK)
    BEGIN
        IF CLK'EVENT AND CLK = '1' THEN
            present_state <= next_state;
        END IF;
    END PROCESS state_clocking;
END a;
```

模擬結果: