CPLD 設計作業

範圍：　資料型別與資料物件

銘傳大學電腦與通訊工程系

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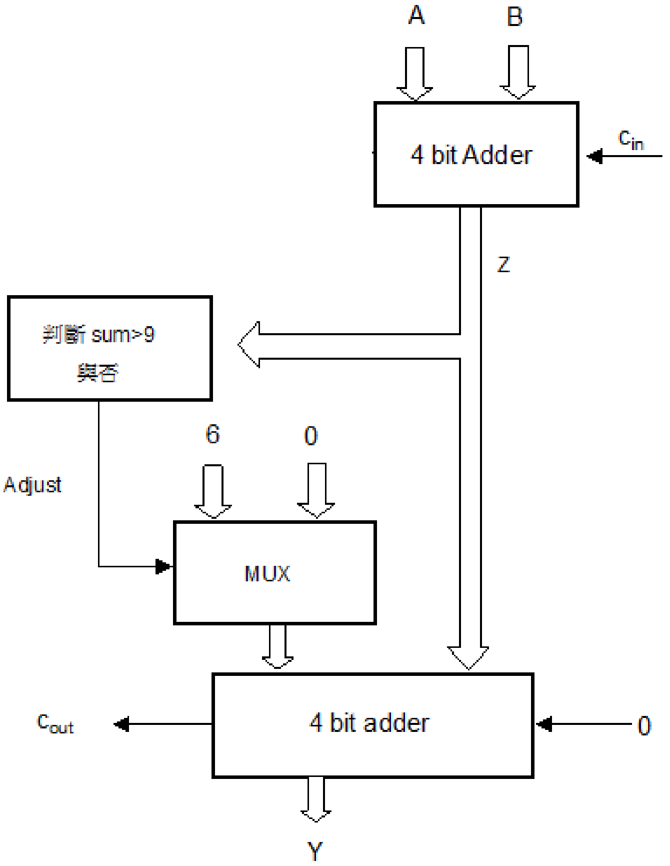
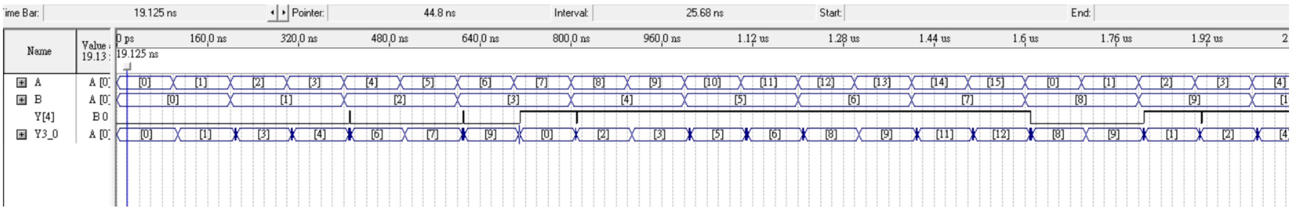
作業成果	應繳作業共 5 題，每題 20 分 我共完成 5 題，應得 100 分
授課教師	陳慶逸

■ 請確實填寫自己寫完成題數，填寫不實者(如上傳與作業明顯無關的答案，或是計算題數有誤者)，本次作業先扣 50 分。

第一題

以整數宣告(Integer)的方式，設計一個四位元的 BCD 加法器



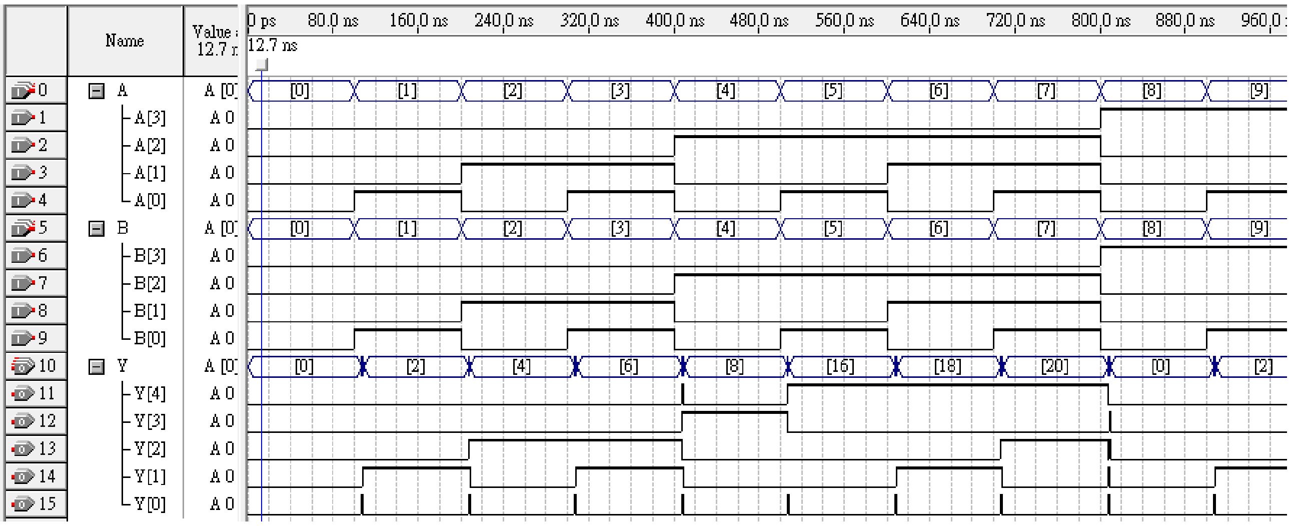

Time Bar: 19.125 ns
Pointer: 44.8 ns
Interval: 25.68 ns
Start:
End:
Name
Value 19.13
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
1.12 us
1.28 us
1.44 us
1.6 us
1.76 us
1.92 us
19.125 ns
A
B
Y[4]
Y3_0
A [0]
A [0]
B 0
A [0]
A: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [0] [1] [2] [3] [4]
B: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
Y3_0: [0] [1] [3] [4] [6] [7] [9] [0] [2] [3] [5] [6] [8] [9] [11] [12] [8] [9] [1] [2] [4]

程式碼:

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;

ENTITY abc IS
PORT (
    A, B : IN Integer Range 0 to 15;
    Y : OUT Integer Range 0 to 31);

END abc;
```

```
ARCHITECTURE Behavior OF abc IS
SIGNAL Z : Integer Range 0 to 15;
SIGNAL Adjust: Integer Range    0 to 1;
BEGIN
          Z <= (0+A) +(0+B);
          adjust <=1 WHEN Z > 9 ELSE
                                    0;
          Y <=Z WHEN (Adjust=0) ELSE
      Z+6;
END Behavior;
```

模擬結果擷圖



第二題

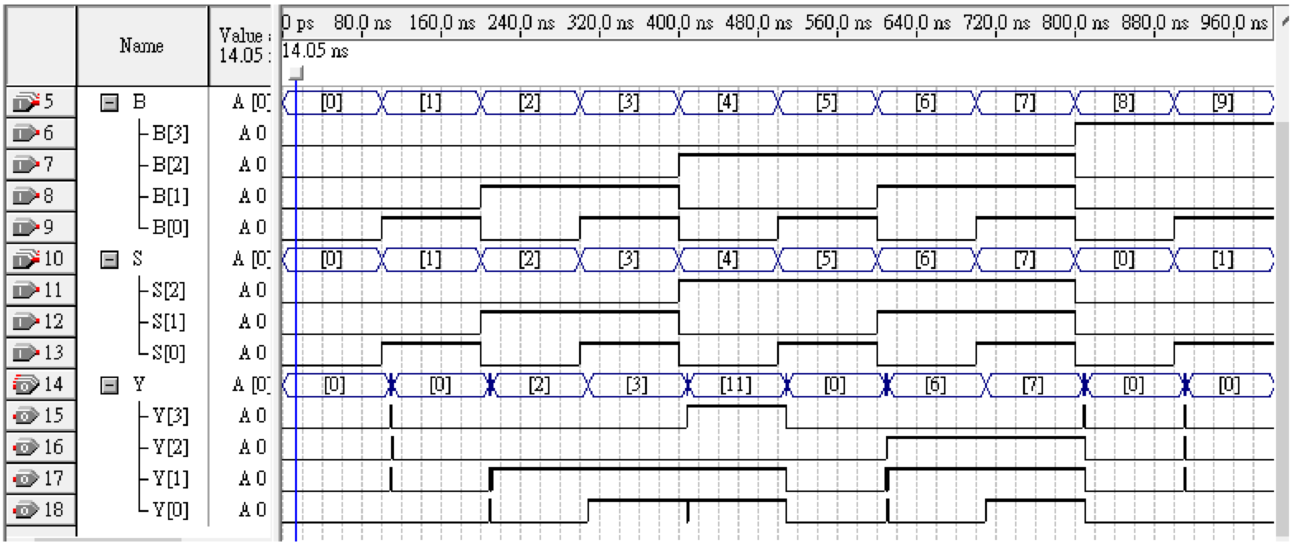
使用 with-select-when 敘述設計 ALU 電路(A, B, & Y 均為 4bits 資料)。

S2	S1	S0	Operation
0	0	0	Y <=A + B;
0	0	1	Y <=A - B;
0	1	0	Y <=A and B;
0	1	1	Y <=A or B;
1	0	0	Y<=not A;
1	0	1	Y<=A xor B;
1	1	0	Y<=A;
1	1	1	Y<=A;

程式碼:

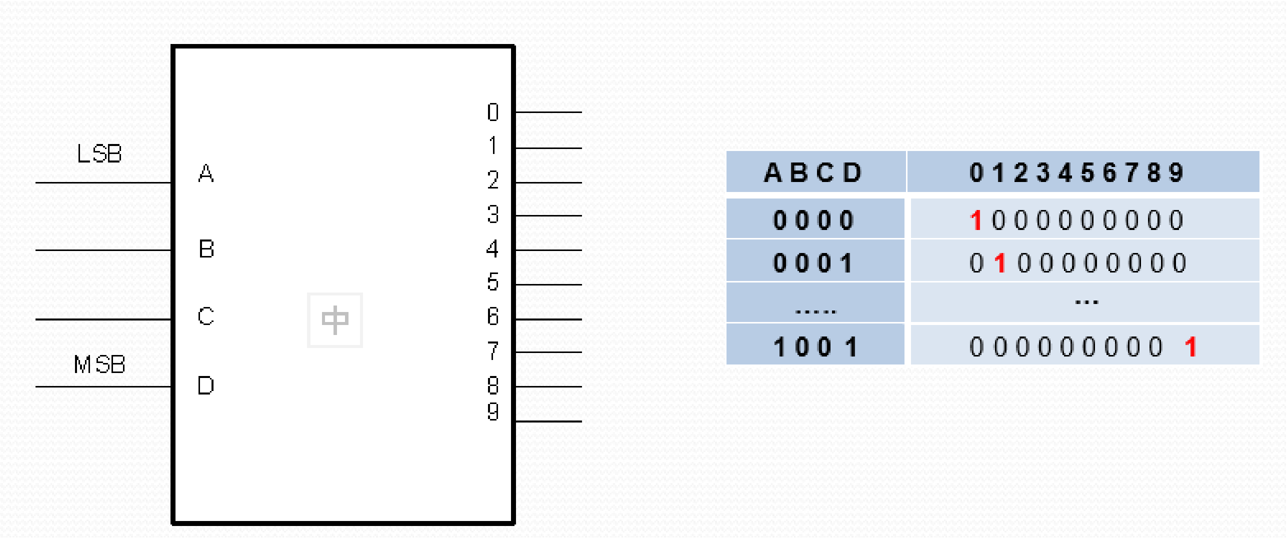
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_logic_unsigned.all;
use IEEE.STD_LOGIC_arith.all;


ENTITY abc IS
PORT (
          Y: OUT STD_LOGIC_vector(3 downto 0);
          S   : IN   STD_LOGIC_VECTOR(2 downto 0);
          A,B: IN STD_LOGIC_vector(3 downto 0));
END abc;

ARCHITECTURE a OF abc IS
BEGIN
   WITH S   SELECT
      Y <=   (A + B) WHEN "000",
               (A - B) WHEN "001",
               (A and B) WHEN "010",
               (A or B) WHEN "011",
                    (not A) WHEN "100",
                    (A xor B) WHEN "101",
                    A WHEN OTHERS;
END a;
```

模擬結果擷圖:



第三題

使用 when-else 敘述設計一個 BCD 至十進位的解碼器電路。



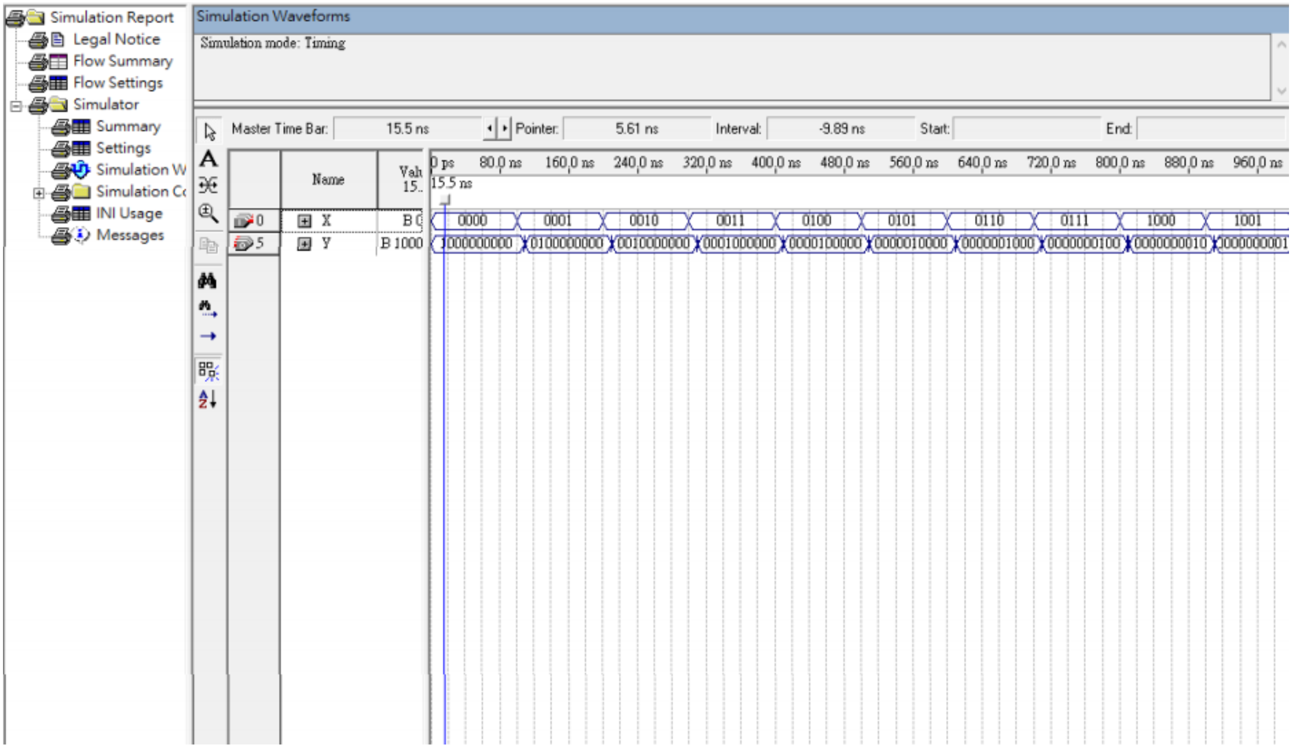
ABCD	0123456789
0000	1000000000
0001	0100000000
.....	...
1001	0000000001

程式碼:

```
library IEEE;
use IEEE.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

ENTITY abc IS
PORT (
            Y: OUT STD_LOGIC_vector(9 downto 0);
            X    : IN STD_LOGIC_VECTOR(3 downto 0);
);
END abc;

ARCHITECTURE a OF abc IS
BEGIN
         Y<="1000000000" when X="0000"else
         Y<="0100000000" when X="0000"else
         Y<="0010000000" when X="0000"else
         Y<="0001000000" when X="0000"else
         Y<="0000100000" when X="0000"else
         Y<="0000010000" when X="0000"else
         Y<="0000001000" when X="0000"else
```

```
        Y<="0000000100" when X="0000"else
        Y<="0000000010" when X="0000"else
        Y<="0000000001" when X="0000"else



end a;
```

模擬結果擷圖:



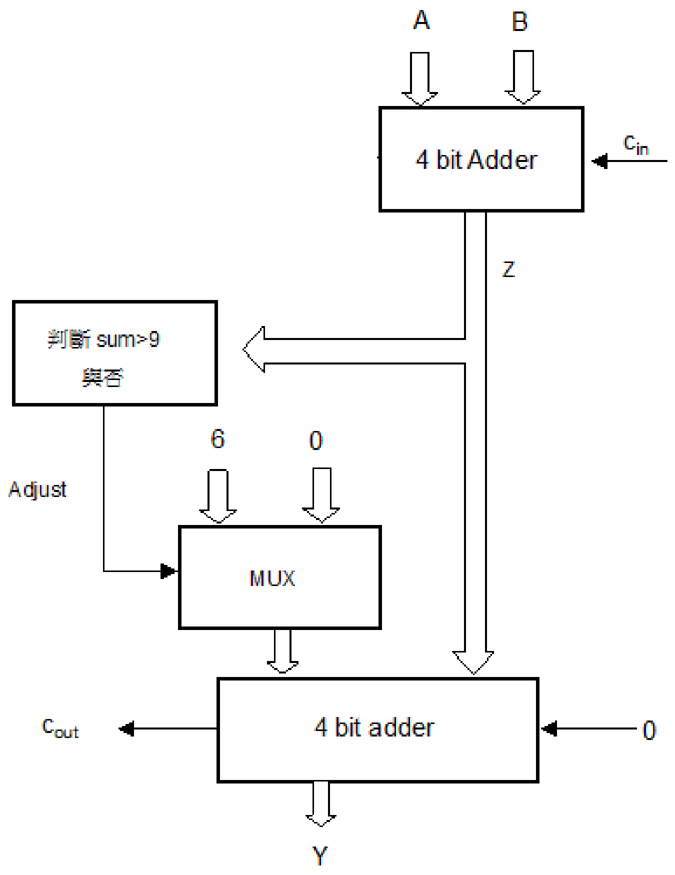
Simulation mode: Timing

Master Time Bar: 15.5 ns　Pointer: 5.61 ns　Interval: -9.89 ns　Start:　End:

```
     Name   Vah    0 ps    80.0 ns    160.0 ns   240.0 ns   320.0 ns   400.0 ns   480.0 ns   560.0 ns   640.0 ns   720.0 ns   800.0 ns   880.0 ns   960.0 ns
            15..   15.5 ns
0    X      B (    0000       0001       0010       0011       0100       0101       0110       0111       1000       1001
5    Y      B 1000 1000000000 0100000000 0010000000 0001000000 0000100000 0000010000 0000001000 0000000100 0000000010 0000000001
```

第四題

使用 If-then-else 敘述重新完成 BCD 加法器

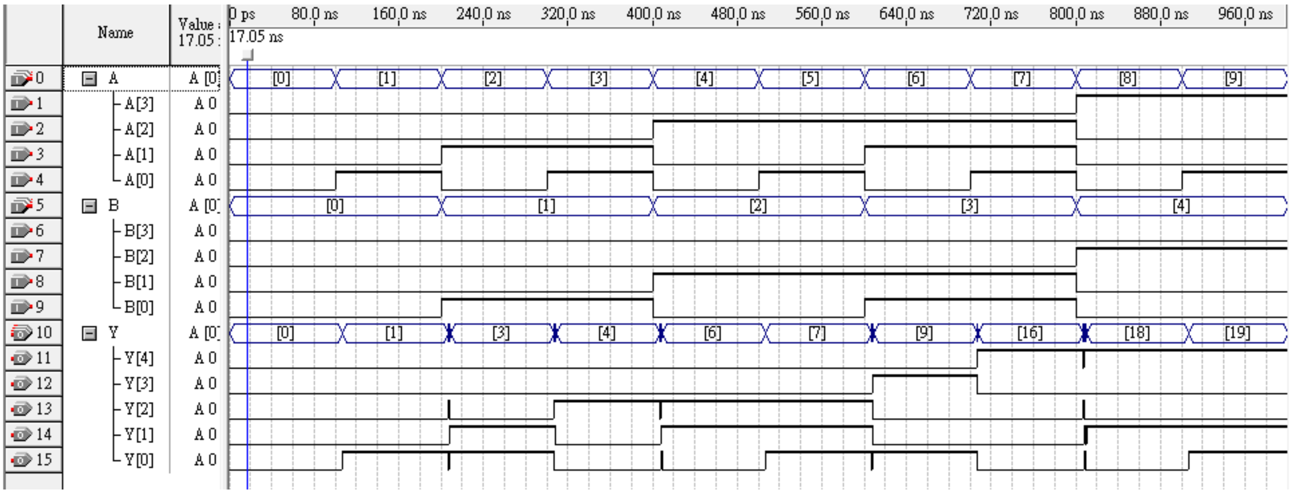


程式碼:

```
library IEEE;
use IEEE.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity abc is
port (
       A, B : IN Integer Range 0 to 15;
      Y : OUT Integer Range 0 to 31);

end abc;


architecture a of abc is
SIGNAL Z : Integer Range 0 to 15;

begin
```

```
process (A, B)
  begin
    Z <= (0+A) +(0+B);
            if    Z > 9 then

            Y<= Z+6;

            else
            Y <=Z;



            end if ;
    end process;
end a;
```

模擬結果擷圖:



第五題

使用 If-then-else 敘述設計 ALU 電路(A, B, & Y 均為 4bits 資料)。

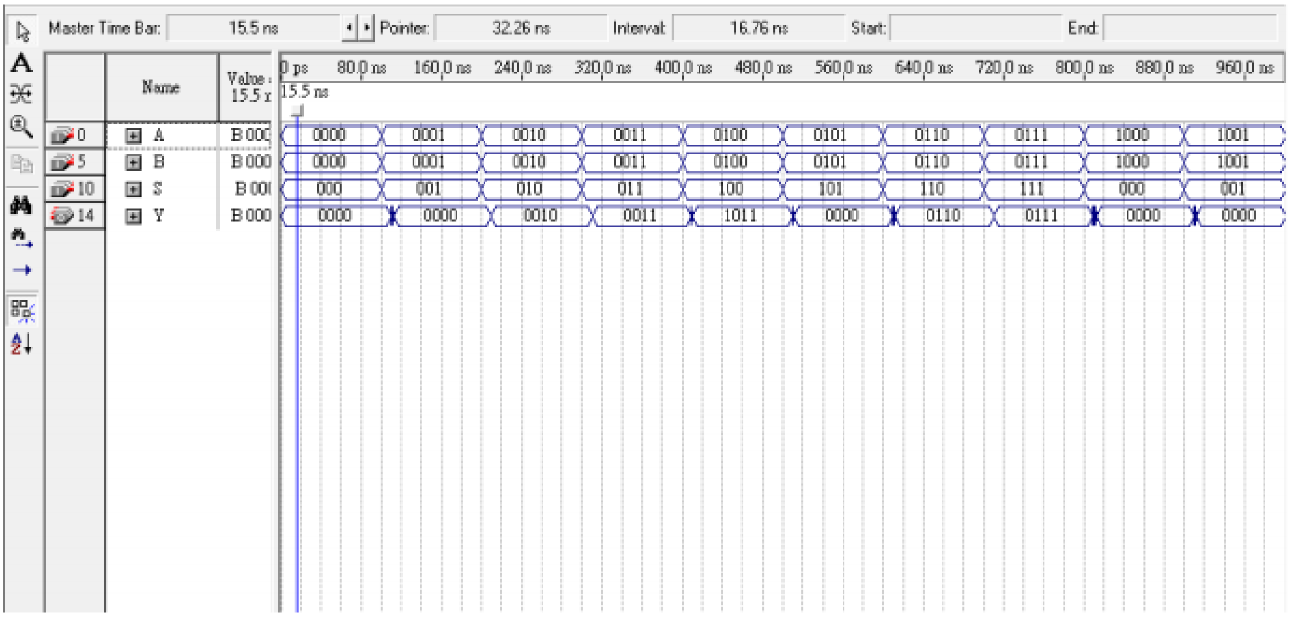
S2	S1	S0	Operation
0	0	0	Y <=A + B;
0	0	1	Y <=A - B;
0	1	0	Y <=A and B;
0	1	1	Y <=A or B;
1	0	0	Y<=not A;
1	0	1	Y<=A xor B;
1	1	0	Y<=A;
1	1	1	Y<=A;

程式碼:

```
library IEEE;
use IEEE.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

ENTITY abc IS
PORT (
        Y: OUT STD_LOGIC_vector(3 downto 0);
        S   : IN   STD_LOGIC_VECTOR(2 downto 0);
        A,B: IN STD_LOGIC_vector(3 downto 0));
END abc;

ARCHITECTURE a OF abc IS
BEGIN

Process(s)
  Begin
         if S="000"then
             Y<=(A+B);
         elseif S="001" then Y<=(A - B);
```

```
            elseif S="010" then Y<=(A and B);
            elseif S="011" then Y<=(A or B);
            elseif S="100" then Y<=(notA);

            elseif S="101" then Y<=(A xor B);
            elseif S="110" then Y<=(A);
            else
                  Y<=(A);
            end if;
end process;
end a;
```

模擬結果擷圖:



Master Time Bar: 15.5 ns Pointer: 32.26 ns Interval: 16.76 ns Start: End:

Name
Value : 15.5 r
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
15.5 ns
0 A B 000(0000 0001 0010 0011 0100 0101 0110 0111 1000 1001
5 B B 000 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001
10 S B 00(000 001 010 011 100 101 110 111 000 001
14 Y B 000 0000 0000 0010 0011 1011 0000 0110 0111 0000 0000