CPLD 設計作業

範圍： 循序邏輯與正反器設計

銘傳大學電腦與通訊工程系

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作業成果	應繳作業共 5 題， 每題 20 分 我共完成 4 題，應得 80 分
授課教師	陳慶逸

- 請確實填寫自己寫完成題數，填寫不實者(如上傳與作業明顯無關的答案，或是計算題數有誤者)，本次作業先扣 50 分。

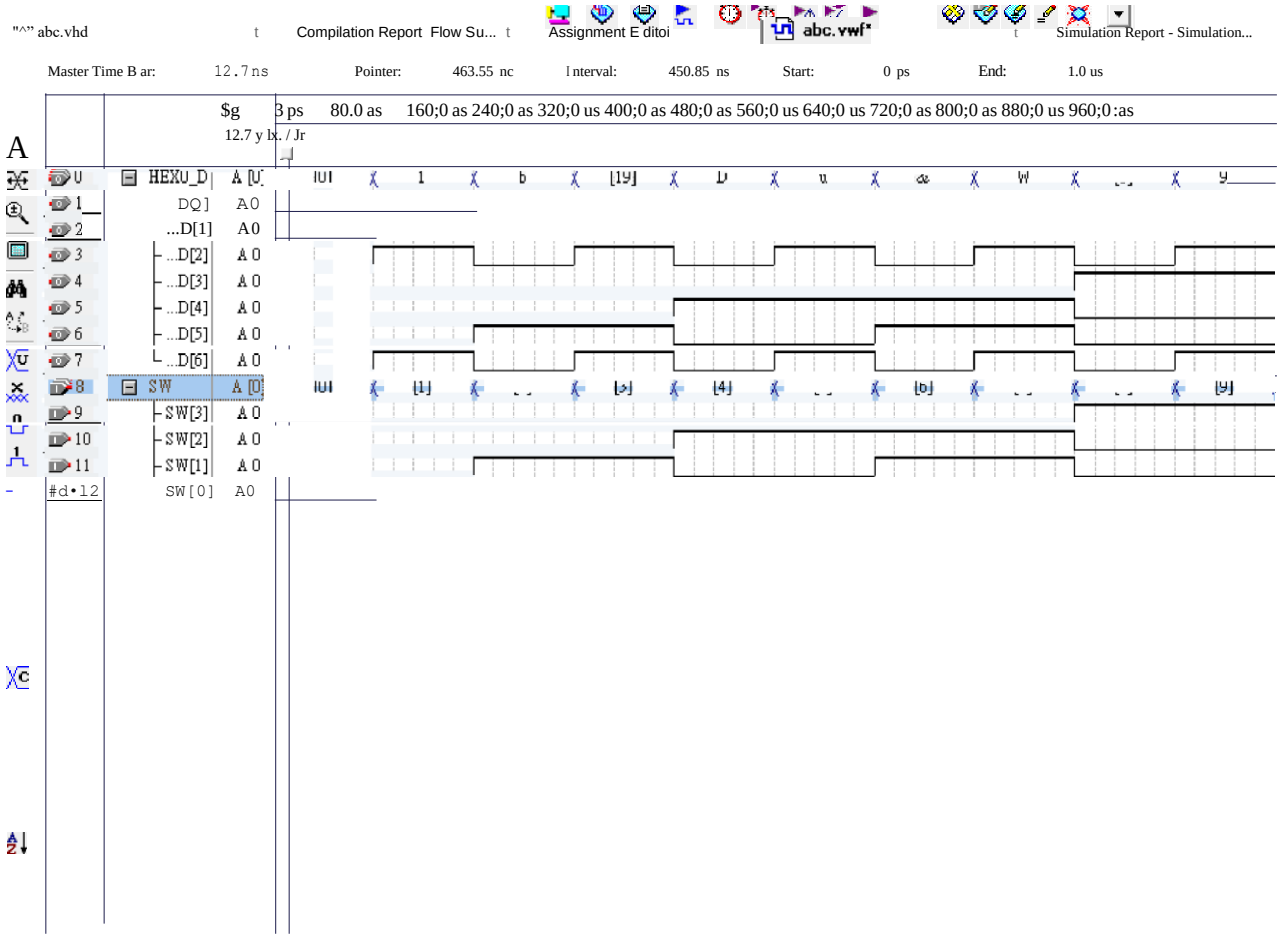
第一題

以 if-then-else 敘述，設計一個可以顯示數字 0-9,A 到 F 的七段顯示器解碼電路(共陽極)。

程式碼:

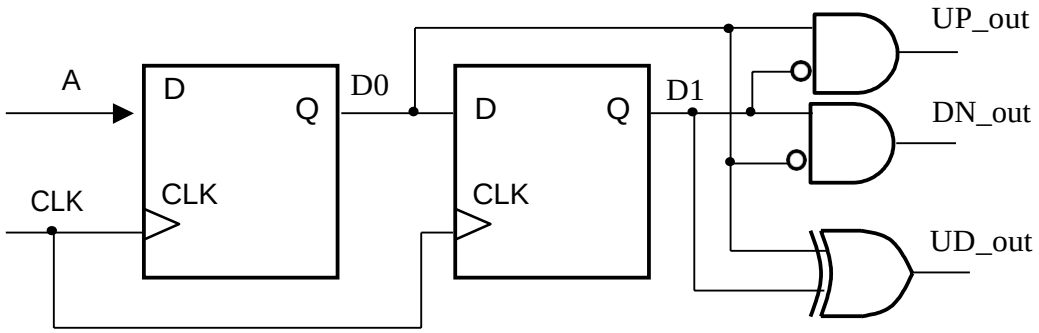
```
library ieee;
use ieee.std_logic_1164.all;
entity abc is
port(    SW:in std_logic_vector(3 downto 0);
           HEX0_D:out std_logic_vector(0    to 6));
end abc;

architecture a of abc is
begin
with SW select
HEX0_D<= "0000001" when "0000",
             "1001111" when "0001",
              "0010010" when "0010",
              "0000110" when "0011",
"1001100" when "0100",
     "0100100" when "0101",
     "0100000" when "0110",
     "0001111" when "0111",
     "0000000" when "1000",
     "0000100" when "1001",
     "0001000" when "1010",
     "1100000" when "1011",
     "0110001" when "1100",
     "1000010" when "1101",
     "0110000" when "1110",
     "0111000" when others;
  end a;
```

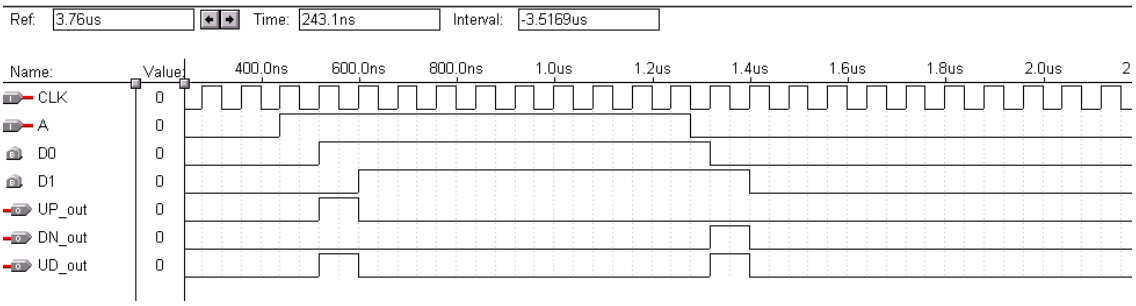
DE0 實驗板驗證結果(請放三張圖，在 HEX0 分別顯示 4, 7, F 三個字元)：


"^" abc.vhd
Compilation Report Flow Su...
Assignment E ditoi
abc.vwf*
Simulation Report - Simulation...
Master Time B ar: 12.7ns
Pointer: 463.55 nc
Interval: 450.85 ns
Start: 0 ps
End: 1.0 us
$g
3 ps
80.0 as
160;0 as 240;0 as 320;0 us 400;0 as 480;0 as 560;0 us 640;0 us 720;0 as 800;0 as 880;0 us 960;0 :as
12.7 y lx. / Jr
HEXU_D
DQ]
...D[1]
...D[2]
...D[3]
...D[4]
...D[5]
...D[6]
SW
SW[3]
SW[2]
SW[1]
SW[0]
#d•12

第二題

試完成下面的微分電路；其中 UP_out 為上緣微分，DN_out 為下緣微分，而 UD_out 為上下緣微分。附上模擬結果以供檢驗程式的正確性。



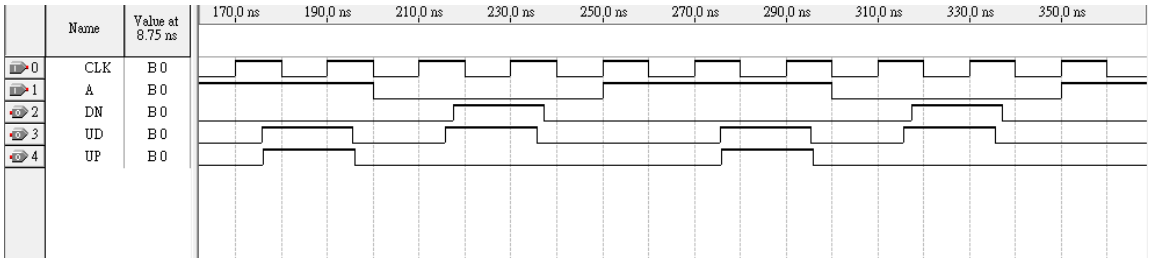


程式碼:

```
library ieee;
use ieee.std_logic_1164.all;

entity hw2 is
   port ( A, CLK : in std_logic;
               UP,DN,UD: out std_logic);
end hw2;

architecture a of hw2 is
   signal D0,D1 : std_logic;
begin
PROCESS (clk)
   BEGIN
      if CLK'event and CLK='1' then
          D1<=D0;
```

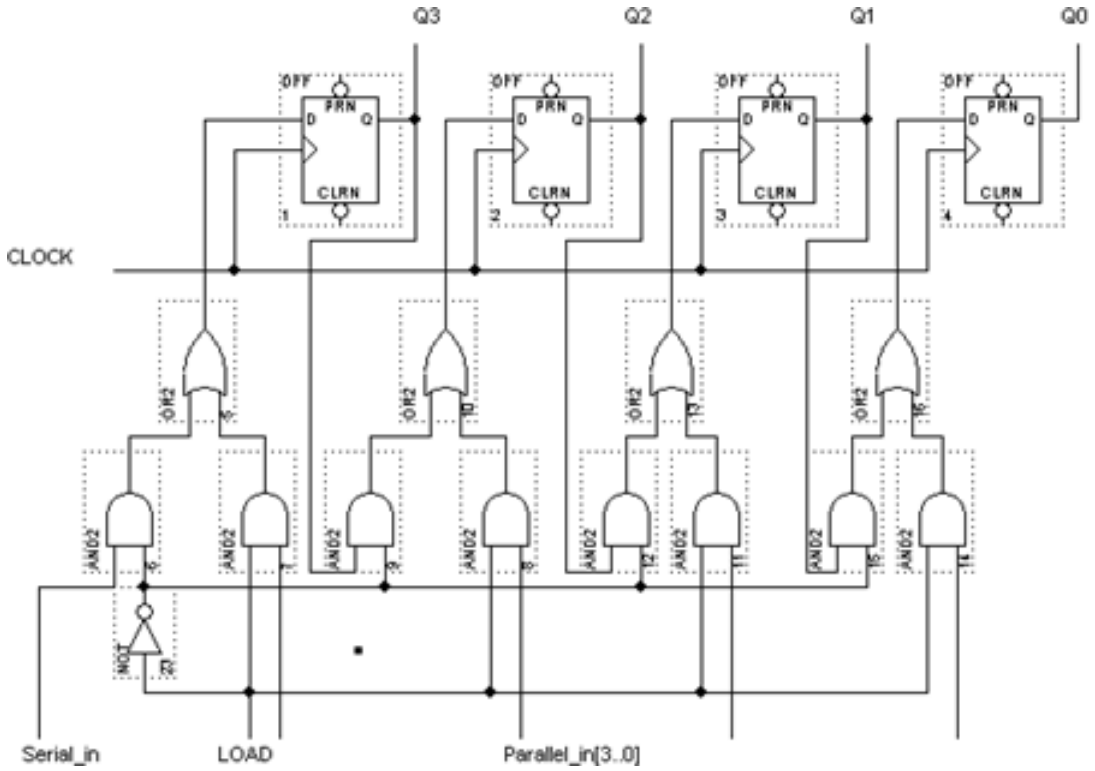
```
            D0<=A;
        end if;
        UP<=D0 and NOT(D1);
            DN<=D1 and NOT(D0);
            UD<=D1 XOR D0;
    END PROCESS;
end a;
```

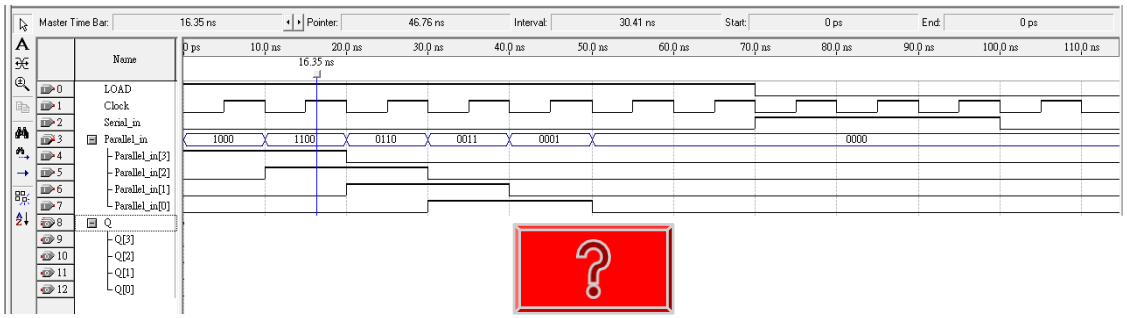
模擬結果擷圖:



第三題

以 IF-then-else 敘述設計下面電路，並請依要求設定模擬的波形。



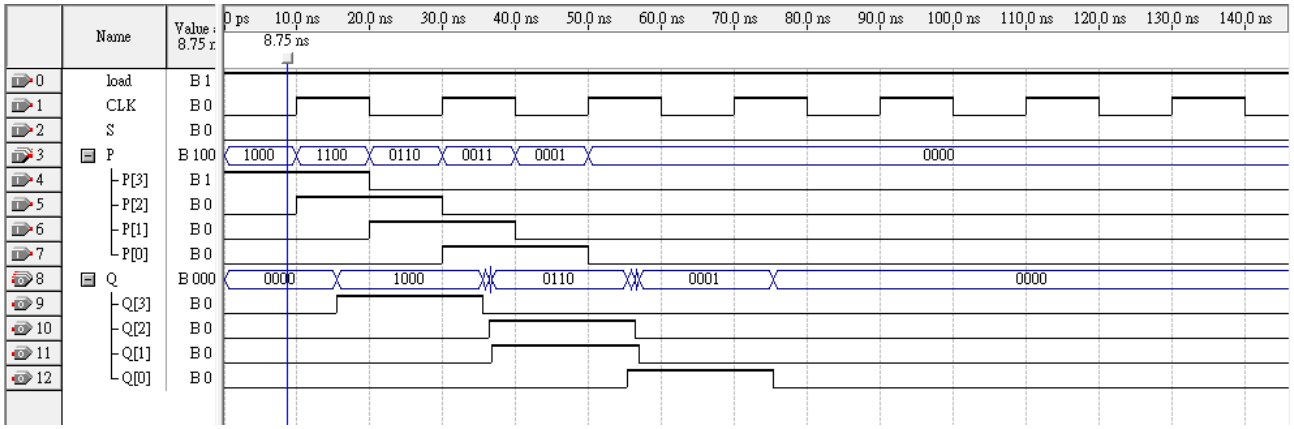


程式碼:

```
library ieee;
use ieee.std_logic_1164.all;

entity hw3 is
   port ( load, CLK,S : in std_logic;
               P : IN STD_LOGIC_VECTOR(3 downto 0);
               Q: OUT STD_LOGIC_VECTOR(3 downto 0));
end hw3;
```

```
architecture a of hw3 is
   signal D0,D1,D2,D3 : std_logic;
begin
PROCESS (CLK)
   BEGIN
      if CLK'event and CLK='1' then
          if load='0'then
               D3<=S;
               D2<=D3;
               D1<=D2;
               D0<=D1;
          elsif load='1'then
                Q<=P;
      end if;
      end if;

   END PROCESS;
end a;
```

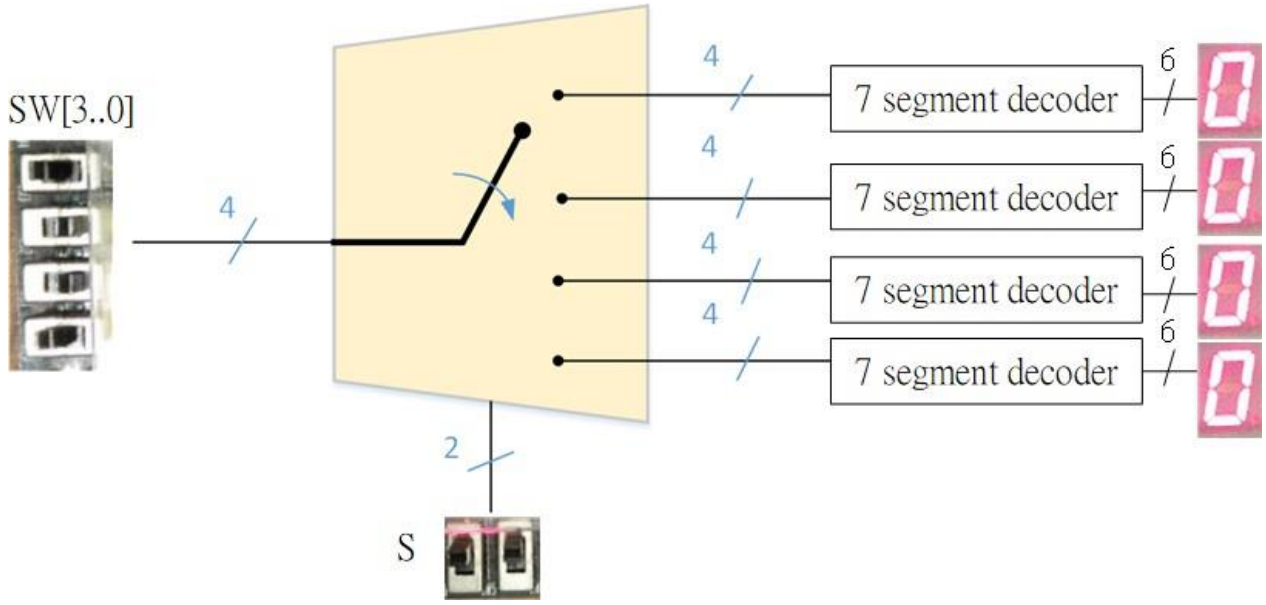
模擬結果擷圖:



第四題

利用解多工器、七段顯示器解碼器，設計下面功能的電路。

Demo: https://www.youtube.com/watch?v=n_PL3VaJOaY&feature=youtu.be



程式碼:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

ENTITY demux1_4b IS
PORT (SW   : IN STD_LOGIC_vector(3 downto 0);
      S      : IN    STD_LOGIC_vector(1 downto 0);
      HEX0_D,HEX1_D,HEX2_D,HEX3_D: OUT STD_LOGIC_vector(0 to 6));
END demux1_4b ;

ARCHITECTURE a OF demux1_4b IS
Signal D0,D1,D2,D3: Std_Logic_Vector(3 downto 0);
begin


      D0<=SW when s = "00" else "0000";
      D1<=SW when s = "01" else "0000";
      D2<=SW when s = "10" else "0000";
```

```
        D3<=SW when s = "11" else "0000";


        with D0 select
                HEX0_D <= "0000001" when "0000",
                        "1001111" when "0001",
                        "0010010" when "0010",
                        "0000110" when "0011",
                        "1001100" when "0100",
                        "0100100" when "0101",
                        "0100000" when "0110",
                        "0001111" when "0111",
                        "0000000" when "1000",
                        "0000100" when "1001",
                        "0001000" when "1010",
                        "1100000" when "1011",
                        "0110001" w


hen "1100",
                        "1000010" when "1101",
                        "0110000" when "1110",
                        "0111000" when others;

        with D1 select
                HEX1_D <= "0000001" when "0000",
                        "1001111" when "0001",
                        "0010010" when "0010",
                        "0000110" when "0011",
                        "1001100" when "0100",
                        "0100100" when "0101",
                        "0100000" when "0110",
                        "0001111" when "0111",
                        "0000000" when "1000",
                        "0000100" when "1001",
                        "0001000" when "1010",
                        "1100000" when "1011",
                        "0110001" when "1100",
                        "1000010" when "1101",
                        "0110000" when "1110",
```

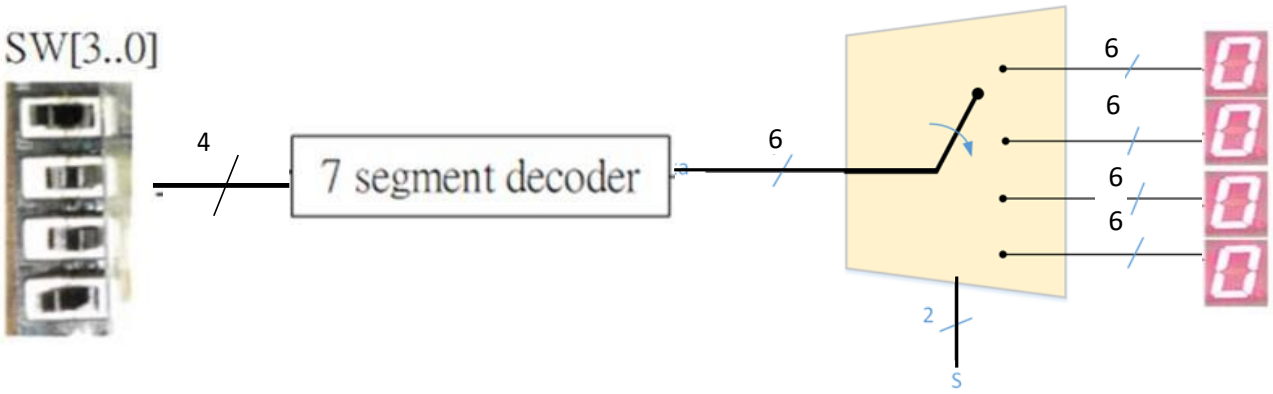
```
                "0111000" when others;

        with D2 select
            HEX2_D <= "0000001" when "0000",
                "1001111" when "0001",
                "0010010" when "0010",
                "0000110" when "0011",
                "1001100" when "0100",
                "0100100" when "0101",
                "0100000" when "0110",
                "0001111" when "0111",
                "0000000" when "1000",
                "0000100" when "1001",
                "0001000" when "1010",
                "1100000" when "1011",
                "0110001" when "1100",
                "1000010" when "1101",
                "0110000" when "1110",
                "0111000" when others;

            with D3 select
            HEX3_D <= "0000001" when "0000",
                "1001111" when "0001",
                "0010010" when "0010",
                "0000110" when "0011",
                "1001100" when "0100",
                "0100100" when "0101",
                "0100000" when "0110",
                "0001111" when "0111",
                "0000000" when "1000",
                "0000100" when "1001",
                "0001000" when "1010",
                "1100000" when "1011",
                "0110001" when "1100",
                "1000010" when "1101",
                "0110000" when "1110",
                "0111000" when others;

END a;
```

請將demo 影片上傳至 youtube，並在下面提供網址:

https://www.youtube.com/watch?v=CEeD8igc0Vo

第五題

利用解多工器、七段顯示器解碼器，設計下面功能的電路。完成後請任課老師 驗收(不限使用 if-then-else，以功能正常為主)



程式碼:

請將demo 影片上傳至 youtube，並在下面提供網址:
https://youtu.be/y_YzSsVjdw8