CPLD 設計作業

範圍：伺服機控制

銘傳大學電腦與通訊工程系

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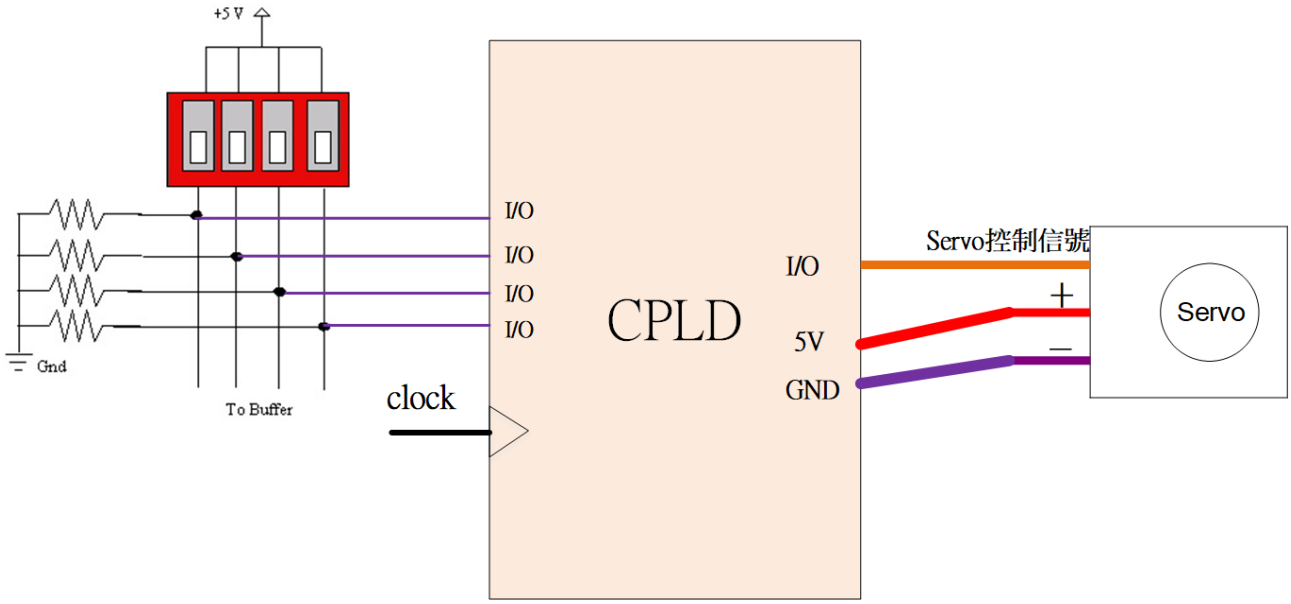
作業成果	應繳作業共 2 題，每題 50 分 我共完成 2 題，應得 100 分
授課教師	陳慶逸

■ 請確實填寫自己寫完成題數，填寫不實者(如上傳與作業明顯無關的答案，或是計算題數有誤者)，本次作業先扣 50 分。

第一題

請設計一個以四個開關來控制伺服機轉動的角度到達 0 度、45 度、90 度、與 135 度的實驗電路，並自行規劃腳位配置以及下載至 DE0 進行功能驗證。



程式碼:

```
library ieee;
 use ieee.std_logic_1164.all;
 use ieee.std_logic_arith.all;
 use ieee.std_logic_unsigned.all;
 entity servo_control is
    generic (divisor: integer :=500);
    port(
          clk : in    std_logic;
          BTN : in    std_logic_vector(3 downto 0);
          q: out std_logic );
 end servo_control;
 architecture a of servo_control is
    signal clk1      : std_logic;    --new clk : 100000Hz
```

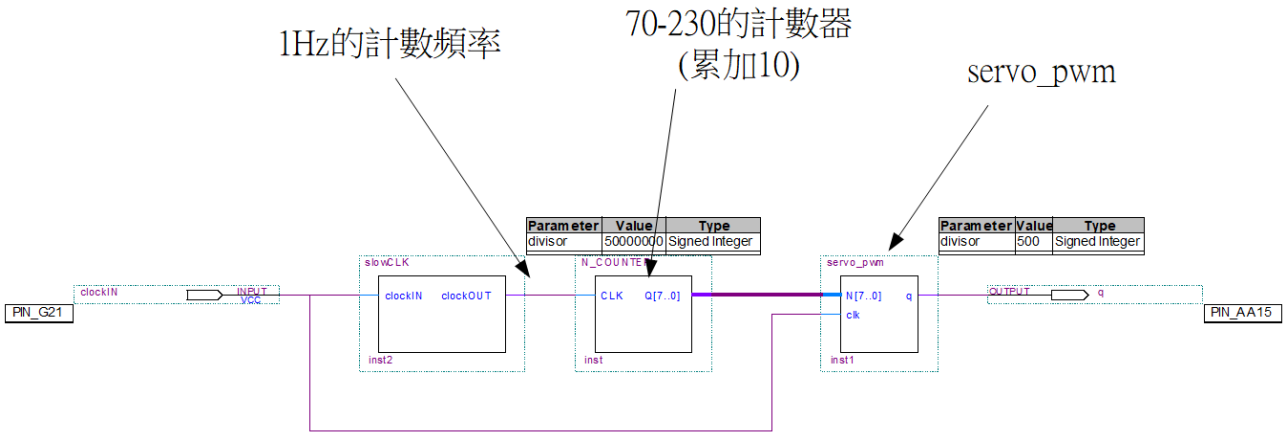
```
    signal cnt2      : std_logic;
    signal data      : integer range 0 to 230;
    signal period : integer range 0 to 1999; --2000 x 0.01ms = 20ms
begin
  ----- clk divider, generate 100000Hz frequence, 0.01ms -----
    process (clk)
        variable cnt1          : integer range 0 to divisor;
        variable divisor2 : integer range 0 to divisor;
  begin
        divisor2 := divisor/2;
if (clk'event and clk='1') then
            if cnt1=divisor then
                cnt1 := 1;
            else
                cnt1 := cnt1 + 1;
            end if;
        end if;

        if (clk'event and clk='1') then
            if (( cnt1=divisor2) or (cnt1=divisor)) then
                cnt2 <= not cnt2;
            end if;
        end if;
        clk1<=    cnt2 ;
    end process;
    process(clk1)
    begin
```

```
        case BTN is
            when "0000" => data <= 70;    --    70(0.7ms)    => 0 degree
            when "0001" => data <= 110; -- 110(1.1ms) => 45 degree
            when "0011" => data <= 150; -- 150(1.5ms) => 90 degree
            when "0111" => data <= 190; -- 190(1.9ms) => 135 degree
            when others => null;
        end case;
    end process;
    ----- up counter -----
    process(clk1,period)
    begin
        if clk1'event and clk1= '1' then
            period <= period + 1;
        end if;
    end process;
    q <= '1' when period < data else '0';
  end a;
```

Demo 網址:

https://youtu.be/F1AYFfXyu3Y

第二題



程式碼 :

```
library ieee;
 use ieee.std_logic_1164.all;
 use ieee.std_logic_arith.all;
 use ieee.std_logic_unsigned.all;
 entity servo_control is
    generic (divisor: integer :=500);
    port(
          clk : in    std_logic;
          BTN : in    std_logic_vector(7 downto 0);
          q: out std_logic );
 end servo_control;
 architecture a of servo_control is
    signal clk1      : std_logic;    --new clk : 100000Hz
    signal cnt2      : std_logic;
    signal data      : integer range 0 to 230;
    signal period : integer range 0 to 1999; --2000 x 0.01ms = 20ms
```

```
begin
  ----- clk divider, generate 100000Hz frequence, 0.01ms -----
    process (clk)
        variable cnt1          : integer range 0 to divisor;
        variable divisor2 : integer range 0 to divisor;
  begin
        divisor2 := divisor/2;
if (clk'event and clk='1') then
            if cnt1=divisor then
                cnt1 := 1;
            else
                cnt1 := cnt1 + 1;
            end if;
        end if;

        if (clk'event and clk='1') then
            if (( cnt1=divisor2) or (cnt1=divisor)) then
                cnt2 <= not cnt2;
            end if;
        end if;
        clk1<=    cnt2 ;
    end process;
    process(clk1)
    begin
        case BTN is
            when "00000000" => data <= 70;    --    70(0.7ms)    => 0 degree
            when "00000001" => data <= 80; -- 80(1.1ms) => 45 degree
```

```
        when "00000010" => data <= 90; -- 150(1.5ms) => 90 degree
        when "00000011" => data <= 100; -- 190(1.9ms) => 135 degree
        when "00000100" => data <= 110;    --    70(0.7ms)    => 0 degree
        when "00000101" => data <= 120; -- 110(1.1ms) => 45 degree
        when "00000110" => data <= 130; -- 150(1.5ms) => 90 degree
        when "00000111" => data <= 140; -- 190(1.9ms) => 135 degree
        when "00001000" => data <= 150;    --    70(0.7ms)    => 0 degree
        when "00001001" => data <= 160; -- 110(1.1ms) => 45 degree
        when "00001010" => data <= 170; -- 150(1.5ms) => 90 degree
        when "00001011" => data <= 180; -- 190(1.9ms) => 135 degree
        when "00001100" => data <= 190;    --    70(0.7ms)    => 0 degree
        when "00001101" => data <= 200; -- 110(1.1ms) => 45 degree
        when "00001110" => data <= 210; -- 150(1.5ms) => 90 degree
        when "00001111" => data <= 220; -- 190(1.9ms) => 135 degree
        when "00010000" => data <= 230; -- 190(1.9ms) => 135 degree
        when others => null;
    end case;
end process;
----- up counter -----
process(clk1,period)
begin
    if clk1'event and clk1= '1' then
        period <= period + 1;
    end if;
end process;
q <= '1' when period < data else '0';
```

```
  end a;
```

```
library ieee;
use ieee.std_logic_1164.all;
entity slowCLK is
generic(divisor:integer:=50000000);
port( clockIN : in std_logic;
clockOUT: out std_logic);
end slowCLK;
architecture arch of slowCLK is
signal PULSE : std_logic;
begin
---------- clk divider ---------------
process(clockIN)
variable counter,divisor2 : integer range 0 to divisor;
begin
divisor2:=divisor/2;
----------- up counter -----------------
if (clockIN 'event and clockIN ='1') then
if counter = divisor then
counter := 1;
else
counter := counter + 1;
end if;
end if;
----- clk generator -----
if (clockIN 'event and clockIN ='1') then
```

```
if (( counter= divisor2) or (counter = divisor))then
PULSE <= not PULSE ;
end if;
end if;
clockOUT <= PULSE ;
end process;
end arch;
```

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
ENTITY UPDOWN_COUNTER is
PORT( CLOCK_50: IN STD_LOGIC;
LEDG : OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
END UPDOWN_COUNTER;
ARCHITECTURE abc OF UPDOWN_COUNTER IS
SIGNAL QN : STD_LOGIC_VECTOR(7 DOWNTO 0);
SIGNAL COUNT: STD_LOGIC;
BEGIN
PROCESS (CLOCK_50)
BEGIN
IF CLOCK_50'event AND CLOCK_50='1' THEN
    if COUNT='0' then
        IF QN ="00010001" THEN
            COUNT<='1';
        ELSE
            QN <= QN+1;
```

```
            END IF;
        ELSE
            QN <="00000000";
            COUNT<='0';
        END IF;
    END IF;
END PROCESS;
LEDG<=QN;
END abc;
```

Demo 網址 :

https://youtu.be/WnHo2qi7g0M