CPLD 設計作業

範圍：Hierarchical Design

銘傳大學電腦與通訊工程系

班級	電通四甲
姓名	余采潔
學號	
作業成果	應繳作業共 3 題，前 2 題每題 30 分，第 3 題 40 分 我共完成 3 題，應得 100 分
授課教師	陳慶逸

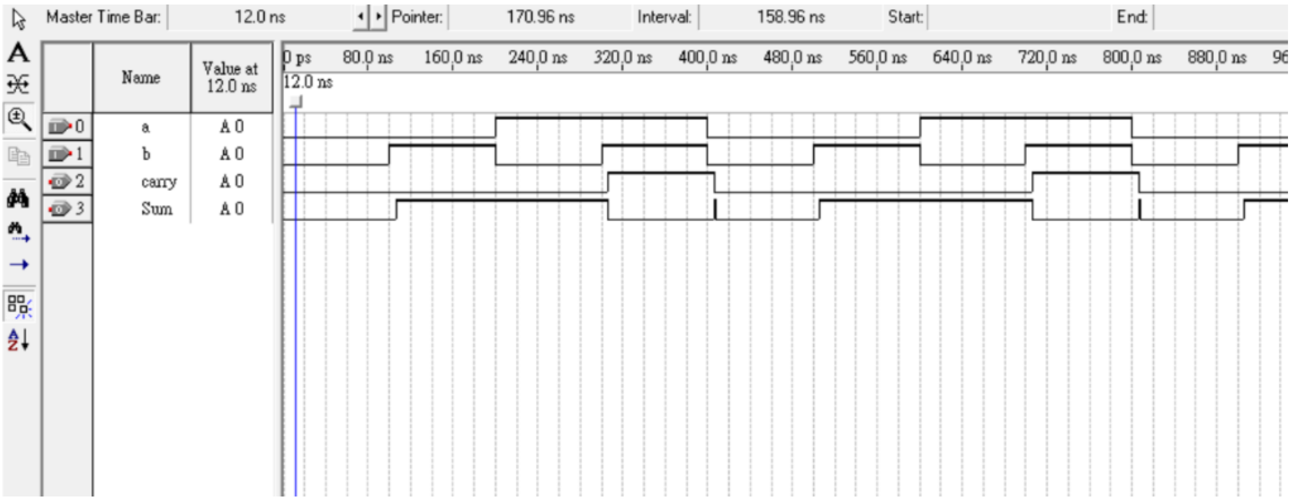
■ 請確實填寫自己寫完成題數，填寫不實者(如上傳與作業明顯無關的答案，或是計算題數有誤者)，本次作業先扣 50 分。

第一題

利用階層式設計實現一個半加法器(h_adder.vhd)。

(互斥或閘: xor_2.vhd, 及閘: and_2.vhd)。

作業應包含程式碼及模擬圖。



Master Time Bar: 12.0 ns　Pointer: 170.96 ns　Interval: 158.96 ns　Start:　End:

	Name	Value at 12.0 ns
0	a	A 0
1	b	A 0
2	carry	A 0
3	Sum	A 0

XOR

```
library ieee;
use ieee.std_logic_1164.all;


entity xor_2 is
port ( X,Y :in std_logic;
S :out std_logic);
end xor_2;


ARCHITECTURE a OF xor_2 IS
begin
S<=X xor Y;
end a;
```

AND

```
library ieee;
use ieee.std_logic_1164.all;
entity and_2 is
port ( M,Z :in std_logic;
C :out std_logic);
end and_2;
ARCHITECTURE a OF and_2 IS
begin
C<=M and Z;
end a;
```

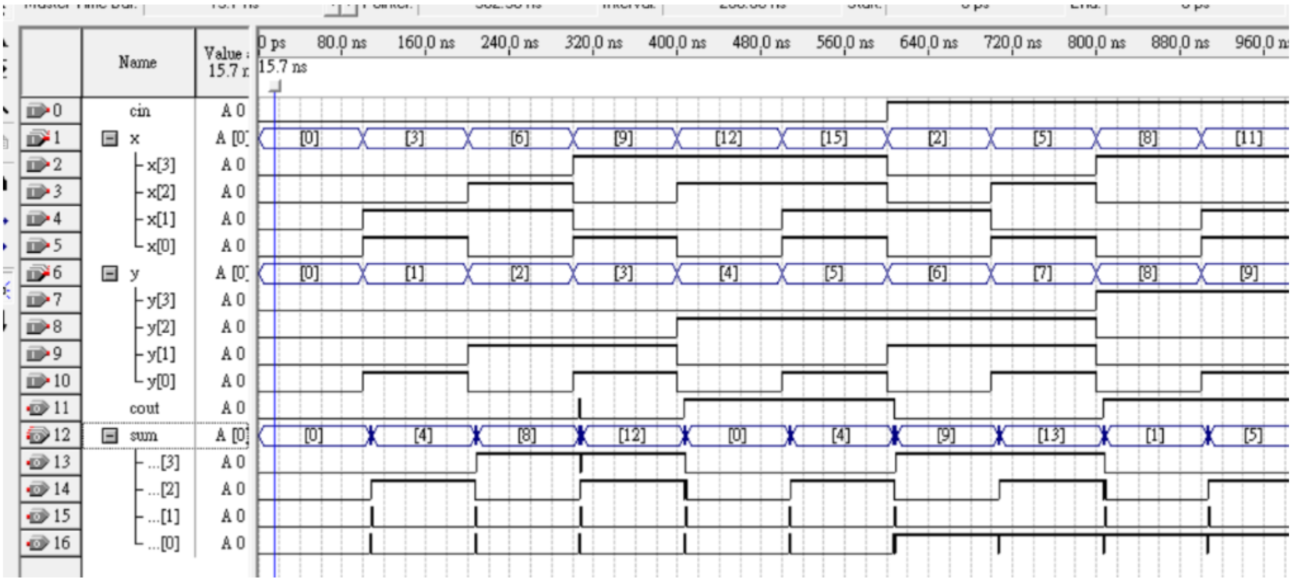
h_adder

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
ENTITY h_adder IS
PORT ( a,b : IN STD_LOGIC;
Sum,carry : out STD_LOGIC);
END h_adder;
ARCHITECTURE a OF h_adder IS
component xor_2
port ( X,Y :in std_logic;
S : out std_logic );
end component;
component and_2
port ( M,Z :in std_logic;
C :out std_logic );

end component;
begin
U1:xor_2 port map (a,b,Sum);
U2:and_2 port map (a,b,carry);
END a;
```

第二題

利用階層式設計實現一個 4-bit 加法器(add_4_bits.vhd)。

(1-bit 加法器: add_1_bit.vhd)。



add_1_bits

```
library IEEE;

use IEEE.STD_LOGIC_1164.all;

ENTITY add_1_bits IS

port

(a :in std_logic;

      b :in std_logic;

            ci:in std_logic;

                  s :out std_logic;

                        c :out std_logic);


end add_1_bits;


ARCHITECTURE a OF add_1_bits IS
```

```
begin
s<=a xor b xor ci;
c<=(a and b ) or (a and ci) or (b and ci);
end a;
```

add_4_bits

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

ENTITY add_4_bits IS
PORT ( x : in STD_LOGIC_vector(3 downto 0);
y : in STD_LOGIC_vector(3 downto 0);
cin : in STD_LOGIC;
sum: out std_logic_vector(3 downto 0);
cout: out std_logic);
END add_4_bits ;

ARCHITECTURE a OF add_4_bits IS
component add_1_bits
port
(
a :in std_logic;
b :in std_logic;
ci:in std_logic;

s :out std_logic;
c :out std_logic
);
end component;

signal s1,s2,s3,s4 : std_logic;
BEGIN
IC1:add_1_bits port map(a=>x(0),b=>y(0),c=>s1,s=>sum(0),ci=>cin);
IC2:add_1_bits port map(a=>x(1),b=>y(1),c=>s2,s=>sum(1),ci=>s1);
IC3:add_1_bits port map(a=>x(2),b=>y(2),c=>s3,s=>sum(2),ci=>s2);
IC4:add_1_bits port map(a=>x(3),b=>y(3),c=>cout,s=>sum(3),ci=>s3);

END a;
```

第三題

以 5 個四對一的多工器實現一個十六對一的多工器。

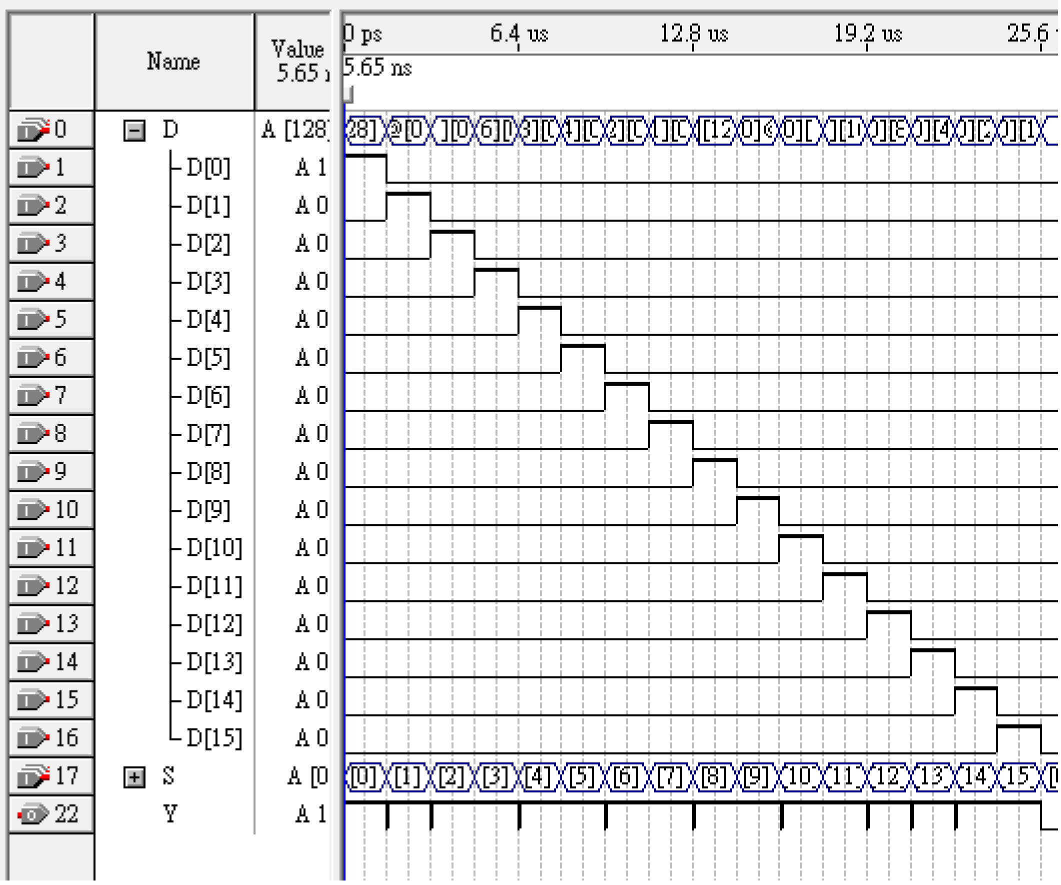
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;


ENTITY zxc IS
PORT (   D : IN STD_LOGIC_vector(0 to 15);
         S : IN    STD_LOGIC_vector(3 downto 0);
         Y : OUT STD_LOGIC);
END zxc ;


ARCHITECTURE a OF zxc IS
   component mux4_1
        port ( d0,d1,d2,d3 :in std_logic;
             S1,S2         :IN std_logic;
             Y        :out std_logic );
   end component;


 signal m :std_logic_vector(0 to 3);
 BEGIN
   mux1:mux4_1 port map(D(0),D(1),D(2),D(3),S(1),S(0),m(0));
   mux2:mux4_1 port map(D(4),D(5),D(6),D(7),S(1),S(0),m(1));
   mux3:mux4_1 port map(D(8),D(9),D(10),D(11),S(1),S(0),m(2));
   mux4:mux4_1 port map(D(12),D(13),D(14),D(15),S(1),S(0),m(3));
   mux5:mux4_1 port map(m(0),m(1),m(2),m(3),S(3),S(2),Y);
```

```
      END a;
```

mux4_1

```
library ieee;
use ieee.std_logic_1164.all;

entity mux4_1 is
port (    d0,d1,d2,d3 :in std_logic;
            S1,S2                :IN std_logic;
            Y                 :out std_logic );
               end mux4_1;

ARCHITECTURE a OF mux4_1 IS
BEGIN
      process (S1,S2,d0,d1,d2,d3)
       begin

      if S1='0' and S2='0'then
             Y <= d0;
      elsif S1='0' and S2='1' then
             Y <= d1;
       elsif S1='1' and S2='0' then
             Y <= d2;
      elsif S1='1' and S2='1' then
```

```
            Y <= d3;
        end if;
        end process;

END a;
```


Name
Value
5.65 ı
0 ps
6.4 us
12.8 us
19.2 us
25.6
5.65 ns
0
D
A [128]
1
D[0]
A 1
2
D[1]
A 0
3
D[2]
A 0
4
D[3]
A 0
5
D[4]
A 0
6
D[5]
A 0
7
D[6]
A 0
8
D[7]
A 0
9
D[8]
A 0
10
D[9]
A 0
11
D[10]
A 0
12
D[11]
A 0
13
D[12]
A 0
14
D[13]
A 0
15
D[14]
A 0
16
D[15]
A 0
17
S
A [0
22
Y
A 1
[0]
[1]
[2]
[3]
[4]
[5]
[6]
[7]
[8]
[9]
10
11
12
13
14
15