Problems in Chapter 1

- **1-3, 1-4, 1-7, 1-12(a), 1-15, 1-16, 1-19**

1-3.*

Decimal, Binary, Octal and Hexadecimal Numbers from $(16)_{10}$ to $(31)_{10}$

Dec	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Bin	1 0000	1 0001	1 0010	1 0011	1 0100	1 0101	1 0110	1 0111	1 1000	1 1001	1 1010	1 1011	1 1100	1 1101	1 1110	1 1111
Oct	20	21	22	23	24	25	26	27	30	31	32	33	34	35	36	37
Hex	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

1-4.

$$96K = 96 \times 2^{10} = 98,304\ Bits$$

$$640M = 640 \times 2^{20} = 671,088,640\ Bits$$

$$4G = 4 \times 2^{30} = 4,294,967,296\ Bits$$

1-7.*

$$(1001101)_2 = 2^6 + 2^3 + 2^2 + 2^0 = 77$$

$$(1010011.101)_2 = 2^6 + 2^4 + 2^1 + 2^0 + 2^{-1} + 2^{-3} = 83.625$$

$$(10101110.1001)_2 = 2^7 + 2^5 + 2^3 + 2^2 + 2^1 + 2^{-1} + 2^{-4} = 174.5625$$

1-12.

a)
$$\begin{array}{r} 1101 \\ \times\underline{1011} \\ 1101 \\ 1101 \\ 0000 \\ \underline{1101} \\ 10001111 \end{array}$$

b)
$$\begin{array}{r} 0101 \\ \times\underline{1010} \\ 0000 \\ 0101 \\ 0000 \\ \underline{0101} \\ 0110010 \end{array}$$

c)
$$\begin{array}{r} 100111 \\ \times\underline{011011} \\ 100111 \\ 100111 \\ 000000 \\ 100111 \\ 100111 \\ \underline{000000} \\ 10000011101 \end{array}$$

1-15.

a)

0	1	2	3	4	5	6	7	8	9
A	B	C	D	E	F	G	H	I	J

b)

$$\begin{array}{r|l} 20\,|\underline{2007} & 7 \\ 20\,|\underline{100} & 0 \\ 20\,|\underline{5} & 5 \\ 0 & \end{array} \longrightarrow 507_{20}$$

c) $(BCI.G)_{20} = 11 \times 20^2 + 12 \times 20^1 + 18 \times 20^0 + 16 \times 20^{-1} = (4658.8)_{10}$

1-16.*

a) $(\mathrm{BEE})_r = (2699)_{10}$

$$11 \times r^2 + 14 \times r^1 + 14 \times r^0 = 2699$$

$$11 \times r^2 + 14 \times r - 2685 = 0$$

By the quadratic equation: $r = 15$ or ≈ -16.27

ANSWER: $r = 15$

b) $(365)_r = (194)_{10}$

$$3 \times r^2 + 6 \times r^1 + 5 \times r^0 = 194$$

$$3 \times r^2 + 6 \times r - 189 = 0$$

By the quadratic equation: $r = -9$ or 7

ANSWER: r = 7

1-19.*

$$(694)_{10} = (0110\ 1001\ 0100)_{BCD}$$
$$(835)_{10} = (1000\ 0011\ 0101)_{BCD}$$

$$
\begin{array}{rrrr}
 & 1 & & \\
 & 0110 & 1001 & 0100 \\
 & \underline{+1000} & \underline{+0011} & \underline{+0101} \\
 & 1111 & 1100 & 1001 \\
 & \underline{+0110} & \underline{+0110} & \underline{+0000} \\
0001 & 0101 & 1\ 0010 & 1001
\end{array}
$$

Problems in Chapter 2-1

- **d; 2-12b; 2-13a, c; 2-14b; 2-15a, c; 2-16b; 2-17b; 2-19a; 2-21; 2-24a, c;**

2-1a

- Demonstrate by means of truth tables the validity of the following identities:

a) $\overline{XYZ} = \bar{X} + \bar{Y} + \bar{Z}$

Verification of DeMorgan's Theorem

X	Y	Z	XYZ	$\overline{XYZ}$	$\bar{X}+\bar{Y}+\bar{Z}$
0	0	0	0	1	1
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	0	1	1
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	1	0	0

2-1b

- Demonstrate by means of truth tables the validity of the following identities:

b) $X + YZ = (X + Y) \cdot (X + Z)$

The Second Distributive Law

X	Y	Z	YZ	$X+YZ$	$X+Y$	$X+Z$	$(X+Y)(X+Z)$
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

2-1c

- Demonstrate by means of truth tables the validity of the following identities:

c) $\bar{X}Y + \bar{Y}Z + X\bar{Z} = X\bar{Y} + Y\bar{Z} + \bar{X}Z$

X	Y	Z	$\bar{X}Y$	$\bar{Y}Z$	$X\bar{Z}$	$\bar{X}Y+\bar{Y}Z+X\bar{Z}$	$X\bar{Y}$	$Y\bar{Z}$	$\bar{X}Z$	$X\bar{Y}+Y\bar{Z}+\bar{X}Z$
0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	0	1	1
0	1	0	1	0	0	1	0	1	0	1
0	1	1	1	0	0	1	0	0	1	1
1	0	0	0	0	1	1	1	0	0	1
1	0	1	0	1	0	1	1	0	0	1
1	1	0	0	0	1	1	0	1	0	1
1	1	1	0	0	0	0	0	0	0	0

2-2a

- Prove the identity of each of the following Boolean equations, using algebraic manipulation:

$$\overline{X}\,\overline{Y} + \overline{X}Y + XY = \overline{X} + Y$$

$$\overline{X}\,\overline{Y} + \overline{X}Y + XY = \overline{X}(\overline{Y} + Y) + XY \qquad \text{Distributive Law}$$

$$= \overline{X} + XY$$

$$= \overline{X} + Y \qquad \text{Simplification Theorem}$$

2-3a

- Prove the identity of each of the following Boolean equations, using algebraic manipulation:

$$AB\overline{C} + B\overline{C}\,\overline{D} + BC + \overline{C}D = B + \overline{C}D$$

$$AB\overline{C} + B\overline{C}\,\overline{D} + BC + \overline{C}D = AB\overline{C} + B\overline{C}\,\overline{D} + (A+\overline{A})BC + (B+\overline{B})\overline{C}D$$

$$= AB(\overline{C}+C) + \overline{A}BC + B\overline{C}(\overline{D}+D) + \overline{B}\,\overline{C}D$$ Distributive Law

$$= AB + \overline{A}BC + B\overline{C} + \overline{B}\,\overline{C}D$$ Minimization Law

$$= B(A + \overline{A}C + \overline{C}) + \overline{B}\,\overline{C}D$$ Simplification Theorem

$$= B(A + C + \overline{C}) + \overline{B}\,\overline{C}D$$

$$= B + \overline{B}\,\overline{C}D$$ Simplification Theorem

$$= B + \overline{C}D$$

2-3c

- Prove the identity of each of the following Boolean equations, using algebraic manipulation:

$$A\overline{D} + \overline{A}B + \overline{C}D + \overline{B}C = (\overline{A} + \overline{B} + \overline{C} + \overline{D})(A + B + C + D)$$

$$Dual - left:$$

$$(A + \overline{D})(\overline{A} + B)(\overline{C} + D)(\overline{B} + C) = (A\overline{A} + AB + \overline{A}\overline{D} + B\overline{D})(\overline{B}\overline{C} + C\overline{C} + \overline{B}D + CD)$$

$$= ABCD + \overline{A}\overline{B}\overline{C}\overline{D}$$

$$Dual - right:$$

$$ABCD + \overline{A}\overline{B}\overline{C}\overline{D}$$

So the original equation is right.

2-6b

- Simplify the following expressions to expressions containing a minimum number of literals:

$$(\overline{A+B+C})\overline{ABC} = \bar{A}\bar{B}\bar{C}(\bar{A}+\bar{B}+\bar{C})$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$$

$$= \bar{A}\bar{B}\bar{C}$$

2-6d

- Simplify the following expressions to expressions containing a minimum number of literals:

$$
\begin{aligned}
\overline{A}\,\overline{B}D + \overline{A}\,\overline{C}D + BD &= \overline{A}\,\overline{B}D + \overline{A}\,\overline{C}D + (A + \overline{A})BD \\
&= \overline{A}\,\overline{B}D + \overline{A}\,\overline{C}D + ABD + \overline{A}BD \\
&= \overline{A}D(\overline{B} + B) + \overline{A}\,\overline{C}D + ABD \\
&= \overline{A}D + \overline{A}\,\overline{C}D + ABD \\
&= \overline{A}D(1 + \overline{C}) + ABD \\
&= \overline{A}D + ABD \\
&= D(\overline{A} + AB) \\
&= D(\overline{A} + B)
\end{aligned}
$$

2-10a

- Obtain the truth table of the following functions, and express each function in sum-of-minterms and product-of-maxterms form:

$(XY + Z)(Y+XZ)$

X	Y	Z	a
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Sum of Minterms: $\bar{X}YZ + X\bar{Y}Z + XY\bar{Z} + XYZ$

Product of Maxterms: $(X + Y + Z)(X + Y + \bar{Z})(X + \bar{Y} + Z)(\bar{X} + Y + Z)$

2-10c

- Obtain the truth table of the following functions, and express each function in sum-of-minterms and product-of-maxterms form:

$$WX\overline{Y} + WX\overline{Z} + WXZ + Y\overline{Z}$$

W	X	Y	Z	c
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Sum of Minterms:

$$\overline{W}\overline{X}Y\overline{Z} + \overline{W}XY\overline{Z} + W\overline{X}Y\overline{Z} + WX\overline{Y}\overline{Z} + WX\overline{Y}Z + WXY\overline{Z} + WXYZ$$

Product of Maxterms:

$$(W+X+Y+Z)(W+X+Y+\overline{Z})(W+X+\overline{Y}+\overline{Z})$$
$$(W+\overline{X}+Y+Z)(W+\overline{X}+Y+\overline{Z})(W+\overline{X}+\overline{Y}+\overline{Z})$$
$$(\overline{W}+X+Y+Z)(\overline{W}+X+Y+\overline{Z})(\overline{W}+X+\overline{Y}+\overline{Z})$$

2-11a

- For the Boolean functions E and F, given in the truth table:

X	Y	Z	E	F
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	1

(a) List the minterms and maxterms of each function

Minterms of E:

$$\overline{X}\,\overline{Y}Z, \overline{X}Y\overline{Z}, X\overline{Y}\,\overline{Z}, XY\overline{Z}$$

Maxterms of E:

$$X+Y+Z, X+\overline{Y}+\overline{Z}, \overline{X}+Y+\overline{Z}, \overline{X}+\overline{Y}+\overline{Z}$$

Minterms of F:

$$\overline{X}\,\overline{Y}\,\overline{Z}, \overline{X}Y\overline{Z}, X\overline{Y}\,\overline{Z}, XYZ$$

Maxterms of F:

2-11b

- For the Boolean functions E and F, given in the truth table:

X	Y	Z	E	F
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	1

(a) List the minterms of E' and F'

Minterms of E':

$$\overline{X}\,\overline{Y}\,\overline{Z}, \overline{X}YZ, X\overline{Y}Z, XYZ$$

Minterms of F':

2-11c

- For the Boolean functions E and F, given in the truth table:

X	Y	Z	E	F
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	1

(a) Express E and F in sum-of-minterms algebraic form

E:

$$E = \overline{X}\,\overline{Y}Z + \overline{X}Y\overline{Z} + X\overline{Y}\,\overline{Z} + XY\overline{Z}$$

F:

$$F = \overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}Y\overline{Z} + X\overline{Y}\,\overline{Z} + XYZ$$

2-12b

- Convert the following expressions into sum-of-products and product-of-sums forms:

  $\overline{X} + X(X + \overline{Y})(Y + \overline{Z})$

$$\overline{X} + X(X + \overline{Y})(Y + \overline{Z}) = (\overline{X} + X)(\overline{X} + (X + \overline{Y})(Y + \overline{Z}))$$ The distributive law

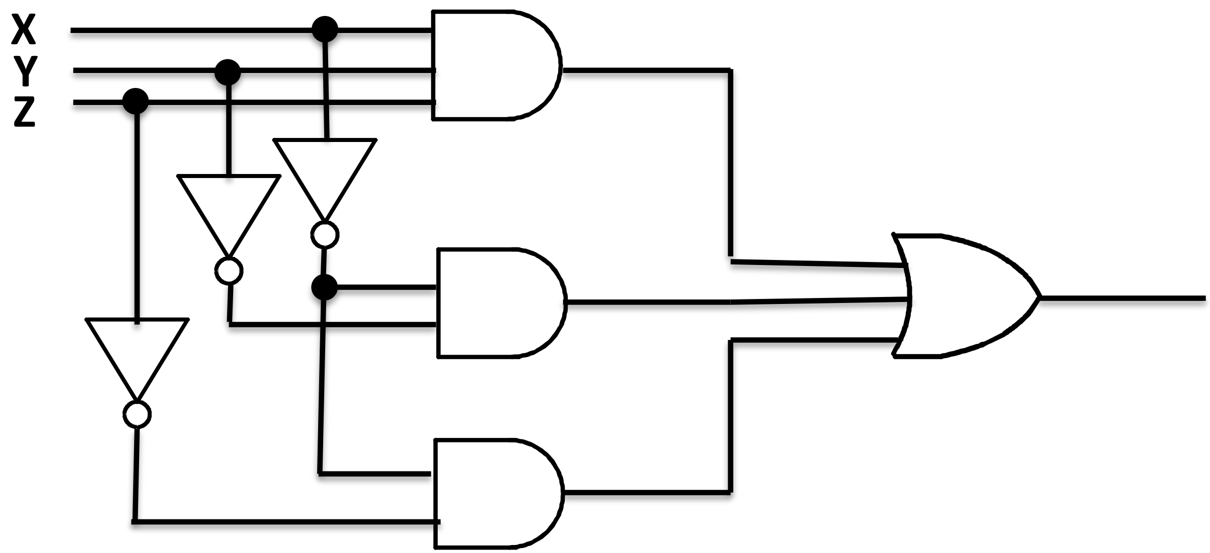
$$= (\overline{X} + X + \overline{Y})(\overline{X} + Y + \overline{Z}) \quad \text{p.o.s.}$$

$$= (1 + \overline{Y})(\overline{X} + Y + \overline{Z}) = \overline{X} + Y + \overline{Z} \quad \text{s.o.p.}$$

2-13a

- Draw the logic diagram for the following Boolean expressions:

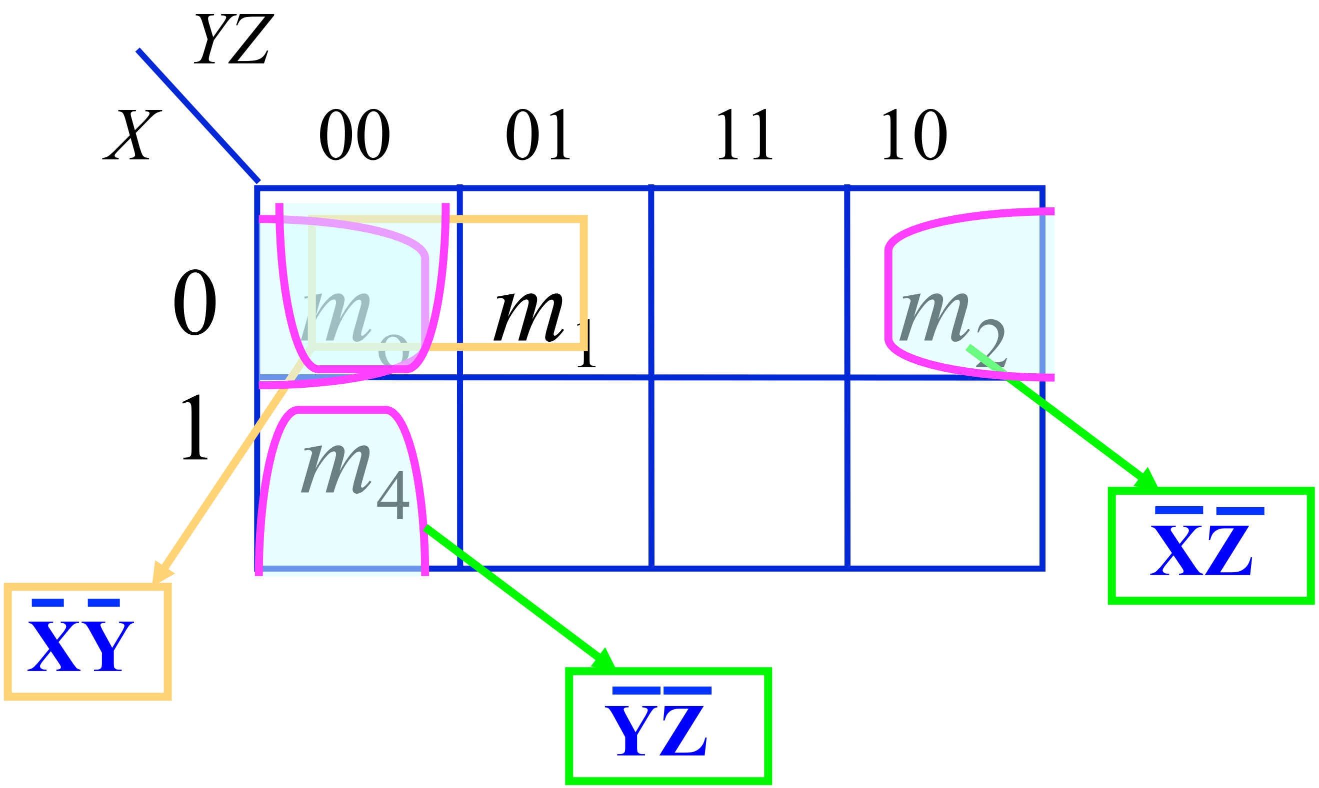
$$XYZ + \overline{X}\,\overline{Y} + \overline{X}\,\overline{Z}$$



2-14b

- Optimize the following Boolean functions by means of a 3-variable map:

$$F(X,Y,Z) = \sum M(0,1,2,4) = \overline{X}\,\overline{Y} + \overline{Y}\,\overline{Z} + \overline{X}\,\overline{Z}$$

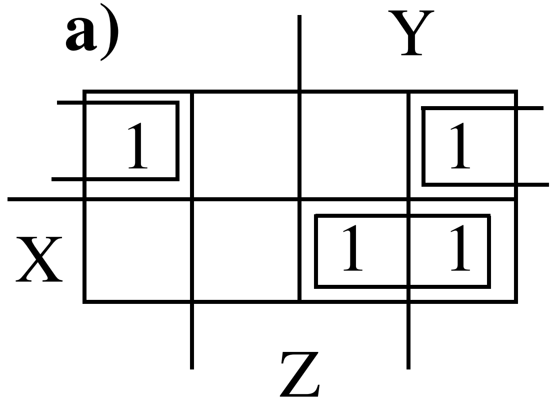


2-15a

- Optimize the following Boolean functions using a map:

$$\overline{X}\,\overline{Z} + Y\overline{Z} + XYZ$$

a)



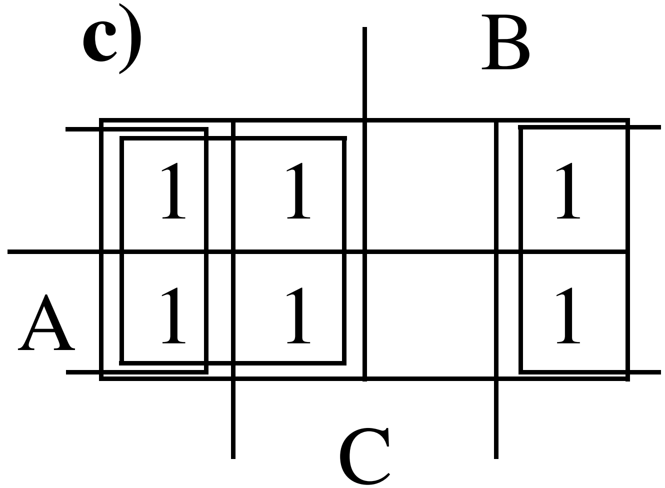
$$\overline{X}\,\overline{Z} + XY$$

2-15c

- Optimize the following Boolean functions using a map:

$$\overline{A}\,\overline{B} + A\overline{C} + \overline{B}C + \overline{A}B\overline{C}$$

c)



$$\overline{B} + \overline{C}$$

2-16b

- Optimize the following Boolean functions by means of a 4-variable map::

$$F(W,X,Y,Z)=\sum m(0,2,5,6,8,10,13,14,15)$$

$$=\overline{X}\,\overline{Z}+Y\overline{Z}+WXZ+X\overline{Y}Z$$

$WX \backslash YZ$	00	01	11	10
00	1			1
01		1		1
11		1	1	1
10	1			1

2-17b

- Optimize the following Boolean functions by means of a 4-variable map:

$$F(A,B,C,D) = \sum m(1,3,6,7,9,11,12,13,15)$$

$$= \overline{B}D + CD + \overline{A}BC + AB\overline{C}$$

$AB \backslash CD$	00	01	11	10
00		1	1	
01			1	1
11	1	1	1	
10		1	1	

2-19a

- Find all the prime implicants for the following Boolean functions, and determine which are essential:

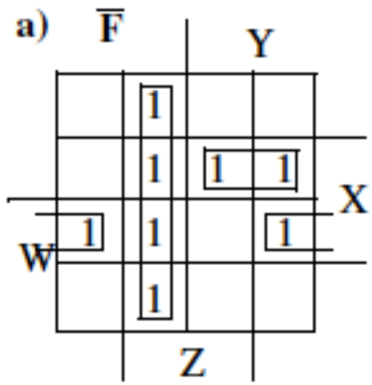
$$F(W,X,Y,Z)=\sum m(0,2,5,7,8,10,12,13,14,15)$$

WX \ YZ	00	01	11	10
00	1			1
01		1	1	
11	1	1	1	1
10	1			1

a) $Prime = XZ, WX, \bar{X}\bar{Z}, W\bar{Z}$

$Essential = XZ, \bar{X}\bar{Z}$

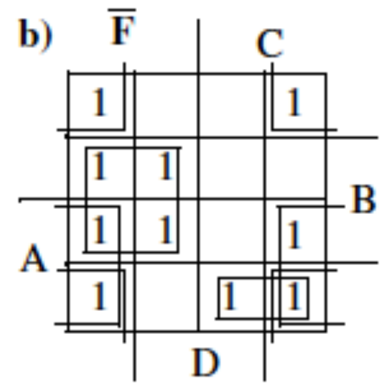
2-21.



$\overline{F} = \Sigma m(1, 5, 6, 7, 9, 12, 13, 14)$

$F = \overline{\bar{Y}Z + WX\bar{Z} + \bar{W}XY}$

$F = (Y + \bar{Z})(\bar{W} + \bar{X} + Z)(W + \bar{X} + \bar{Y})$

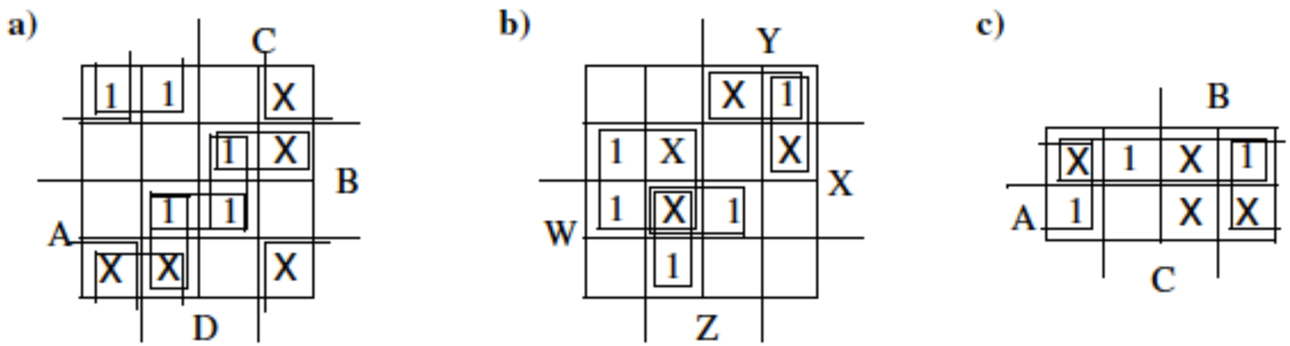


$\overline{F} = \Sigma m(0, 2, 4, 5, 8, 10, 11, 12, 13, 14)$

$F = \overline{B\bar{C} + \bar{B}\bar{D} + A\bar{D} + A\bar{B}C}$

$F = (\bar{B} + C)(B + D)(\bar{A} + D)(\bar{A} + B + \bar{C})$

2-24.



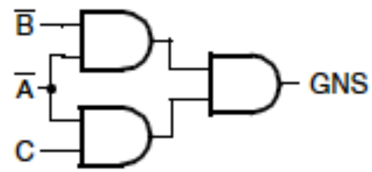
$F = \overline{B}\,\overline{C} + BCD + ABD$ $\quad F = X\overline{Y} + W\overline{Y}Z + WXZ + (\overline{W}\,\overline{X}Y \text{ or } \overline{W}Y\overline{Z})$ $\quad F = \overline{A} + \overline{C}$

3-7, 3-8, 3-11, 3-13, 3-14, 3-16, 6-5, 6-6
Note: in Figure 6-26, the coordinates along the time axis are 0, 0.08, 0.16, 0.24, ……

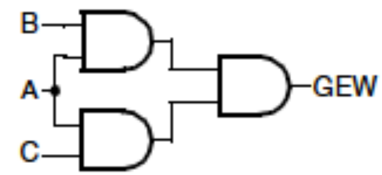
3-24, 3-25, 3-27, 3-28, 3-29, 3-37, 3-44, 3-47

3-7.+

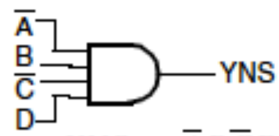
ABCD	GNS	YNS	RNS	GEW	YEW	REW
0000	1	0	0	0	0	1
0001	1	0	0	0	0	1
0011	1	0	0	0	0	1
0010	1	0	0	0	0	1
0110	1	0	0	0	0	1
0111	1	0	0	0	0	1
0101	0	1	0	0	0	1
0100	0	0	1	0	0	1
1100	0	0	1	1	0	0
1101	0	0	1	1	0	0
1111	0	0	1	1	0	0
1110	0	0	1	1	0	0
1010	0	0	1	1	0	0
1011	0	0	1	1	0	0
1001	0	0	1	0	1	0
1000	0	0	1	0	0	1



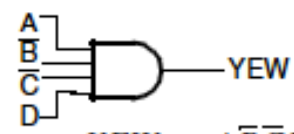
$$GNS = \overline{A}C + \overline{A}\overline{B}$$



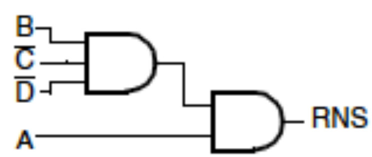
$$GEW = AB + AC$$



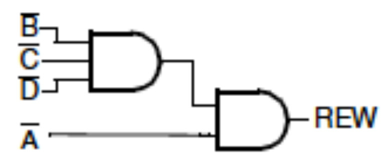
$$YNS = \overline{A}B\overline{C}D$$



$$YEW = A\overline{B}\overline{C}D$$



$$RNS = A + B\overline{C}\overline{D}$$



$$REW = \overline{A} + \overline{B}\overline{C}\overline{D}$$

3-8.

A	B	C	S5	S4	S3	S2	S1	S0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

$S0 = C$

$S1 = 0$

$S2 = \overline{A}B\overline{C} + AB\overline{C}$

$S3 = \overline{A}BC + A\overline{B}C$

$S4 = A\overline{B} + AC$

$S5 = AB$

3-11.

a)

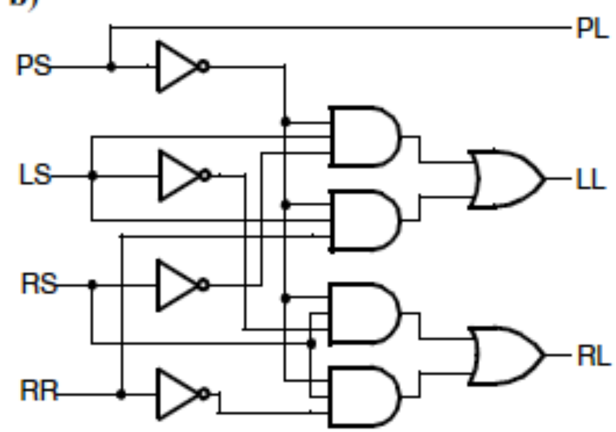
PS	LS	RS	RR	PL	LL	RL
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

$PL = PS$

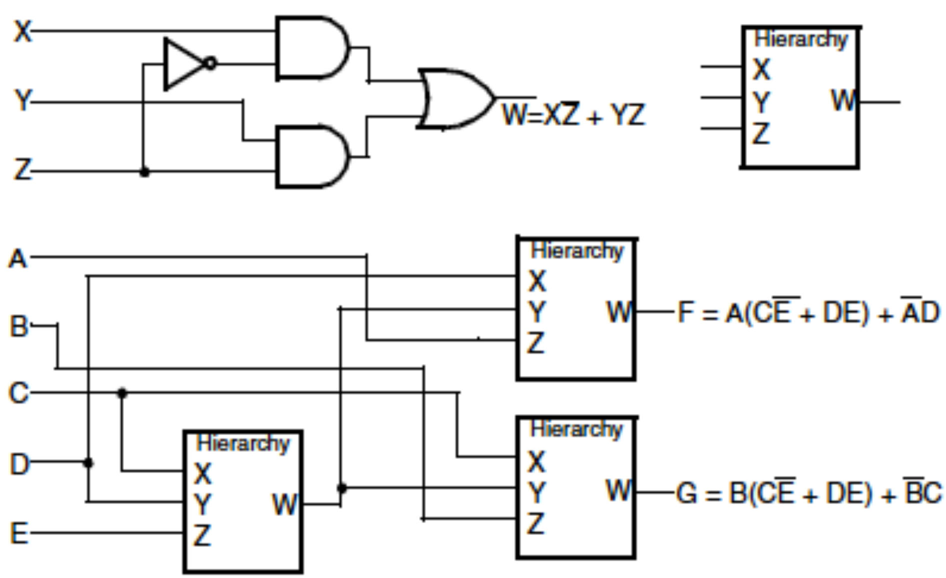
$LL = \overline{PS}\, LS\, \overline{RS} + \overline{PS}\, LS\, RR$

$RL = \overline{PS}\, \overline{LS}\, RS + \overline{PS}\, RS\, \overline{RR}$

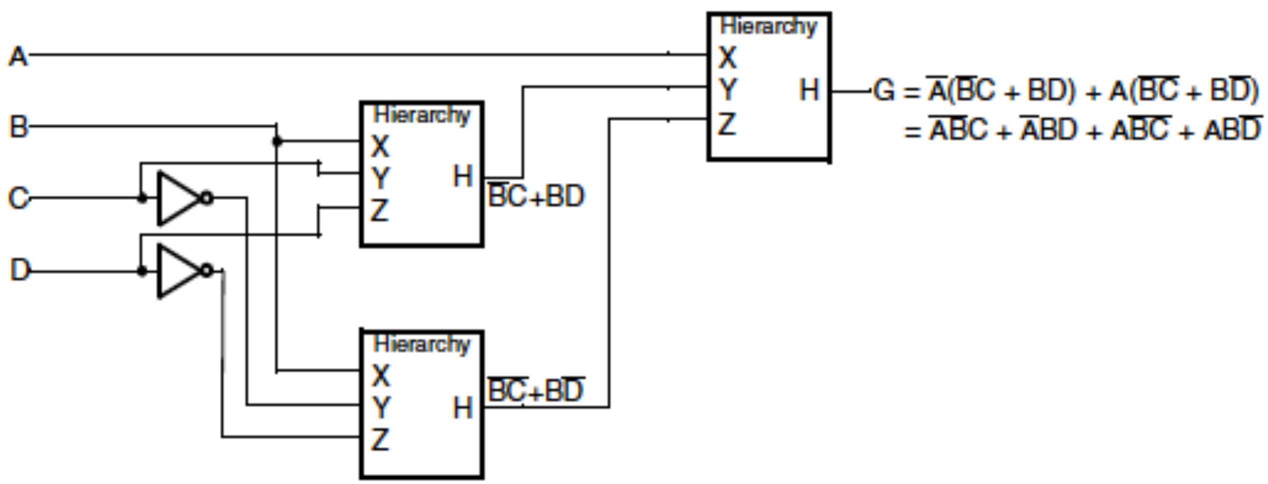
b)



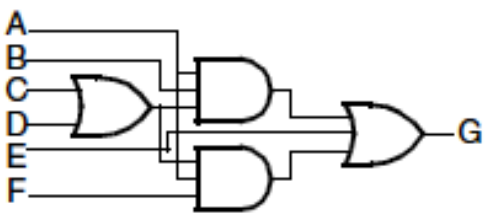
3-13.


X
Y
Z
$W = X\bar{Z} + YZ$
Hierarchy
X
Y
Z
W
A
B
C
D
E
Hierarchy
X
Y
Z
W
$F = A(C\bar{E} + DE) + \bar{A}D$
Hierarchy
X
Y
Z
W
$G = B(C\bar{E} + DE) + \bar{B}C$
Hierarchy
X
Y
Z
W

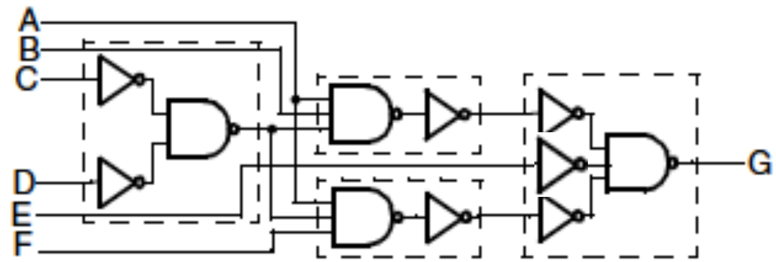
3-14.


A
B
C
D
Hierarchy
X
Y
Z
H
$\bar{B}C+BD$
Hierarchy
X
Y
Z
H
$\overline{BC}+B\bar{D}$
Hierarchy
X
Y
Z
H
$G = \bar{A}(\bar{B}C + BD) + A(\overline{BC} + B\bar{D})$
$= \bar{A}\bar{B}C + \bar{A}BD + A\overline{BC} + AB\bar{D}$

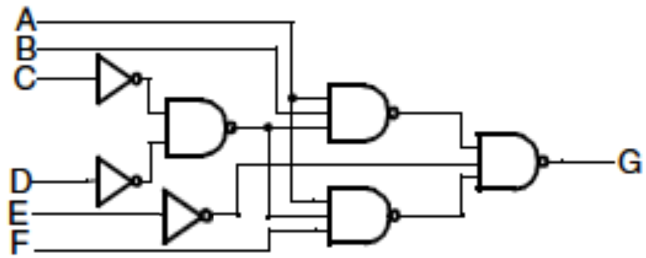
3-16.



a) Original circuit

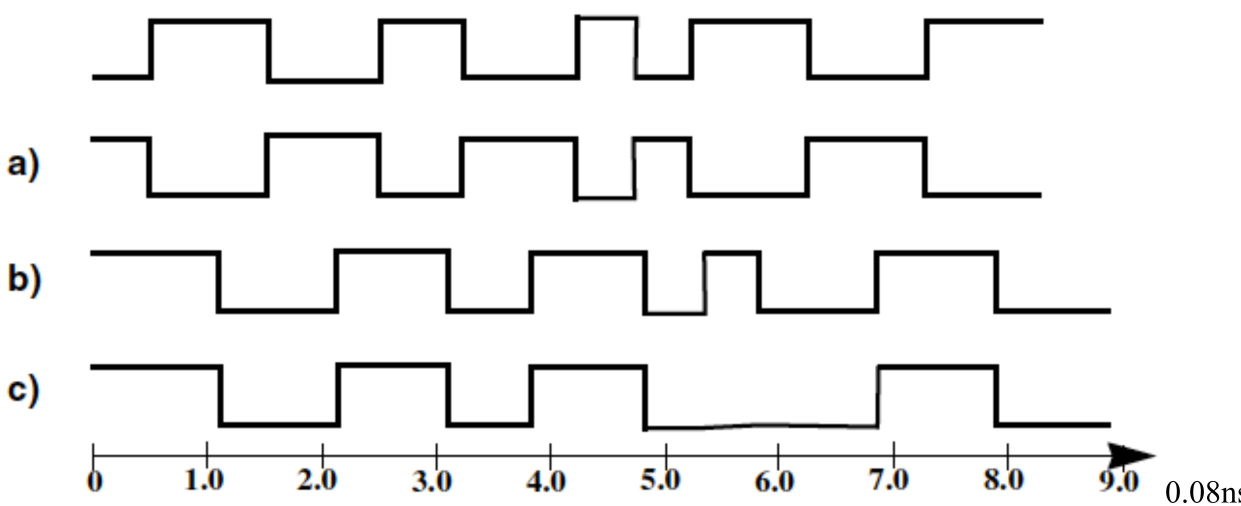


b) Replacement with equivalents

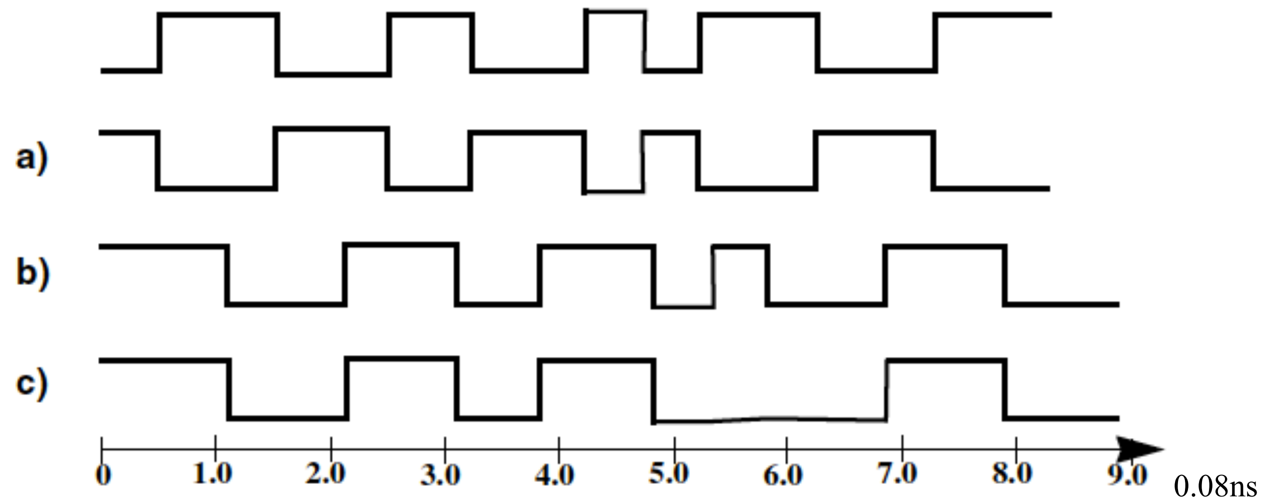


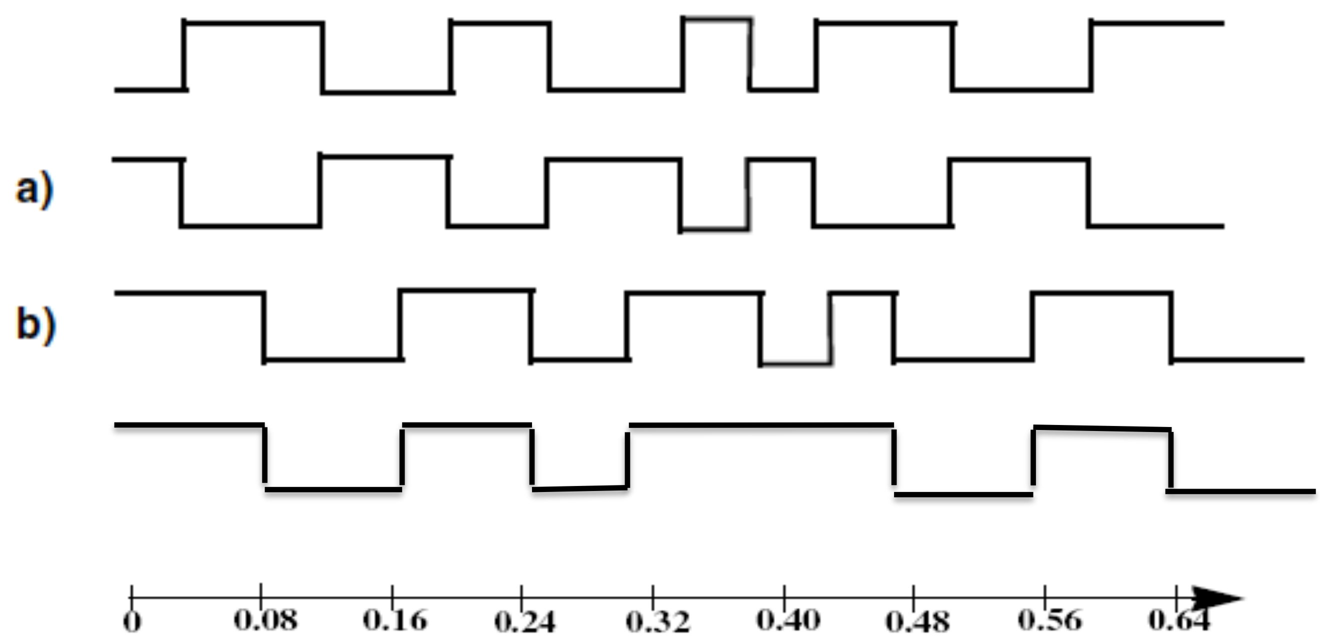
c) Cancel inverters

6-5.



6-5.


a)
b)
c)
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
0.08ns


a)
b)
0
0.08
0.16
0.24
0.32
0.40
0.48
0.56
0.64

6-6.

a) $t_{PHL\text{-}C,D \text{ to } F} = 2\,t_{PLH} + 2t_{PHL} = 2(0.36) + 2(0.20) = 1.12$ ns

$t_{PLH\text{-}C,D \text{ to } F} = 2t_{PHL} + 2t_{PLH} = 2(0.20) + 2(0.36) = 1.12$ ns

$t_{pd} = 1.12$ ns

$t_{PHL\text{-}\overline{B} \text{ to } F} = 2t_{PHL} + t_{PLH} = 2(0.20) + (0.36) = 0.76$ ns

$t_{PLH\text{-}\overline{B} \text{ to } F} = 2\,t_{PLH} + t_{PHL} = 2(0.36) + (0.20) = 0.92$ ns

$t_{pd\text{-}\overline{B} \text{ to } F} = 0.92 + 0.76 = 0.84$ ns

$t_{PHL\text{-}A,B,\overline{C} \text{ to } F} = t_{PLH} + t_{PHL} = 0.36 + 0.20 = 0.56$ ns

$t_{PLH\text{ - }A,B,\overline{C} \text{ to } F} = t_{PHL} + t_{PLH} = 0.20 + 0.36 = 0.56$ ns

$t_{pd\text{ - }A,B,\overline{C} \text{ to } F} = 0.56$ ns

b) $t_{pd\text{-}C,D \text{ to } F} = 4\,t_{pd} = 4(0.28) = 1.12$ ns

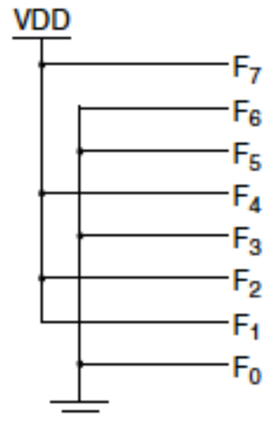
$t_{pd\text{-}\overline{B} \text{ to } F} = 3\,t_{pd} = 3(0.28) = 0.84$ ns

$t_{pd\text{-}A,B,C} \text{ to } F = 2\,t_{pd} = 2(0.28) = 0.56$ ns

c) For paths through an odd number of inverting gates with unequal gate t_{PHL} and t_{PLH}, path t_{PHL}, t_{PLH}, and t_{pd} are different. For paths through an even number of inverting gates, path t_{PHL}, t_{PLH}, and t_{pd} are equal.

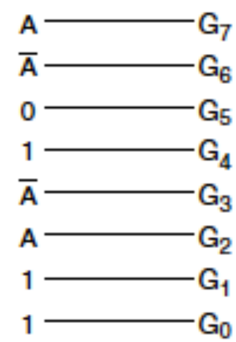
3-24.*

a)



VDD
F7
F6
F5
F4
F3
F2
F1
F0

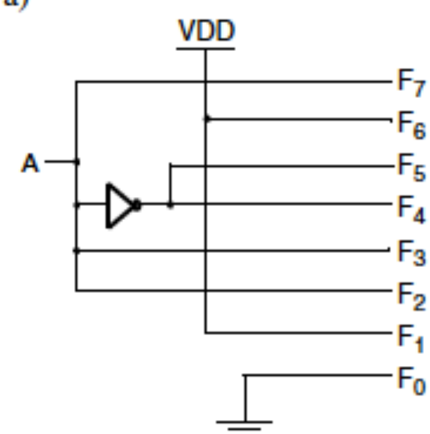
b)



A G7
Ā G6
0 G5
1 G4
Ā G3
A G2
1 G1
1 G0

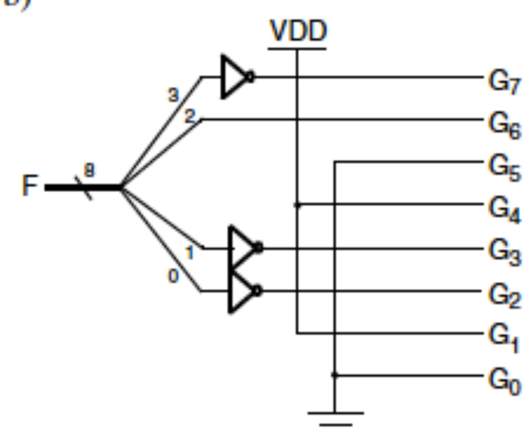
3-25.

a)



VDD
A
F7
F6
F5
F4
F3
F2
F1
F0

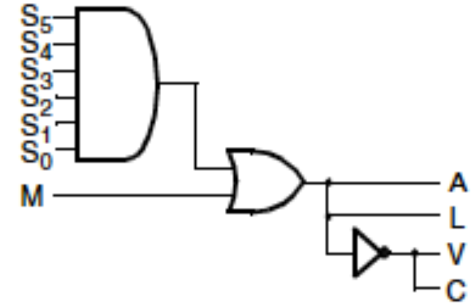
b)



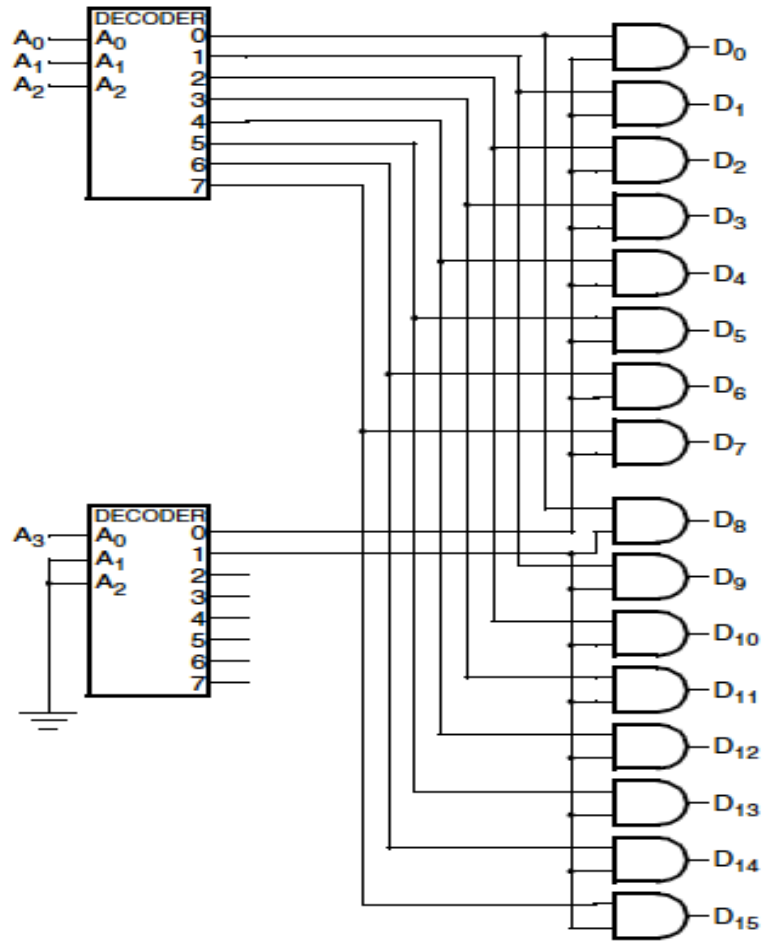
VDD
F
8
3
2
1
0
G7
G6
G5
G4
G3
G2
G1
G0

3-27.

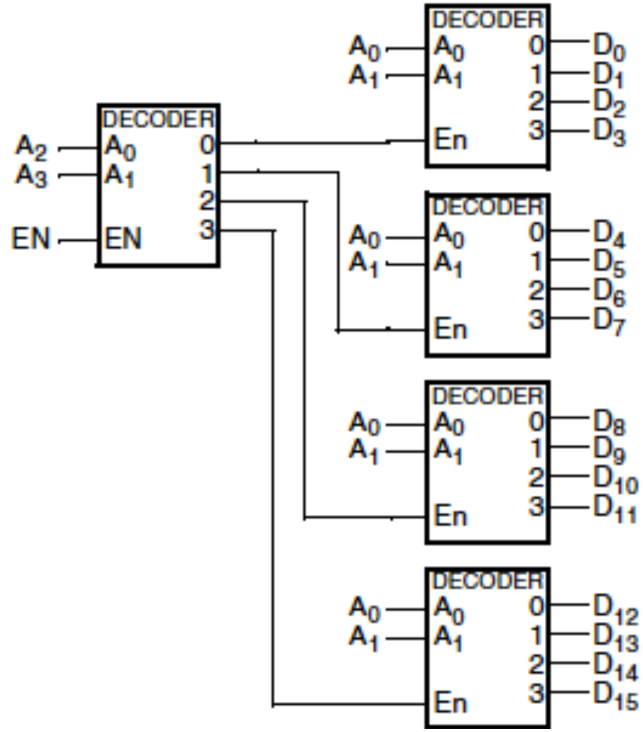
$$A = (S_0 \cdot S_1 \cdot S_2 \cdot S_3 \cdot S_4 \cdot S_5) + M$$
$$L = A$$
$$V = \bar{A} = \overline{(S_0 \cdot S_1 \cdot S_2 \cdot S_3 \cdot S_4 \cdot S_5) + M}$$
$$C = V$$



3-28.

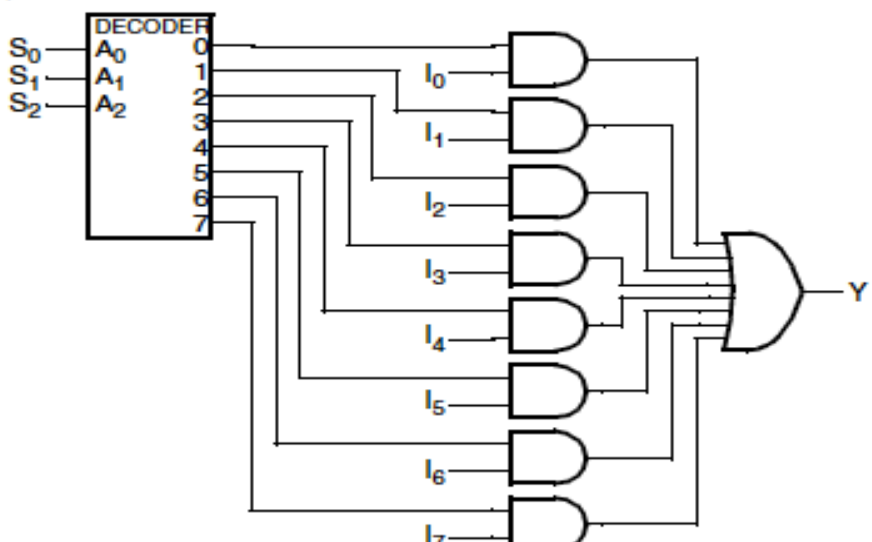


3-29.

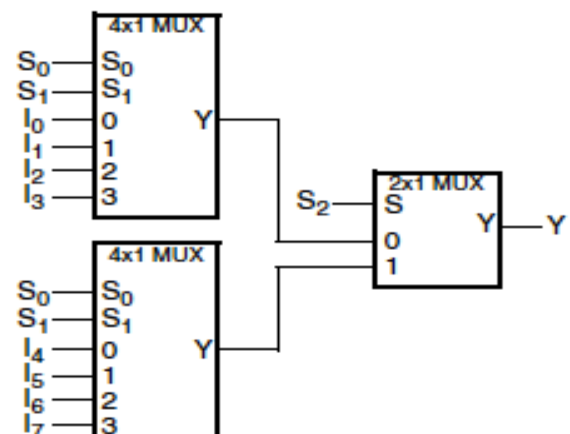

DECODER
A2
A3
EN
A0
A1
EN
0
1
2
3
A0
A1
En
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

3-37.

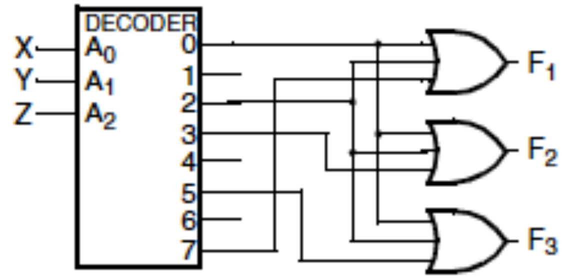
a)


DECODER
S0
S1
S2
A0
A1
A2
0
1
2
3
4
5
6
7
I0
I1
I2
I3
I4
I5
I6
I7
Y

b)


4x1 MUX
S0
S1
I0
I1
I2
I3
I4
I5
I6
I7
0
1
2
3
Y
2x1 MUX
S2
S
Y

3-44.



3-47.*

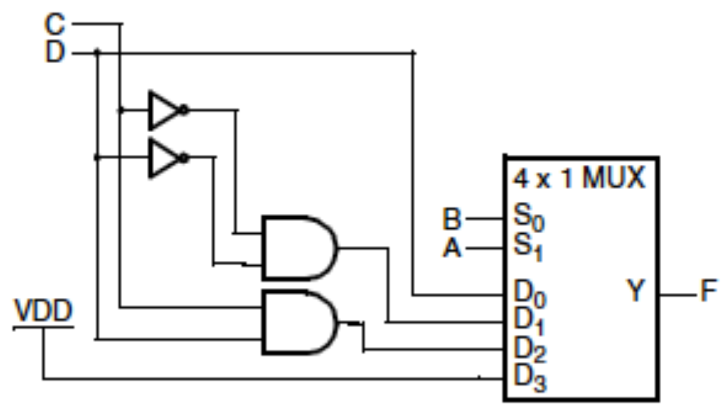
A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$F=D$

$F=\overline{C}\,\overline{D}$

$F=C\,D$

$F=1$



4-2； 4-3； 4-4； 4-14

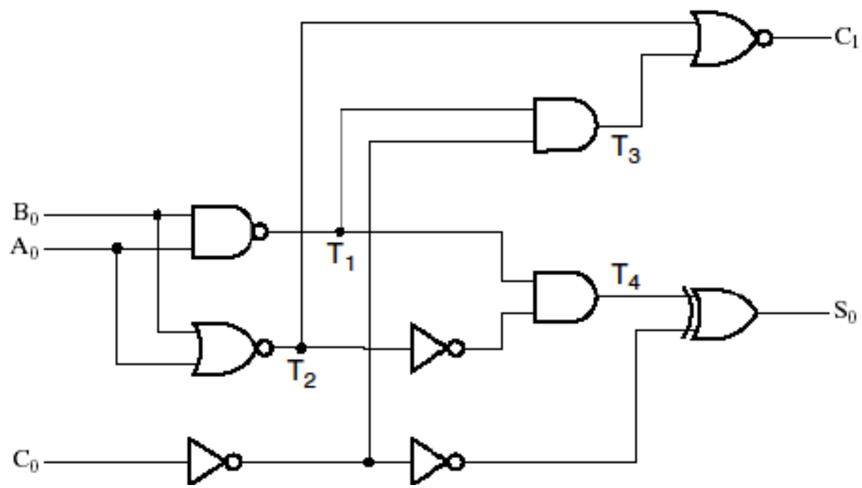
4-2.*

$$C_1 = \overline{T_3 + T_2} = \overline{T_1\bar{C}_0 + T_2} = \overline{\overline{A_0B_0}\,\bar{C}_0 + \overline{A_0 + B_0}} = \overline{(\bar{A}_0 + \bar{B}_0)\bar{C}_0 + \bar{A}_0\bar{B}_0} = (A_0B_0 + C_0)(A_0 + B_0)$$

$$C_1 = A_0B_0 + A_0C_0 + B_0C_0$$

$$S_0 = C_0 \oplus T_4 = C_0 \oplus T_1\bar{T}_2 = C_0 \oplus \overline{A_0B_0}(A_0 + B_0) = C_0 \oplus (\bar{A}_0 + \bar{B}_0)(A_0 + B_0) = C_0 \oplus A_0\bar{B}_0 + \bar{A}_0B_0$$

$$S_0 = A_0 \oplus B_0 \oplus C_0$$



4-3.*(5-3)

Unsigned	1001 1100	1001 1101	1010 1000	0000 0000	1000 0000
1's Complement	0110 0011	0110 0010	0101 0111	1111 1111	0111 1111
2's Complement	0110 0100	0110 0011	0101 1000	0000 0000	1000 0000

4-4.(5-4)

a) $$\begin{array}{r} 11010 \\ +\ \underline{01111} \\ 01001 \end{array}$$

b) $$\begin{array}{r} 11110 \\ +\ \underline{10010} \\ 10000 \end{array}$$

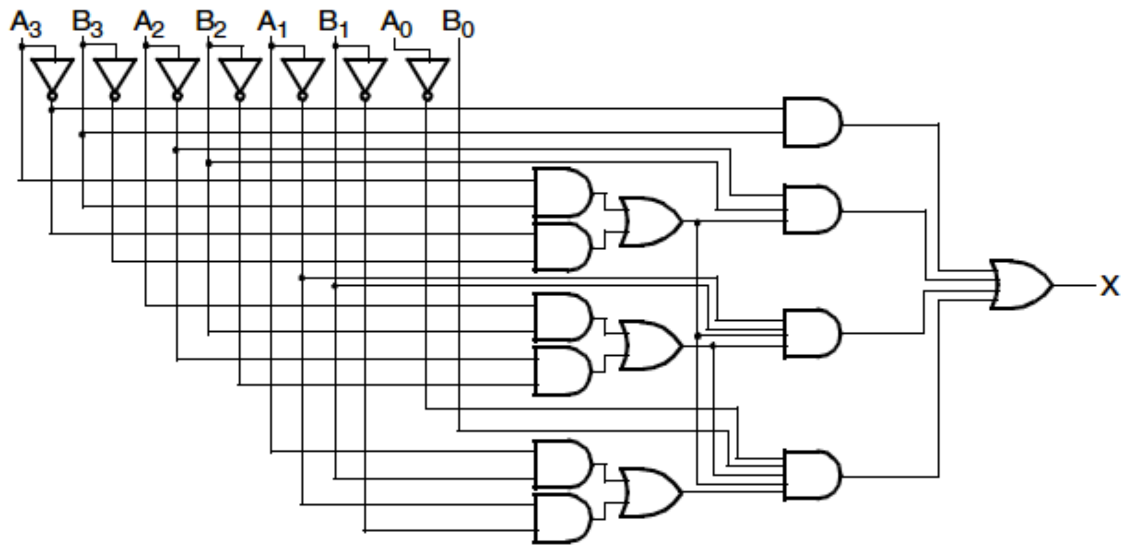
c) $$\begin{array}{r} 1111110 \\ +\ \underline{0000010} \\ 0000000 \end{array}$$

d) $$\begin{array}{r} 101001 \\ +\ \underline{111011} \\ 100100 \end{array}$$

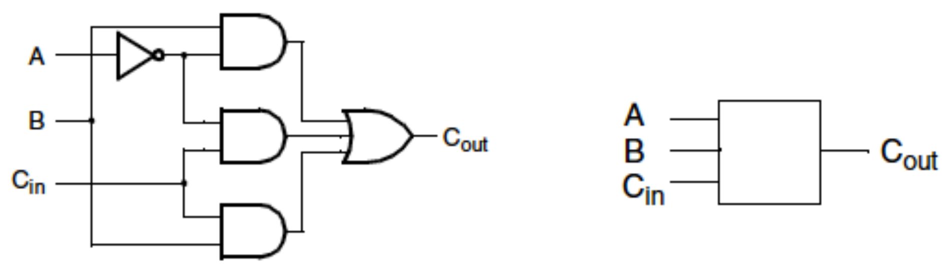
4-11.

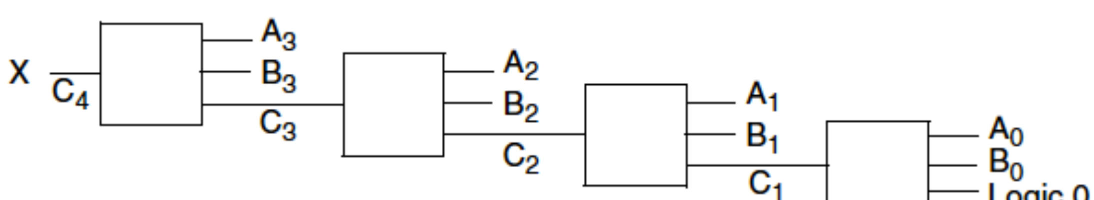
Proceeding from MSB to LSB: $A < B$ if $A_i < B_i(\bar{A}_i B_i = 1)$ and for all j > i, $A_j = B_j(A_j B_j + \bar{A}_j \bar{B}_j = 1)$
Based on the above,

$$X = \bar{A}_3 B_3 + (A_3 B_3 + \bar{A}_3 \bar{B}_3)\bar{A}_2 B_2 + (A_3 B_3 + \bar{A}_3 \bar{B}_3)(A_2 B_2 + \bar{A}_2 \bar{B}_2)\bar{A}_1 B_1$$
$$+ (A_3 B_3 + \bar{A}_3 \bar{B}_3)(A_2 B_2 + \bar{A}_2 \bar{B}_2)(A_1 B_1 + \bar{A}_1 \bar{B}_1)\bar{A}_0 B_0$$



4-12.+





4-14.+

This problem requires two decisions: Is A > B? Is A = B? Two "carry" lines are required to build an iterative circuit, G_i and E_i. These carries are assumed to pass through the circuit from right to left with $G_0 = 0$ and $E_0 = 1$. Each cell has inputs A_i, B_i, G_i, and E_i and outputs G_{i+1} and E_{i+1}. Using K-maps, cell equations are:

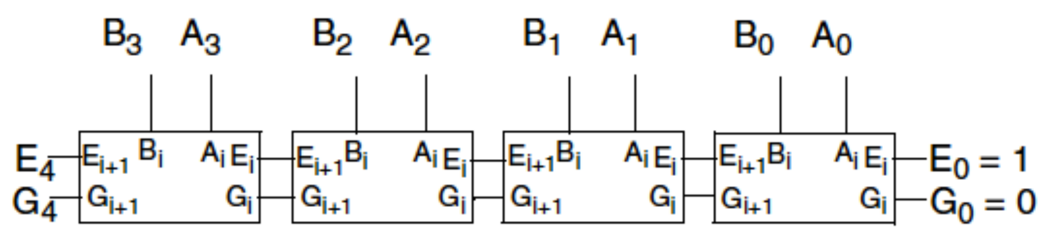
$$E_{i+1} = \overline{A}_i\overline{B}_i\, E_i + A_iB_i\, E_i$$

$$G_{i+1} = A_i\overline{B}_i\, E_i + (A_i + \overline{B}_i)\, E_i$$

Using multilevel circuit techniques, the cost can be reduced by sharing terms:

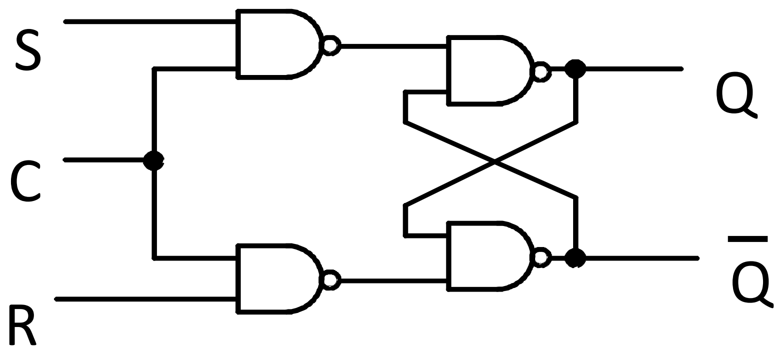
$$E_{i+1} = \overline{(A_i\overline{B}_i + \overline{A}_iB_i)}\, E_i$$

$$G_{i+1} = (A_i\overline{B}_i + \overline{(\overline{A}_iB_i)})\, G_i$$



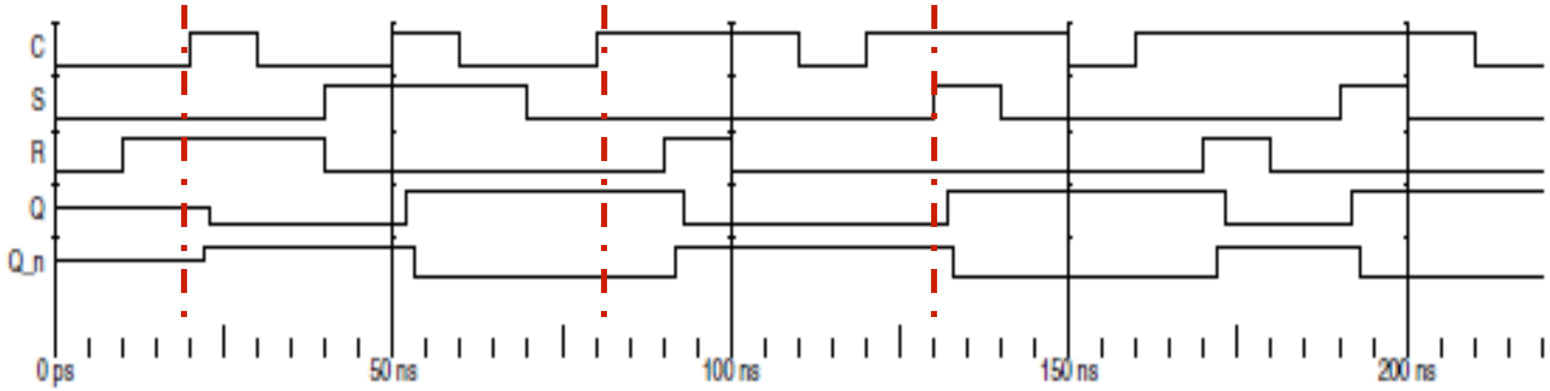
Problems of Chapter 5

5-2 Behavior Stimulation



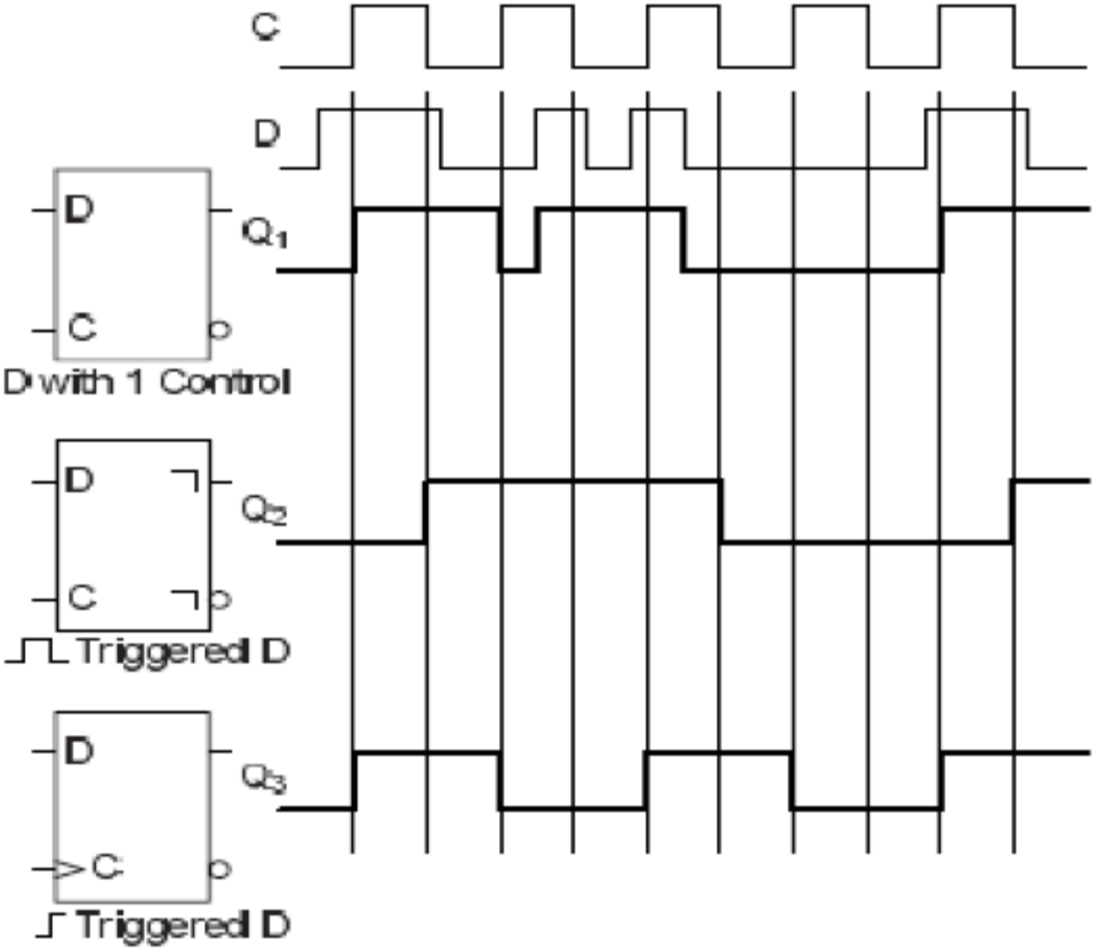
C	S	R	Q(t+1)	Comment
0	x	x	No change	No change
1	0	0	No change	No change
1	0	1	0	Clear Q
1	1	0	1	Set Q
1	1	1	???	Indeterminate

Answer:



5-4 Draw Output Waveforms

Answer:

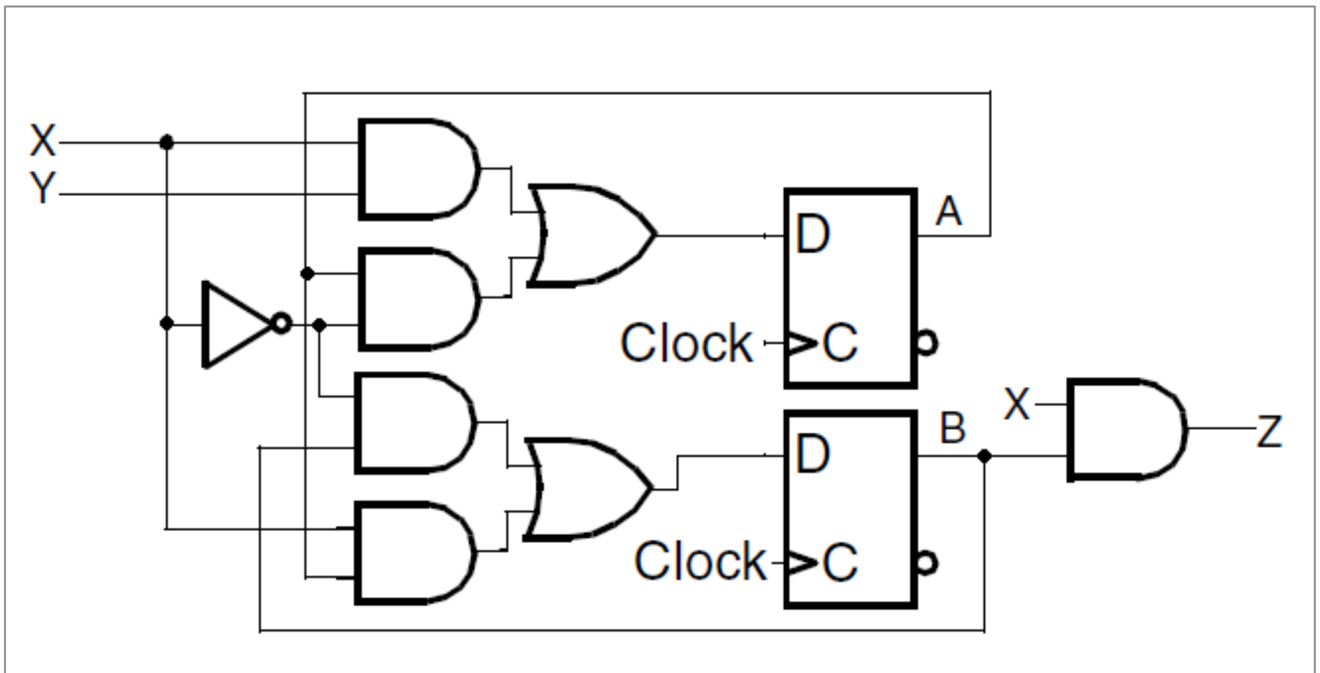


5-6 Circuit Analysis

$$D_A = \bar{X}A + XY$$
$$D_B = \bar{X}B + XA$$
$$Z = XB$$

- a) Draw the logic diagram of the circuit.

Answer:



5-6 Circuit Analysis

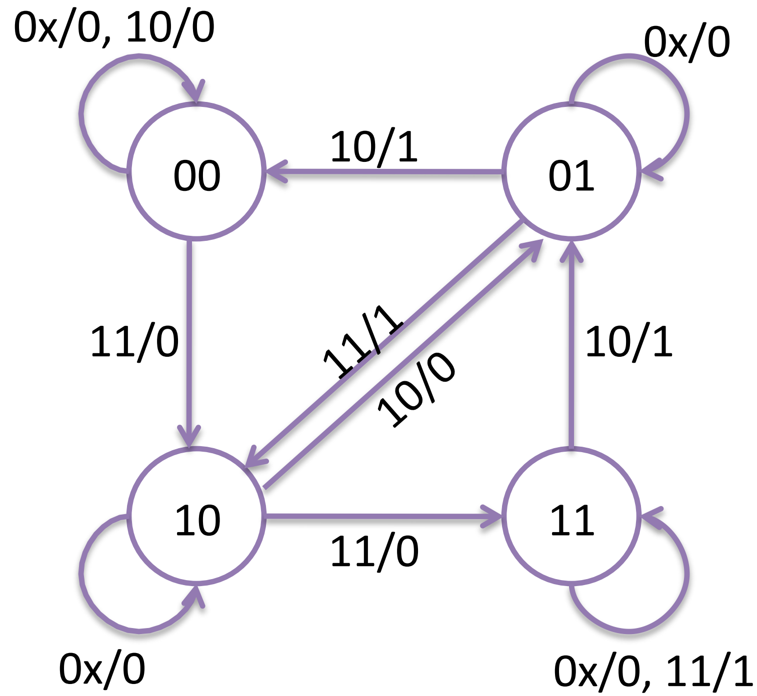
$$D_A = \bar{X}A + XY$$
$$D_B = \bar{X}B + XA$$
$$Z = XB$$

- b) Derive the state table. c) Derive the state diagram

Answer:

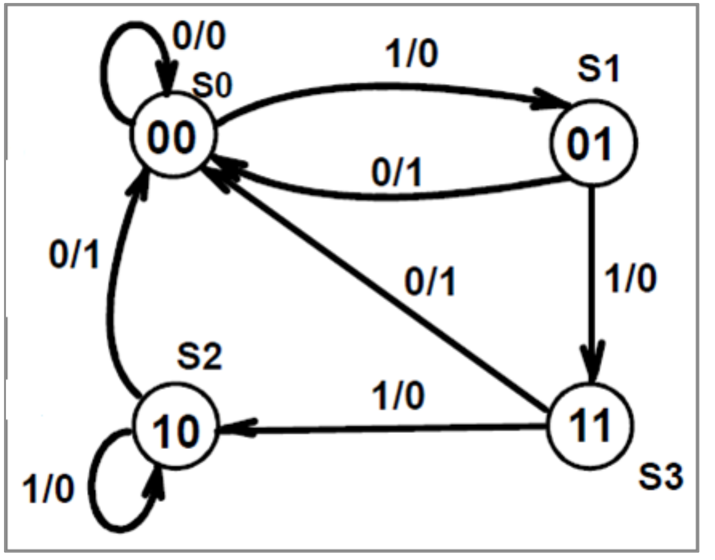
Present state		Inputs		Next state		Output
A	*B*	*X*	*Y*	*A*	*B*	*Z*
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	1	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	1	0
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	0	1	1
1	1	1	1	1	1	1

Answer:



5-9 State Transition

- Start from state 00.
- Apply 10011011110.



Answer:

Present State	00	01	00	00	01	11	00	01	11	10	10
Input	1	0	0	1	1	0	1	1	1	1	0
Output	0	1	0	0	0	1	0	0	0	0	1
Next State	01	00	00	01	11	00	01	11	10	10	00

5-11 State Table & State Diagram

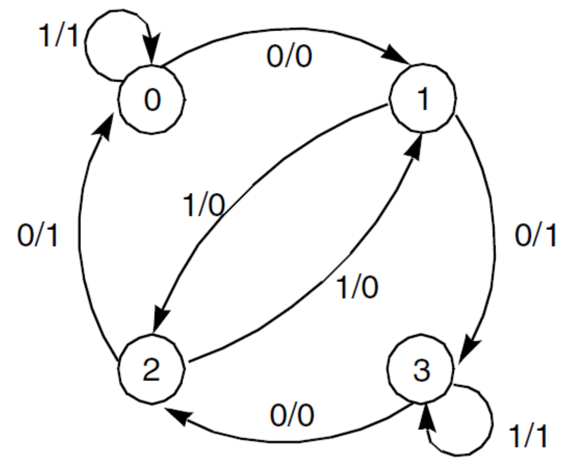
- Derive the function of the circuit as follows:

$$S_A = B \qquad S_B = \overline{X \oplus A}$$

$$R_A = \overline{B} \qquad R_B = X \oplus A$$

Answer:

Present state		Input	Next state		Output
A	*B*	*X*	*A*	*B*	*Y*
0	0	0	0	1	0
0	0	1	0	0	1
0	1	0	1	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	1	0	0
1	1	1	1	1	1

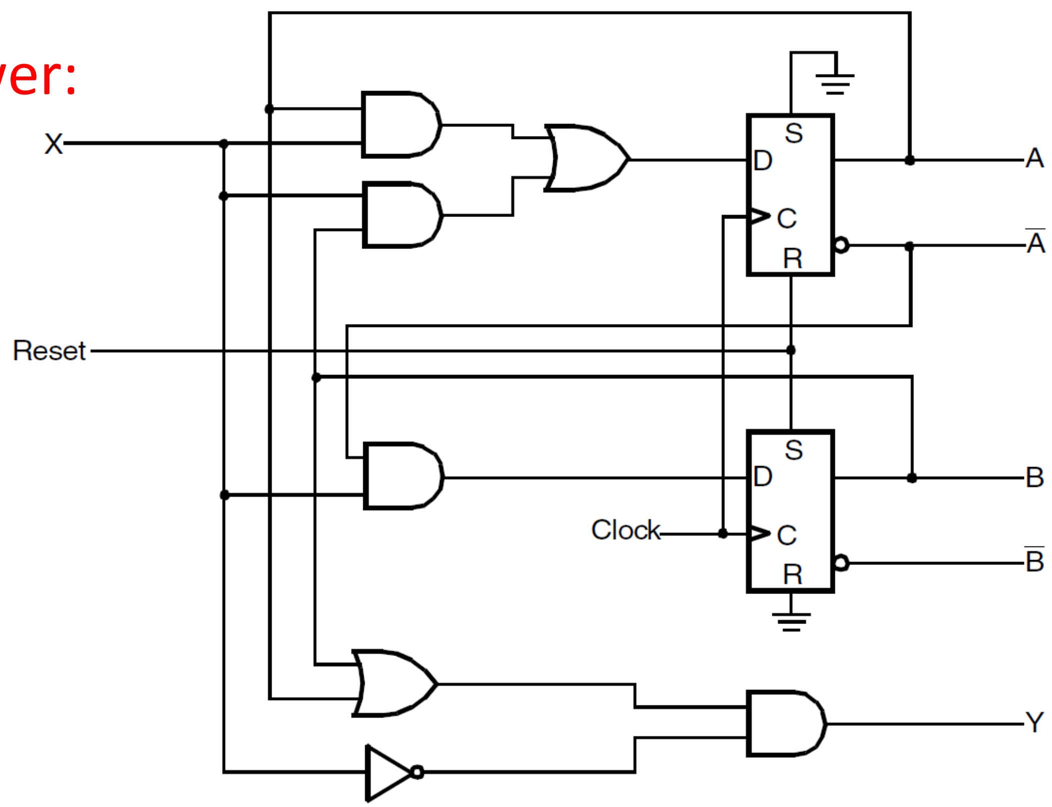


Format: X/Y

5-12 Circuit Modification

- a) When Reset=1, asynchronously reset state A=0,B=1.

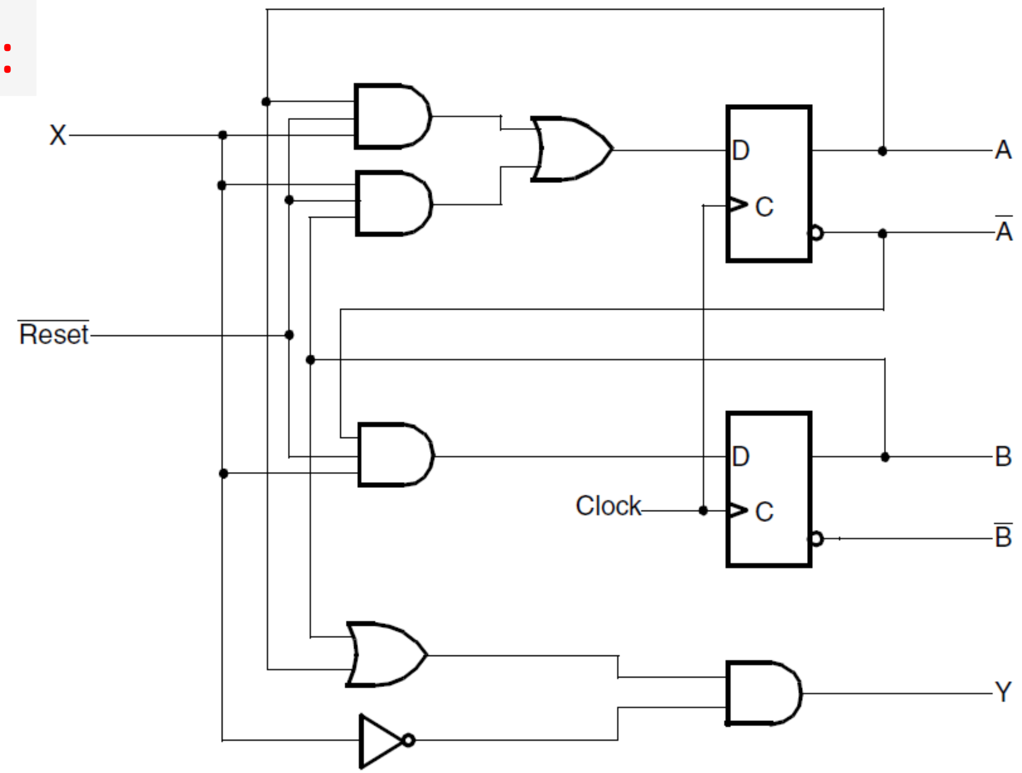
Answer:



5-12 Circuit Modification

- b) When Reset=0, synchronously reset state A=0,B=0.

Answer:



5-20 Flag Circuit Design

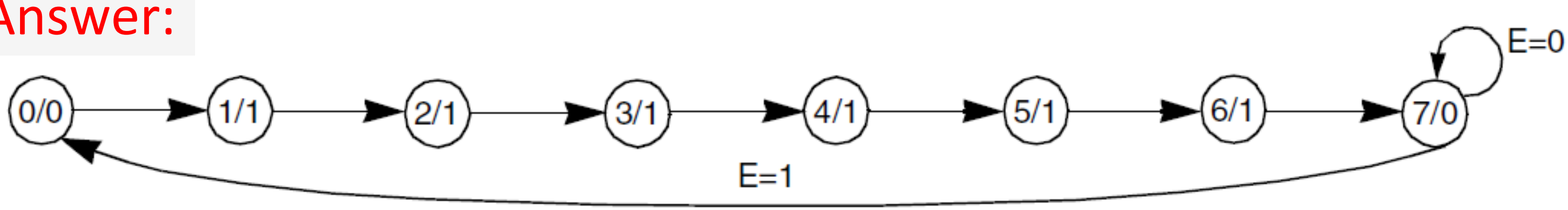
The Flag

- E=1 produces $\boxed{01111110}$

  Assumes for E=0, output remains at 0

a) Draw the Moore state diagram.

Answer:



5-20 Flag Circuit Design

b) State table and state assignments.

Answer:

Present state	Next State For Input		Output
$D_2D_1D_0$	*E=0*	*E=1*	*Z*
000	001	001	0
001	010	010	1
010	011	011	1
011	100	100	1
100	101	101	1
101	110	110	1
110	111	111	1
111	111	000	0

$$D_2(t+1) = D_2\overline{D_1} + D_2\overline{D_0} + \overline{D_2}D_1D_0 + D_2\overline{E} \quad (D_2D_1D_0\overline{E})$$

$$D_1(t+1) = D_1\overline{D_0} + \overline{D_1}D_0 + D_2D_0\overline{E} \quad (D_2D_1\overline{E}, \quad D_2D_1D_0\overline{E})$$

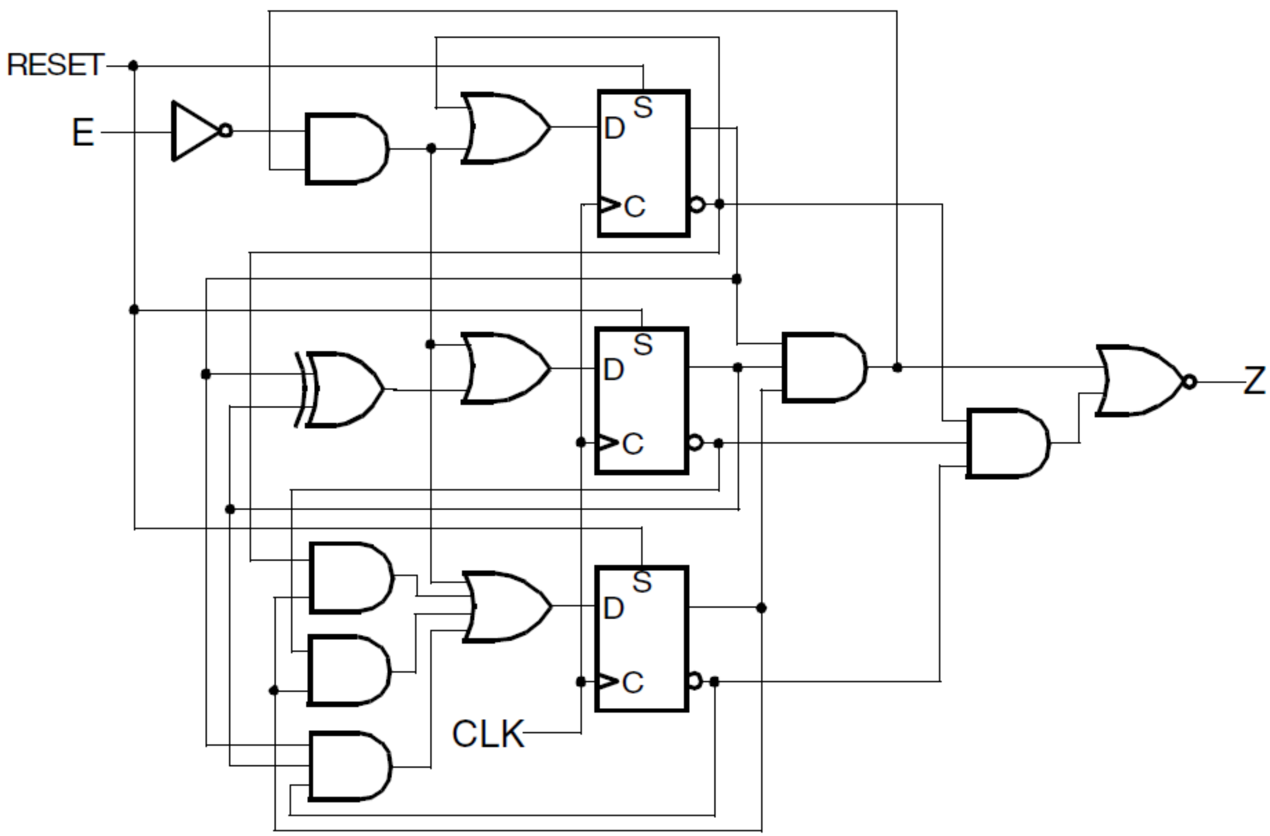
$$D_0(t+1) = \overline{D_0} + D_2D_1\overline{E} \quad (D_2D_1D_0\overline{E})$$

$$Z = \overline{D_2D_1D_0 + \overline{D_2}\,\overline{D_1}\,\overline{D_0}} = D_1\overline{D_0} + D_2\overline{D_1} + \overline{D_2}D_0 = \overline{D_1}D_0 + \overline{D_2}D_1 + D_2\overline{D_0}$$

5-20 Flag Circuit Design

c) Circuit design with D flip-flops and logic

Answer: es.



5-21 Zero Insertion Circuit

- Description:
  - Since we use *flag 01111110* as the beginning of a message, at most 5 1's in sequence may appear anywhere else.
  - So we insert 0 after the 5th 1.
- Example:

Input X : 01111110011111111000001011110101

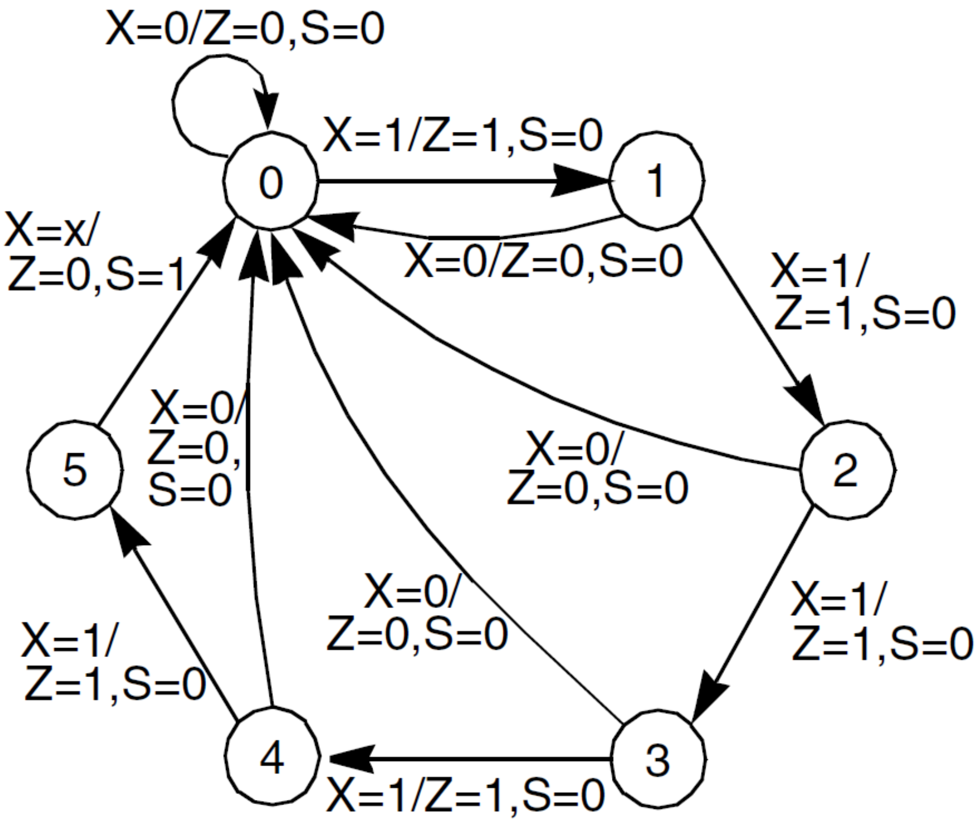
Output Z: 01111100011111011000001011110101

Output S: 00000010000000100000000000000000

5-21 Zero Insertion Circuit

a) State diagram.

Answer:



5-21 Zero Insertion Circuit

b) State table and state assignments.

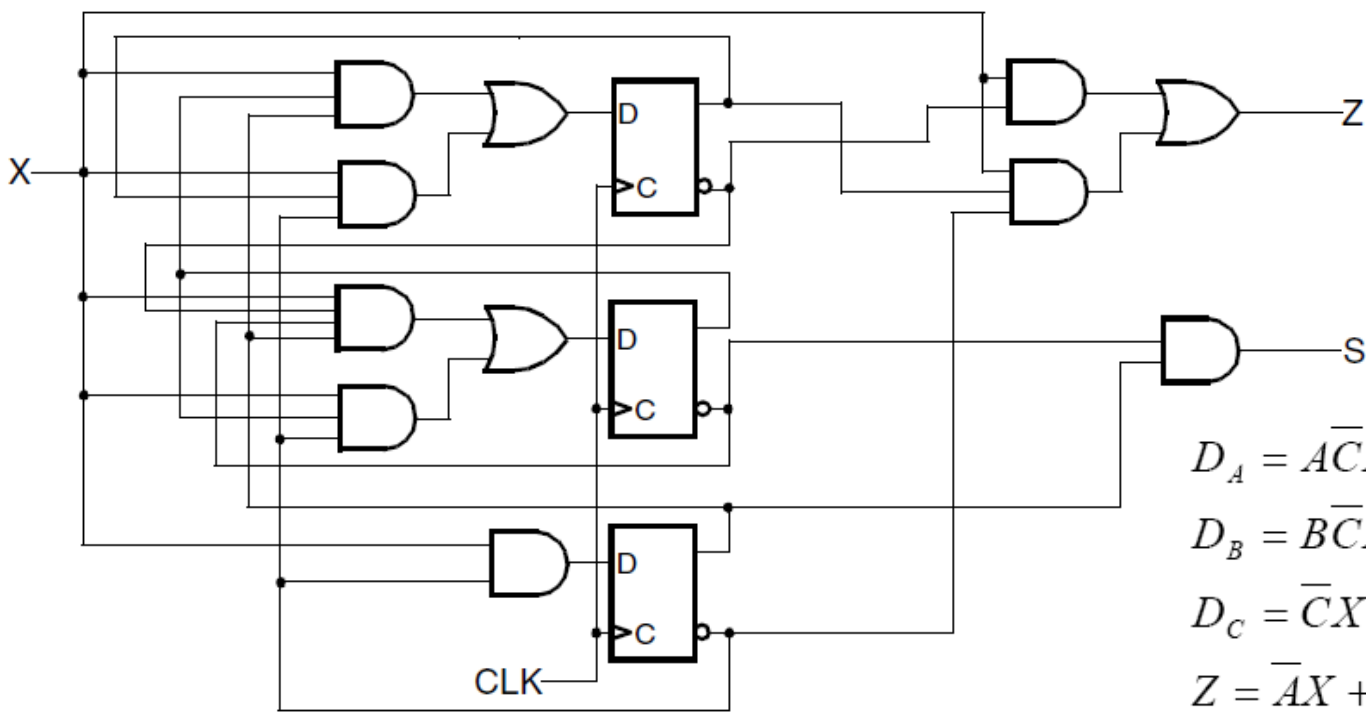
Answer:

Present state			Input	Next state			Output	
A	*B*	*C*	*X*	*A*	*B*	*C*	*Z*	*S*
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	1	1	1	0
0	1	1	0	0	0	0	0	0
0	1	1	1	1	0	0	1	0
1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	1	0
1	0	1	0	0	0	0	0	1
1	0	1	1	0	0	0	0	1

5-21 Zero Insertion Circuit

c) Circuit design with D flip-flops and logic

Answer:



$$D_A = A\overline{C}X + BCX$$

$$D_B = B\overline{C}X + \overline{A}\,\overline{B}CX$$

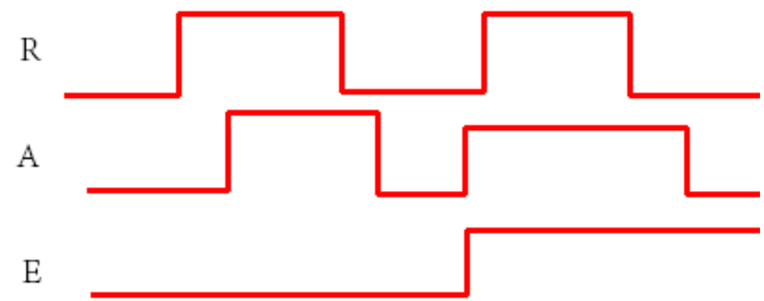
$$D_C = \overline{C}X$$

$$Z = \overline{A}X + \overline{C}X = (\overline{A} + \overline{C})X$$

$$S = AC$$

5-24 Handshake Checker

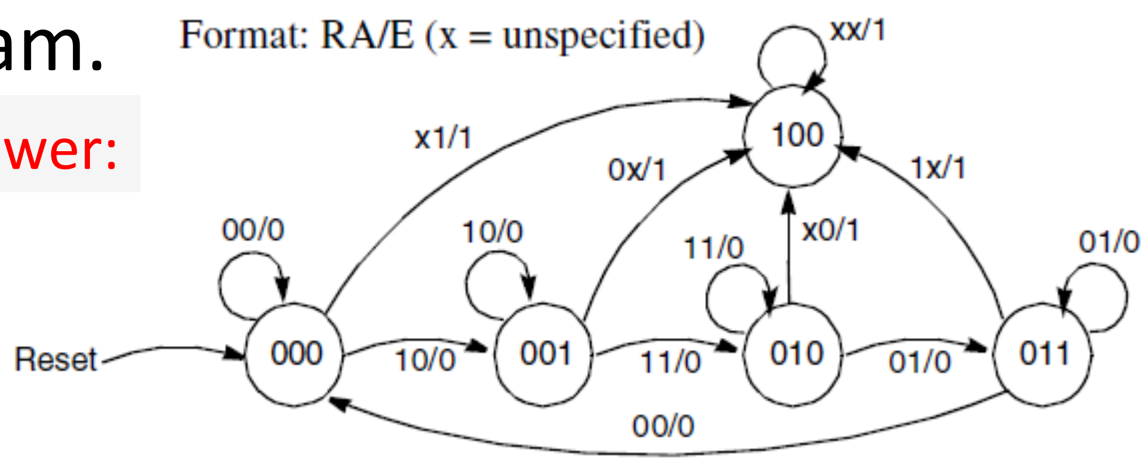
A *handshake* is a pair of signals Request(R) and Acknowledge(A).



A *handshake checker* is to verify the transaction order. *RA: 00->10->11->01*

a) State diagram.

Answer:



5-24 Handshake Checker

b) State table.

Answer:

Present state			Inputs		Next state			Output
B	*C*	*D*	*R*	*A*	*B*	*C*	*D*	*E*
0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	1
0	0	0	1	0	0	0	1	0
0	0	0	1	1	1	0	0	1
0	0	1	0	0	1	0	0	1
0	0	1	0	1	1	0	0	1
0	0	1	1	0	0	0	1	0
0	0	1	1	1	0	1	0	0
0	1	0	0	0	1	0	0	1
0	1	0	0	1	0	1	1	0
0	1	0	1	0	1	0	0	1
0	1	0	1	1	0	1	0	0

Present state			Inputs		Next state			Output
B	*C*	*D*	*R*	*A*	*B*	*C*	*D*	*E*
0	1	1	0	0	0	0	0	0
0	1	1	0	1	0	1	1	0
0	1	1	1	0	1	0	0	1
0	1	1	1	1	1	0	0	1
1	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	1
1	0	0	1	0	1	0	0	1
1	0	0	1	1	1	0	0	1

5-28 Counter Design

Design a 3-bit twisted ring counter with no inputs according to the state table.

a) Circuit design with D flip-flops.

Present State	Next State
ABC	ABC
000	100
100	110
110	111
111	011
011	001
001	000
010	XXX
101	XXX

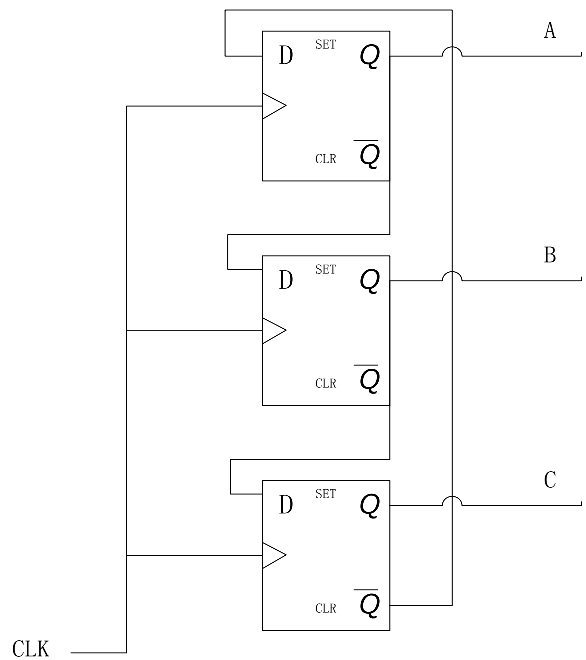
Unused states

Answer:

$D_A = \overline{C}$

$D_B = A$

$D_C = B$



5-28 Counter Design

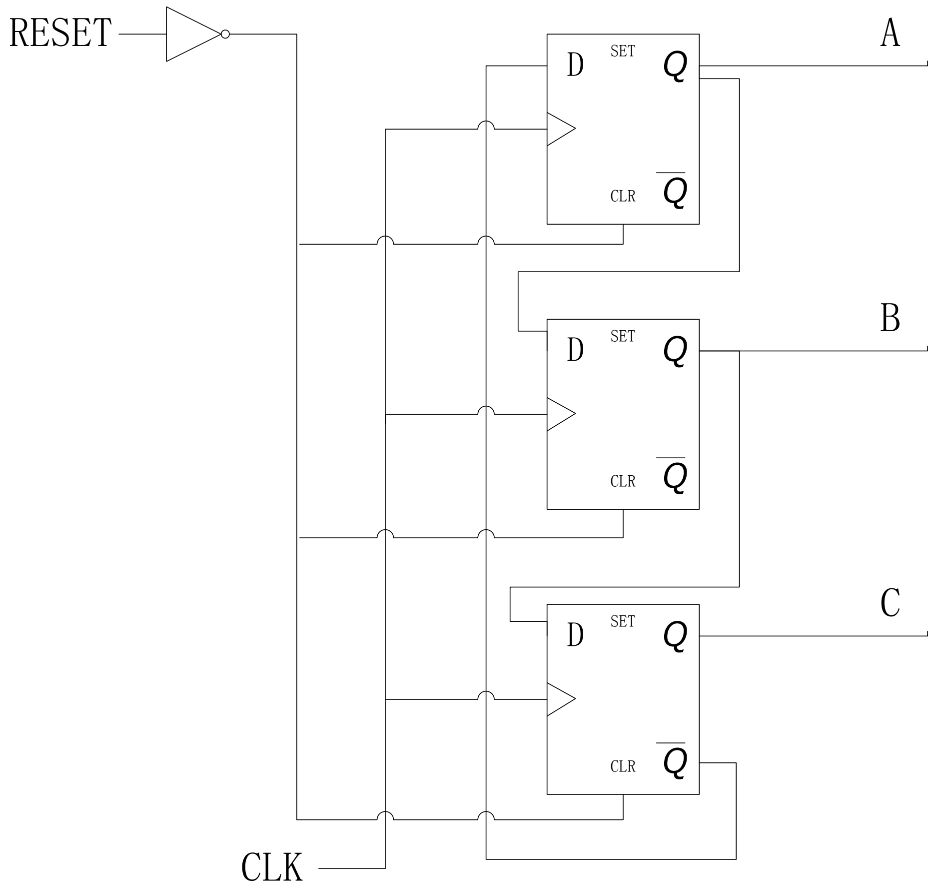
b) Add reset function to the circuit.

Answer:

Clear A = $\overline{\text{Reset}}$

Clear B = $\overline{\text{Reset}}$

Clear C = $\overline{\text{Reset}}$



5-28 Counter Design

c, d, e, f) Deal with the unused states

Answer:

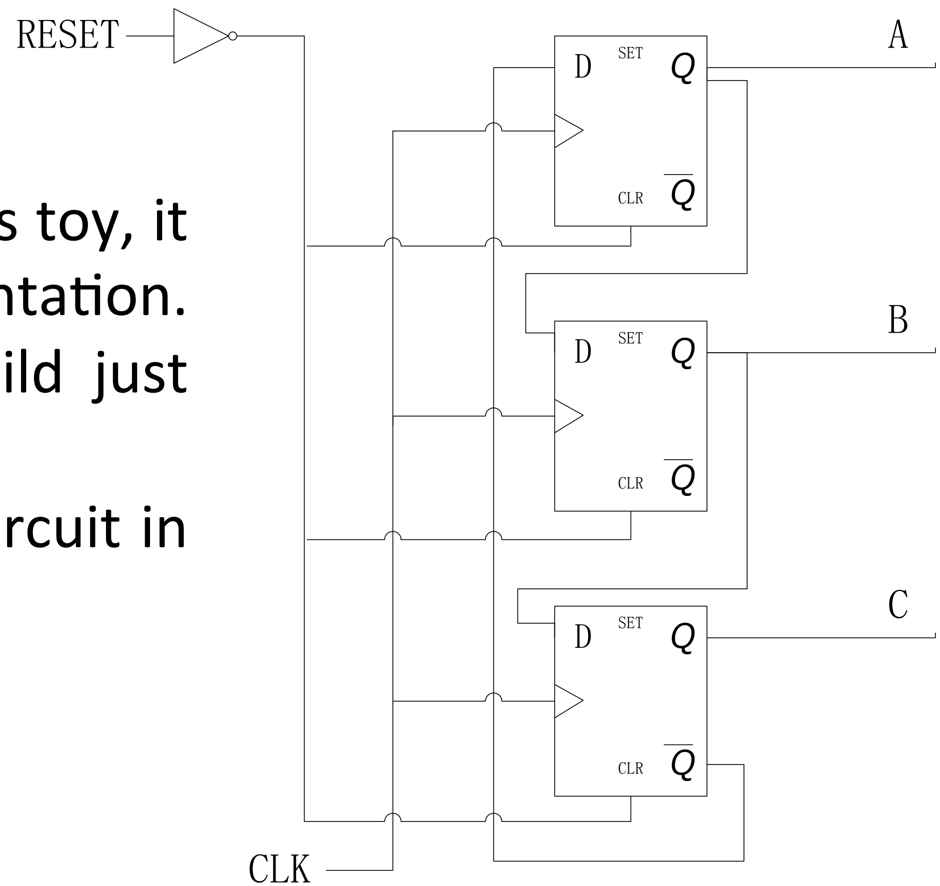
The circuit is suitable for child's toy, but not for life critical applications. In the case of the child's toy, it is the cheapest implementation. If an error occurs the child just needs to reset it. In life critical applications, the immediate detection of errors is critical. The circuit above enters invalid states for some errors. For a life critical application, additional circuitry is needed for immediate detection of the error (Error = $\overline{A}B\overline{C} + A\overline{B}C$). This circuit using the design in a), does return from the invalid states to a valid state automatically after one or two clock periods.

5-28 Counter Design

c,d) In case of child's toy.

Answer:

- In the case of the child's toy, it is the cheapest implementation. If an error occurs the child just needs to reset it.
- The circuit is just like circuit in part (b).



5-28 Counter Design

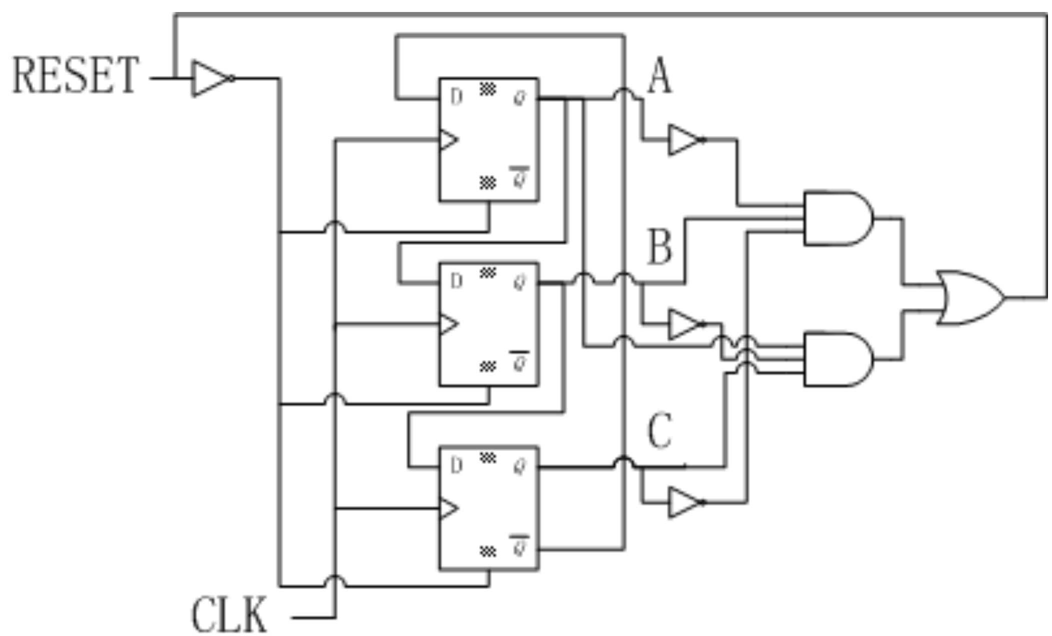
e,f) In case of engine control.

Answer:

- In life critical applications, the immediate detection of errors is critical. The circuit above enters invalid states for some errors.

- Example solution:

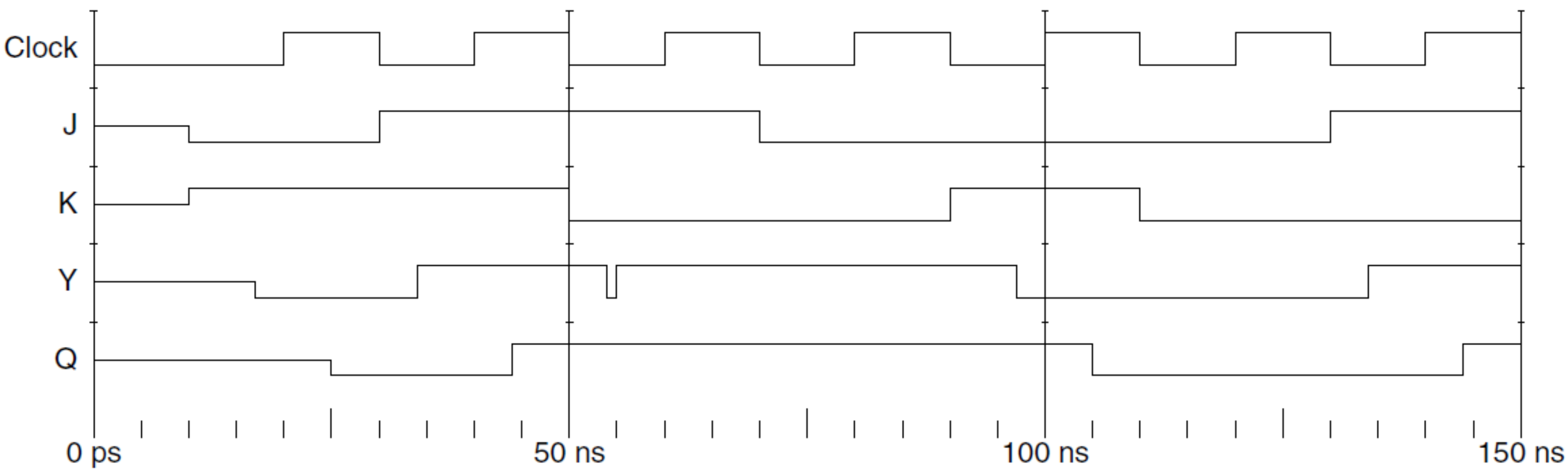
$$\boxed{RESET = \overline{A}B\overline{C} + A\overline{B}C}$$



5-33 J-K Flip-flop

- Draw timing diagram of a positive-edge-triggered JK flip-flop.

Answer:



6-9, 6-10, 6-12, 6-20

6-9.

a) There is a setup time violation at 28 ns. There is an input combination violation around 24 ns.

b) There is a setup time violation just before 24 ns, There is an input combination violation around 24 ns.

c) There is a setup time violation at 28ns.

d) There is a hold time violation at 16ns and a setup time violation at 24ns.

6-10.*

a) The longest direct path delay is from input X through the two XOR gates to the output Y.

$$t_{delay} = t_{pdXOR} + t_{pdXOR} = 0.20 + 0.20 = 0.40 \text{ ns}$$

b) The longest path from an external input to a positive clock edge is from input X through the XOR gate and the inverter to the B Flip-flop.

$$t_{delay} = t_{pdXOR} + t_{pd\ INV} + t_{sFF} = 0.20 + 0.05 + 0.1 = 0.35 \text{ ns}$$

c) The longest path delay from the positive clock edge is from Flip-flop A through the two XOR gates to the output Y.

$$t_{delay} = t_{pdFF} + 2\ t_{pdXOR} = 0.40 + 2(0.20) = 0.80 \text{ ns}$$

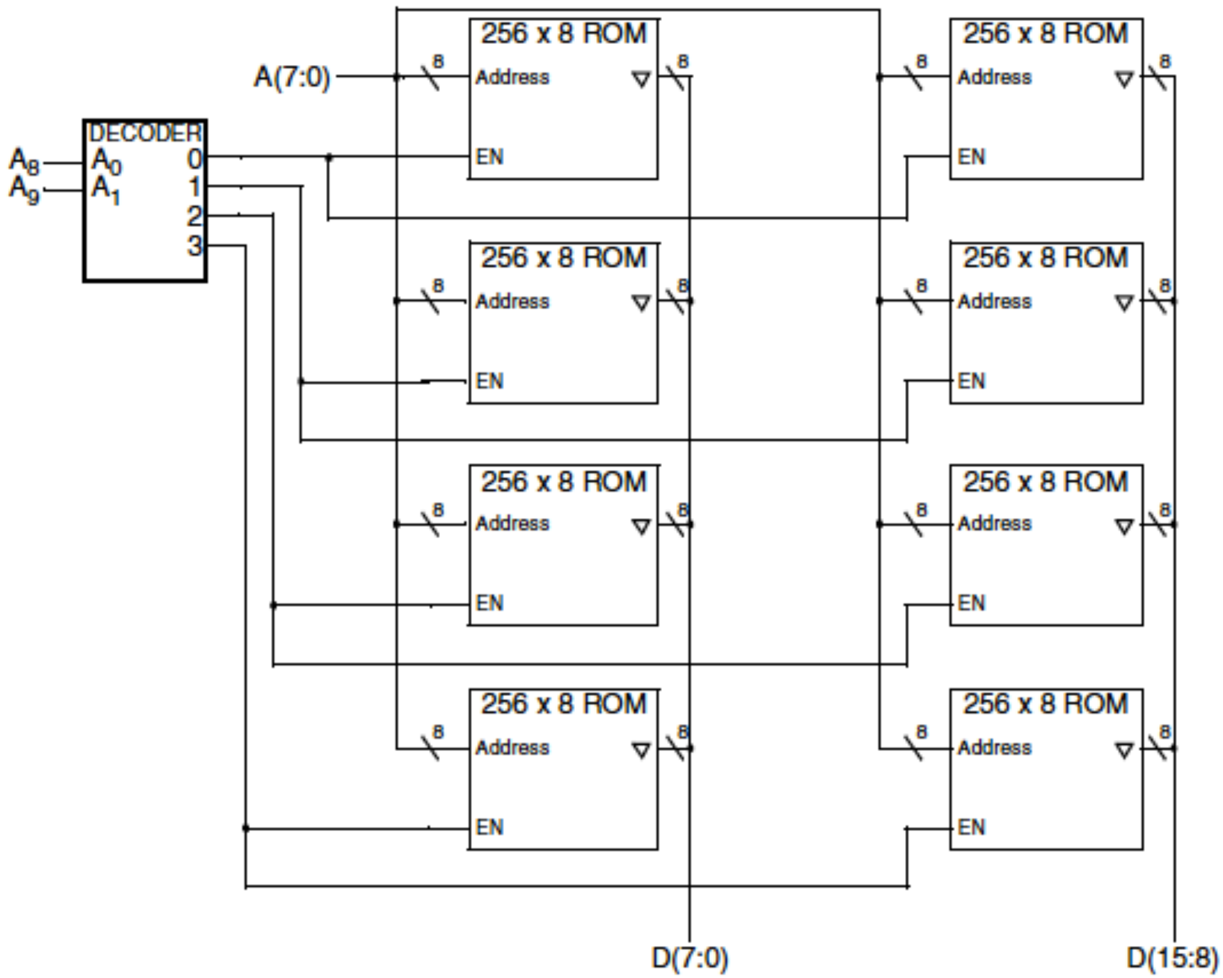
d) The longest path delay from positive clock edge to positive clock edge is from clock on Flip-flop A through the XOR gate and inverter to clock on Flip-flop B.

$$t_{delay\text{-}clock\ edge\ to\ clock\ edge} = t_{pdFF} + t_{pdXOR} + t_{pdINV} + t_{sFF} = 0.40 + 0.20 + 0.05 + 0.10 = 0.75 \text{ ns}$$

e) The maximum frequency is $1/t_{delay\text{-}\ clock\ edge\ to\ clock\ edge}$. For this circuit, $t_{delay\text{-}clock\ edge\ to\ clock\ edge}$ is 0.75 ns, so the maximum frequency is 1/0.75 ns = 1.33 GHz.

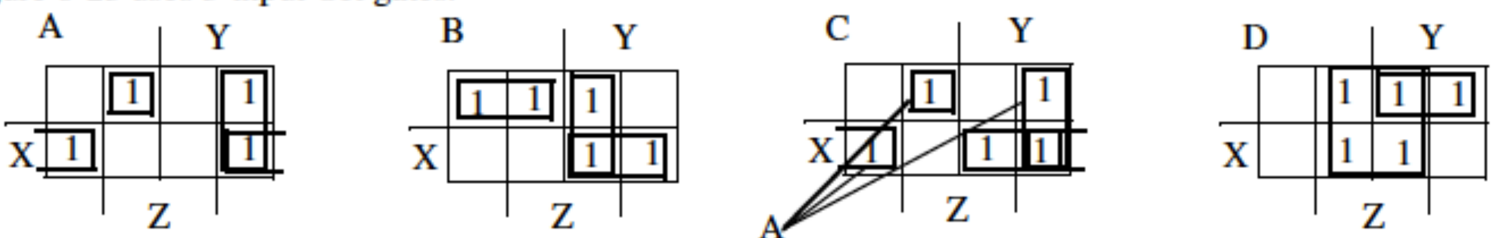
Comment: The clock frequency may need to be lower due to other delay paths that pass outside of the circuit into its environment. Calculation of this frequency cannot be performed in this case since data for paths through the environment is not provided.

6-12.



6-20.

Figure 6-23 uses 3-input OR gates.



$A = X\overline{Z} + Y\overline{Z} + \overline{X}\,\overline{Y}Z$ $B = XY + YZ + \overline{X}\,\overline{Y}$ $C = A + XY$ $D = \overline{X}Y + Z$

A, B, and D each require three or fewer product terms so can be implemented with 3-input OR gates.
C requires four terms so cannot be implemented with a 3-input OR gate. But because the first PAL device output can used as an input to implement other functions it can be assigned to A and A can then be used to implement C using just two inputs of a 3-input OR gate.

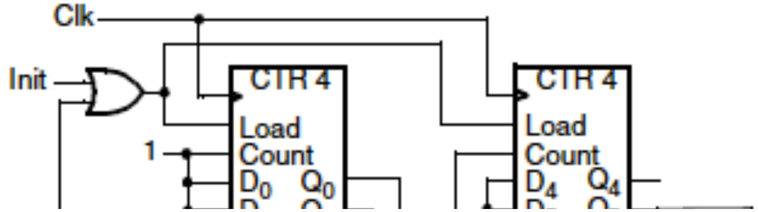
7-6、7-12、7-15、7-16、7-17、7-20、7-24、7-30

7-6.*

a) 1000, 0100, 0010, 0001, 1000. ...

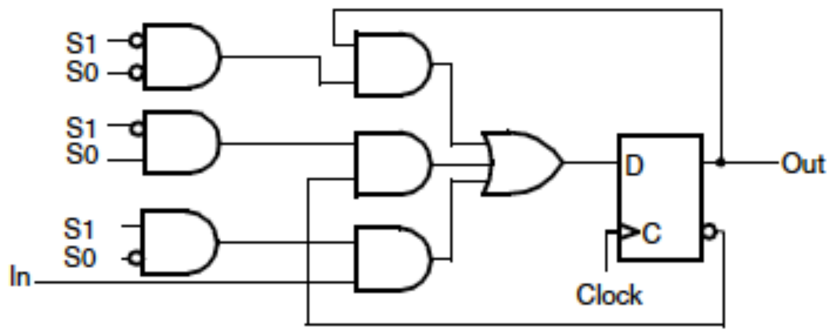
b) # States = n

7-12.



7-16.

The basic cell of the register is as follows:



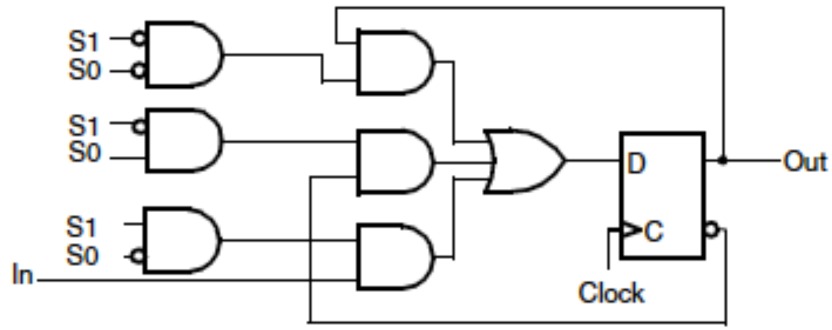
A	*B*	*C*	*A*	*B*	*C*
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	0	0	0

$D_B = B$

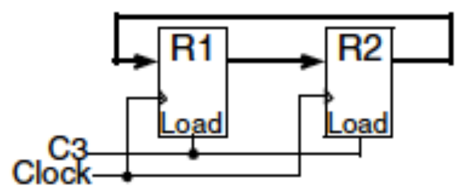
$D_C = \overline{B}C + B\overline{C}$

7-16.

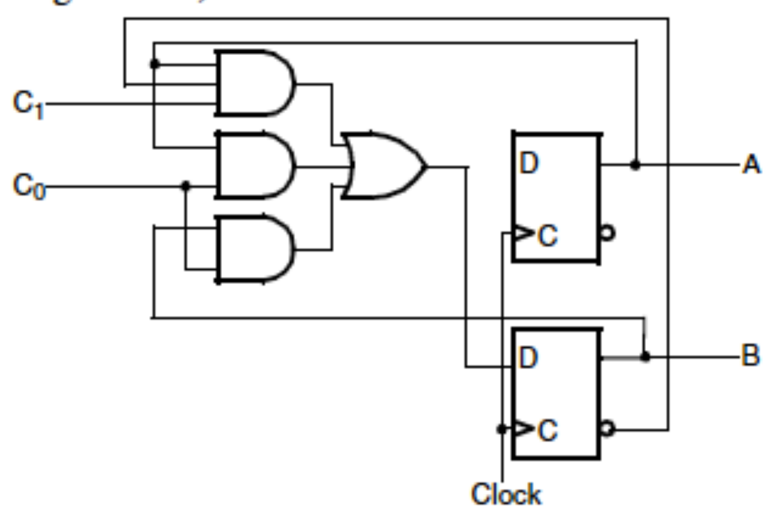
The basic cell of the register is as follows:



7-17.*

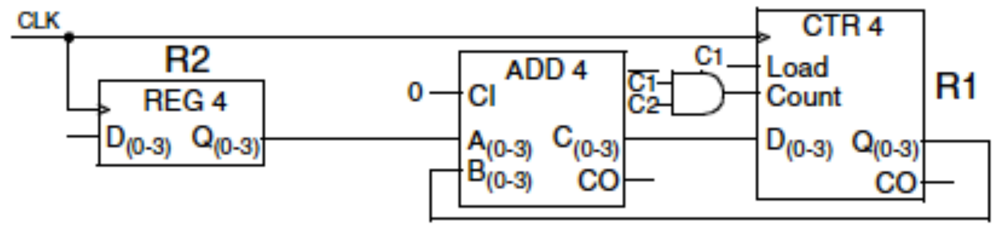


7-20. (Errata: Change "register A" to "register B")

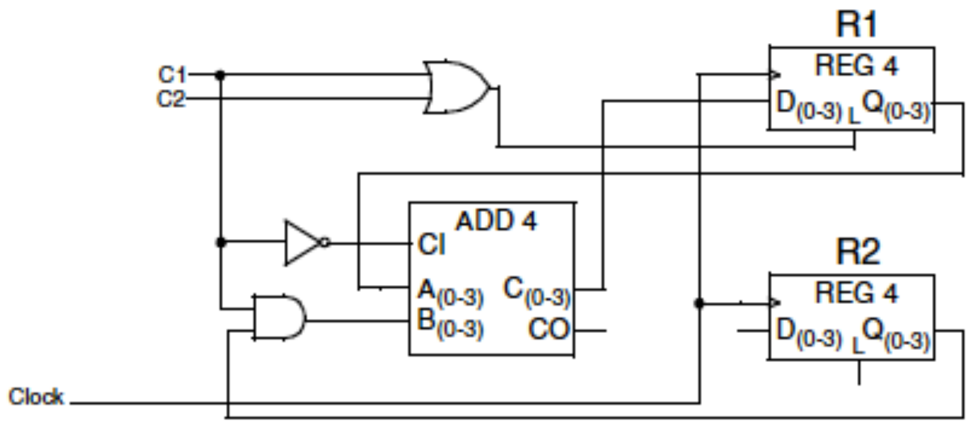


7-24.*

a)



b)



7-30.*

0101, 1010, 0101, 1010, 1101, 0110, 0011, 0001, 1000

8-1, 8-4, 8-5, 8-8

8-1.*

a) A = 16, D = 8 b) A = 19, D = 32 c) A = 26, D = 64 d) A = 31, D = 1

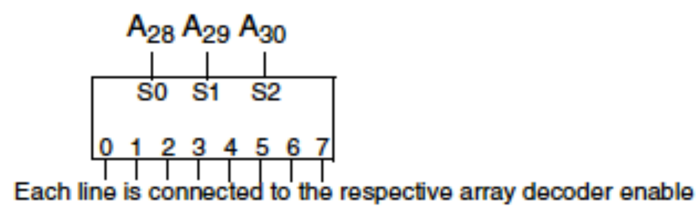
8-1.*

a) A = 16, D = 8 b) A = 19, D = 32 c) A = 26, D = 64 d) A = 31, D = 1

8-4.

a) Number of RAM cell arrays = 8 $(2G = 2^{31})/(2^{14} \times 2^{14} = 2^{28}) = (2^3 = 8)$

b)



8-5.

15 row pins + 14 column pins = 2^{29} = 512M addresses

8-8.*

a) 2 MB/128 K x 16 = 2MB/ 256 KB = 8 b) With 2 byte/word, 2MB/2B = 2^{20}, Add Bits = 20

128K addresses per chip implies 17 address bits. c) 3 address lines to decoder, decoder is 3-to-8-line