《计算机体系结构》课程试卷

考试时间：__*120*_____分钟　开课学院___*计算机*_____任课教师_____

姓名_____ 学号_____班级 _____

一	二	三(1)	三(2)	三(3)	三(4)	Total
22	16	12	15	15	20	100

Answer table for Section One:

1	2	3	4	5	6	7	8	9	10
11	12	13	14	15	16	17	18	19	20
21	22								

一、 There are 22 questions or uncompleted statements in this section. Beneath every subject there are a few phases or statements marked A, B, C and D. Choose the statement which correctly answer the question, or the phrase that best completes the sentence. (22 points) (***Please write your answers in above answer table.***)

1. Amdahl's Law states that the _____ performance improvement to be gained from using some faster mode of execution is limited by the fraction of the time the _____ can be used. Amdahl's Law defines the speedup that can be gained by using a particular feature. The most speedup overall is limited by _____.
   A. overall \ enhanced mode \ 1/(1-F)　　B. enhanced mode \ overall \ 1/(1-F)
   C. faster mode \ overall \ 1/(1-F)　　D. overall \ 1/(1-F) \ enhanced mode

2. Which of the following architecture is used in MIPS?
   A. load-store　　B. register-register　　C. register-memory　　D. memory-memory

3. Which of the following statements about two-level cache is NOT correct?
   A. With two-Level cache, we can decrease miss penalty.
   B. The first-level cache should be large enough to obtain a small miss rate.
   C. The second-level cache generally uses a bigger block size than that of the first-level cache.
   D. The second-level cache should be large enough and use higher association to catch almost all memory accesses in the second level.

4. Which of the following type of data hazards will occur in MIPS 5 stages pipeline? _____.
   A. RAR　　B. WAW　　C. RAW　　D. WAR

5. Which of the following descriptions about "Computer architecture" is NOT true?
   A. Computer architecture should include instruction set design.
   B. Computer architecture only means the implementation of a machine, which has two components: organization and hardware.
   C. Computer architecture design needs to provide support to compilers.
   D. Computer architecture is intended to cover all three aspects of computer design ---- instruction set architecture,

organization and hardware.

6. Labor costs belongs to _____
A. gross margin B. direct cost C. component cost D. average discount

7. According to the structure of recent compilers, global and local optimizations belong to which of the following part?
A. front end per language B. code generator C. global optimizer D. high-level optimization

8. CPU time can be further divided into _____.
A. user CPU time and system CPU time. B. Response time and I/O time
C. Elapsed time wall-clock time D. System CPU time and process switch time

9. Which of the following relationship is always correct?
A. geometric mean $\leqslant$ arithmetic mean $\leqslant$ harmonic mean
B. harmonic mean $\leqslant$ arithmetic mean $\leqslant$ geometric mean
C. harmonic mean $\leqslant$ geometric mean $\leqslant$ arithmetic mean
D. arithmetic mean $\leqslant$ harmonic mean $\leqslant$ geometric mean

10. Compared with the memory-memory architecture, the Register-register architecture has
A. Fixed-length instruction encoding B. Less instructions to complete a function.
C. Higher CPI D. Large variation in instruction size.

11. In the following selections, which is NOT the measurement for reducing the cache miss penalty ?
A. Higher associativity B. Critical word first C. Merging write buffer D. Nonblocking caches

12. Which RAID level is Bit-Interleaved Parity?
A. RAID 1 B. RAID 0 C. RAID3 D. RAID 5

13. To reduce data hazards,.we can use ___ to ____ as forwarding path.
A. MEM/WB.ALUoutput, DM input B. MEM/WB.LMD ,DM input
C. MEM/WB.LMD,ALUinput D. EX/MEM.ALUoutput, DM input

14. We often use a technique named_____ to solve register allocation problem.
A. colored paging B. graph coloring C. colored graph D. page coloring

15. Which is NOT the characteristic of CISC machine?
A. Powerful instruction functions. B. Use a complex instruction set.
C. Complex memory addressing mode D. Use the Load/Store architecture.

16. The extension of MIPS pipeline to handle multi-cycle operation will bring about_____ hazard.
A. WAW B. WAR C. RAW D. RAR

17. We often use _____ to allocate statically declared objects.
A. register B. stack C. heap D. global data area

18. Which of the following policy will NOT improve virtual memory performance?
A. Write through B. full-associative map C. TLB cache D. LRU replacement

19. In the following selections, which is a measurement for resolution of data hazard?
A. To calculate the branch destination address as in the earlier pipeline stages as possible.
B. Delayed branch.
C. Bypass.
D. Double bump.

20. In MIPS pipeline, “Updating the PC” is completed in _____ clock cycle.
A. IF B. ID C. EX D.MEM E. WB

21. ____ hazards arise when an instruction depends on the results of a previous instruction in a way that is exposed by the overlapping of instructions in the pipeline. ____ hazards arise from the pipelining of branches and other instructions that change the PC.

A. Data, Structural B. Structural, Structural C. Data, Control D. Structural, Control

22. Assume there are M blocks in a cache, and every K blocks are grouped in one set, then which following description is correct?

A. If K=1, then it's a direct mapped cache.
B. If K=1, then it's a full-associative cache.
C. If K=M, then it's a direct mapped cache.
D. If K>1 and K<M, then it's a M/K-way set associative cache.

二、 Fill in the blanks (16 points)

1. Suppose a computer spends 90 percent of its time handling a particular type of computation when running a given program, and its manufacturers make a change that improves its performance on that type of computation by factor of 10. The speedup is _____.

2. Suppose the hardware implementation is the classic 5-stage RISC pipeline. Unconditional branch is resolved after the end of ID stage, while the branch-target address is known at ID too. But the branch condition is evaluated till the end of EX stage. The branch strategy is predict-taken. Then how many stalls must each type of instruction take?

Branch taken:_____cycles; Branch untaken: _____cycle

3. A cache has 64-KB capacity, 128-bytes/line, and is 4-way set-associative. The system containing the cache uses 32-bit addresses.

The cache has _____ lines. The cache has _____ sets.

Tag information is_____ bits.

4. Assume the performance of the basic memory organization is:

4 clock cycles to send the address
56 clock cycles for the access time per word
2 clock cycles to transfer a word of data

Given a cache block of four words, and that a word is 8 bytes, the miss penalty is _____(Calculation expression should be given out.) clock cycles, with a memory bandwidth of _____ bytes per clock cycle.

三、 Calculations（62 points）

1. **(12 points)**Your company is developing a program with high requirement on computation. You asked your R&D department to make some improvements on the execution time. After several months, they give you two solutions. The first one is to use a new hardware technology, by which 40% of the computation can be accelerated by 10 times. Another solution is focused on algorithm design, which can enhance 60% and 10% of the total computation by 2 and 20 times respectively.
Question:
a) What is the overall enhancement of the hardware solution?
b) What is the overall enhancement of the software solution?
c) Which one will you choose?

2. **(15 points)**Within some **memory/cache** memory hierarchies, there are 2 words in a block. Access time of Cache is 8ns and miss penalty is 70ns. For the following C code, assumes that each element is one word in array (**A[i])**. Variable **s** has be loaded into registers. Please answer questions:

```
for ( i=0; i<100; i++)
    s=s+A[i] ;
```

(1) What is the miss rate for data accesses?

(2) What is the average memory access time for data read?

(3) What is the overall CPI including memory access? Assume processor runs at 1.1GHz and has a CPI of 1 excluding memory accesses. Ignores instructions misses and data hazard and control hazard. Assumes assembler code is below:

```
                ……
LOOP:   LOAD    R2,   0(R1)        ; R2 ←Mem[R1+0]
        ADD     R5,   R1,   #4     ; R5 ←R1+4
        ADD     R3,   R2,   R3     ; R3 ←R2+R3, s was stored in R3
        BNE     R5,   LOOP         ; if R5≠0, then goto LOOP
                ……..
```

3. **(15 points)** Consider the following pipeline. All instructions have five cycles but autoincrement addressing instruction, which is IF, ID, EX, MEM, WB. Branch will complete at the third cycle. The pipeline extended MIPS pipeline in autoincrement addressing mode which have seven pipe stages. The Fig 1 is an example in autoincrement addressing:

eg: Add R1, (R2)+

means: Regs[R2]←Regs[R2]+4

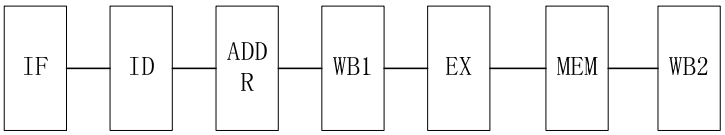
Regs[R1]←Regs[R1] + Mem[Regs[R2]]

Fig 1: example instruction of autoincrement addressing

The register files can perform two reads and two write every clock cycle. To handle reads and writes to the same register, assume the register write in the first half of the clock cycle and the read in the second half.

Read the following code segment . The pipeline has forwarding path.

```
Loop:  LW R1, 4(R2)
       ADD R2, (R1)+
       ADDI R3, R3, #4
       SUB R4, R1, R2
       SW R2, 4(R4)+
       BNEZ R3, Loop
```



IF: Instruction fetch

ID: Instruction decode

ADDR: AutoIncrement Addressing

WB1: Write Result of ADDR to Register file

EX: Memory Reference: Calculate the absolute address

ALU Instruction: Calculate.

MEM: Memory Access

WB2: Write Result to Register file

Fig 2: seven pipeline stage of the autoincrement addressing

(1) if the pipeline has no delay slot, find out how forwarding path work in every instruction? Draw the pipe stage diagram, mark the every forwarding path in diagram.

(2) if the pipeline has one delay slot, how to adjust the code segment. Draw the pipe stage diagram.

4 **(20 points)** You are building a system around a processor with inorder execution that runs at 1.1GHz and has a CPI of 0.7 excluding memory accesses. The only instructions that read or write data from memory are loads(20% of all instructions) and stores(5% of all instructions).

The memory system for this computer is composed of a split L1 cache that imposes no penalty on hits. Both the I-cache and D-cache are direct mapped and hold 32 KB each. The I-cache has a 2% miss rate and 32-byte blocks, and the D-cache is write through with a 5% miss rate and 16-byte blocks. There is a write buffer on the D-cache that eliminates stalls for 95% of all writes.

The 512KB write-back, unified L2 cache has 64-byte blocks and an access time of 15ns. It is connected to the L1 cache by a 128-bit data bus that runs at 266 MHz and can transfer one 128-bit word per bus cycle. Of all memory references sent to the L2 cache in this system, 80% are satisfied without going to main memory. Also, 50% of all blocks replaced are dirty.

The 128-bit-wide main memory has an access latency of 60ns, after which any number of bus words may be transferred at the rate of one per cycle on the 128-bit-wide 133 MHz main memory bus.

a) [5 points] What is the average memory access time for instruction accesses?

b) [5 points] What is the average memory access time for data read ?

c) [5 points] What is the average memory access time for data writes ?

When a write miss occurred, Assume write back use write allocated, and write through use write around. So no matter whether there a write miss, we should write data to second level cache.

d) [5 points] what is the overall CPI, including memory accesses?