浙江大学 2018–2019 学年秋冬学期

《数字逻辑设计》课程期末考试试卷

课程号：211C0060，开课学院：计算机科学与技术学院

考试试卷：A卷√、B卷（请在选定项上打√）

考试形式：闭√、开卷（请在选定项上打√），允许带/入场

考试日期：2019 年 1 月 16 日，考试时间：120 分钟

诚信考试，沉着应考，杜绝违纪。

Name: **Student ID:** **Dept.:**

Section	1	2	3	4	5	Total
Score						
Reviewer						

1. (20%) Fill in the blanks

1) (3%) Convert the following number to the indicated bases : $(189.625)_{10}$ = (_____)$_2$ = (_____)$_8$=(_____)$_{16}$.

2) (2%) The sum of two binary numbers $(1011)_2$ and $(101)_2$ is _____; the product is _____. (Without converting results to decimal)

3) (2%) The 2's complement of unsigned binary number 10000000 is_____.

4) (2%) A binary number can be converted to be viewed on a 7-segment display by a/an _____.

5) (2%) A 4–to–1-line multiplexer has _____ signal inputs, _____ select inputs and one output.

6) (1%) Normally, the speed of Flip-flop is _____ than that of latch.

7) (2%) The _____of a Flip-flop is the minimum amount of time that an input must remain stable before an active clock transition.

8) (2%) How many Flip-flops will be complemented in an 8-bit binary up counter to reach the

next count after the count 10101111: _____.

9) (2%) A 4K×16 ROM has _____ address lines and _____ data lines..

10) (2%) In the Verilog language, variable of _____type represents a circuit connection, which can't be used for information storage; variable of _____ type is used for data storage.

2. (20%) Choose the best answer to fill the blanks

1) Which of the following logical gates can be used as a controllable inverter? _____.

A. AND gate B. OR gate C. NOR gate D. XOR gate

2) The two types of gates which are called universal gates are _____.

A. AND/OR B. NAND/NOR C. AND/NAND D. OR/NOR

3) The gate input cost (with NOT, GN) for logic expression $F = AB(C + D) + C(B\overline{D} + \overline{A}D)$ is _____.

A. 15 B. 16 C. 17 D. 18

4) The dual of function $F = X(\bar{Y}\bar{Z} + \bar{Y}Z)$ is _____.

A. $X + (\bar{Y} + \bar{Z})(Y + Z)$ B. $\bar{X} + (Y + Z)(Y + \bar{Z})$

C. $X + (\bar{Y} + \bar{Z})(\bar{Y} + Z)$ D. $\bar{X}(Y + Z)(Y + \bar{Z})$

5) A programmable device that uses a look-up table (LUT) to generate logic is _____.

A. a PAL B. a PLA C. an FPGA D. a ROM

6) A negative-edge-triggered J-K flip-flop is presently in the CLEAR state. Which of the following input conditions will cause it to change states? (Note: PGT: Clock transition from '0' to '1', NGT: Clock transition from '1' to '0') _____.

A. CLK = NGT, J = 1, and K = 0 B. CLK = NGT, J = 0, and K = 1

C. CLK = PGT, J = 1, and K = 0 D. CLK = PGT, J = 0, and K = 1

7) What is the output frequency of a 3-bit binary counter with an input clock frequency of 80 kHz? _____.

A. 15 kHz B. 20 kHz C. 5 kHz D. 10 kHz

8) What is the output state of a Modulo 64 counter after 92 input pulses if the starting state is 000000? _____.

A. 011100 B. 100100 C. 011110 D. 010110

9) The first step in a read or write operation for a Random Access Memory is to _____.

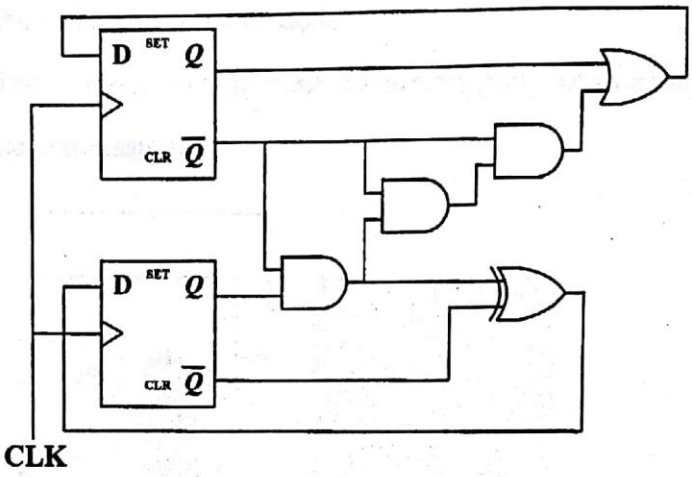
A. activate the read or write input

B. send or obtain the data

C. place a valid address on the address bus

D. start a refresh cycle

10) The timing parameter for the gates and flip-flops in the sequential circuit given below are as follows: AND Gate: t_{pd} = 7.0ns; OR Gate: t_{pd} = 8.0ns; XOR Gate: t_{pd} = 11.0ns; Flip-flop: t_{pd} = 8.0ns, t_s = 4.0ns, t_h = 1.0ns. The maximum frequency of operation of the sequential circuit is _____.



A. 33.33MHz

B. 18.18MHz

C. 24.39MHz

D. 22.72MHz

3. (15%) Verilog and Kaunaugh Map

1) (6%) Draw the logic diagram of the circuit specified by the following Verilog description:

```
module Circuit_A (A, B, C, D, F);
  input A, B, C, D;
  output F;
  wire w, x, y, z, a, d;
  or (x, B, C, d);
  and (y, a ,C);
  and (w, z ,B);
  and (z, y, A);
  or (F, x, w);
  not (a, A);
```

```
    not (d, D);
endmodule
```

2) (4%) Please simplify the function using algebraic manipulation, and give the identities or laws in the steps where necessary.

$$F = \bar{A}B(\overline{D} + \overline{C}\,D) + B(A + \bar{A}CD)$$

3) (5%) Simplify the function using Karnaugh maps:

$$F(A,B,C,D) = \sum(0,3,5,7,8,9,11,15) + \sum d(2,10,13)$$

and answer the following questions. (Note: the most significant bit is A)

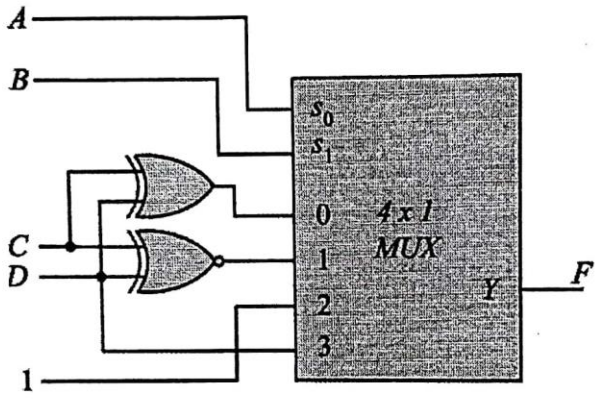
a) (2%) Draw the K-Map of the function

b) (1%) List the essential prime implicants:

c) (2%) Perform the optimization in the form of SOP

4. (15%) Analyze the following circuits

1) (7%) According to the following logic circuit diagram, write down the canonical sum of product expression.



2) (8%) The following register transfer operations will be implemented where K1, K0 are two input Boolean variables:

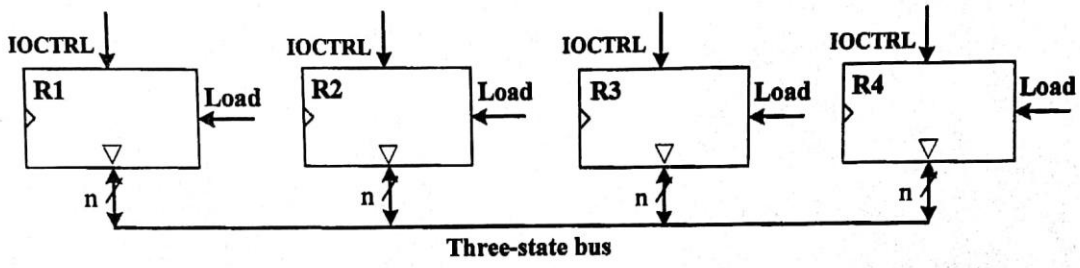
$\overline{K1}\ \overline{K0}$: R1 ← R2

$\overline{K1}\ K0$: R2 ← R3

$K1\ \overline{K0}$: R3 ← R2

$K1\ K0$: R1 ← R4

All four n-bit registers R1, R2, R3, and R4 have three-state bi-directional data input/output lines connecting to a shared bus as shown in the figure below. Fill in the control signals (Load and IOCTRL) to each of these four registers so that the above conditional register transfer operations can be realized. (Note: IOCTRL=0: read data from bus, IOCTRL=1: write data to bus)



	Load	IOCTRL
R1		
R2		
R3		
R4		

5. (30%) Circuit design

1) (10%) Design a full-subtractor circuit with three inputs X, Y, B_{in} and two outputs Diff and B_{out}. The circuit subtracts $X - Y - B_{in}$, where B_{in} is the input borrow, B_{out} is the output borrow, and Diff is the difference. Please find the circuit's truth table, Boolean equation, and a logic diagram.

2) (20%) Design a sequential circuit with two D flip-flops A and B, and one input x_in. When x_in = 0, the state of the circuit remains the same. When x_in = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats. Please write down the state diagram, state table, next state function, input equation and draw the circuit.