

LAB REPORT

R2P2, NANO-X PROGRAM

SPARC WORKSHOP, IIITH.



SUBMITTED BY-

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I-V characteristics of photo-voltaic cells.(Prof. Subhadeep (16/12/2024))

Objective:-

To study the behaviour of photovoltaic cells under different illumination conditions and analyze the impact of wire grid thickness on current generation.

Materials and Apparatus

- Photovoltaic cell with an aluminium base and surface wire grids.
- (silicon wafer)
- Light sources:
- Ambient light (normal illumination).
- Phone flash (intense illumination).
- Multimeter for measuring current and resistance.
- 1k resistor.

Theory:-

A photovoltaic cell operates by optically sweeping minority charge carriers in the depletion region of a p-n junction. When light falls on this region, photons generate hole-electron pairs. The inbuilt electric field within the depletion region sweeps holes and electrons in opposite directions, leading to a flow of current.

Connecting a load between the terminals allows this photocurrent to drive the circuit.

Wire grid design is critical:

1. Thin wires: Higher resistance, leading to inefficiencies in current collection.
2. Thick wires: Reduced effective surface area exposed to light, lowering current generation.

Experimental Procedure

Setup:

Connect the photovoltaic cell to a variable resistor of 1kohm and multimeter and DC power source using a breadboard.

Place the cell under controlled illumination conditions sequentially:

- a. No illumination (dark).
- b. Normal room illumination.
- c. Phone flash illumination.

Measurements:

Measure and record current (I) and voltage (V), resulting in an I-V graph for each condition, by varying the DC power source voltage from -2V to 2V.

Graph

Plot a graph of Current (I) vs. Voltage (V) for each illumination condition. Include annotations highlighting significant changes.

Analysis and Discussion

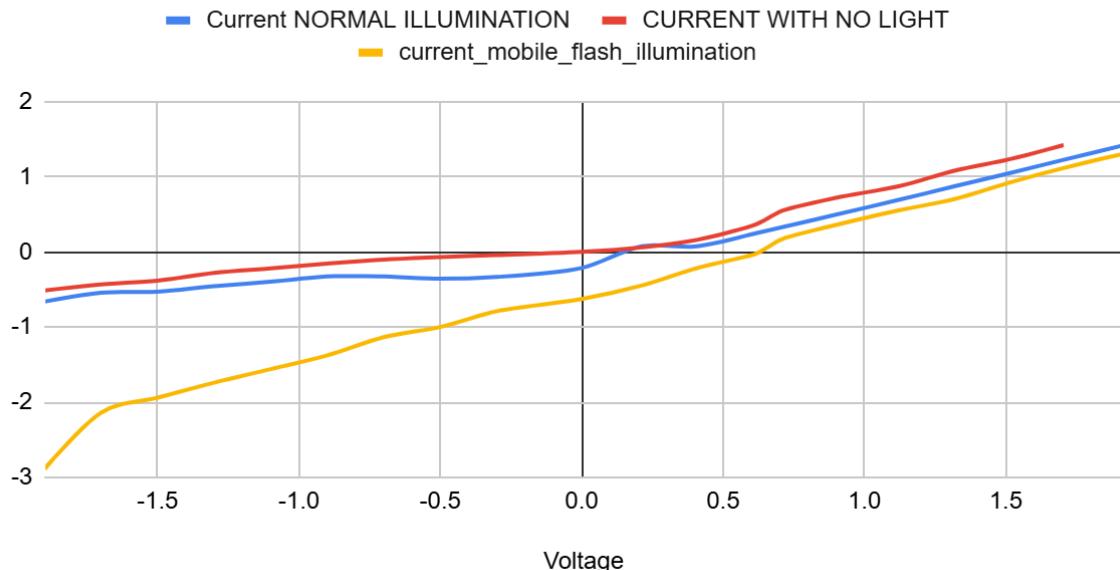
Impact of Illumination:

Compare current generation across the three conditions.

Discuss the relationship between photon intensity and current generation.

Voltage	Current NORMAL ILLUMINATION	CURRENT WITH NO LIGHT	current_mobile_flash_illumination
-1.9	-0.662	-0.514	-2.89
-1.7	-0.545	-0.433	-2.14
-1.5	-0.53	-0.383	-1.94
-1.3	-0.457	-0.28	-1.74
-1.1	-0.398	-0.22	-1.56
-0.9	-0.328	-0.156	-1.377
-0.7	-0.328	-0.104	-1.135
-0.5	-0.358	-0.069	-1
-0.3	-0.334	-0.043	-0.789
0	-0.215	0	-0.627
0.212	0.073	0.059	-0.448
0.408	0.074	0.159	-0.216
0.617	0.248	0.366	-0.025
0.709	0.328	0.546	0.17
0.899	0.494	0.718	0.358
1.125	0.695	0.876	0.554
1.322	0.875	1.082	0.705
1.516	1.05	1.234	0.924
1.705	1.224	1.42	1.115
1.914	1.415		1.3

Current NORMAL ILLUMINATION, DARK and current_mobile_flash_illumination



Observations:-

With increasing intensity, in reverse bias, the current magnitude increases with increased illumination at a fixed reverse bias voltage.

- The **current increases with light intensity**, showing the photovoltaic effect, where photons from light generate electron-hole pairs that produce current.
- The **current-voltage characteristics** exhibit a typical diode-like behavior, where the current is positive for forward bias and negative for reverse bias.
- The **open-circuit voltage and short-circuit current** are key metrics to assess the performance of the solar cell under varying light conditions.
- The reverse current should ideally remain small but will increase slightly with increased light intensity.
- In reverse bias, as you decrease the voltage, you may see a small reverse current (which can be negative). This is the reverse saturation current in a solar cell.
- The short-circuit current (the current when the voltage is zero) should be significantly higher under higher illumination compared to lower illumination or dark conditions.

DAY - (UNKNOWN 3.0) – (22/12/2024)

Microfluidic devices.

Use mostly for life sciences devices.

It can be used for controlled drug delivery.

We went to the Lab headed by Prof. Shishir and guided by Naveen B Sir and Sayma Ma'am.

Soft lithography :

Techniques for fabricating structures using elastomeric stamps, moulds and photo masks.

DFR: Dry film resist

We used dry film photoresist:- They are not in solvent form and are available as sheets.

We used DFR in the lab. It consists of 3 different layers. The outer layer is made of PET (polyethylene terephthalate) while the middle sheet is an actual photo-sensitive sheet.

Advantages of Dry Film Resists (DFR) over liquid photo-resist?

1. Comes as a rolled sheet. Spin coating and ensuring uniform coating are not required.
The bead effect is also not observed since spin coating is not required to ensure smooth code.
2. Non-carcinogenic unlike some liquid photoresists.
3. Chemical waste generation is negligible compared to Liquid Photoresist.
4. Unlike liquid photoresists, DFR often doesn't require cleanroom conditions for the fabrication of micro-level microfluidic devices.

DFR is a negative photoresist sensitive to UV light. This implies that the exposed part of DFR hardens (due to cross-linking happening in the constituent polymer of the photo-sensitive part). In contrast, the unexposed part is weak, i.e it will be dissolved by the developer solution.

Soft lithography: Materials generally used.

1. PDMS (Polydimethylsiloxane)
(we used this one in the lab session)
2. OSTERmers (off-stoichiometry thiol-ene polymer)

PDMS Preparation:

We take 10:1 PDMS: curing agent solution in a cup and use a desiccator with a rotary vacuum pump. We keep the solution inside for 20-30 minutes to ensure any air inside the solution comes to the solution's surface as bubbles of increasing size. Eventually, the air is sucked out by the vacuum pump.

It ensures we don't have any air cavity in the PDMS mould we will obtain at a later stage.

Mask Preparation:

- Take a glass substrate.
- Go to the workbench with red/yellow blue light.

- Cut the DFR of the size of the glass substrate using scissors.
- Paste 2 scotch tapes on the opposite sides of the DFR. Peel the film layers in opposite directions by holding them from the scotch tapes. Discard the thinner layer obtained devoid of the photo-sensitive layer. Take the thicker photosensitive layer and laminate it on the glass substrate using the laminator process. Laminate it 3-4 times to ensure there are no air bubbles in between the film and the glass substrate.
- Now take the hard mask we already have on a chrome-coated glass substrate.
- Alternatively, we can use PET sheets and print the required mask/patterns using a printer capable of resolving feature sizes of tens of micron ranges.
- Place the glass substrate on top of the mask, keeping it directly over the substrate. Turn on the UV exposure. Our batch sustained exposure for 55 seconds.
- At the end of the duration, we develop it using developer liquid .
- The obtained patterns were less prominent than required. The major reason for this is insufficient UV exposure time.
- We can make pneumatic switches using multilayer microfluidic devices.

DAY(24/12/2024)

Morning session — CVD and graphene deposition (Prof. SHISHIR)

CVD - Process and machinery , vacuum pumps , vacuum seals , actuators.
locking and welding process (orbital welding) , Kf , CVR , CV.
MFC's, (mostly instrumentation parts of the CVD are presented and machinery usage), pneumatics and electronic controls for the CVD machinery.

CVD of GRAPHENE—Graphene properties, bonding in graphene, graphene deposition, factors affecting graphene deposition (like temperature), reduction of activation energy, catalysis using other gases like Ar and other catalysis for graphene deposition, CVD graphene cooling rate, and some chemistry of gas-phase graphene.

CVD Carbon NanoTubes -

CVD process

Steps Pass a hydrocarbon gas through a reactor, use a supported transition metal catalyst, and operate at high temperatures

Results CNTs are generated on the surface of the catalyst or substrate

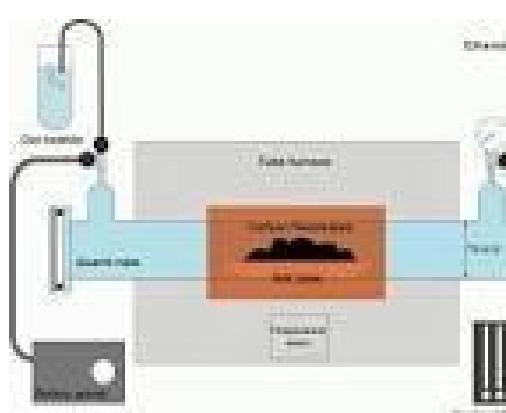
Yield	Can synthesize 90–99% CNTs
Application	Electronics, catalysts, ceramics, protective coatings, and more

Here are some more details about the CVD process:

- **Catalyst**
Metal nanoparticles are mixed with catalyst support, such as MgO or Al₂O₃, to increase the surface area for the catalytic reaction.
- **Substrate activation**
The substrate is activated using thermal heating, radiation, or plasma.
- **Deposition**
The final product is a solid deposit that usually occurs at a thermal gradient of around 1000°C.
- **Catalyst removal**
The catalyst support is removed via an acid treatment, which can sometimes destroy the original structure of the CNTs.
- **Catalyst deactivation**
The catalyst becomes deactivated during the CVD process, probably due to the formation of carbons on the catalyst nanoparticles.

Other methods for synthesizing CNTs include laser ablation and arc discharge.

The synthesis of CNTs (single- or multiple-walled) by CVD involves the catalytic decomposition of a carbon precursor (e.g., CO, hydrocarbons, or alcohol) on nanostructured transition metal catalysts like Co, Ni, or Fe. Typical CVD temperatures vary between 600 and 1000 °C.



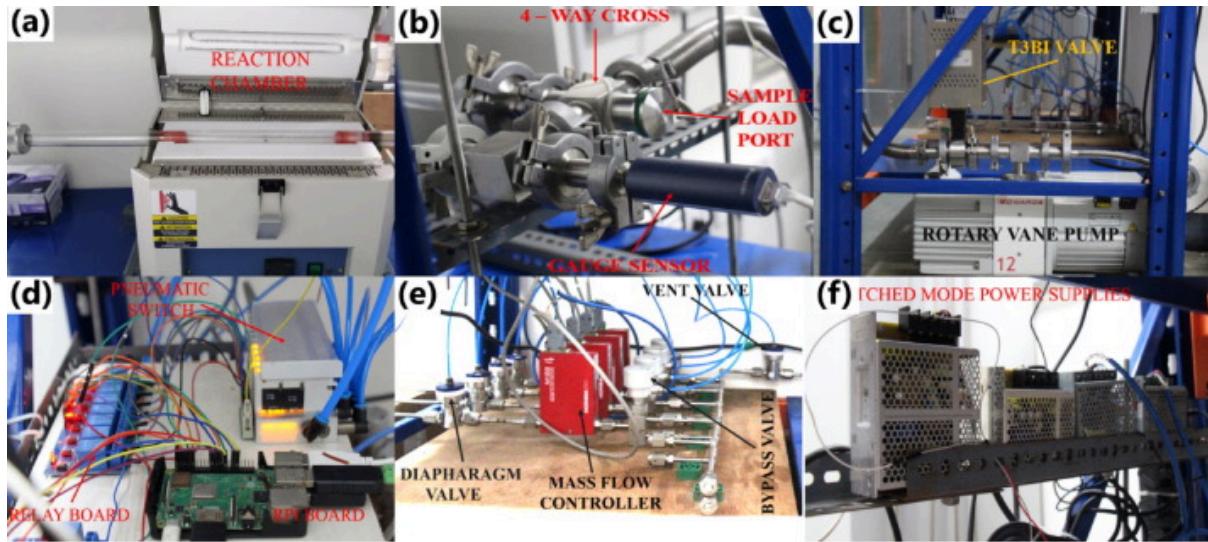
CVD VACUUM SETUP – (Types of vacuum pumps)-----

Rotary pumps, Scroll pumps, Turbo pumps.

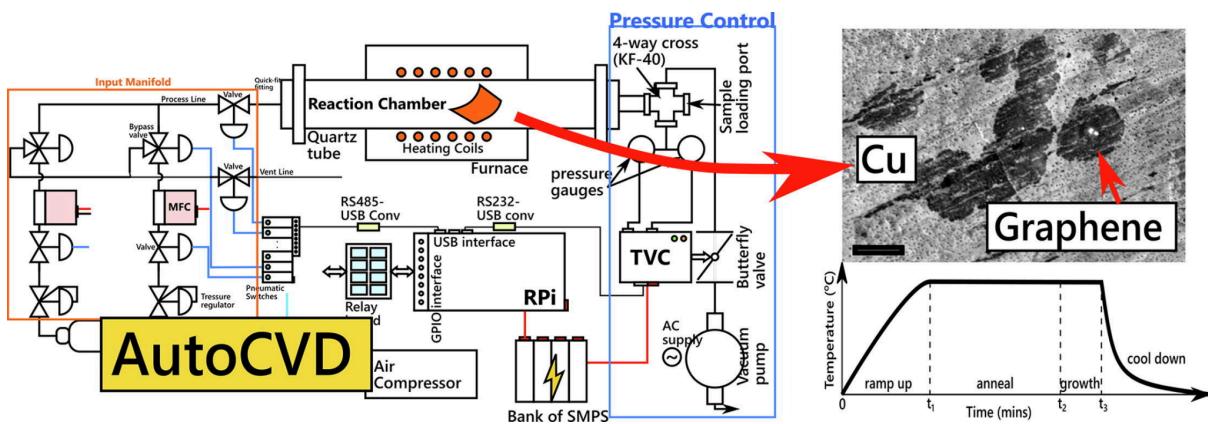
(Types of Vacuum seals) -----

VCR face sealings , KF fittings , CF fittings .

(MFC) ----- mass flow controllers



Setup of CVD for 2D structures:-



The software part of this CVD ---

all the commands generated from user interactions were recorded with a timestamp in the GUI itself and could be saved as scripts. Later, these scripts were used for automated

```

Log file name: Run details: Start Logging View Logs
Update at: 1000 ms
sw-ventline
Input Manifold
sw-ch4-1-in: 20.00 sw-ch4-1-by: 0.1000
sw-ar-1-in: 100.00 sw-ar-1-by: 0.1000
sw-h2-1-in: 0.0000 sw-h2-1-by: 0.0000
Pressure Control
TVC: 0.0911 Torr 100.0 % TVC
Butterfly valve: Open
Furnace
Scripting Interface
Commands to be executed:
1562140932413 sw-ventline set_state 1
1562140933880 sw-ventline set_state 0
1562140927371 sw-ventline set_state 1
1562140927371 sw-ventline set_state 0
1562140945946 nfc-h2-1-in set_flow 100
1562140945946 nfc-h2-1-in set_flow 0
1562140940017 sw-pump-ctrl set_state 1
1562140940017 sw-pump-ctrl set_state 0
1562140940017 sw-pump-ctrl set_state 1
1562140940017 sw-pump-ctrl set_state 0
1562150999017 nfc-ch4-1 set_flow 20
1562150999017 nfc-ch4-1 set_flow 0
1562150999017 nfc-ch4-1 set_flow 1
1562150999017 nfc-ch4-1 set_flow 0
1562150999017 nfc-ch4-1 set_flow 1
1562150999017 nfc-ch4-1 set_flow 0
1562151002332 sw-ch4-1-in set_state 1
1562151002332 sw-ch4-1-in set_state 0
1562151312464 sw-h2-1-by set_state 1
1562151312464 sw-h2-1-by set_state 0
1562151327081 sw-ch4-1-in set_state 0

```

sessions.

AFTER- NOON ----- (CLEAN ROOM) (TA- trinidad ji, Naveen ji, Aditya ji).

Usage of Laser writer to write TLM structures on Silicon substrate.

Lab Report: Direct Writing on Silicon Wafer Using Laser Printer

Objective: To fabricate TLM (Transmission Line Method) pad structures on a silicon wafer using a laser printer for direct writing. The aim was to create structures with specific aspect ratios and spacing to facilitate contact resistance characterization.

Introduction: The use of direct writing techniques in microfabrication eliminates the need for traditional photomasks, streamlining the process and reducing costs. This experiment focused on employing a laser printer to write directly on a silicon wafer. The designed structures consisted of TLM pads with precise dimensions and varying spacings to assess the feasibility and resolution of the process.

Materials and Equipment:

- Silicon wafer (cleaned and prepared)
- Laser printer for direct writing
- Mask design software
- Alignment tools (if required)
- Measurement tools (microscope, profilometer)

Methodology:

1. **Mask Design:**
 - Designed TLM pad structures with an aspect ratio of 1:2.
 - Pad sizes: 80 microns and 160 microns.
 - Spacing:
 - Initial gap: 10 microns.
 - Incremental increase: 5 microns.
 - Maximum gap: 25 microns.
2. **Direct Writing:**
 - Configured the laser printer for precise direct writing on the silicon wafer.
 - Loaded the designed pattern into the laser printer software.
 - Performed a test run to calibrate laser intensity and focus.
 - Directly wrote the pattern onto the silicon wafer.
3. **Post-Processing:**
 - Inspected the wafer under a microscope to ensure proper definition of structures.
 - Verified dimensions and spacing using measurement tools.

Results:

- The TLM pad structures were successfully fabricated on the silicon wafer.
- Observations:
 - The aspect ratio of 1:2 was maintained.
 - Pads with dimensions of 80 microns and 160 microns showed clear edges.
 - Spacing between pads: The smallest gap of 10 microns was achieved, and the incremental gaps (up to 25 microns) were distinct and uniform.
- Challenges: Minimal alignment errors were observed, which might require further optimization of the laser focus and positioning system.

Discussion: The direct writing approach proved to be an efficient alternative to traditional photomask methods. The laser printer exhibited adequate resolution to fabricate the designed patterns. The TLM pads created with varying spacings will allow for comprehensive analysis of contact resistance.

- Optimize laser settings to further enhance edge definition and alignment.
- Explore smaller feature sizes to test the resolution limits of the system.
- Perform electrical characterization of the fabricated TLM structures.

Conclusion: Direct writing using a laser printer demonstrated its capability to fabricate intricate TLM pad structures on a silicon wafer. The process successfully maintained the designed aspect ratios and spacings, making it a promising technique for microfabrication applications.

Lab Report: Usage of Laser Writer in Microfabrication

Objective: To utilize a laser writer for direct patterning on silicon wafers, detailing the design and fabrication process, along with an understanding of the equipment and its components.

Introduction: Laser writers are critical tools in microfabrication, allowing for precise and maskless patterning on substrates. This report documents the usage of a laser writer in a cleanroom environment, focusing on the design process, conversion of design files, and the functionality of the system's components.

Materials and Equipment:

- **Software:**
 - CleWin software for designing patterns.
 - Laser writer software for file conversion and operation.
- **Hardware:**
 - Laser writer system with lens modules and a CCD camera.
 - Silicon wafer.

Methodology:

1. Pattern Design:

- Designed TLM (Transmission Line Method) pad structures using CleWin software.
- Saved the design as a .cf file.
- Converted the .cf file to a .ldf file using the laser writer software for compatibility with the machine.

2. Laser Writer Setup:

- Configured the system using **Lens 3** for the writing process.
- Adjusted parameters for optimal laser intensity and focus.
- Utilized the built-in CCD camera for alignment and real-time monitoring during the writing process.

3. Direct Writing:

- Loaded the .ldf file into the laser writer.
- Calibrated the system using the red light for initial positioning and focus adjustments.
- Executed the direct writing process on the silicon wafer.

Equipment Details:

1. Lens Modules:

- **Lens 1:** High-resolution lens for extremely fine patterns; typically used for feature sizes below 1 micron.
- **Lens 2:** General-purpose lens for medium-resolution applications, balancing speed and accuracy.
- **Lens 3:** High-speed lens used for large-area patterning with good resolution; ideal for the current experiment.
- **Lens 4:** Low-magnification lens designed for coarse features or initial alignment processes.
- Lenses offered feature sizes of 4um, 2um and 1um.

2. CCD Camera:

- Used for precise alignment of the substrate and monitoring during the writing process.
- Ensures real-time adjustments to correct for any misalignments or focus issues.

3. Red Light:

- The red light is a visible alignment aid, ensuring accurate positioning of the laser on the wafer, nearly 640 nm range!!!!
- It is non-destructive to the wafer surface and allows for quick adjustments before initiating the actual laser writing process.

4. Laser Specifications:

- **Wavelength:** The laser operates at **405 nm**, which is within the violet range of the visible spectrum.

- **Diode Type:** The system uses a **405 nm GaN (Gallium Nitride) diode laser**, known for its high efficiency and precision.

Results:

- The TLM pad structures were successfully patterned onto the silicon wafer.
- The design integrity was maintained during the conversion and writing process.
- Real-time monitoring with the CCD camera minimized alignment errors, and Lens 3 provided a balance of speed and resolution.

Discussion: The laser writer's versatility in direct writing eliminates the need for photomasks, streamlining the fabrication process. The system's modular lens configuration allows for adaptability to various feature sizes and resolutions. The use of the 405 nm GaN diode laser ensures precision, while the CCD camera and red light provide essential support for alignment and calibration.

Future Work:

- Explore the capabilities of other lenses for finer resolution or larger-scale patterning.
- Investigate the effect of laser power variations on writing quality.
- Conduct post-fabrication testing to evaluate the electrical properties of the TLM structures.

Conclusion: The laser writer demonstrated its efficiency and adaptability for direct patterning on silicon wafers. By leveraging software tools like CleWin and the laser writer's advanced features, precise TLM pad structures were successfully fabricated, paving the way for further microfabrication applications.

Day --(23/12/2024)

Clean room session wafer cleaning and spin coating.

Lab Report: Wafer Cleaning Process

Aim:

To clean silicon wafers effectively by removing organic matter, particles, and metallic contaminants, preparing them for spin coating.

Objective:

- To ensure the silicon wafer surface is free of contaminants.
- To create a hydrophilic surface suitable for subsequent processes.

- To protect the wafer from contamination using passivation layers.

Materials Required:

1. Personal protective equipment (PPE):
 - o Shoe covers
 - o Bunny suits
 - o Head covers
 - o Gloves
2. Cleanroom with laminar airflow setup
3. Chemicals:
 - o Ammonium hydroxide
 - o Hydrogen peroxide
 - o Hydrochloric acid
 - o Sulfuric acid
 - o Deionized water
4. Quartz tanks (heated)
5. Nitrogen gas blower

Steps to Follow:

Preparation:

1. Wear PPE in the following order: shoe covers, bunny suits, head cover, and gloves.
2. Enter the cleanroom and remain under the laminar airflow for 10–15 seconds to remove any surface contaminants.

Wafer Cleaning Procedure:

1. Step A: SC1 Cleaning

- Prepare the APM solution (ammonium hydroxide-hydrogen peroxide-water).
- Use this solution to remove organic matter and particles from the silicon wafer surface.

2. Step B: SC2 Cleaning

- Prepare the HPM solution (6 parts deionized water, 1 part hydrochloric acid, 1 part hydrogen peroxide).
- Use this solution to remove metallic contaminants left after SC1 cleaning.
- Allow the process to form a thin passivation layer that protects the wafer from contamination.

3. Step C: Piranha Etch Cleaning

Prepare the **Piranha solution (3 parts sulfuric acid to 1 part hydrogen peroxide)**.

Use the solution to remove residual organic materials.

Note: Perform this step in heated quartz tanks and handle the solution with care due to its highly corrosive nature.

Post-Cleaning Procedure:

1. Blow nitrogen gas through the blower to remove any remaining droplets from the wafer surface.
2. Ensure the wafer is dry and clean, ready for spin coating.

Conclusion:

The wafer cleaning process ensures the removal of contaminants and prepares the silicon wafer with a hydrophilic surface for subsequent processes like spin coating. Each step, SC1, SC2, and Piranha etch, contributes to thorough cleaning and passivation of the wafer surface. Proper handling and adherence to protocols ensure safety and efficiency.

Lab Report: Spin Coating Process

Aim:

To uniformly coat a silicon wafer with photoresist using the spin coating method and achieve the desired resist thickness.

Objective:

- To apply a uniform layer of photoresist on the silicon wafer.
- To control the thickness of the photoresist based on process requirements.
- To prepare the wafer for subsequent lithography processes.

Materials Required:

1. Cleaned silicon wafer
2. Oven or hot plate (set to ~110°C)
3. Spin coater
4. Positive photoresist (e.g., S1813)
5. Graph for resist thickness vs. rpm
6. Timer

Steps to Follow:

Preparation:

1. Bake the Wafer:

Heat the cleaned silicon wafer at ~110°C to remove any remaining liquid droplets.

Spin Coating Procedure:

2. Photoresist Application:

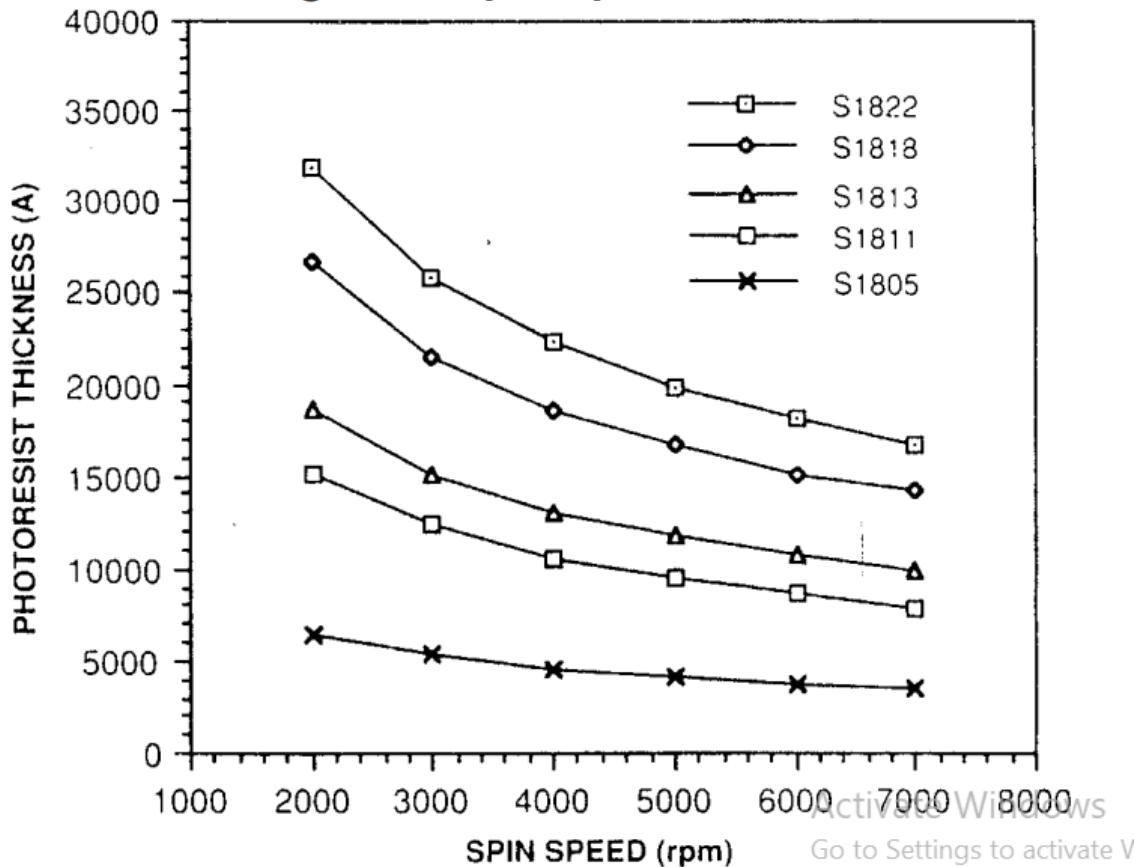
- o Place the baked wafer in the spin coater.
- o Pour droplets of S1813 positive photoresist onto the wafer surface.

3. Set Spin Parameters:

- o Refer to the provided graph to determine the rpm required for the desired photoresist thickness.

MICROPOSIT S1800 PHOTO RESIST UNDYED SERIES

Figure 1. Spin Speed Curves



4. Spin Coating Process:

- o Part A: Spin the wafer at ~500 rpm for the first 5 seconds to evenly distribute the photoresist.
- o Part B: Increase the rpm to 6000 and spin for 50–55 seconds to achieve the desired resist thickness.

5. Result:

- o Remove the wafer with the desired thickness of photoresist, ensuring it is ready for further processing.

Conclusion:

Spin coating provides a controlled and uniform photoresist layer on silicon wafers. By adjusting the spin speed and time, the desired thickness is achieved, preparing the wafer for subsequent laser writing step

(TA- question sputterer - Navin anna sir)

Plasma Etcher:-

It has vacuum pumps to ensure both plasma can be created at low temperatures comparatively and also to ensure there is no unwanted particulate contamination.

Questions posed by Naveen Sir and their answers.

1) What is plasma?

Plasma is a state of matter consisting of free electrons and ions, often referred to as the "fourth state of matter." It forms when gas is heated or subjected to a strong electromagnetic field, causing its atoms to lose electrons. This results in a highly ionized, electrically conductive medium that exhibits unique properties, such as emitting light and responding to magnetic and electric fields.

2) How is plasma generated?

Plasma is generated by providing sufficient energy to a gas to ionize it. Common methods include:

- Electrical Discharge: Applying a high voltage across a gas, as in plasma arc welding or neon lights.
- Thermal Energy: Heating the gas to a high temperature (e.g., in a plasma torch).
- Microwave or Radiofrequency (RF) Energy: Ionizing gases using electromagnetic waves.
- Laser Ablation: Using high-intensity lasers to heat and ionize materials.

3) What are different kinds of electrodes?

Electrodes are used to initiate and sustain the plasma discharge. Common types include:

1. **Cathodes and Anodes:** Basic components in DC plasma systems.
2. **Tungsten Electrodes:** Used in plasma torches for their high melting point and conductivity.
3. **Graphite Electrodes:** Common in industrial applications due to their thermal stability.
4. **Copper Electrodes:** Provide excellent conductivity and are often water-cooled.
5. **Hollow Electrodes:** Allow for gas flow through the electrode to stabilize the plasma.

4) Why is nitrogen used and why can't we use compressed air?

Nitrogen Use: Nitrogen is chemically inert at low temperatures and provides excellent thermal stability at high temperatures. It helps prevent oxidation of materials and is used to create a protective atmosphere in many plasma applications.

Compressed Air: Air contains oxygen, which can cause oxidation, contamination, or undesired chemical reactions with the material being processed. However, air is sometimes used in applications where oxidation is not a concern.

5) Why is oxygen used in plasma generation? Why can't we use any other gas like argon?

Oxygen Use: Oxygen is often used for cutting or etching applications because it reacts with materials to enhance the cutting speed and efficiency. The exothermic reaction between oxygen and the material increases the energy available for processing.

Why not Argon? Argon is chemically inert and does not react with most materials, making it unsuitable for applications requiring reactive processes. However, argon is used in specific applications (e.g., in inert atmospheres for delicate materials) or in combination with other gases to stabilize plasma.

6) What is reflectance, why is it made to zero and how will it affect the process ?

Reflectance: Reflectance refers to the portion of electromagnetic waves (e.g., RF or microwave energy) that is reflected back rather than absorbed by the plasma or the target material.

Why Zero Reflectance? Making reflectance zero ensures maximum energy transfer to the plasma, improving its stability and efficiency. Minimizing energy loss enhances the effectiveness of the process.

Impact: Reduced reflectance leads to better ionization, consistent plasma generation, and improved performance in applications like cutting, welding, or coating. High reflectance can cause inefficiencies and potential equipment damage due to back-reflected energy.

Day - unknown- 4.0 — (TA - Harsh Mishra ji, aditya madam ji, Nikhil anna).

(Clean room)

Sputtering and UV lithography :

Definition:

Sputtering is a physical vapor deposition (PVD) process used to deposit thin films of material onto a substrate. It involves ejecting atoms from a target material and depositing them onto the surface of a substrate.

Working Principle:

1. A plasma is created using a gas, often argon.
 2. High-energy ions from the plasma collide with the target material.
 3. These collisions eject atoms from the target, which then travel and deposit onto the substrate to form a thin film.
-

Types of Sputtering:

1. DC Sputtering: Used for conductive materials.

-
2. RF Sputtering: Suitable for both conductive and non-conductive targets.
 3. Magnetron Sputtering: Uses magnets to confine the plasma, increasing efficiency.
 4. Reactive Sputtering: Involves adding reactive gases (e.g., oxygen, nitrogen) to form compounds (e.g., oxides, nitrides).
-

Applications:

- Fabrication of semiconductor devices.
 - Coating of optical lenses.
 - Deposition of decorative or wear-resistant coatings.
 - Manufacturing thin-film solar cells.
-

UV Lithography

Definition:

UV lithography is a photolithographic process used in microfabrication to transfer a pattern from a photomask onto a substrate (usually silicon). This process is fundamental in the manufacturing of integrated circuits and microelectromechanical systems (MEMS).

Working Principle:

1. A light-sensitive material called photoresist is applied to the substrate.
 2. A photomask containing the desired pattern is aligned over the substrate.
 3. Ultraviolet (UV) light is used to expose the photoresist through the mask.
 4. The exposed (or unexposed) areas of the photoresist are removed during development, depending on whether the photoresist is positive or negative.
 5. The developed pattern is used for subsequent processes like etching or deposition.
-

Key Parameters:

- Wavelength of UV Light: Determines resolution; shorter wavelengths (e.g., deep UV at 193 nm) allow finer features.
- Photoresist Type: Positive (exposed areas dissolve) or negative (unexposed areas dissolve).
- Alignment Accuracy: Critical for multi-layer devices.

Applications:

- Fabrication of semiconductor chips (e.g., processors, memory).
- MEMS device production.
- Patterning optical and photonic devices.

Comparison of Sputtering and UV Lithography:		
Feature	Sputtering	UV Lithography
Purpose	Deposits thin films on a substrate.	Transfers patterns onto a substrate.
Type	Physical deposition process.	Photolithographic patterning process.
Material	Coatings (metals, oxides, nitrides).	Photoresist and substrate materials.
Applications	Coatings, sensors, optics.	Semiconductor and MEMS fabrication.

Both are key processes in advanced manufacturing but serve distinct roles in material deposition and pattern creation.

Lab Report: Fabrication of MEMS Structures using Silicon Wet Bulk Micromachining (30-12-2024)

Aim: The objective of this experiment was to study and perform wet bulk micromachining of silicon to fabricate microstructures, such as cantilevers, using anisotropic etching in a CMOS-compatible process.

Theory:

Bulk micromachining is a microfabrication process used to create MEMS structures by selectively removing the bulk of the substrate. This experiment focuses on wet bulk micromachining, which involves chemical solutions to etch silicon. Two types of wet etching are commonly employed:

- Isotropic etching: The etch rate is uniform in all directions.
- Anisotropic etching: The etch rate varies based on the crystallographic orientation of the silicon. For example, the {111} planes etch slower than {100} and {110} planes.

Anisotropic etching is particularly significant for fabricating free-standing MEMS structures like cantilevers and diaphragms. TMAH (tetramethylammonium hydroxide) is used as the etchant due to its CMOS compatibility.

Materials and Equipment:

- Silicon (Si) {100} wafer with a 1 µm thick silicon dioxide (SiO₂) masking layer
- Positive photoresist (AZ1512HS)
- Hexamethyldisilane (HMDS)
- Buffered HF solution (HF:NH₄F = 1:7)
- TMAH solution (25 wt. % UV lithography setup (Mask aligner: MIDAS MDA-400M))
- Optical microscope (Olympus STM6)
- Spin coater
- Hot air oven
- Developer solution (NaOH:H₂O = 1:3)
- Acetone and deionized (DI) water

Experimental Procedure:

Wet Etching of SiO₂ Layer We began with a silicon {100} wafer coated with a 1 µm SiO₂ masking layer. The wafer was patterned using UV lithography as follows:

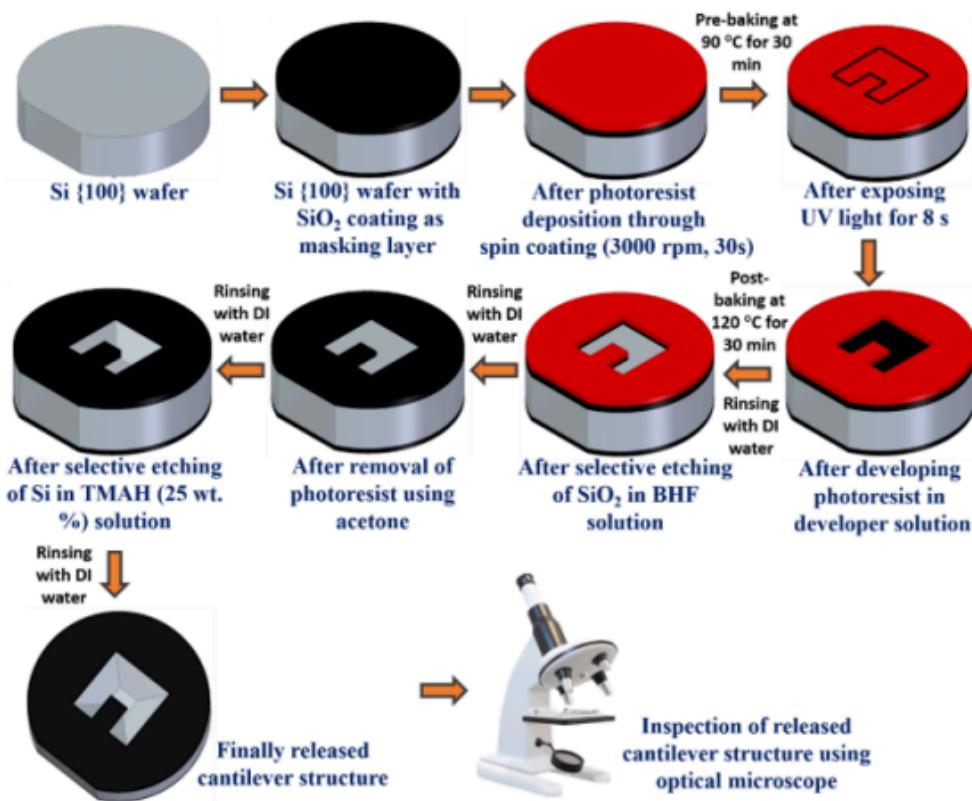
1. Spin coating of HMDS followed by positive photoresist (AZ1512HS) was performed at 3000 rpm for 30 seconds.
2. The wafer was pre-baked at 90 °C for 30 minutes in a hot air oven.
3. A photomask containing the cantilever patterns was aligned, and UV exposure was carried out for 8 seconds.
4. The exposed wafer was developed in NaOH:H₂O (1:3) for 2 minutes and rinsed with DI water.
5. Post-baking at 120 °C for 30 minutes was performed.

The SiO₂ layer was selectively etched using a buffered HF solution. The etched wafer was rinsed thoroughly with DI water and inspected under a microscope to verify the patterns.

Anisotropic Etching with TMAH

We proceeded to fabricate cantilever structures through anisotropic etching:

1. The photoresist was removed using acetone, and the wafer was cleaned with DI water.
2. The wafer was diced into smaller chips for easier handling.
3. A 25 wt.% TMAH solution was heated to 70 °C, and its temperature was monitored continuously.
4. The chips were immersed in the TMAH bath. Periodic inspections were conducted at 30-minute intervals to monitor the etching progress.
5. The etching process was stopped once the cantilever structures were fully released.
6. The fabricated structures were cleaned with DI water and characterized using an optical microscope.



Observations and Results

- The SiO₂ layer was effectively patterned and etched using buffered HF.
- TMAH etching successfully fabricated cantilever structures, as verified under the microscope.
- KOH was avoided due to its incompatibility with CMOS processes, emphasizing the importance of using TMAH for this application.
- Optical microscopy revealed well-defined cantilever structures.



(a) Etched Silicon Wafer



(b) Wet Etching Station where Wet Etching is done

Figure 4: Observations from the Lab

Conclusion

The experiment demonstrated the fabrication of MEMS structures using silicon wet bulk micromachining. Anisotropic etching with TMAH proved effective in releasing free-standing cantilever structures. This process showcases the precision and feasibility of MEMS fabrication using wet bulk micromachining.

Lab Report:

Silicon Wafer Etching using Olympus LEXT 30-12- 2024

Meta Description :

We know about the benefits of silicon wafer etching technique using the Olympus LEXT OLS5100 laser confocal microscope for micro-texturing of the silicon front surface to improve the performance of solar panels, and the potential gains it can offer solar parks across India.

Introduction:

Silicon wafer etching is a crucial process to improve light trapping by modifying the surface reflectivity of silicon wafers, primarily for solar panel manufacturing. This process, known as micro-texturing, involves the use of alkaline solutions to form micro-sized pyramidal structures on the silicon surface. Parameters such as surface roughness and surface area are essential as they increase with etching time, helping to optimize the etching process for desired results.

Challenges in Conventional Techniques Conventional techniques like SEM (Scanning Electron Microscope}

Conventional techniques like SEM (Scanning Electron Microscopy) require cutting samples to observe the cross-section, making the process tedious and cost-ineffective.

Solution:

Olympus LEXT OLS5100 Laser Confocal Microscope offers an easy and sophisticated alternative for analyzing silicon wafer etching.

Benefits

- Submicron Level 3D Observation and Measurement: Enables accurate observation of submicron unevenness on the silicon wafer's texture.
- Surface Roughness Measurement: Provides ISO-compliant measurements, transitioning from line profile to aerial observation for a new standard of roughness measurement.
- Speed and Efficiency: A non-contact, non-destructive technique that requires no sample preparation, allowing immediate measurement.

Functional Capabilities

- Etched Silicon Wafer Imaging: Captures height of individual peaks and calculates

maximum peak values (Sp), surface roughness, surface area, and pyramid volume.

- Volume and Surface Area Measurement: Analyzes peak and valley volumes, enabling optimization for homogeneous peak distribution and minimal valley zones.
- Peak Density and Direction Analysis: Measures Spd (density of peaks per unit area), Spc (arithmetic mean of principal curvature of peaks), and Std (texture direction angle).
- Periodicity Analysis: The PSD parameter provides insights into the periodicity of pyramidal structures.

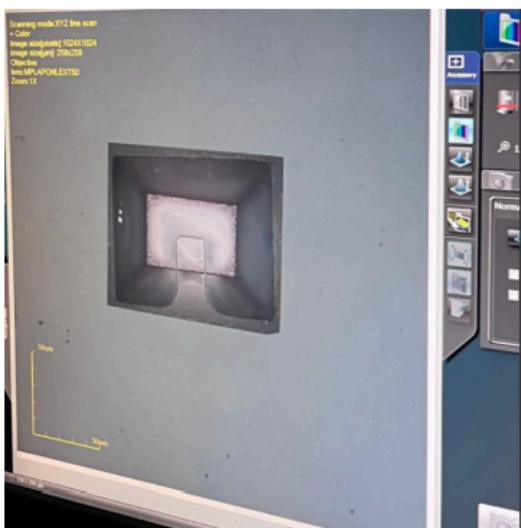
Advantages of the Olympus OLS5100

- Eliminates the need for destructive sample preparation.
- Ensures non-contact analysis, preventing contamination.
- Automates data collection and visualization with a smart experiment manager, reducing errors and simplifying workflows.
- Provides head map analysis, displaying all relevant data in a single sheet without the need for individual file handling.

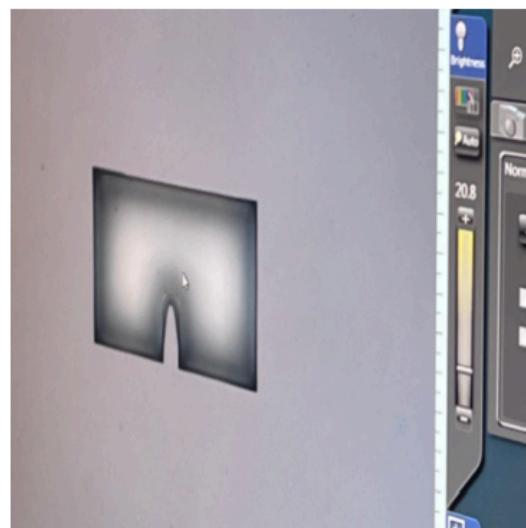
Observation

During the etching process, the following phenomena were observed:

- Undercutting: Significant undercutting at mask edges not aligned with 111 planes, especially in convex patterns.
- Plane-Specific Etching: 100 and 110 planes showed faster etching rates compared to the slower 111 planes.
- Concave and Convex Cutting: Concave mask patterns aligned well with 111 planes, whereas convex patterns exhibited prominent underetching effects.
- Undercutting and Surface Morphology: Prolonged etching revealed 111 facets on the sidewalls of fabricated structures, emphasizing orientation dependency.



(a) Perfectly Etched: We can see the transparent SiO₂ layer



(b) Under Etched structure

Conclusion :

The Olympus LEXT OLS5100 laser confocal microscope revolutionizes silicon wafer etching analysis by providing precise, non-destructive, and automated measurements.

It plays a significant role in optimizing processes for solar panel manufacturing, contributing to improved performance and efficiency in solar energy applications.

Lab Report: Vibrometer Characterization 30-12-2024

4.1 Objective

The purpose of this experiment was to characterize the vibration properties of a system using a Doppler vibrometer.

This included measuring frequency and mode shapes, as well as damping and quality factors.

4.2 Introduction

A Doppler vibrometer (LDV) is a scientific instrument used to measure vibrations on a surface without physical contact.

The LDV operates by detecting the Doppler effect of a reflected laser beam and is widely used in engineering and biomedical applications.

4.2.1 Applications of LDVs

- Engineering: Non-contact measurement of vibrations and sounds in industrial machinery, motors, and electronic equipment.
- Biomedical: Hearing research and other medical applications.

4.2.2 Specifications of the LDV System

- Frequency measurement range: 0.1 Hz to 250 kHz (analog), up to 5 MHz (digital).
- Velocity measurement range: Adjustable from 10 mm/s to 2 m/s based on resolution.
- Resolution: Velocity: $0.02 \mu\text{m/s}/\sqrt{\text{Hz}}$, Displacement: 1 pm.
- Demodulation system: FPGA digital decoding system for real-time output.

4.3 Experimental Procedure

- The accelerometer was placed on the test surface, and the Doppler vibrometer was set up to measure the vibration characteristics.
- The system was excited, and the laser beam was focused on the vibrating surface to record the Doppler shift.
- The frequency spectrum of the vibrations was obtained, and the resonant peak was identified.
- High precision bandwidth (HPBW) was used to calculate the quality factor (Q).

4.4 Observations

- The magnitude versus frequency spectrum was analyzed.
- The resonant peak occurred at a frequency of 71.56 kHz.
- The half-power bandwidth (HPBW) was measured as 938 Hz.

4.5 Calculations

4.5.1 Quality Factor (Q)

The quality factor is calculated using the formula: $Q = f_0 / \text{HPBW}$

Where:

- $f_0 = 71.56 \text{ kHz}$
- $\text{HPBW} = 938 \text{ Hz}$

Substituting the values: $Q = 71,560 / 938 \approx 76.26$

4.6 Results

- Resonant Frequency: 71.56 kHz.
- Half-Power Bandwidth: 938 Hz.
- Quality Factor: 76.26.



Figure 6: Magnitude v/s Frequency Response of Accelerometer when place inside LDV



Figure 7: A Doppler vibrometer, also known as a laser Doppler vibrometer (LDV)

4.7 Conclusion

The experiment successfully characterized the vibration properties of the test system. The resonant peak was identified at 71.56 kHz, and the quality factor was calculated as approximately 76.26, indicating the sharpness of the resonance. The Doppler vibrometer proved to be an effective tool for non-contact vibration analysis, providing precise and reliable measurements.

Reactive Ion Etching : (cleanroom – 30/12/2024) — (question sputterer anna, Kishore anna, Nandana ji , Ritu ji, Bipul ji)

Reactive Ion Etching (RIE)

Definition:

Reactive Ion Etching (RIE) is an advanced plasma-based etching technique used in microfabrication. It combines physical sputtering and chemical reactions to remove material from a substrate in a controlled and anisotropic manner. RIE is widely used in semiconductor manufacturing to create fine, precise patterns, mostly for anisotropic etching and control of etching used in MEMS (worked on this on 30/12/2024) .

Working Principle:

1. Plasma Generation:

- A low-pressure chamber is filled with a reactive gas (e.g., CF₄, SF₆(we used this), O₂).
- A high-frequency RF (radio frequency) voltage is applied, ionizing the gas to create plasma.

2. Ion Bombardment:

- Positively charged ions are accelerated towards the substrate by the electric field, physically sputtering material off the surface.

3. Chemical Reactions:

- The reactive species in the plasma chemically interact with the material to form volatile byproducts, which are then evacuated by the vacuum system.

4. Anisotropic Etching:

- The combination of directional ion bombardment and localized chemical reactions allows for anisotropic etching, creating vertical sidewalls critical for high-resolution patterns.
-

Key Parameters:

- **Gas Mixture:** Determines the nature of chemical reactions (e.g., CF₄ for silicon etching).
 - **RF Power:** Controls the energy of the ion bombardment and etch rate.
 - **Chamber Pressure:** Influences the plasma density and ion directionality.
 - **Bias Voltage:** Affects the degree of physical sputtering.
 - **Etch Selectivity:** Ratio of etch rates between the target material and mask material.
-

Advantages:

- Highly anisotropic etching for fine, vertical features.
 - Precise control over etch depth and rate.
 - Compatibility with a wide range of materials (e.g., silicon, oxides, nitrides).
-

Limitations:

- May cause surface damage due to energetic ion bombardment.
 - Process complexity and higher cost compared to wet etching.
 - Requires careful optimization of parameters for specific materials and designs.
-

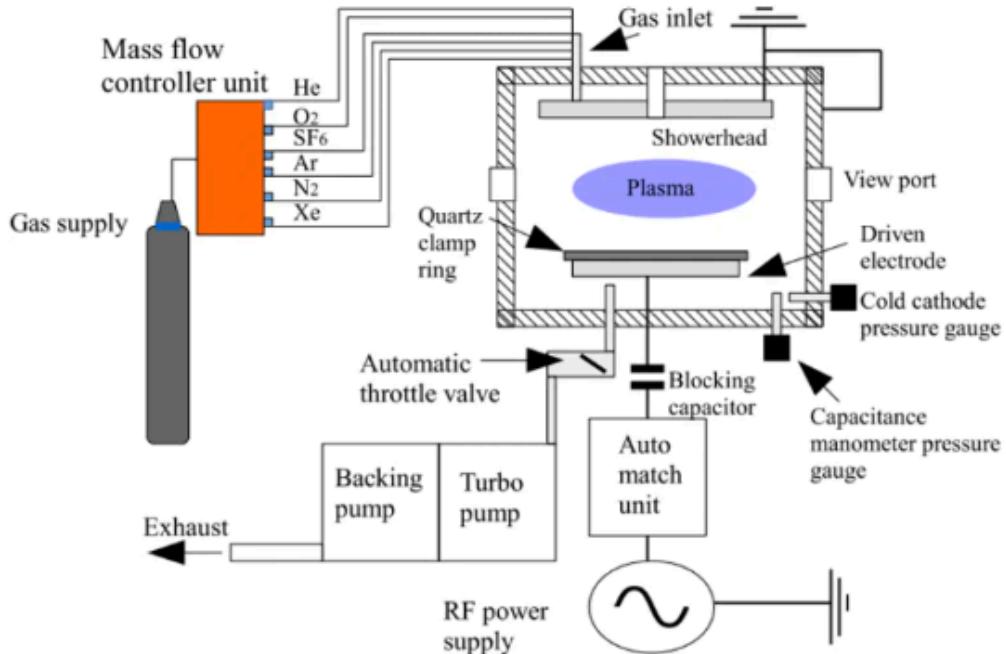
Applications:

- Fabrication of high-aspect-ratio structures in semiconductor devices.
- Etching trenches and vias in integrated circuits.
- MEMS fabrication (e.g., accelerometers, gyroscopes).
- Nanostructure formation in photonic and electronic devices.

Comparison with Other Etching Techniques:

Feature	RIE	Wet Etching
Etching Nature	Dry, plasma-based etching.	Wet, liquid-based etching.
Etch Profile	Anisotropic (vertical sidewalls).	Isotropic (undercutting common).
Selectivity	Moderate to high, tunable by chemistry.	High for specific materials.
Resolution	High, suitable for micro/nanostructures.	Lower, limited by diffusion.
Damage	Possible ion-induced damage.	Minimal, gentle on the surface.

RIE plays a crucial role in modern microfabrication, enabling the creation of advanced devices with precise and complex geometries.



ICP and RF in Reactive Ion Etching (RIE)

ICP (Inductively Coupled Plasma) and **RF (Radio Frequency)** are two key technologies that enhance the capabilities of RIE systems. They are used to generate plasma and control the etching process more precisely. Here's how they fit into RIE:

Inductively Coupled Plasma (ICP)

What is ICP?

Inductively Coupled Plasma is a high-density plasma generation method. It uses an inductive coil to produce plasma independently of the RF bias applied to the substrate, allowing for better control of the ion density and energy.

How it Works:

- A high-frequency RF power source (e.g., 13.56 MHz) energizes an inductive coil wrapped around the etching chamber.
- This coil generates an oscillating magnetic field that ionizes the gas in the chamber, producing a dense plasma.
- ICP generates a high plasma density while keeping the ion energy relatively low.

Advantages of ICP in RIE:

- **Independent Plasma Control:** High plasma density can be maintained without increasing ion bombardment energy, reducing damage to the substrate.

- **Improved Etch Rates:** Higher plasma density increases the etching rate.
 - **Better Uniformity:** Plasma density is more uniform, leading to consistent etching across the substrate.
 - **Low Pressure Operation:** ICP systems operate at lower pressures, enabling more anisotropic (vertical) etching.
-

RF (Radio Frequency) in RIE

What is RF Power?

Radio Frequency power is used in RIE to generate the electric field that accelerates ions from the plasma toward the substrate. This acceleration enables directional (anisotropic) etching by sputtering material from the substrate surface.

How it Works:

- A low-pressure gas (e.g., CF₄, SF₆) is introduced into the chamber.
- RF power, typically at 13.56 MHz, is applied to the substrate holder (electrode), creating an oscillating electric field.
- This electric field causes ions in the plasma to accelerate towards the substrate, physically sputtering and chemically reacting with the material to remove it.

RF Bias in RIE:

- The RF power applied to the substrate holder creates a **bias voltage**, which controls the energy of ion bombardment.
 - Higher RF power increases the bias voltage, enhancing physical sputtering and etch rate.
 - By adjusting the RF power, the balance between physical and chemical etching can be fine-tuned.
-

ICP-RIE: Combining ICP and RF

In ICP-RIE systems, ICP and RF are used together to achieve better etching precision and flexibility:

- **ICP Power (Plasma Generation):** Controls the plasma density (number of reactive species).
- **RF Power (Ion Acceleration):** Controls the ion energy for directional etching.

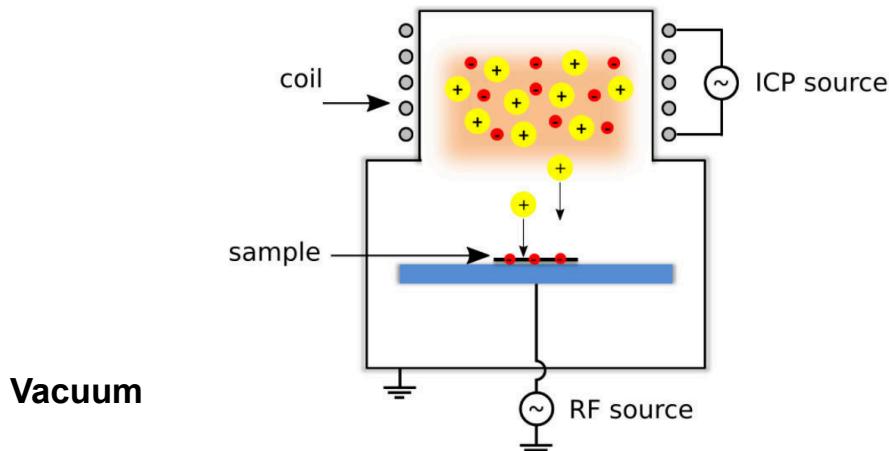
Advantages of ICP-RIE:

1. **Decoupled Control:** Allows independent control of plasma density and ion energy, optimizing the etch profile and minimizing substrate damage.
2. **High Aspect Ratios:** Can achieve deep, vertical etching with excellent anisotropy.

3. **Versatility:** Suitable for etching a wide range of materials (e.g., silicon, oxides, nitrides).
-

Applications of ICP-RIE:

- **Semiconductor Industry:** High-aspect-ratio trenches and vias for advanced integrated circuits.
- **MEMS Fabrication:** Creation of deep, precise structures in MEMS devices like accelerometers and gyroscopes.
- **Photonics:** Patterning nanostructures for waveguides and optical devices.



Schematics of an ICP-RIE machine. A high-density plasma is generated by sending a RF signal into a coil. The plasma is then injected into a separated chamber in which a second RF accelerates electrons and ions in the plasma towards the sample.

Pumps in and Main Chamber)

RIE (Load Lock

1. Load Lock Chamber Vacuum Pumps:

- **Purpose:**
The load lock chamber isolates the main processing chamber to minimize contamination and maintain vacuum integrity during wafer loading/unloading. It transitions the substrate from atmospheric pressure to the vacuum environment of the main chamber.
- **Common Vacuum Pumps:**
 - **Roughing Pumps (Mechanical Pumps):**
Used to bring the pressure from atmospheric (~760 torr) to a medium vacuum level (~ 10^{-3} torr). Rotary vane pumps are common.
 - **Turbomolecular Pumps:**
Used for finer vacuum levels (~ 10^{-6} torr). They may be employed after the roughing pump to prepare the substrate before it enters the main chamber.

2. Main Chamber Vacuum Pumps:

- **Purpose:**
Maintain a stable, ultra-low pressure environment for plasma generation and reactive ion etching.
 - **Common Vacuum Pumps:**
 - **Cryogenic Pumps:**
Capable of achieving high vacuum levels ($\sim 10^{-7}$ to 10^{-8} torr) to maintain clean and contaminant-free conditions.
 - **Turbomolecular Pumps:**
Common in RIE systems for maintaining pressures in the range of 10^{-3} to 10^{-7} torr.
 - **Backing Pumps (Dry Scroll or Rotary Pumps):**
Support turbomolecular pumps by handling the initial pressure drop from roughing levels.
-

Pressure in RIE

- **Pressure Range in Main Chamber:**
 - Typical operating pressure is **1–100 mTorr**, depending on the process requirements.
 - Low pressure (1–10 mTorr): Facilitates anisotropic etching by ensuring longer mean free paths for ions.
 - Higher pressure (>10 mTorr): Enhances chemical etching by increasing the number of collisions and reactive species.
 - **Pressure Control:**
 - Achieved using a combination of mass flow controllers (to regulate gas flow) and throttling valves (to adjust pumping rate).
 - Precise pressure control is critical for plasma stability and etch uniformity.
-

Oxygen Heating in RIE

- **Role of Oxygen (O_2):**
 - Oxygen is often used to clean residues or etch specific materials like photoresist or polymers.
 - It forms reactive oxygen species (e.g., O^+ , O^- , O , O_2^+) that chemically react with organic compounds.
 - **Oxygen Plasma Heating:**
 - Plasma itself generates heat, which can elevate substrate temperature.
 - **Substrate Heating Control:** Wafer temperature is controlled using cooling systems (e.g., helium backside cooling) to prevent overheating.
-

Plasma Control in RIE

- **Parameters for Plasma Stability:**
 1. **RF Power:** Controls ion energy for directional etching.
 2. **Gas Flow Rate:** Determines the concentration of reactive species.
 3. **Pressure:** Influences ion mean free path and etching characteristics.
 4. **Magnetic Fields (if ICP-RIE):** Used to enhance plasma density and uniformity.
 - **Real-time Monitoring:**

Optical emission spectroscopy (OES) or endpoint detection systems are often used to monitor plasma and detect process completion.
-

Lining of the Base Layer in Main Chamber

- **Purpose of Lining:**
 - Protects the chamber walls from corrosive gases and plasma damage.
 - Prevents contamination by ensuring any sputtered material from the chamber does not interfere with the process.
- **Common Lining Materials:**
 - **Alumina (Al_2O_3):** Resistant to chemical attack and plasma erosion.
 - **Quartz:** Chemically inert and used for processes requiring high purity.
 - **Anodized Aluminum:** Provides durability and resistance to plasma etching.
- **Base Layer Maintenance:**
 - Periodic cleaning or replacement of the liner is required to prevent particle contamination and maintain process consistency.

Summary Table

Aspect	Details
Vacuum Pumps (Load Lock)	Roughing pumps, turbomolecular pumps for medium to high vacuum ($\sim 10^{-6}$ torr).
Vacuum Pumps (Main Chamber)	Cryogenic, turbomolecular pumps, dry scroll pumps for ultra-low pressure.
Pressure Range	1–100 mTorr; low pressures for anisotropic etching, higher for chemical etching.
Oxygen Heating	Reactive oxygen species for residue removal or polymer etching; temperature controlled.
Plasma Control	RF power, gas flow rate, pressure, and magnetic fields for stability.
Chamber Lining	Alumina, quartz, or anodized aluminum to protect walls and ensure purity.

Fourier Optics Demonstration (30/12/2024 —Nikhil anna and Kushagra ji) ----- (most of the experimental setup was from THOR LABS and experimental procedure can also be found there.)

Fourier optics explores how optical systems can be analyzed and designed using the principles of Fourier transforms. A basic demonstration can involve a setup that shows how lenses and diffraction create Fourier transforms of an optical signal.

Basic Optical Bench for Fourier Optics Demonstration

Components:

1. **Laser Source:** Provides coherent and monochromatic light.
2. **Spatial Filter:** Cleans up the laser beam, typically consisting of a pinhole and a lens.
3. **Collimating Lens:** Produces a collimated beam of light.
4. **Object/Pattern (e.g., Slits or Transparency):** Serves as the input signal for Fourier transformation.
5. **Fourier Transform Lens:** A convex lens focuses light to create the Fourier transform of the object.
6. **Screen/Camera:** Captures the Fourier transform or intermediate optical signals.
7. **Translation Stage:** For precise alignment and positioning of components.

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7. **Translation Stage:** For precise alignment and positioning of components.

Procedure:

1. Align the laser beam using the optical bench.
2. Pass the beam through a spatial filter and collimating lens.
3. Place the object (e.g., a grid, slits, or transparency) in the path of the collimated beam.
4. Position the Fourier transform lens after the object at its focal length.
5. Place the screen at the back focal plane of the lens to observe the Fourier transform.
6. Experiment with different objects to observe how the Fourier spectrum changes (e.g., single slit, double slit, periodic gratings).

Photoluminescence (PL) Measurement

Principle:

Photoluminescence occurs when a material absorbs photons and re-emits them at a longer wavelength.

Setup Components:

1. **Excitation Source:** Often a laser or a high-intensity LED.
2. **Sample Holder:** Holds the material under study.
3. **Monochromator (Optional):** Filters the excitation light.
4. **Detector:** Measures emitted light (e.g., photodiode, spectrometer, or CCD camera).
5. **Filters:** Block scattered excitation light and allow only the emitted light to reach the detector.

Procedure:

1. Illuminate the sample with the excitation source.
2. Collect the emitted photoluminescence using a lens.
3. Use filters to block the excitation wavelength and transmit only the emitted light.
4. Detects and analyzes the emission spectrum or intensity using a spectrometer.

Aspect	Photoluminescence (PL)	Fluorescence
Mechanism	General re-emission of photons	Singlet-singlet electronic transitions
Time Scale	Can include slow processes (e.g., phosphorescence)	Fast (nanoseconds to microseconds)
Excitation Source	Laser, LED, or UV lamp	UV or visible light source
Applications	Semiconductor characterization, quantum dots	Biological imaging, sensing

Practical Considerations for Both Measurements:

1. **Excitation Wavelength:** This should match the absorption peak of the material.
2. **Alignment:** Use an optical bench for precise alignment of components.
3. **Stray Light:** Minimize by using optical filters and properly designed enclosures.
4. **Calibration:** Calibrate the detector for accurate intensity or wavelength measurements.

Working of the Detector

Optical detectors are devices used to convert light signals into electrical signals. Their working depends on the material's ability to generate a measurable electrical response when exposed to photons. Here's a breakdown of how optical detectors work:

1. Basic Principle of Photodetectors

When light (photons) strikes a photodetector:

- **Photon Absorption:** The energy of the photons excites electrons from the valence band to the conduction band, creating electron-hole pairs.
- **Charge Separation:** The detector's internal electric field separates these charges.
- **Current/Voltage Generation:** The movement of electrons and holes generates a photocurrent or voltage, which can be measured.

Avalanche Principle in Detectors

1. What is the Avalanche Effect?

The avalanche effect refers to the **impact ionization** process, where a single high-energy charge carrier (electron or hole) accelerates in a strong electric field, collides with other atoms, and generates additional charge carriers.

2. How It Works in Avalanche Photodiodes (APD):

1. **Photon Absorption:**
 - Incident photons create electron-hole pairs in the semiconductor.
2. **Electric Field Acceleration:**
 - A high reverse bias voltage generates a strong electric field in the APD.
 - The primary electron accelerates due to this field.
3. **Impact Ionization:**
 - The accelerated electron collides with the lattice atoms, generating secondary electron-hole pairs.
 - These secondary carriers are also accelerated, creating a cascade or avalanche effect.
4. **Signal Amplification:**

- This process multiplies the initial signal, amplifying the weak input signal for detection.
-

3. Advantages of Avalanche Photodiodes:

- **High Sensitivity:** Capable of detecting very weak light signals due to internal gain.
- **Fast Response:** Suitable for high-speed optical communication and time-resolved measurements.
- **Low Noise:** Compared to external amplifiers, APDs introduce less noise during amplification.

Cleanroom Day- Unknown (27/12/2024).

E-Beam Lithography (Electron Beam Lithography)

What is E-Beam Lithography?

E-Beam Lithography (EBL) is a high-resolution technique used to create nanoscale patterns on a substrate by exposing it to a focused electron beam. It is widely used in research and semiconductor fabrication for developing intricate patterns beyond the limits of traditional photolithography.

How E-Beam Lithography Works

1. Substrate Preparation:

- A substrate (e.g., silicon or glass) is coated with an electron-sensitive resist (e.g., PMMA).

2. Exposure to Electron Beam:

- A highly focused electron beam writes the desired pattern directly onto the resist.
- The interaction of the electron beam with the resist changes its solubility properties.

3. Development:

- The exposed resist is developed using a chemical solution, removing either the exposed or unexposed regions depending on the resist type (positive or negative).

4. Etching or Deposition:

- The developed pattern is transferred to the substrate through etching or material deposition.

5. Resist Removal:

- The remaining resist is stripped off, leaving the final pattern.
-

Advantages of E-Beam Lithography

1. **High Resolution:**
 - Capable of achieving feature sizes below 10 nm due to the short wavelength of electrons.
 2. **Direct Write Process:**
 - No need for masks; patterns are directly written, allowing for rapid prototyping and design flexibility.
 3. **Versatility:**
 - Can pattern various materials and create complex, arbitrary shapes.
 4. **Customizability:**
 - Ideal for research and development, where design changes are frequent.
-

Limitations of E-Beam Lithography

1. **Slow Throughput:**
 - Writing patterns is a serial process (one point at a time), making it significantly slower than photolithography for large-scale production.
 2. **High Cost:**
 - Equipment and operational costs are very high due to the complexity of electron optics and vacuum systems.
 3. **Proximity Effect:**
 - Scattered and secondary electrons can expose unintended areas, leading to pattern distortion, especially at higher densities.
 4. **Resist Sensitivity:**
 - Electron resists are less sensitive than photoresists, requiring longer exposure times.
 5. **Substrate Charging:**
 - Non-conductive substrates can accumulate charge during exposure, leading to beam deflection and patterning errors.
 6. **Depth of Focus:**
 - Depth of focus is limited, making it less suitable for uneven or thick substrates.
-

Applications of E-Beam Lithography

1. **Nanofabrication:**
 - Creating nanostructures for plasmonics, photonics, and quantum devices.
2. **Semiconductor Industry:**
 - Used in mask fabrication for extreme ultraviolet lithography (EUVL).
3. **MEMS/NEMS:**
 - Patterning micro- and nano-electromechanical systems.

Comparison with Other Lithography Techniques

Aspect	E-Beam Lithography	Photolithography
Resolution	Sub-10 nm	~40-50 nm (extreme UV)
Throughput	Slow (serial writing)	Fast (parallel exposure)
Cost	Very high	High for mask-making, lower for production.
Flexibility	Maskless, suitable for prototyping	Requires masks, suited for mass production.
Applications	Research, nanofabrication	Large-scale semiconductor manufacturing

Positive Resists (e.g., PMMA, ZEP): High resolution, good for nanoscale features but require higher doses.

Negative Resists (e.g., SU-8, ma-N): Higher sensitivity and etch resistance but lower resolution.

Dosage depends on resist type, thickness, and the desired resolution, ranging from **20 to 500 $\mu\text{C}/\text{cm}^2$** .

Electron Beam Energy:

- Higher energies (e.g., 50 keV) result in smaller beam diameters and higher resolution but can lead to proximity effects.
- Lower energies (e.g., 10 keV) reduce proximity effects but increase beam size.

Resist Thickness:

- Thicker resists require higher doses for complete exposure.

Development Process:

- Developer type and concentration affect feature resolution and line edge roughness.

Source of Electron Beam in E-Beam Lithography (EBL)

The electron beam in EBL systems is generated by an **electron gun**, which is a key component in the electron optics system. The electron gun produces a stream of electrons that are focused and steered onto the resist-coated substrate to create the desired pattern.

Types of Electron Sources Used in EBL

1. Thermionic Emission Sources

- **Principle:**
Electrons are emitted from a heated filament when the thermal energy overcomes the work function of the material.
 - **Common Materials:**
 - **Tungsten (W):** Robust and inexpensive, but has a lower brightness.
 - **Lanthanum Hexaboride (LaB₆):** Higher brightness and longer lifespan than tungsten.
 - **Advantages:**
 - Simple and cost-effective.
 - Reliable for moderate-resolution applications.
 - **Limitations:**
 - Lower brightness compared to field emission sources.
 - Broader energy spread of emitted electrons.
-

2. Field Emission Sources (FES)

- **Principle:**
Electrons are emitted via quantum tunneling from a sharp, cold cathode tip under a high electric field.
 - **Types:**
 - **Cold Field Emission (CFE):** Emits electrons at room temperature.
 - **Thermal Field Emission (TFE):** Combines field emission with slight heating to enhance stability.
 - **Common Materials:**
 - **Tungsten Tips:** Often used due to their sharpness and durability.
 - **Advantages:**
 - Extremely high brightness and small beam spot size, enabling sub-10 nm resolution.
 - Narrow energy spread improves beam focus.
 - **Limitations:**
 - Requires ultra-high vacuum (UHV) conditions.
 - More expensive and maintenance-intensive than thermionic sources.
-

3. Schottky Emission Sources

- **Principle:**
A heated tip coated with a low-work-function material (e.g., zirconium oxide) emits electrons due to thermionic and field-enhanced emission.
- **Advantages:**
 - High brightness and stability.
 - Less demanding vacuum requirements compared to CFE sources.
 - Suitable for high-resolution and long-term operation.
- **Limitations:**
 - Moderate cost and complexity compared to thermionic sources.

Source of Electron Beam in E-Beam Lithography (EBL)

The electron beam in EBL systems is generated by an **electron gun**, which is a key component in the electron optics system. The electron gun produces a stream of electrons that are focused and steered onto the resist-coated substrate to create the desired pattern.

Types of Electron Sources Used in EBL

1. Thermionic Emission Sources

- **Principle:**
Electrons are emitted from a heated filament when the thermal energy overcomes the work function of the material.
 - **Common Materials:**
 - **Tungsten (W):** Robust and inexpensive, but has a lower brightness.
 - **Lanthanum Hexaboride (LaB₆):** Higher brightness and longer lifespan than tungsten.
 - **Advantages:**
 - Simple and cost-effective.
 - Reliable for moderate-resolution applications.
 - **Limitations:**
 - Lower brightness compared to field emission sources.
 - Broader energy spread of emitted electrons.
-

2. Field Emission Sources (FES)

- **Principle:**
Electrons are emitted via quantum tunneling from a sharp, cold cathode tip under a high electric field.
- **Types:**
 - **Cold Field Emission (CFE):** Emits electrons at room temperature.
 - **Thermal Field Emission (TFE):** Combines field emission with slight heating to enhance stability.
- **Common Materials:**
 - **Tungsten Tips:** Often used due to their sharpness and durability.
- **Advantages:**
 - Extremely high brightness and small beam spot size, enabling sub-10 nm resolution.
 - Narrow energy spread improves beam focus.
- **Limitations:**
 - Requires ultra-high vacuum (UHV) conditions.
 - More expensive and maintenance-intensive than thermionic sources.

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- **Limitations:**

- Moderate cost and complexity compared to thermionic sources.
-

Components of the E-Beam Source

1. **Electron Gun:**

- Generates the electron beam (e.g., thermionic, field, or Schottky emission).

2. **Anode:**

- Accelerates the electrons, determining their energy (typically 10-50 keV for EBL).

3. **Electromagnetic Lenses:**

- Focus the electron beam to a fine spot size, crucial for high-resolution patterning.

4. **Deflectors:**

- Steer the electron beam to write patterns directly on the resist without mechanical movement.

5. **Apertures:**

- Limit the beam size and remove stray electrons, enhancing resolution.
-

Lab Report: SEM, TEM, and XRD Observations with Advantages and Disadvantages

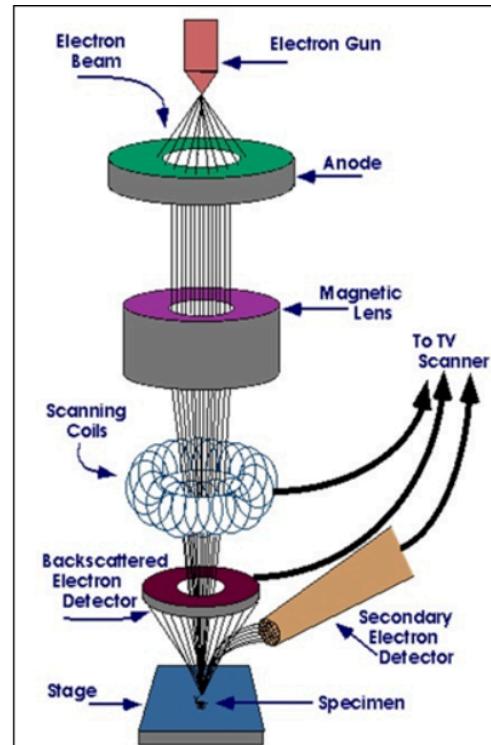
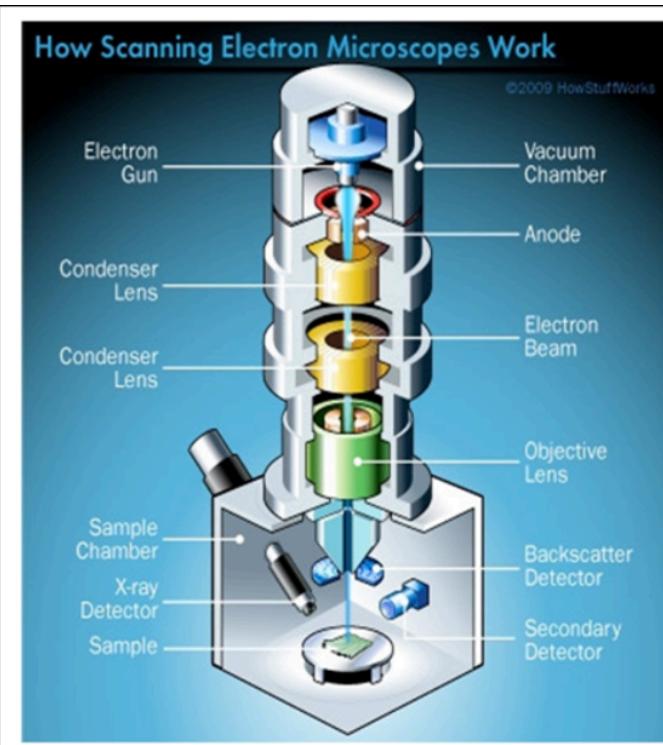
1. Scanning Electron Microscope (SEM) —(TA- Arkya Ji)

Key Observations:

- Depth analysis capability: Up to **2.5 nm**, depending on material properties.
- **Tilted Holder:** A **70° holder** is used for cross-sectional imaging.
- **Sample Mounts:** Utilizes **32 mm stubs** and **12 mm stubs** for sample placement.
- **Sample Conductivity:** Samples must be conductive to avoid charge accumulation during scanning.

- **Challenges:**

- **Wobbling:** Imaging instability due to mechanical or electrical inconsistencies.
- **Stigmation:** Aberrations in the electron beam causing distorted images.



Key Parameters:

- **Accelerating Voltage:** Controls electron beam energy.
- **Probe Current:** Determines the density of electrons in the beam.

Spot Size:

- Larger spot sizes and higher probe currents are needed for elemental analysis.

Beam Energy:

- Higher energy requires a longer path to focus but allows deeper penetration.
- A **dense electron beam** provides higher resolution.

Modes of Operation:

- **FE-SEM:** Generates the electron beam using the **Schottky effect**.
- **Ion Milling:** Can also be achieved for sample preparation.

Demonstration:

- **Gold Nanocubes:** Surface analysis and elemental composition were performed.
- **Graphical Representation:** Peaks in the photo vs. element type graph indicate element concentrations.

Working Principle:

- Primary electrons bombard the sample, ejecting **secondary electrons**. Image intensity depends on the intensity of collected electrons.

Advantages:

1. High-resolution surface imaging (up to 1-2 nm).
2. Capable of elemental analysis using EDS.
3. Easy to use for a variety of sample types (with proper preparation).

Disadvantages:

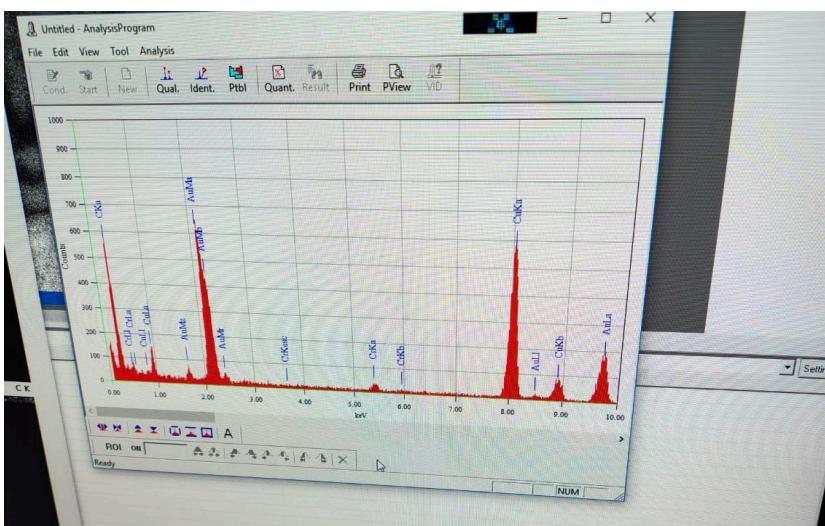
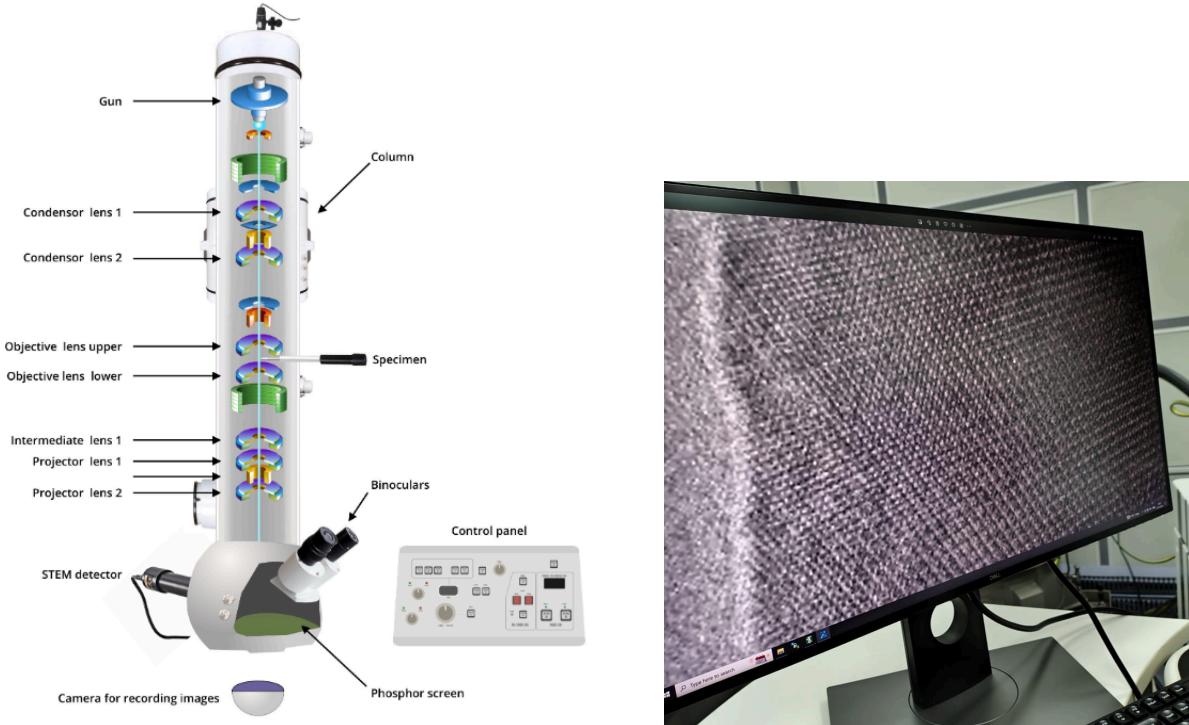
1. Limited to surface analysis; cannot probe internal structures.
2. Requires conductive samples or coating for non-conductive materials.
3. Image quality can be affected by wobbling and stigmation.

2. Transmission Electron Microscope (TEM)

Key Observations:

- **Principle:** Transmitted **primary electrons** are collected to form an image.

- **Magnification:** Achieves up to **10,00,000x - 20,00,000x**, far exceeding SEM.
- **Modes of Operation:**
 - **Scanning Mode:** For detailed imaging of small areas.
 - **Capture Mode:** For static image acquisition.



Demonstration:

- **Gold Nanofoil:** Composition analysis was conducted. Software-generated images showed the concentration distribution of individual elements.
- **Diffraction Patterns:** Observed due to atomic arrangements, providing crystallographic information.

Applications:

- Capable of both **bulk** and **surface analysis**.

Advantages:

1. Atomic-level resolution (sub-nm).
2. Provides detailed internal structure and defect analysis.
3. Diffraction patterns enable crystallographic studies.

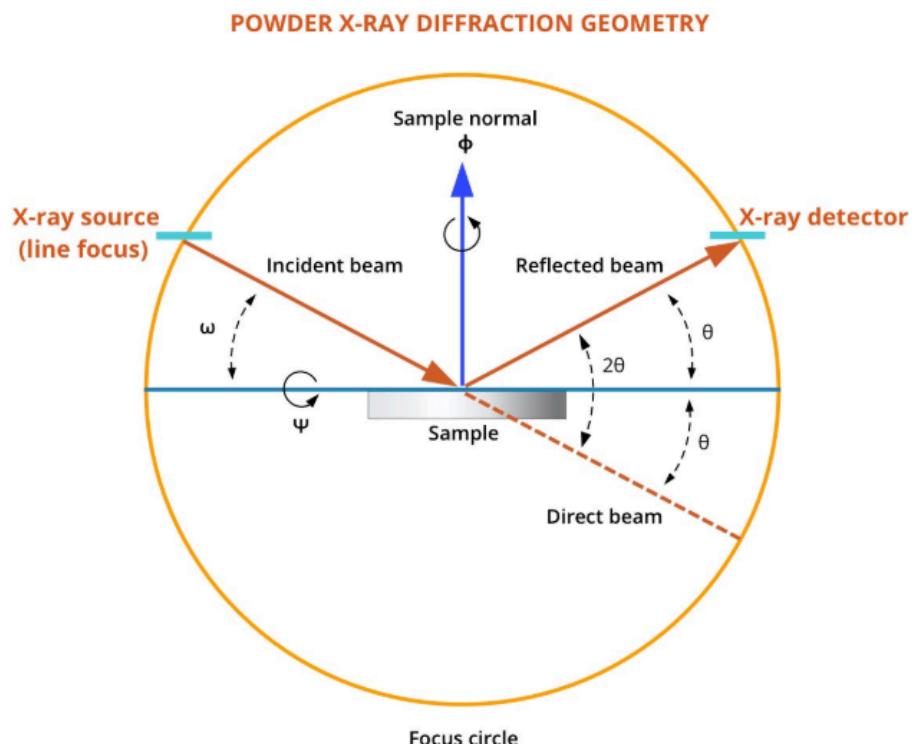
Disadvantages:

1. Extremely expensive and complex to operate.
 2. Sample preparation is time-consuming and requires ultra-thin specimens.
 3. High vacuum conditions limit certain material analyses.
-

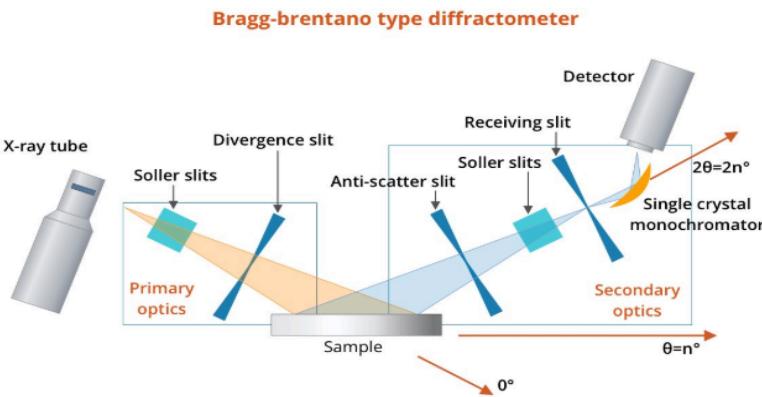
3. X-Ray Diffraction (XRD)

Key Observations:

- X-ray wavelength: **0.01 to 100 nm**, suitable for sub-micrometer feature analysis.
- **θ - 2θ Geometry**: Source rotates by θ , and detector by 2θ for precise measurements.
- **Bragg's Law**: $n\lambda = d \sin \theta_n$. This relates wavelength (λ), interatomic distance (d), and diffraction angle (θ_n).



Applications:



- Crystal structure, phase composition, and lattice constant analysis.

Advantages:

1. Non-destructive and fast analysis.
2. Provides detailed crystallographic information.
3. Effective for bulk material analysis.

Disadvantages:

1. Cannot resolve surface features or internal defects.
2. Requires crystalline samples for accurate diffraction.
3. Limited resolution compared to SEM or TEM.

Feature	XRD (X-Ray Diffraction)	SEM (Scanning Electron Microscope)	TEM (Transmission Electron Microscope)
Purpose	Crystallographic structure determination	Surface morphology analysis	Internal structure at atomic resolution
Working Principle	Diffraction of X-rays by crystal planes	Electron beam scans surface, detecting signals	Electron beam passes through the sample, producing high-res images
Resolution	Limited to crystal lattice spacing (micron to sub-nm)	Up to 1 nm	Sub-nm, atomic resolution
Dimensional Analysis	Bulk, polycrystalline analysis	2D surface analysis	2D internal structure
Sample Requirements	Crystalline samples, powders	Conductive or coated samples	Ultra-thin samples (typically <100 nm thick)
Quantitative Analysis	Yes (phase identification, lattice constants)	Limited (elemental using EDS, semi-quantitative)	Yes (structural and compositional analysis)
Speed	Rapid for phase identification	Medium	Time-intensive due to sample prep and analysis
Cost and Complexity	Moderate cost; relatively simpler setup	Higher cost; intermediate complexity	Very high cost; complex setup
Key Applications	Crystal structure, phase analysis	Surface topography, grain size analysis	Defect structure, dislocations, atomic-level imaging

Report : TAIWAN PROFESSOR'S LECTURES

Title: "Lecture on Development and Future Trends of 3D-IC Packaging Technology"

Overview: On December 18, 2024, IIT Hyderabad hosted the first day of lectures under the SPARC Program as part of the Indo-Taiwan/US Collaborative Workforce Development Program in Semiconductor Manufacturing (Phase 2). Professor Chang Chun Lee from the Department of Power Mechanical Engineering, NTHU, Taiwan, delivered a session focusing on the evolution, advancements, and future directions of 3D-IC packaging technology. The lecture emphasized the critical role of packaging technologies in enhancing device performance, integration, and functionality in the semiconductor industry.

Key Topics Covered:

1. Fab-Out Packaging

- Current development status and future prospects.

2. 3D-IC Packaging

- TSV (Through Silicon Via) and microbump technologies.
- Bonding methodologies: chip-to-wafer and wafer-to-wafer.

3. 2.5D Packaging

- CoWoS (Chip on Wafer on Substrate).

4. Heterogeneous Integrated Packaging

- Key technologies and development trends.

5. Advanced Packaging Techniques:

- InFO (Integrated Fan-Out).
- Surface Mounting Technology (SMT).
- Small Outline Package (SOP) and Quad Flat Package (QFP).
- TSOP (Thin Small Outline Package) and BGA (Ball Grid Array).
- Flip Chip Bumping and Flip Chip BGA Packaging.

6. Patents Impacting Semiconductor Packaging:

- Fan-out package-level designs.
- Redistributed Layer (RDL) and Package-on-Package (PoP) technologies.

7. Vehicle Design and Analysis:

- Applications in 3D-IC packaging systems.
-

Key Learnings:

1. Emerging Trends:

- TSV and microbump technologies are pivotal in achieving higher density and integration.
- Advancements in bonding techniques, such as wafer-to-wafer bonding, are improving packaging reliability.
- CoWoS and InFO are setting new benchmarks in 2.5D and fan-out packaging solutions.

2. Technological Innovations:

- Redistributed Layers (RDL) enhance signal routing and electrical performance.
- Package-on-Package (PoP) is becoming increasingly popular for multi-die integration.

3. Industry Focus:

- The convergence of patents with new packaging technologies highlights a shift towards compact, high-performance semiconductor solutions.
-

Important Keywords:

TSV, Microbump, Wafer Bonding, CoWoS, InFO, SMT, SOP, QFP, TSOP, BGA, Flip Chip, RDL, PoP.

Conclusion: The lecture by Professor Chang Chun Lee illuminated the rapid advancements in 3D-IC packaging technologies and their transformative potential in the semiconductor industry. Attendees gained valuable insights into cutting-edge technologies, including TSV, microbump, and fan-out packaging methods, as well as their practical applications. These advancements prepare professionals and researchers for future innovations in the field, emphasizing the importance of integration, reliability, and high performance in packaging technologies.

Title: Lecture on “Manufacturing Processes of Advanced Nanodevices”

On December 19, 2024, IIT Hyderabad hosted the second day of lecture under the SPARC Program as part of the Indo-Taiwan/US Collaborative Workforce Development Program in Semiconductor Manufacturing (Phase 2).

The session was delivered by Professor Tsung-Chieh Cheng from the Department of Mechanical Engineering, National Kaohsiung University of Science and Technology, Taiwan.

Overview

The lecture delved into the intricate processes underlying the manufacturing of advanced nanodevices, emphasizing the historical evolution, technological advancements, and the meticulous fabrication methods required to create modern semiconductor devices.

Key Topics

1. Historical Developments in Electronics and Semiconductors

- Early innovations such as Vacuum Tubes, the ENIAC computer, and the first transistor from Bell Laboratories.
- The evolution and importance of integrated circuits (ICs).

2. Wafer Fabrication and IC Manufacturing

- Overview of wafer size evolution and the critical role of cleanroom and sub-fabrication facilities.
- Detailed explanation of stages of IC fabrication, including wafer-level packaging and process flow diagrams.

3. Advanced Semiconductor Processes

- Concepts such as Moore's Law, Gate All Around (GAA) technology, MOSFET (NMOS), and FinFETs.
- Basic semiconductor processes, including crystal growth, ingot processing, and thermal SiO₂ oxidation.

4. Oxidation Techniques

- Types of oxidation processes: dry oxidation and wet thermal oxidation.
- Key equipment like vertical and horizontal tube furnaces.
- Specialized processes like local oxidation of silicon (STI process).

5. Photolithography

- Evolution of photolithography and its role in IC manufacturing.
 - Steps involved: resist spin coating, mask overlay accuracy, and alignment masks.
 - Key concepts: resolution of lithography, SEM (Scanning Electron Microscope), and the lift-off process.
-

Key Learnings

1. Technological Evolution

From vacuum tubes to advanced transistors, the lecture traced the path of innovation in electronic devices.

2. Fabrication Processes

The complexity of manufacturing advanced ICs through processes like photolithography, thermal oxidation, and crystal growth was thoroughly explored.

3. Future-Oriented Technologies

Emerging technologies such as Gate All Around transistors and FinFETs signify the direction of semiconductor advancements.

4. Precision and Accuracy in Fabrication

Processes like mask alignment, resolution control, and thermal oxidation highlight the need for precision in nanodevice manufacturing.

Important Keywords:

1. Vacuum Tubes
 2. ENIAC
 3. Gate All Around (GAA)
 4. FinFET
 5. Photolithography
 6. Thermal Oxidation
 7. SEM
 8. IC Fabrication
-

Conclusion:

Prof. Cheng's lecture provided an in-depth exploration of the processes and technologies critical to the manufacturing of advanced nanodevices. By combining historical insights with modern advancements, the session highlighted how innovations in materials science, precision engineering, and semiconductor processes continue to shape the future of nanotechnology. This knowledge is invaluable for researchers, students, and professionals in the field, offering a robust understanding of both the challenges and opportunities in nanodevice fabrication.

Title: Lecture on "The Trends of Advanced Heterogeneous Integrated (HI) Packaging"

Event Details:

- **Date:** December 20, 2024
- **Venue:** IIT Hyderabad
- **Program:** SPARC Program, Indo-Taiwan/US Collaborative Workforce Development Program in Semiconductor Manufacturing (Phase 2)

- **Speaker:** Professor Menkai Shih, Department of Mechanical and Electro-Mechanical Engineering, National Taiwan University of Science and Technology (NSUT Taiwan)

Objective: To gain insights into the advancements, challenges, and solutions in Heterogeneous Integrated (HI) Packaging technologies within the field of semiconductor manufacturing.

Introduction: Heterogeneous Integrated (HI) Packaging plays a pivotal role in modern semiconductor manufacturing by enabling efficient electrical connections, thermal dissipation, and mechanical protection of semiconductor devices. Professor Menkai Shih's lecture provided an in-depth exploration of the emerging trends and challenges in HI Packaging, including innovations such as wafer-level chip scale packaging (WLCSP) and system-in-package (SiP) technologies.

Key Topics Covered:

1. **Importance of Packaging:**
 - **Mechanical Protection:** Safeguards semiconductor components from physical damage.
 - **Electrical Interconnections:** Ensures efficient signal transmission.
 - **Thermal Dissipation:** Facilitates heat management to enhance device reliability and performance.
2. **Types of Advanced Packaging:**
 - **WLCSP (Wafer-Level Chip Scale Package):** Reduces size and improves electrical performance. However, thermal and mechanical challenges remain.
 - **2D, 2.5D, and 3D Architectures:**
 - **2D:** Traditional planar designs.
 - **2.5D:** Horizontal integration using interposers like Intel's Embedded Multi-die Interconnect Bridge (EMIB).
 - **3D:** Vertical stacking for higher performance and space efficiency.
3. **Drivers of Advanced Packaging:**
 - Increasing demand for high performance and miniaturization.
 - Integration of diverse components in a single package.
 - Necessity for enhanced thermal and mechanical reliability.
4. **Heterogeneous Integration Solutions:**
 - **Fan-Out Embedded Bridge (SPIL):** Supports high-density interconnections and cost efficiency.
 - **Intel's EMIB:** Enables high-speed communication between dies.
 - **Flip Chip Hybrid Solutions (e.g., SESUB, aEASI):** Improve integration and thermal management capabilities.
5. **Thermal Management Challenges:**
 - Modes of heat transfer (conduction, convection, radiation) are critical to device reliability.
 - Addressing thermal resistance and optimizing conductivity are essential for sustaining performance.

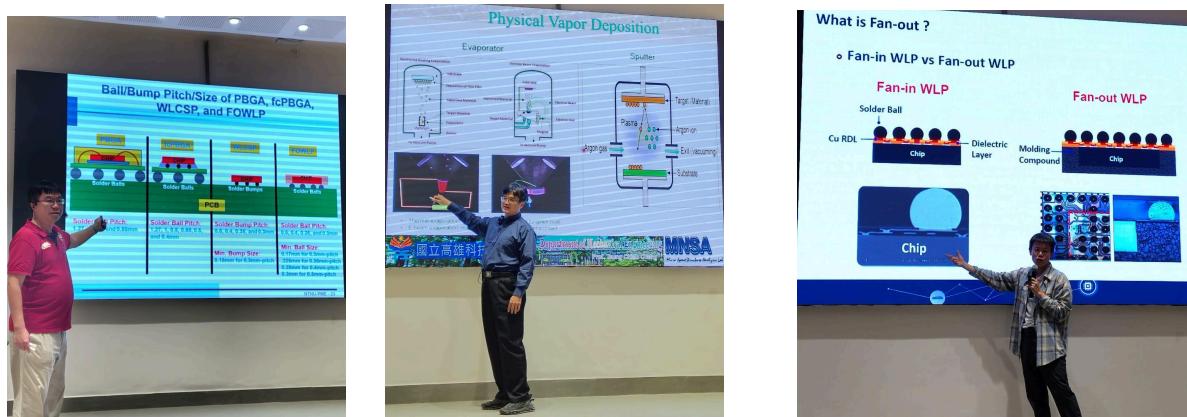
Key Learnings:

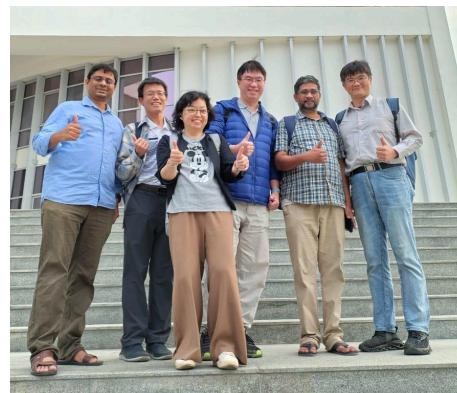
- **WLCSP (Wafer-Level Chip Scale Package):** Provides a compact form factor and improved signal integrity but demands solutions for thermal and mechanical stress.
- **BLRT (Board-Level Reliability Testing):** Assesses the durability of packages under thermal cycling and mechanical stresses.
- **Intel's EMIB:** A cost-effective approach for high-speed die communication.
- **Fan-Out Packaging:** Increases connection density while maintaining compactness.
- **Thermal Management Techniques:** Essential for ensuring device reliability through optimized conduction, convection, and radiation processes.

Discussion: The lecture emphasized the critical role of interdisciplinary collaboration in advancing HI packaging technologies. The integration of diverse components and the development of innovative solutions to challenges such as thermal management and board-level reliability are essential for meeting the growing demands of semiconductor applications.

Conclusion: Professor Menkai Shih highlighted the significance of global collaboration in semiconductor manufacturing and the importance of interdisciplinary approaches to address challenges in HI packaging. Advancements in HI packaging technologies, such as WLCSP and EMIB, are paving the way for next-generation semiconductor devices, but continued innovation and collaboration are required to overcome existing challenges.

References: Lecture content delivered by Professor Menkai Shih during the SPARC Program session on December 20, 2024.





CV Characteristics of an MOS Capacitor

Title: Capacitance-Voltage (C-V) Characteristics of a Metal-Oxide-Semiconductor (MOS) Capacitor

Experimental Setup

Instruments Used:

1. Semiconductor Device Analyzer
 2. Probe Station
-

Theory

A MOS capacitor's C-V characteristics are determined by the behavior of charge carriers in the semiconductor substrate under an applied voltage. The three main regions of operation are:

1. Accumulation Region:

- **Condition:** Negative gate voltage (for a p-type substrate).
- **Mechanism:** Holes accumulate at the semiconductor-oxide interface.
- **Capacitance Behavior:** The capacitance is at its maximum value and is equal to the oxide capacitance, C_{ox} .
- **Capacitance Formula:** $C = \epsilon_{ox} A / t_{ox}$

where:

- ϵ_{ox} : Permittivity of the oxide layer
- A: Area of the capacitor
- t_{ox} : Thickness of the oxide layer

2. Depletion Region:

- **Condition:** Small positive gate voltage (for a p-type substrate).
- **Mechanism:** Holes are repelled from the interface, leaving behind immobile ionized acceptor atoms, creating a depletion layer.
- **Capacitance Behavior:** The capacitance decreases as the depletion layer width increases.
- **Capacitance Formula:** $C = \epsilon_s A / W$

where:

- ϵ_s : Permittivity of the semiconductor
- W: Width of the depletion region

3. Inversion Region:

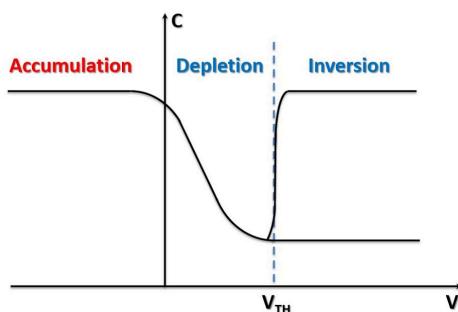
- **Condition:** Large positive gate voltage (for a p-type substrate).
 - **Mechanism:** Inversion occurs as electrons accumulate at the semiconductor-oxide interface, forming an inversion layer.
 - **Capacitance Behavior:**
 - **High Frequency:** The capacitance stabilizes at the oxide capacitance value due to the inability of minority carriers to respond to high-frequency signals.
 - **Low Frequency:** The capacitance appears to rise back to a value similar to the accumulation region due to minority carrier generation and recombination.
-

Experimental Procedure

1. The MOS capacitor was placed on the probe station.
 2. The gate voltage was varied from a negative value to a positive value using the Semiconductor Device Analyzer.
 3. Capacitance measurements were recorded at both high and low frequencies.
-

Results and Observations

C-V Graph:



Capacitance Values:

- **Accumulation Region:** Maximum capacitance = C_{ox}
 - **Depletion Region:** Capacitance decreases with voltage.
 - **Inversion Region:**
 - High Frequency: Capacitance stabilizes at a lower value.
 - Low Frequency: Capacitance increases toward C_{ox} .
 -
-

Discussion

- In the accumulation region, the capacitor behaves like a parallel-plate capacitor with $C=C_{ox}$.
 - In the depletion region, the capacitance decreases due to the widening of the depletion layer, which increases the effective separation between charges.
 - In the inversion region, the behavior of the capacitance depends on the signal frequency.
 - The high-frequency response is dominated by the fixed oxide capacitance, while the low-frequency response considers minority carrier dynamics.
-

Conclusion

The C-V characteristics of the MOS capacitor were successfully measured using the Semiconductor Device Analyzer and Probe Station. The experiment demonstrated the dependence of capacitance on gate voltage and frequency, which is critical for understanding the electrical properties of MOS devices.