11/9/24, 8:01 AM about:blank

## ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Session: UG, Semester V W. E. F.: 22-07-2024

2024-25

Format: Course Code (Type) | Section (Batch) | Class Room (Faculty)

Days/TimeSlots	08:00- 08:55AM	09:00- 09:55AM	10:00- 10:55AM	11:00- 11:55AM	12:00- 12:55PM	01:00- 01:55PM	02:00- 02:55PM	03:00- 03:55PM	04:00- 04:55PM	05:00- 05:55PM	06:00- 06:55PN
						22ECT302 (P) UG3EC-E5 VLSIDSL (BC)	22ECT302 (P) UG3EC-E5 VLSIDSL (BC)				
Monday	22ECT201 (L) UG3EC-ALL VLTC-L208 (ANK)	(L) UG3EC-ALL UG	22ECT302 (L) UG3EC-ALL VLTC-L208 (BC)	22ECT301 (L) UG3EC-ALL VLTC-L208 (RPY)		22ECP309 (P) UG3EC-E2 DEML (RAB) 22ECT301 (P) UG3EC-E1 Antenna Lab (RPY)	22ECP309 (P) UG3EC-E2 DEML (RAB) 22ECT301 (P) UG3EC-E1 Antenna Lab (RPY)	21ECT839 (L) UG3EC-ALL VLTC-L208 (LB)	21ECT000 (L) UG3EC-ALL VLTC-L208 (VS)		
						22ECP308 (P) UG3EC-E4 ES Lab (VS)	22ECP308 (P) UG3EC-E4 ES Lab (VS)				
	22ECT203 (L)	22ECT201 (L)	22ECT303 (L)	22ECT301 (L)		(P) UG3EC-E1 VLSIDSL (BC) 22ECP309 (P) UG3EC-E3 DEML	(P) UG3EC-E1 VLSIDSL (BC) 22ECP309 (P) UG3EC-E3 DEML	21ECT839 (L)	21ECT000 (L)		
Tuesday	UG3EC-ALL VLTC-L208 (REE)	UG3EC-ALL VLTC-L208 (ANK)	UG3EC-ALL VLTC-L208 (AMJ)	UG3EC-ALL VLTC-L208 (RPY)		(RAB) 22ECT301 (P) UG3EC-E2 Antenna Lab (MMS)	(RAB) 22ECT301 (P) UG3EC-E2 Antenna Lab (MMS)	VLTC-L208 (LB)	VLTC-L208 (VS)		
						22ECP308 (P) UG3EC-E5 ES Lab (LB)	22ECP308 (P) UG3EC-E5 ES Lab (LB)				
Wednesday	22ECT304 (L) UG3EC-ALL VLTC-L208 (RAB)	22ECT203 (L) UG3EC-ALL VLTC-L208 (REE)	21ECT871 (L) UG3EC-ALL VLTC-L208 (M)	22ECT301 (L) UG3EC-ALL VLTC-L208 (RPY)		22ECT302 (P) UG3EC-E2 VLSIDSL (BC)	22ECT302 (P) UG3EC-E2 VLSIDSL (BC)			22ECT302 (L) UG3EC-ALL VLTC-L208 (BC)	
						22ECP309 (P) UG3EC-E4 DEML (RAB)	22ECP309 (P) UG3EC-E4 DEML (RAB)				
						22ECT301 (P) UG3EC-E3 Antenna Lab (REE)	22ECT301 (P) UG3EC-E3 Antenna Lab (REE)				

about:blank 1/3

11/9/24, 8:01 AM about:blank

3/24, 0.01 AW						about.bic					
Days/TimeSlots	08:00- 08:55AM	09:00- 09:55AM	10:00- 10:55AM	11:00- 11:55AM	12:00- 12:55PM	01:00- 01:55PM	02:00- 02:55PM	03:00- 03:55PM	04:00- 04:55PM	05:00- 05:55PM	06:00- 06:55PN
						22ECP308 (P) UG3EC-E1 ES Lab (AMJ) 22ECT302 (P) UG3EC-E3	22ECP308 (P) UG3EC-E1 ES Lab (AMJ) 22ECT302 (P) UG3EC-E3				
Thursday	22ECT201 22ECT303 21ECT871 (L) (L) (L) UG3EC-ALL VLTC-L208 (ANK) (AMJ) (M)	(L) UG3EC-ALL U- VLTC-L208 V	(L) UG3EC-ALL VLTC-L208	22ECT304 (L) UG3EC-ALL VLTC-L208 (RAB)		VLSIDSL (BC) 22ECP309 (P) UG3EC-E5 DEML (RAB) 22ECT301 (P)	VLSIDSL (BC) 22ECP309 (P) UG3EC-E5 DEML (RAB) 22ECT301 (P)	21ECT839 (L) UG3EC-ALL VLTC-L208 (LB)	21ECT000 (L) UG3EC-ALL VLTC-L208 (VS)		
		(RAD)		UG3EC-E4 Antenna Lab (RPY) 22ECP308 (P) UG3EC-E2 ES Lab (LB)	UG3EC-E4 Antenna Lab (RPY) 22ECP308 (P) UG3EC-E2						
Friday					22ECT302 (P) UG3EC-E4 VLSIDSL (BC)	ES Lab (LB)  22ECT302 (P)  UG3EC-E4  VLSIDSL (BC)					
	22ECT203 (L) UG3EC-ALL VLTC-L208 (REE)	21ECT871 (L) UG3EC-ALL VLTC-L208 (M)	22ECT303 (L) UG3EC-ALL VLTC-L208 (AMJ)	22ECT302 (L) UG3EC-ALL VLTC-L208 (BC)		(P) UG3EC-E1 DEML (RAB) 22ECT301 (P) UG3EC-E5 Antenna	(P) UG3EC-E1 DEML (RAB) 22ECT301 (P) UG3EC-E5 Antenna				
						Lab (RPY) 22ECP308 (P) UG3EC-E3 ES Lab (AMJ)	Lab (RPY) 22ECP308 (P) UG3EC-E3 ES Lab (AMJ)				
Saturday											
Sunday											

#	Course Code	Course Name	Course Structure L-T-P-S	
1	21ECT000	CAD Algorithm for VLSI Physical Design	3-0-0-0	
2	21ECT839	CAD Algorithm for Synthesis of VLSI System	3-0-0-0	

#	Faculty Code	Faculty Name
1	AMJ	Dr. AMIT MAHESH JOSHI
2	ANK	Dr. Ankit
3	ВС	Dr. BHARAT CHOUDHARY
4	М	Dr. MENKA
5	RAB	Dr. RAKESH BAIRATHI
6	REE	Dr. Reena Kumari

#	Classroom Code	Classroom Name				
1	DEML	Digital Electronics & Microprocessor Lab				
2	ES Lab	Embedded System and IoT Lab				
3	Antenna Lab	Microwave Antenna and Communication Lab				
4	VLSIDSL	VLSI Design and Simulation Lab				

11/9/24, 8:01 AM

Course

21ECT871

22ECP308

22ECP309

22ECT201

22ECT203

22ECT301

22ECT302

10 22ECT303

11 22ECT304

6

**Course Name** 

VLSI Testing &

**Embedded Systems** 

Microprocessors Lab

Digital Logic Design

Communication

Antenna & Wave

Digital CMOS IC

Microprocessors

Embedded Systems

Propagation

(M2)

Testability

Design Lab

Code

Course

3-0-0-0

0-0-2-0

0-0-2-0

3-0-0-0

3-0-0-0

3-0-2-0

3-0-2-0

3-0-0-0

3-0-0-0

Structure L-T-P-S

## about:blank

		about:blank
#	Faculty Code	Faculty Name
7	LB	Prof. LAVA BHARGAVA
8	MMS	Prof. M. M. SHARMA
9	RPY	Prof. R. P. YADAV
10	VS	Prof. VINEET SAHULA

#	Classroom Code	Classroom Name
5	VLTC-L208	VLTC-L208

## Cordinator - Time Table

Head of the Department

about:blank 3/3