EFM32
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Hardware Design Considerations

AN0002 - Application Note

Introduction

This application note is intended for system designers who require an overview of the hardware design considerations for the EFM32. Topics that are covered specifically are how to provide a robust supply power to the chip, connection to the debug interface and external clock sources.

Hardware reference designs for the various EFM32 devices are also included.

This application note includes:

- This PDF document
- Reference Design (zip)
  - OrCAD schematic design files
  - PDF Schematics
  - Symbol libraries (OrCad, CSV and Edif formats)

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

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1 Power Supply

1.1 Introduction

Even though the EFM32 supports a wide voltage range and has an exceptionally small average current consumption, proper decoupling is crucial. As for all digital circuits, current is drawn in short pulses occurring on the clock edges. Particularly when several I/O lines are switching simultaneously, current pulses on the power supply lines can be in the order of several hundred mA. If the I/O lines are not loaded the pulse width may be only a few ns. Therefore, even if the average current consumption of the EFM32 is very small, the current drawn during short pulses can be considerable.

Such kind of current spikes cannot be properly delivered over long power supply lines without introducing considerable noise in the supply voltage. This noise is reduced by using decoupling capacitors which act as supplementing current sources during these short transients.

1.2 Power Supply Decoupling

All power pins must be connected to external decoupling capacitors. Different topologies have different performance in terms of component cost and supply noise suppression. In the following subsections one standard and one improved topology are presented. The first is favorable due to its low component cost, whereas the second has better supply noise suppression. The latter is relevant for example when higher ADC accuracy is required.

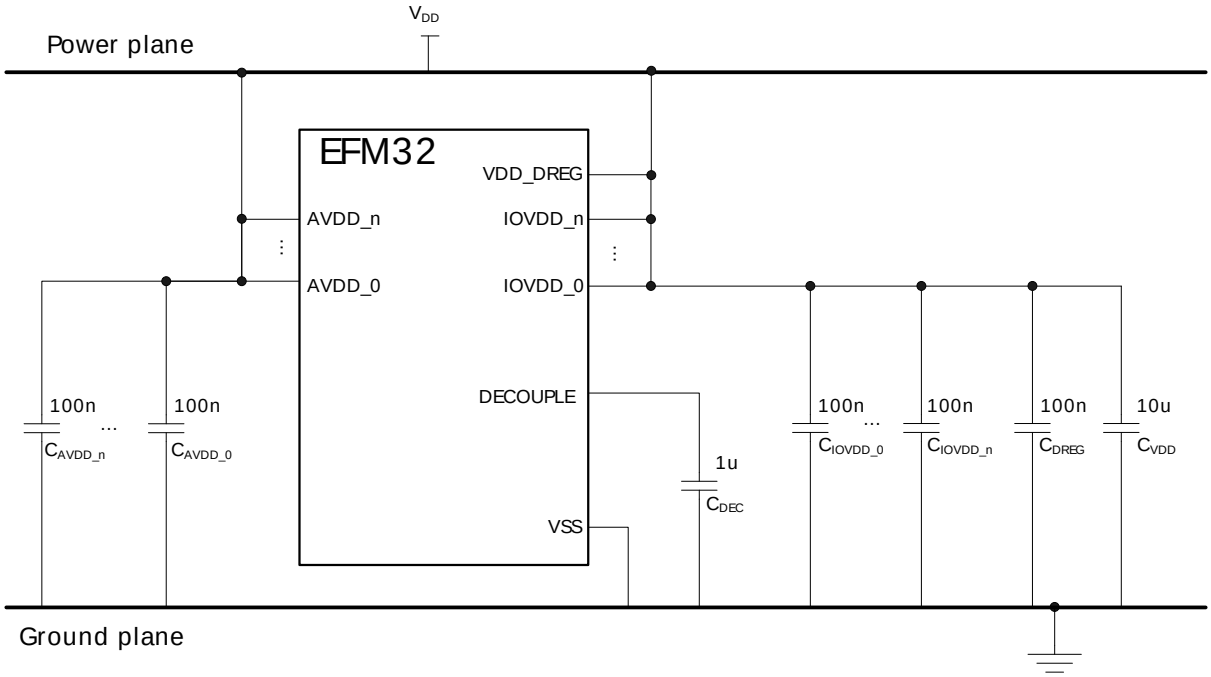
Decoupling capacitors make the current loop between supply, MCU and ground as short as possible for high frequency transients. Therefore all decoupling capacitors should be placed as close as possible to each of their respective power supply pin and ground pin and PCB (Printed Circuit Board) ground plane.

All external decoupling capacitors should have a temperature range reflecting the environment in which the EFM32 should be used. Ceramic capacitors with X5R material with a change in capacitance of ±15% over the temperature range -55°C - +85°C would be a good choice covering the entire operating temperature range of the EFM32 with a reasonable accuracy.

1.2.1 Standard Decoupling

In Figure 1.1 (p. 3) a standard approach for decoupling is illustrated.

Figure 1.1. Power supply



The topology consists of one large common capacitor (C_{VDD}) of around 10 µF along with one 100nF capacitor for each power pin (C_{AVDD_i}, C_{IOVDD_i} and C_{DREG}).

This topology is attractive since it simple and utilizes few components, while the noise suppression performance is sufficient for many applications.

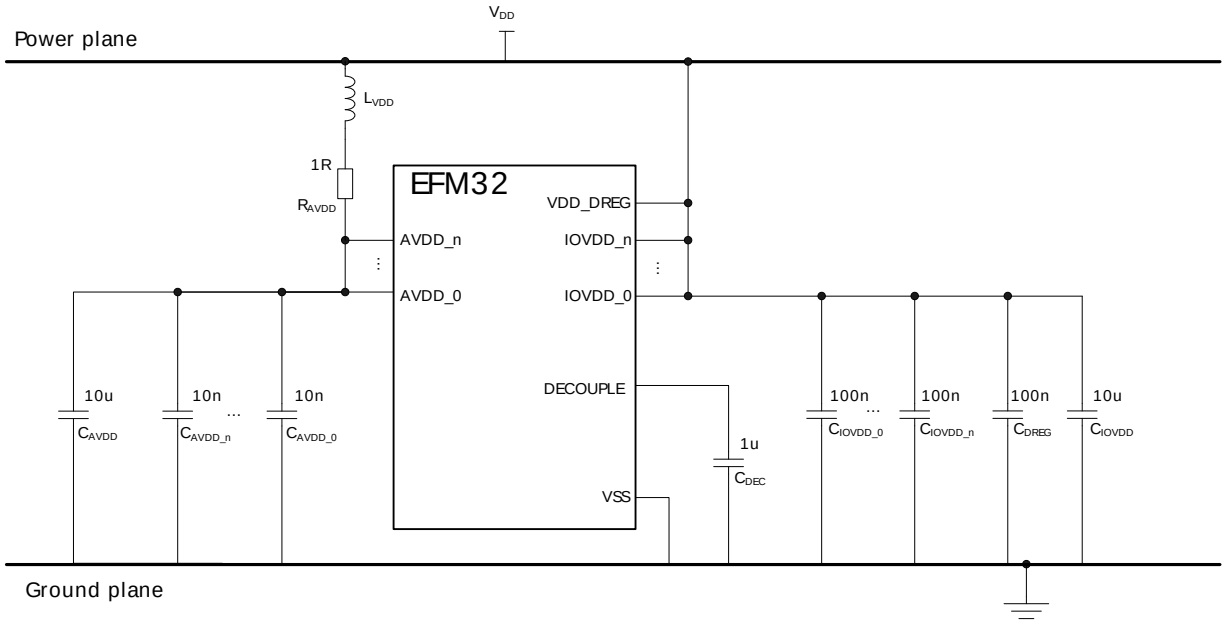
Note

The number of analog power pins (AVDD_n), I/O power pins (IOVDD_n) and ground pins (VSS) depend on the device package. Please refer to the device datasheet for package and pinout information.

1.2.2 Decoupling With Improved Supply Noise Suppression

In Figure 1.2 (p. 4) a decoupling approach providing better noise suppression and isolation between the digital and analog power pins is illustrated. This topology is a good alternative when for example higher ADC accuracy is required.

Figure 1.2. Power supply



The topology separates the analog and the digital power domain by using an inductor and a resistor in addition to the capacitors.

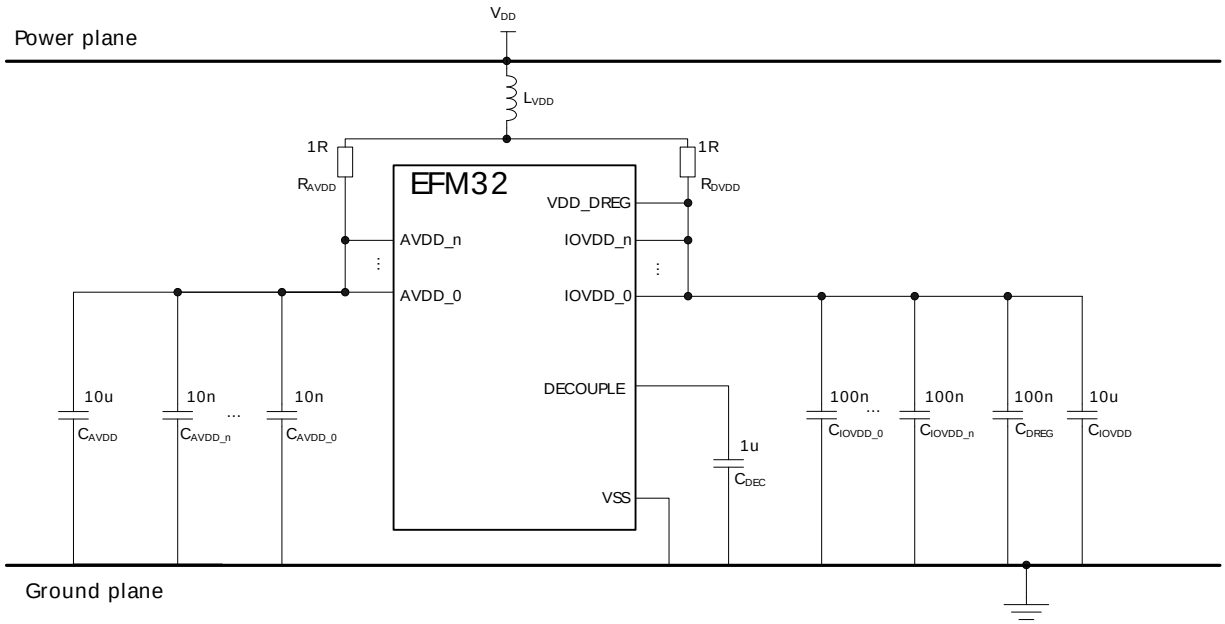
The inductor gives a relatively high impedance path between the power plane and the analog power pins during current pulses, effectively reducing the noise in the power plane. Evidently, the series resistance of the inductor must be so small that it does not give a significant DC voltage drop (An EMI/RFI suppressor similar to BLM21B102S could be a good choice for L_{VDD}).

The resistor is also inserted in order to improve the isolation between the power domains. The resistor value should be small in order to prevent a high DC drop, on the other hand it should offer some isolation. A value of 1 Ohm is a good trade-off.

Both domains should have a large common capacitor (C_{IOVDD} and C_{AVDD}) of around 10 µF, in addition to one capacitor per power pin. For the digital domain, the capacitors (C_{IOVDD_i}) can be around 100 nF, whereas for the analog domain the capacitors (C_{AVDD_i}) should be 10 nF.

During power-on, the AVDD_x pins must not be powered up after the IOVDD_x and VDD_DREG pins. If the rise time of the power supply is short, the filter in Figure 1.2 (p. 4) can cause a significant delay on the AVDD_x pins. Therefore, the topology in Figure 1.2 (p. 4) should not be used if the internal resistance of the power supply is less than 7 Ohm. If the power supply has a smaller internal resistance than 7 Ohm, the topology in Figure 1.3 (p. 5) should be used instead.

Figure 1.3. Power supply



1.2.3 DECOUPLE Pin

This pin is to provide external decoupling to the internal regulated supply power. This capacitor, C_{DEC}, (ref. Figure 1.1 (p. 3)) should be in the order of 1 µF to filter transients from this power domain.

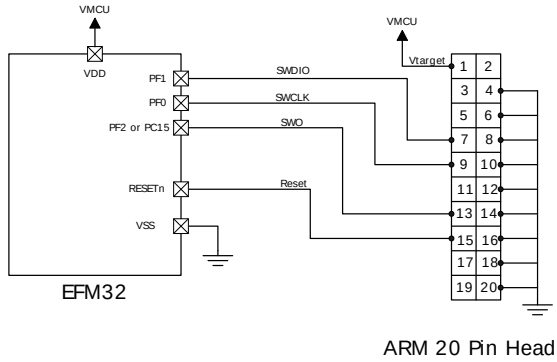
2 Debug Interface and External Reset Pin

2.1 Debug Interface

The debug interface basically consists of the SWCLK (clock input) and SWDIO (data in/out) lines, in addition to the optional SWO (serial wire output). The SWO line is for example used for instrumentation trace and program counter sampling, and is not needed for programming and normal debugging. However, it can be valuable in advanced debugging scenarios, and it is therefore recommended to include this line in a design.

The connection to an ARM 20 pin debug connector is shown in Figure 2.1 (p. 6) . Pins with no connection should be left unconnected.

Figure 2.1. Connecting the EFM32 to an ARM 20 pin debug header



Note

The Vtarget connection is not for supplying power, only sensing the target voltage.

2.2 External Reset Pin (RESETn)

Forcing the RESETn pin low generates a reset of the EFM32. The RESETn pin includes an internal pull-up resistor and can therefore be left unconnected if no external reset source is required. Also connected to the RESETn line is a low-pass filter which prevents noise glitches from resetting the EFM32. The characteristics of the pullup and input filter is identical to the corresponding characteristic of a GPIO pin, which is found in the device datasheet.

3 External Clock Sources

3.1 Introduction

The EFM32 supports different external clock sources to generate the low and high frequency clocks in addition to the internal LF and HF RC oscillators. The possible external clock sources for both the LF and HF domains are external oscillators (square or sine wave) or crystals/ceramic resonators. This section describes how the external clock sources should be connected.

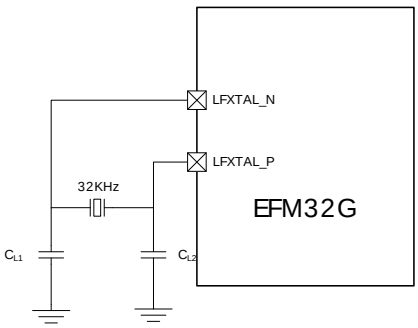
3.2 Low Frequency Clock Sources

The external low frequency clock can be generated from a crystal/ceramic resonator or from an external clock source.

3.2.1 Low Frequency Crystals and Ceramic Resonators

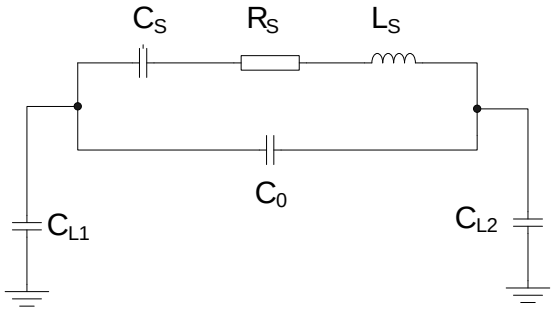
The hardware configuration of the crystal and ceramic resonator is indicated in Figure 3.1 (p. 7). The crystal is to be connected across the LFXTAL_N and LFXTAL_P pins of the EFM32.

Figure 3.1. Low Frequency Crystal



The crystals/ceramic resonators oscillate mechanically and have an electrical equivalent circuit as shown in Figure 3.2 (p. 7). In the electrical circuit C_S represents the motional capacitance, L_S the motional inductance, R_S the mechanical losses during oscillation and C_0 the parasitic capacitance of the package and pins. C_{L1} and C_{L2} represent the load capacitance. This circuit is valid for both crystals and ceramic resonators. For more information, refer to the EFM32 Oscillator Design Considerations application note.

Figure 3.2. Equivalent Circuit of a Crystal/Ceramic Resonator

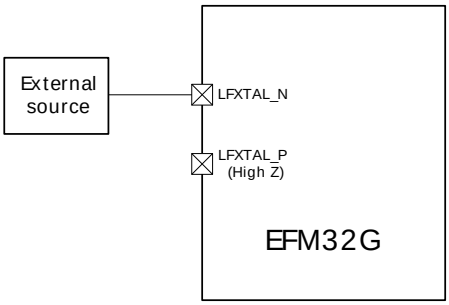


3.2.2 Low Frequency External Clocks

The EFM32 can also be clocked by a LF external clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle and signal levels. The external clock signal can either be square wave or a sine signal with a frequency of 32.768 kHz. The external clock source must be connected as indicated in Figure 3.3 (p. 8) .

When a square wave source is used the LFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%, as specified in the device datasheet. When a sine source is used, the amplitude must be in accordance with the device datasheet. The sine signal is buffered through the LFXO buffer, whose input is AC-coupled.

Figure 3.3. Low Frequency External Clock



3.3 High Frequency Clock Sources

The external high frequency clock can be generated from a crystal/ceramic resonator or from an external square or sine wave source.

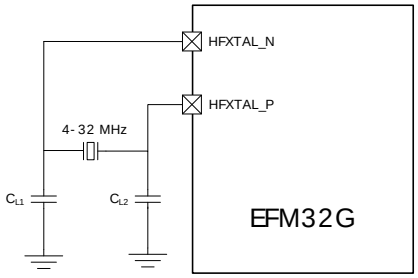
3.3.1 High Frequency Crystals and Ceramic Resonators

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 3.4 (p. 8). The crystal is to be connected across the HFXTAL_N and HFXTAL_P pins.

The electrical equivalent circuit of the HF crystal/ceramic resonators is equal to the one for LF crystals/ ceramic resonators in Figure 3.2 (p. 7) .

Right choice of C_L is important for proper operating frequency. See the EFM32 Oscillator Design Considerations application note for more information.

Figure 3.4. High Frequency Crystal Oscillator

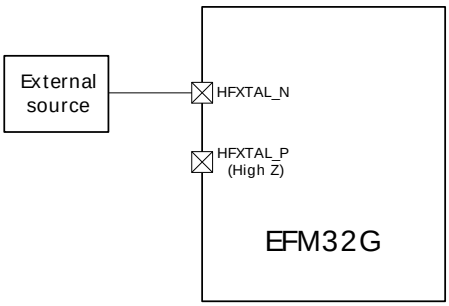


3.3.2 High Frequency External Clocks

The EFM32 can also be clocked by an external HF clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle and signal levels. The external clock signal can either be square wave or a sine signal with a frequency in accordance with the device datasheet. The external clock source must be connected as indicated in Figure 3.5 (p. 9) .

When a square wave source is used the HFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%. Please refer to the device datasheet for further details. When a sine source is used, the sine amplitude must be in accordance with what is specified in the device datasheet. The sine signal is buffered through the HFXO buffer, whose input is AC-coupled.

Figure 3.5. External High Frequency Clock



3.4 PCB Design Considerations

Keeping the PCB traces between the crystal, external capacitors and the EFM32 as short as possible is of high importance. Very small currents are running in the crystal oscillator and long lines make it more sensitive to EMC, ESD and crosstalk. Long lines also add parasitic capacitance and some series resistance to the oscillator which could reduce the startup margin of the oscillator.

It is recommended to guard the crystal traces with ground traces and keep other clock lines and signal lines that are switching frequently as far away from the crystal connections as possible. Placing a ground plane underneath the crystal and load capacitors reduces interference from other layers.

Because very small currents are running in the crystal oscillator, it is of importance to avoid dirt and soldering residue on the PCB. Such contaminations can degrade the performance of the oscillator and increase energy consumption over time. In harsh operating environments it is advised to protect the circuit in an air-tight housing to keep the circuit board clean.

See AN0016 EFM32 Oscillator Design Considerations for more information on oscillator design.

4 Reference Design

When starting a new EFM32 design, some parts of the layout are almost always required regardless of the application. Attached to this application note are example schematics for power decoupling, reset, external clocks and debug interface. Using this reference design as a template can improve development speed in the early stages of a new design. The reference design and included symbols are compatible with Cadence OrCAD 9.0 and later versions.

This application note does not include footprints for the devices, but these can be found in .bxl format on www.silabs.com.

4.1 Contents

The application note folder includes several zip-files with the following contents:

- CSV pin list files
- Edif symbols
- OrCAD OLB symbols
- OrCAD DSN example schematics
- PDF example schematics

The schematics and symbols are included for the following device families:

- EFM32ZG
- EFM32TG
- EFM32G
- EFM32LG
- EFM32WG
- EFM32GG

4.2 Comments on the Schematics

4.2.1 Power Supply Decoupling

The decouple pin uses a 1uF capacitor to filter transients in the power domain for the internal voltage regulator.

Each power pin has a 100nF decoupling capacitor in addition to the common 10uF decoupling capacitor, as described in Section 1.2 (p. 2) . The digital power supply is separated from the analogue power supply to reduce EMI. To further improve the switching noise of the analogue power, an EMI suppressor is put in series between V_{MCU} and the analogue power pins.

The active low reset pin is connected to ground through a normally open switch, as well as to the debug interface connector.

4.2.2 Debug Interface

A standard ARM 20 debug pin connector is connected to the EFM32 debug pins.

4.2.3 High/Low Frequency Clock

Both the high and low frequency clock pins are connected to crystal oscillators using two of the recommended crystals from the AN0016 Oscillator Design Considerations application note.

5 Revision History

5.1 Revision 1.40

2014-05-07

Added symbols and schematics for EFM32WG and EFM32ZG devices.

Corrected numbering for EM4WU pins for EFM32TG devices in symbols and schematics.

5.2 Revision 1.36

2013-10-14

New cover layout

5.3 Revision 1.35

2013-08-14

Updated section on power supply decoupling

5.4 Revision 1.34

2013-05-08

Added note about decoupling capacitor purpose.

Added new design files for new packages and devices.

5.5 Revision 1.33

2012-03-21

Added CSV and Edif formats for schematic symbols.

5.6 Revision 1.32

2012-03-16

Added OrCAD reference designs and OrCAD symbols for more parts.

5.7 Revision 1.31

November 23th, 2010.

Corrected schematic values.

Added information on power sequencing considerations.

5.8 Revision 1.30

November 17th, 2010.

Added information on alternate schematic recommendations.

5.9 Revision 1.20

September 13th, 2010.

Merged sections on PCB design considerations and external clock sources.

Modified chapter on external clock sources to correspond with AN0016 EFM32 Oscillator Design Considerations.

Added OrCAD and PDF reference designs.

5.10 Revision 1.10

May 6th, 2010.

Added debug interface section.

5.11 Revision 1.00

October 21th, 2009.

Initial revision.

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