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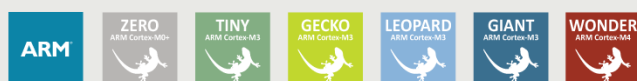
Analog Comparator

AN0020 - Application Note

Introduction

This application note describes how to use the EFM32 Analog Comparator Module to compare the voltage of two analog inputs, trigger interrupts or use two comparators for window mode.

This application note includes:

• **This PDF document**
• **Source files (zip)**
    • **Example C-code**
    • **Multiple IDE projects**
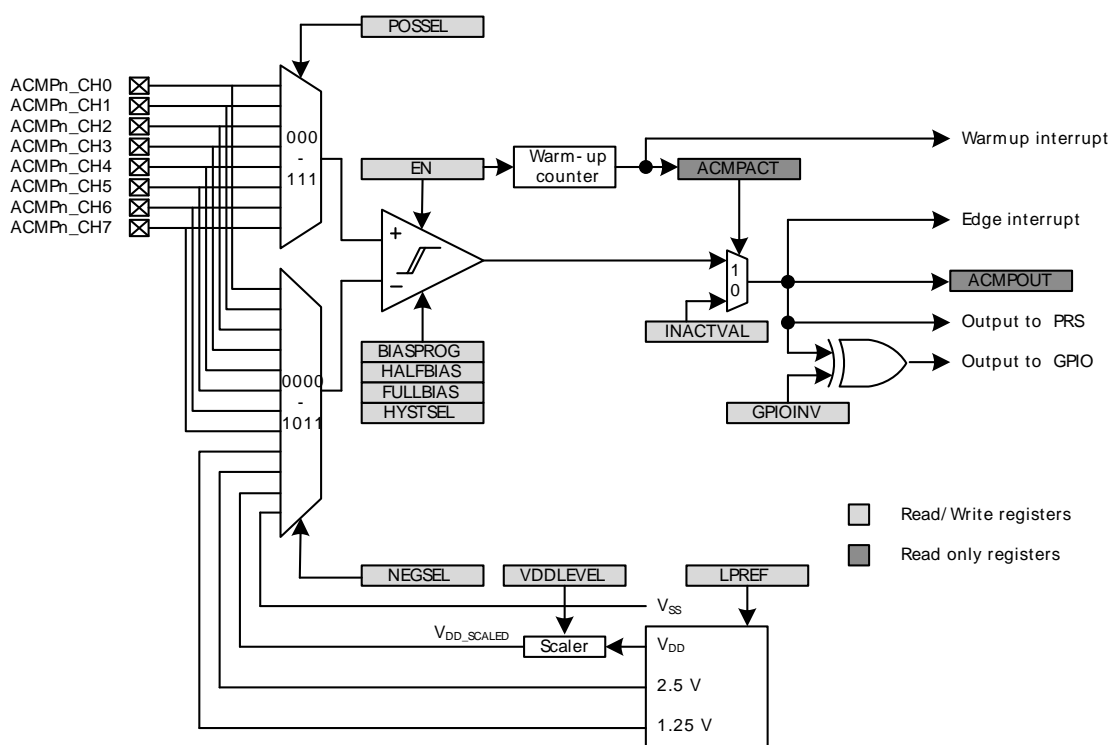
1 Analog Comparator

1.1 Introduction

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. The comparator output can be sent directly to GPIO or PRS. A capacitive sense mode is also available, this enables the comparator to be used for capacitive touch applications. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator. The internal references can operate both in normal and low power mode.

1.2 Overview

The next image illustrates the internal connections of the inputs, the reference selection and output modes.

Figure 1.1. Analog Comparator Internal Connections

The comparator has two analog inputs, one positive and one negative. When the comparator is active, the output indicates which of the two input voltages is higher. When the voltage on the positive input is higher than the negative input voltage, the digital output is high and vice versa.

One of the eight input pins can be selected as both positive and negative input to the comparator. The internal references are selectable only as negative inputs.

The output of the comparator can be read in the ACMPOUT bit in ACMPn_STATUS. It is possible to switch inputs while the comparator is enabled, but all other configuration should only be changed while the comparator is disabled.

2 Configuration

2.1 Input Selection

The POSSEL and NEGSEL fields in ACMPn_INPUTSEL controls which signals are connected to the two inputs of the comparator. 8 external pins are available for both the negative and positive input. For the negative input, 3 additional internal reference sources are available; 1.25 V bandgap, 2.5V bandgap and VDD. The VDD reference is scalable by a configurable factor, which is set in VDDLEVEL (in ACMPn_INPUTSEL) according to the following formula:

V$_{DD}$ Scaled

$$V_{DD\_SCALED} = V_{DD} \times VDDLEVEL/63 \tag{2.1}$$

2.2 Warm-Up

When the EN bit in ACMPn_CTRL is set, the comparator must stabilize before becoming active and the outputs can be used. This time period is called the warm-up time.

The warm-up time is a configurable number of peripheral clock (HFPERCLK) cycles, set in WARMTIME, which should be set to at least 10 μs. When the comparator is enabled and warmed up, the ACMPACT bit in ACMPn_STATUS will indicate that the comparator is active. The output value when the comparator is inactive is set to the value in INACTVAL in ACMPn_CTRL.

If HFPERCLK is 14 MHz, 140 cycles equals a delay of 10us, the closest available selection above this is 256 cycles.

2.3 Interrupts and PRS

The analog comparator includes an edge triggered interrupt flag (EDGE in ACMPn_IF). If either IRISE and/or IFALL in ACMPn_CTRL is set, the EDGE interrupt flag will be set on rising and/or falling edge of the comparator output respectively. An interrupt request will be sent if the EDGE interrupt flag in ACMPn_IF is set and interrupt is enabled through the EDGE bit in ACMPn_IEN. The edge interrupt can also be used to wake up the device from EM3-EM1.

The analog comparator also includes a warm-up complete interrupt flag, WARMUP in ACMPn_IF, which is set when the warm-up sequence has finished. An interrupt request will be sent if the WARMUP interrupt flag in ACMPn_IF is set and the warm-up interrupt is enabled through the WARMUP bit in ACMPn_IEN.

The synchronized comparator outputs are also available as a PRS output signals. This can be configured with the PRS_SourceSignalSet function in efm32_prs.c.

2.4 Output to GPIO

The output from the comparator and the capacitive sense are available as alternate functions to the GPIO pins. Set the ACMPPEN bit in ACMPn_ROUTE to enable output to pin. The LOCATION bits selects the output pin location. Even though the GPIO pin is automatically configured as output when the ACMPPEN bit is set, the drive level and other GPIO features are not changed, and should be configured prior to setting the ACMPPEN bit. The pin output can be inverted by setting the GPIOINV bit in ACMPn_CTRL.

For example, if setting the ACMPPEN bit in ACMP0_ROUTE and enabling an alternate location by setting the LOCATION bits to 1, the output will be enabled and routed to PE2.

2.5 Software Example

The **acmp_conf** example configures ACMP0 with channel 4 (PC4) as positive input and the 1.25 V bandgap reference as negative input. The warm-up time is configured for 14 MHz. Output to GPIO is

also activated and routed to the alternative location, which is PE2 for ACMP0 on the Gecko and Giant Gecko Starter Kit and PD6 on the Tiny Gecko Starter Kit. The EFM32 wakes up every 100 ms and updates the LCD with the current comparator output value.

Use a small lead to short the comparator input to either GND or VDD and see the result on the LCD.

The **acmp_int** example uses the ACMP0 edge interrupt to wake up the EFM32 from EM2. Input is applied to channel 4 (PC4) and the 2.5 V bandgap reference is used as the negative input. The LCD is only updated every time the compare output is updated. The analog comparator can also wake the EFM32 up from EM3, but this example uses the LCD, which is not active in EM3.

3 Additional Features

3.1 Hysteresis

In the analog comparator, hysteresis can be turned off or configured to 7 different levels, this is done through the HYSTSEL field in ACMPn_CTRL. When the hysteresis level is set above 0, the digital output will not toggle until the positive input voltage is at a voltage equal to the hysteresis level above or below the negative input voltage. This feature can be used to filter out uninteresting input fluctuations around zero and only show changes that are big enough to breach the hysteresis threshold.

Figure 3.1. 20 mV Hysteresis Selected
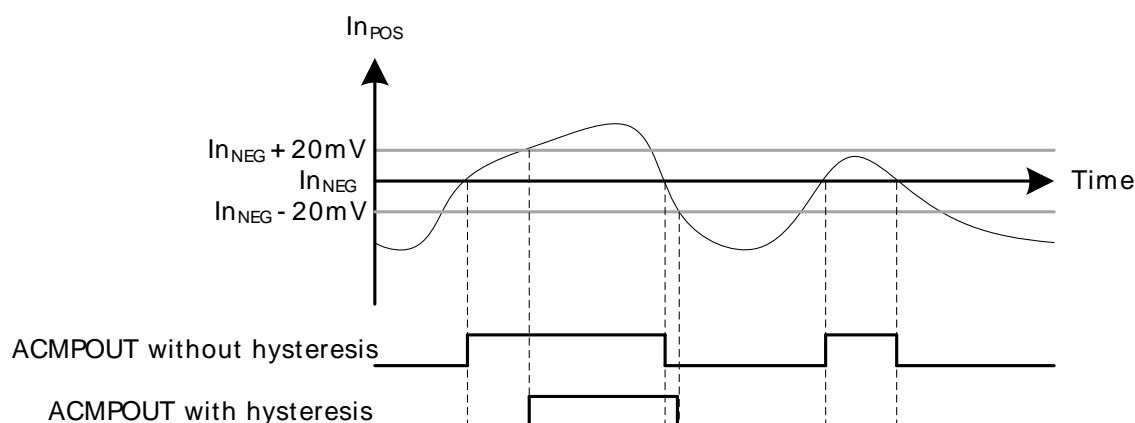
3.2 Response Time

There is a delay from when the actual input voltage changes polarity, until the output toggles. This period is called the response time and can be altered by increasing or decreasing the bias current to the comparator through the BIASPROG, FULLBIAS and HALFBIAS fields in the ACMPn_CTRL register. Setting the HALFBIAS bit in ACMPn_CTRL effectively halves the current, while setting the FULLBIAS bit multiplies the current by 65. Setting a lower bias current will result in lower power consumption, but a longer response time. For a table with actual current values, the reader is referred to the reference manual.

If the FULLBIAS bit is set, the highest hysteresis level should be used to avoid glitches on the output.

3.3 Low Power Reference

A low power reference mode can be enabled by setting the LPREF bit in ACMPn_INPUTSEL. In this mode, the power consumption in the reference buffer (VDD and bandgap) is lowered at the cost of accuracy. Low power mode will only save power if VDD with VDDLEVEL higher than 0 or a bandgap reference is selected. During warm-up of the analog comparator the LPREF bit should be 0.

4 Window Mode

4.1 Window Mode with two Analog Comparators

Often it is necessary to know if a voltage is between, above or below two predefined thresholds. This is possible using two analog comparators (see Figure 4.1 (p. 6)). The input signal is sent to the positive input of both comparators, compared against the lower threshold using one comparator, and compared against the upper threshold using the other comparator. If both comparators outputs 0, the signal is below the lower threshold, if the lower threshold comparator outputs 1 and the upper threshold comparator outputs 0, the input is within the selected range. Finally if both comparators outputs 1, the input is above the predefined range (see Figure 4.2 (p. 7)).

Since the input signal needs to be available to both comparators at the same time, one need to connect the positive input pins for the two comparators together.
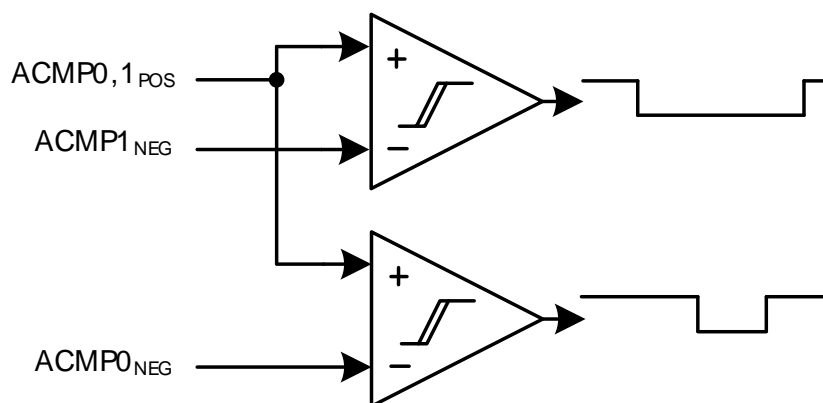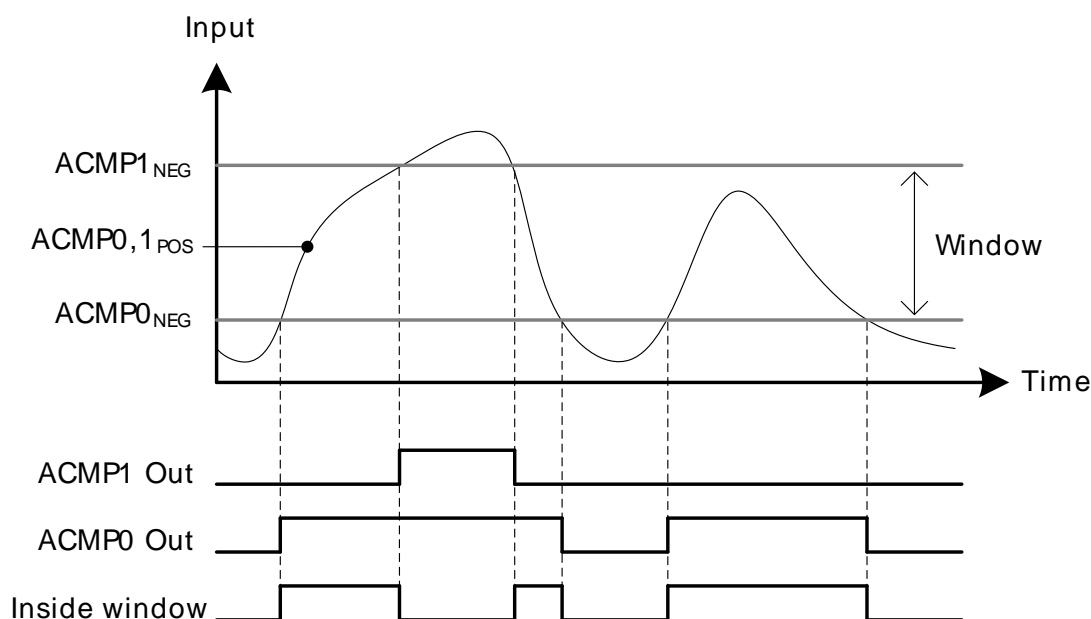
Figure 4.1. Two Analog Comparators in Window Mode

Figure 4.2. Example Wave Form, Window Mode

4.2 Software Example

The **acmp_window** example is available on the Gecko and Tiny Gecko Starter Kit. It configures analog comparator 0 as lower boundary with the VDD scaled to 1 V as negative input. Analog comparator 1 is configured as upper boundary with VDD scaled to 2 V as its negative input. The scaling of the upper and lower boundary assumes that VDD is 3.3 V.

The positive input is channel 4 for both comparators, this corresponds to PC4 and PC12 for ACMP0 and ACMP1 respectively. These pins should be connected together externally using a jumper cable. This is easy on both the DVK and STK because these pins are located on the protoboard for the DVK and the expansion header of the STK.

5 Revision History

5.1 Revision 1.09

2014-05-07

Updated example code to CMSIS 3.20.5

Changed to Silicon Labs license on code examples

Added example projects for Simplicity IDE

Removed example makefiles for Sourcery CodeBench Lite

5.2 Revision 1.08

2013-10-14

New cover layout

5.3 Revision 1.07

2013-05-08

Added software projects for ARM-GCC and Atollic TrueStudio.

5.4 Revision 1.06

2012-11-12

Adapted software projects to new kit-driver and bsp structure.

Added projects for Tiny and Giant Gecko STKs.

5.5 Revision 1.05

2012-04-20

Adapted software projects to new peripheral library naming and CMSIS_V3.

5.6 Revision 1.04

2011-11-17

Updated IDE project paths with new kits directory.

5.7 Revision 1.03

2011-07-14

Changed window mode example to use scaled VDD.

Changed interrupt driven example to use 1V25 bandgap.

Updated projects to align with new bsp version.

5.8 Revision 1.02

2011-05-18

Updated projects to align with new bsp version.

5.9 Revision 1.01

2010-11-16

Removed lcdcontroller.c from IDE-project files.

Changed example folder structure, removed build and src folders.

Updated chip init function to newest efm32lib version.

5.10 Revision 1.00

2010-09-27

Initial revision.

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