Description of your approach towards designing the two-stage op-amp, including equations and calculations of transistor's dimensions, DC current sources, capacitors, etc. (20 points)

Step 1.

We decided to choose $L = 1\mu$ m

Step 2.

$C_C > 0.22 * C_L$ where $C_L = 1$ pF

$C_C > 0.22 * 1pF$

$C_c > 0.22\,pF$

We can choose $C_C = 0.25$ pF

Step 3.

$$SR = \frac{I_{D5}}{C_C}$$

$$I_{D5} = SR * C_C \Rightarrow (100\,V/\mu s) * (0.25\,pF) = 25\mu A$$

$$I_{D5} = 22\mu A$$

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D5}}{2}$$

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 11\mu A$$

Step 4.

$$V_{IN,MAX} = [V_{DD} + V_{TH1}] - [\sqrt{\frac{I_{D5}}{\mu_P C_{ox}(\frac{W}{L})_3}} + |V_{TH3}|]$$

Where $V_{TH1} = V_{THN}$, $V_{TH3} = V_{THP}$

$$1.4 = [1.8 + 0.345] - [\sqrt{\frac{22\mu A}{50\mu A*(\frac{W}{L})_3}} + 0.415]$$

$$0.33 = \sqrt{\frac{22\mu A}{50\mu A*(\frac{W}{L})_3}}$$

$$(\frac{W}{L})_3 = (\frac{W}{L})_4 = 4.35$$

$$gm_3 = gm_4 = \sqrt{2\mu_P c_{ox}(\frac{W}{L})_3 I_{D3}}$$

$$gm_3 = gm_4 = \sqrt{2 * (50\mu A) * (4.35) * (11\mu A)} = 69.17369442\mu S$$

Step 5.

$$gm_1 = GB * C_C \Rightarrow 50MHz * 0.22pF * 2\pi$$

$$gm_1 = gm_2 = 69.11503838\mu S$$

$$gm_1 = \sqrt{2 * \mu_n c_{ox} * (\frac{W}{L})_1 * I_{D1}}$$

$$69.11503838\mu S = \sqrt{2 * (250\mu A/V^2) * \frac{W}{L}_1 * (11\mu A)}$$

$$\frac{W}{L}_1 = 0.86852$$

So here we can estimate the $\frac{W}{L}_1 = \frac{W}{L}_2 \approx 1$

Step 6.

$$V_{IN,MIN} = V_{TH1} + \sqrt{\frac{I_{D5}}{\mu_n c_{ox} * \frac{W}{L}_1}} + \sqrt{\frac{2I_{D5}}{\mu_n c_{ox} * \frac{W}{L}_5}}$$

$$0.7 = 0.345 + \sqrt{\frac{22\mu A}{250\mu A * 0.987}} + \sqrt{\frac{2*(22\mu A)}{250\mu A * \frac{W}{L}_5}}$$

$\frac{W}{L}_5 = 130.74860$

Here we can estimate $\frac{W}{L}_5 \approx 131$

Step 7.

using $gm_6 \geq 10gm_1$ *decide a value for* gm_6

$gm_6 \geq 10 * 69.11503838\mu S$

$gm_6 \geq 691.1503838\mu S$

Step 8.

$V_{SG4} = V_{SG6}$

$$\frac{gm_6}{gm_4} = \frac{\frac{W}{L}_6}{\frac{W}{L}_4}$$

$$\frac{691.1503838\mu S}{69.17369442\mu S} = \frac{\frac{W}{L}_6}{4.35}$$

$$\frac{W}{L}_6 = 43.46311405$$

$$gm_6 = \sqrt{2 * \mu_P c_{ox} * \frac{W}{L}_6 * I_{D6}}$$

$$691.1503838\mu s = \sqrt{2 * 50\mu A * 43.46 * I_{D6}}$$

$$I_{D6} = 119.4\mu A$$

$$I_{D6} = I_{D7} = 119.4\mu A$$

Step 9.

$$\frac{I_{D7}}{I_{D5}} = \frac{\frac{W}{L}_7}{\frac{W}{L}_5}$$

$$\frac{119.4\mu A}{22\mu A} = \frac{\frac{W}{L}_7}{130.74860}$$

$$\frac{W}{L}_7 = 709.6083109$$

We also need to find $\frac{W}{L}_8$

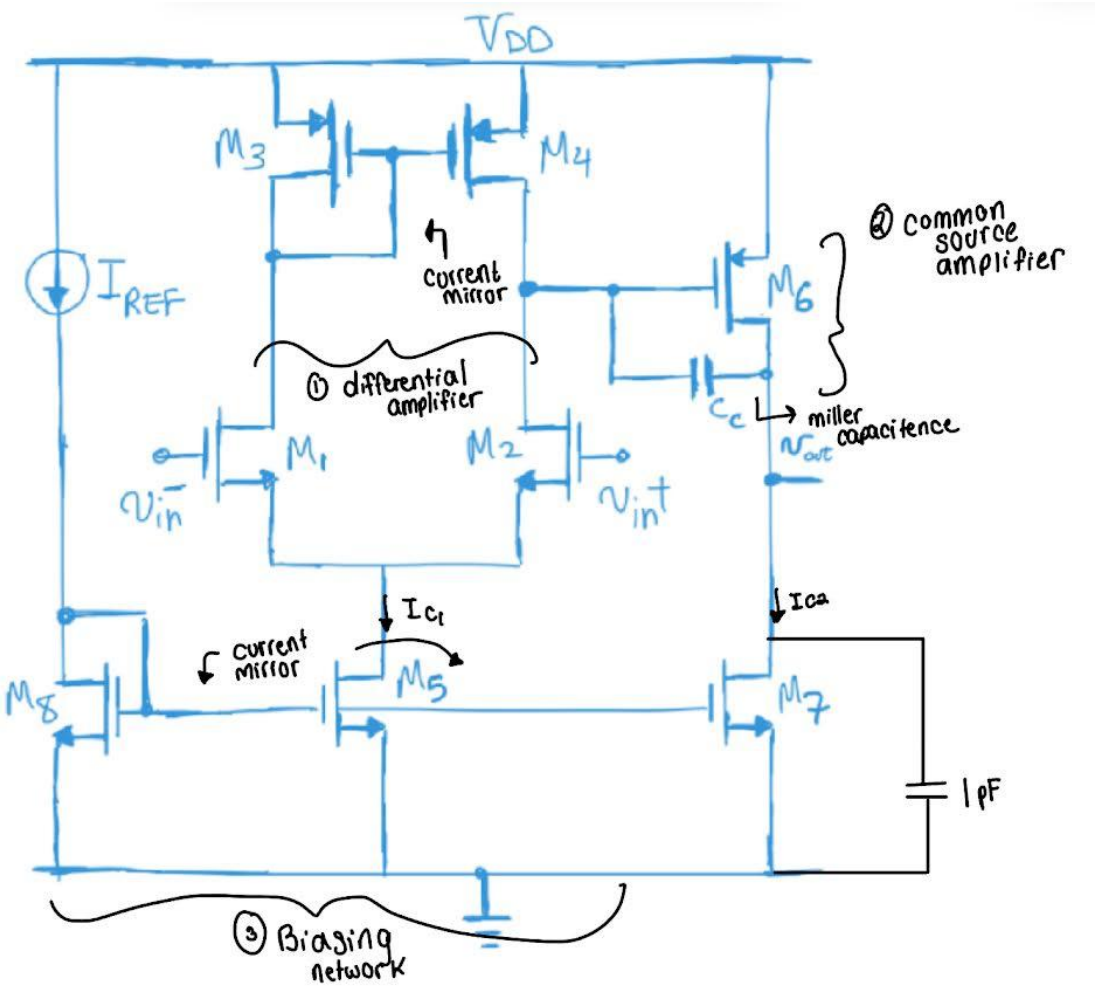
$$\frac{I_{D8}}{I_{D7}} = \frac{\frac{W}{L}_8}{\frac{W}{L}_7} \; where \; I_{REF} = I_{D8} \; and \; we'll \; assume \; that \; I_{REF} = 10\mu A$$

$$\frac{10\mu A}{119.4\mu A} = \frac{\frac{W}{L}_8}{709.6083}$$

$$\frac{W}{L}_8 = 59.43118182$$

Some FETs were in subthreshold or triode region, and so we had to make more adjustments to the $\frac{W}{L}$ ratios, dominant pole compensation capacitance, and the input bias current.

Transistor-level schematic of your op-amp. Identify the functionality of each part. For example, stage 1 of amplification, stage 2 of amplification, current mirrors, etc.



The above circuit is a two-stage CMOS Op-Amp.

1. The middle segment of the circuit (denoted as 1) functions as the input stage and comprises the differential amplifier, consisting of M1 to M5. Within this configuration, a MOS differential pair operates with a current-mirror load. Additionally, a differential input exists between M1 and M2, contributing to both voltage gain and high input resistance (due to no current going through the gate terminal). The drain terminal of M4 is linked to a single-ended output, offering common-mode rejection properties.
2. The rightmost part of the circuit (labeled 2) is the output-stage. This consists of M6 and M7. In this stage, there is a common source amplifier with a current source load. M7 is the active load, supplying constant current. This stage provides voltage gain and high output resistance.

3. The bottom section of the circuit represents the biasing network. M8, M5, and M7 are in a current mirror arrangement. The bias current of the input differential pair is provided by M5. The bias current of the second stage is provided by M7.

The capacitor helps make the circuit more stable in terms of poles and phase margins.

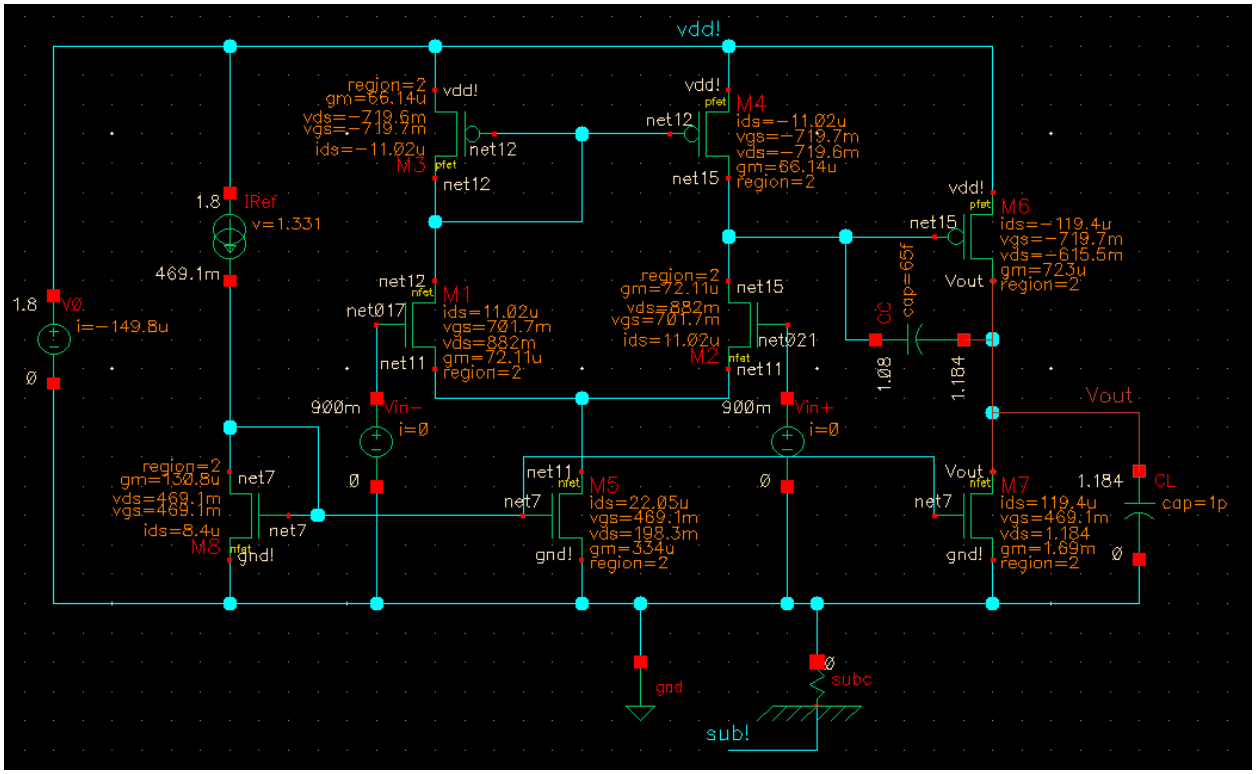
A table summarizing dimensions of the transistors (W/L) and value of resistors and capacitors used in your circuit.

MOSFET	$Adjusted\ \frac{W}{L}\ ratio$
M1 = M2	1
M3 = M4	4.35
M5	15.2
M6	46
M7	59.7
M8	6

Simulation Results:

1. DC Analysis

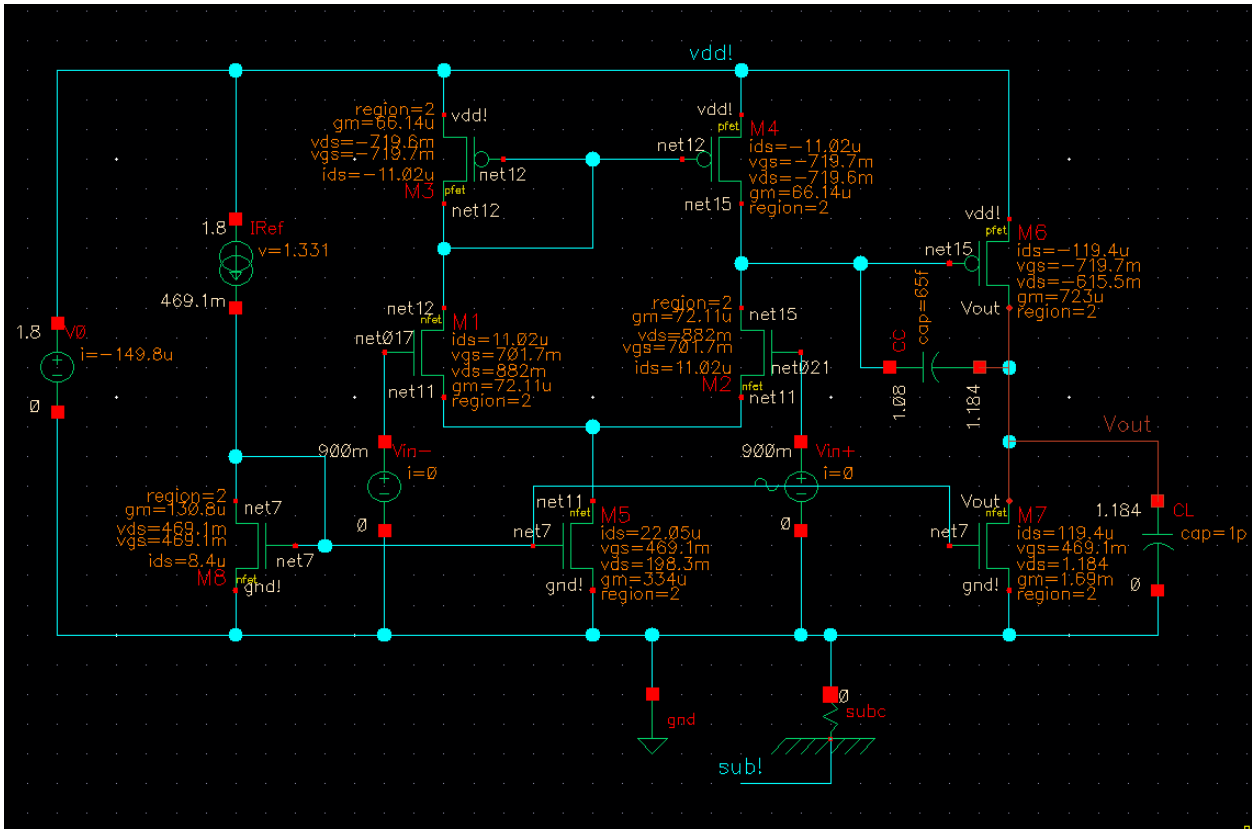
We produced this schematic using the adjusted $\frac{W}{L}$ ratios, where all the MOSFETs are in the saturation region (region 2) and for Vout we got 1.184V.



2. AC Analysis

For our schematic we had to make adjustments to our input bias current, dominant pole compensation capacitor, and the $\frac{W}{L}$ ratio of the output transistor (M6) . We increased the $\frac{W}{L}$ ratio for the output transistor allowing us to shift our pole to a lower frequency on the bode plot allowing us to meet the required gain bandwidth, however doing so also made us decrease our input bias current. Reducing the compensation capacitance also helped us achieve 60dB for our low frequency voltage gain. Below is our schematic with all adjustments done, and our bode plot for the AC analysis where we show that we obtained a 60.05dB, 50.18MHz, and a 25° phase margin.

Additionally, in our simulations, we noticed that there was an intricate relationship between bandwidth, voltage gain, and phase margin. As we fine-tuned these parameters, it became evident that decreasing both the bandwidth and voltage gain increases the phase margin. For instance, in another design, we had the voltage gain, bandwidth, and phase margin at 57.35 dB, 42.05 MHz, and 50°, respectively. This highlights the inherent trade-offs in analog circuits to achieve the most effective solution for any application. Our optimized solution, 60.05dB, 50.18MHz, and a 25° phase margin, showed the most stability for this assignment.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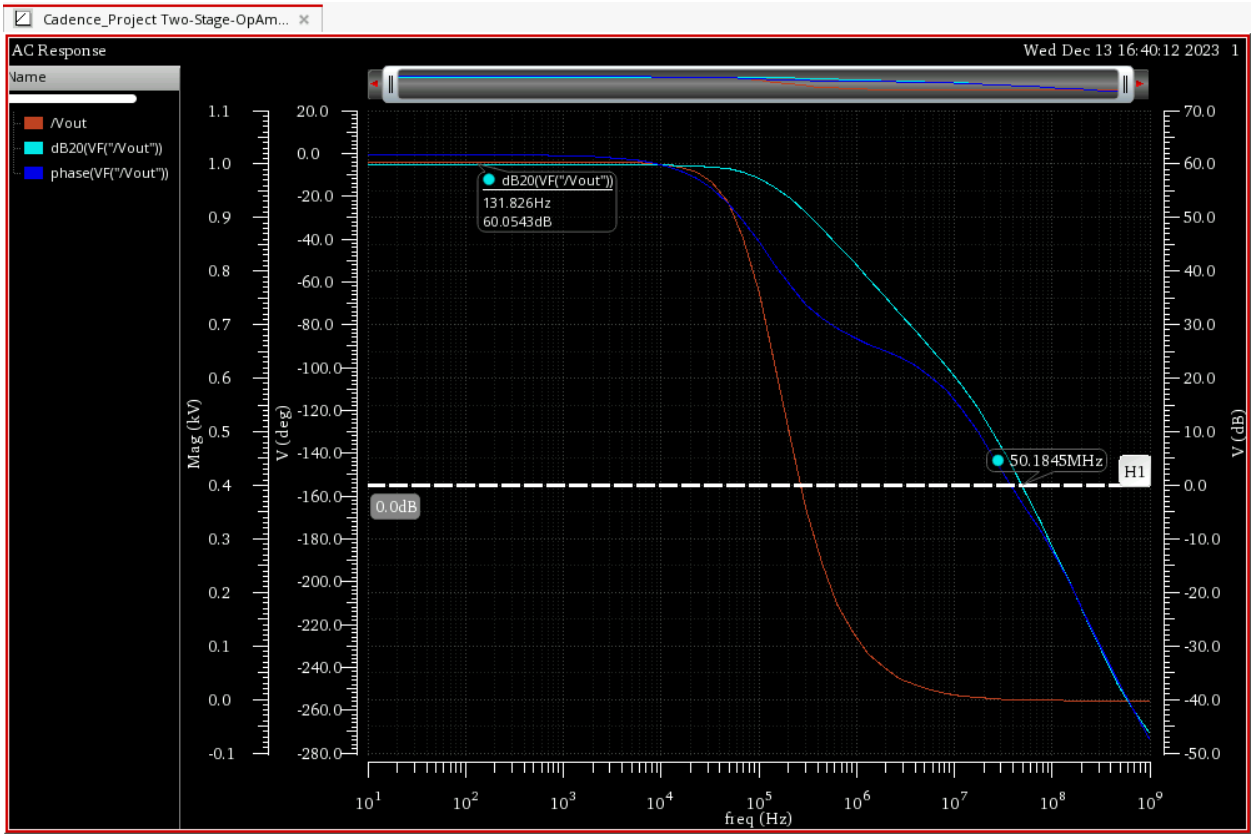
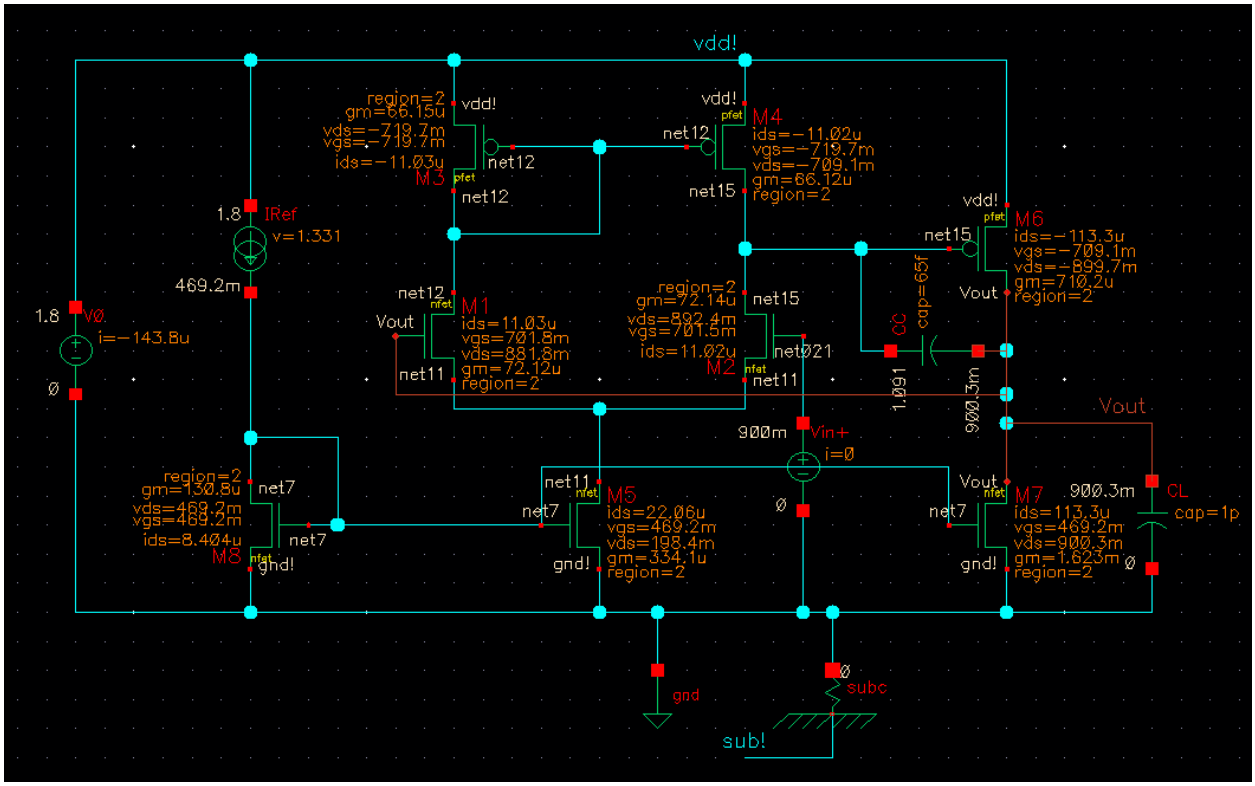
gm=66.14u
vds=-719.6m
vgs=-719.7m
ids=-11.02u
M3
pfet
net12
vdd!
pfet
M4
net12
ids=-11.02u
vgs=-719.7m
vds=-719.6m
gm=66.14u
region=2
net15
1.8
IRef
v=1.331
469.1m
vdd!
pfet
M6
net15
ids=-119.4u
vgs=-719.7m
vds=-615.5m
gm=723u
region=2
Vout
net12
nfet
M1
ids=11.02u
vgs=701.7m
vds=882m
gm=72.11u
region=2
net017
net11
region=2
gm=72.11u
vds=882m
vgs=701.7m
ids=11.02u
M2
net15
net021
net11
nfet
Cc
cap=65f
1.08
1.184
1.8
V0
i=-149.8u
0
900m
Vin-
i=0
900m
Vin+
i=0
Vout
region=2
gm=130.8u
vds=469.1m
vgs=469.1m
ids=8.4u
M8
nfet
net7
gnd!
0
net11
nfet
M5
ids=22.05u
vgs=469.1m
vds=198.3m
gm=334u
region=2
net7
gnd!
0
Vout
nfet
M7
ids=119.4u
vgs=469.1m
vds=1.184
gm=1.69m
region=2
net7
gnd!
1.184
CL
cap=1p
0
gnd
0
subc
sub!



3. Measure Input Common Mode Range (ICMR)

Below we have our schematic that's been configured as a unity-gain buffer. Our closed loop gain is set to 1, and so the output voltage should be identical to the input voltage. From our Vout vs Vin plot, we can see that the slope is essentially equal to one. The ICMR range is 0.69948V to 1.4V meaning our numbers indeed meet the requirements.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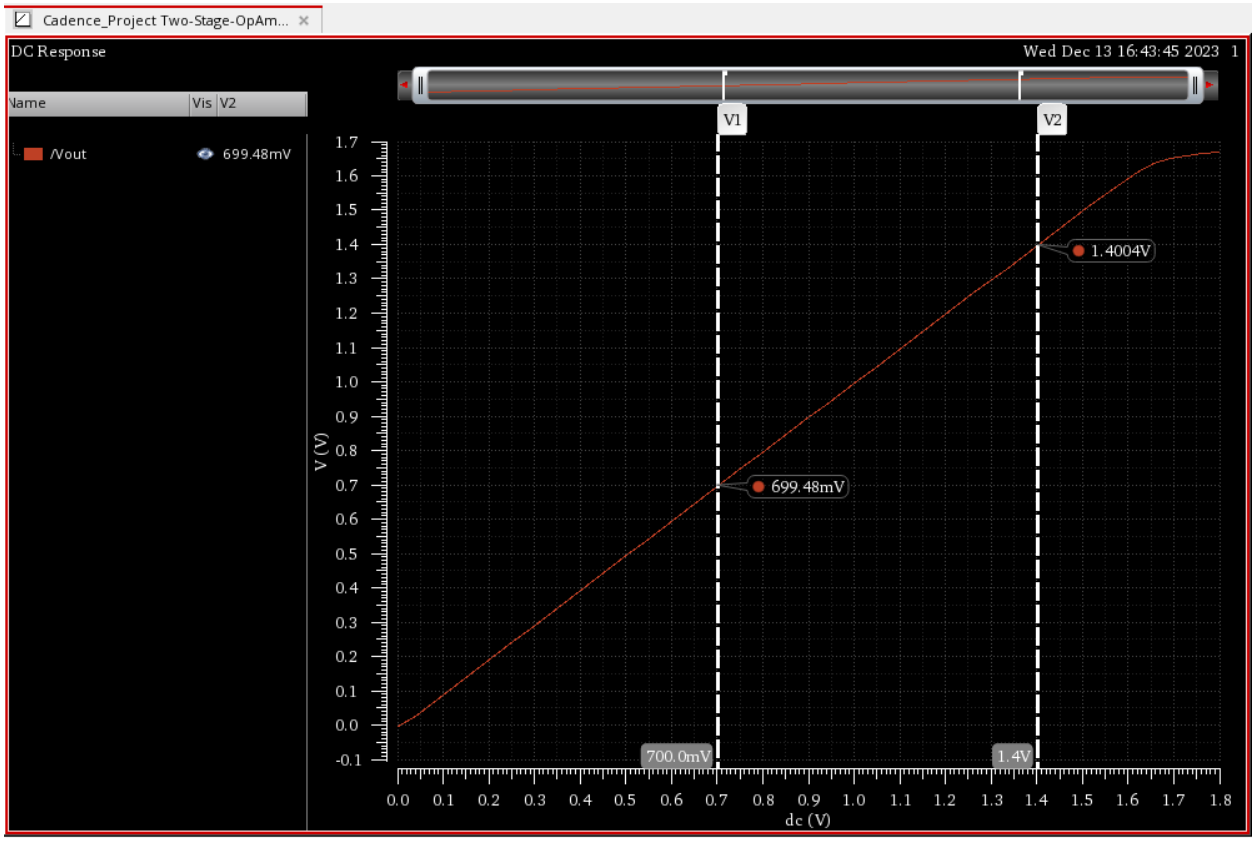
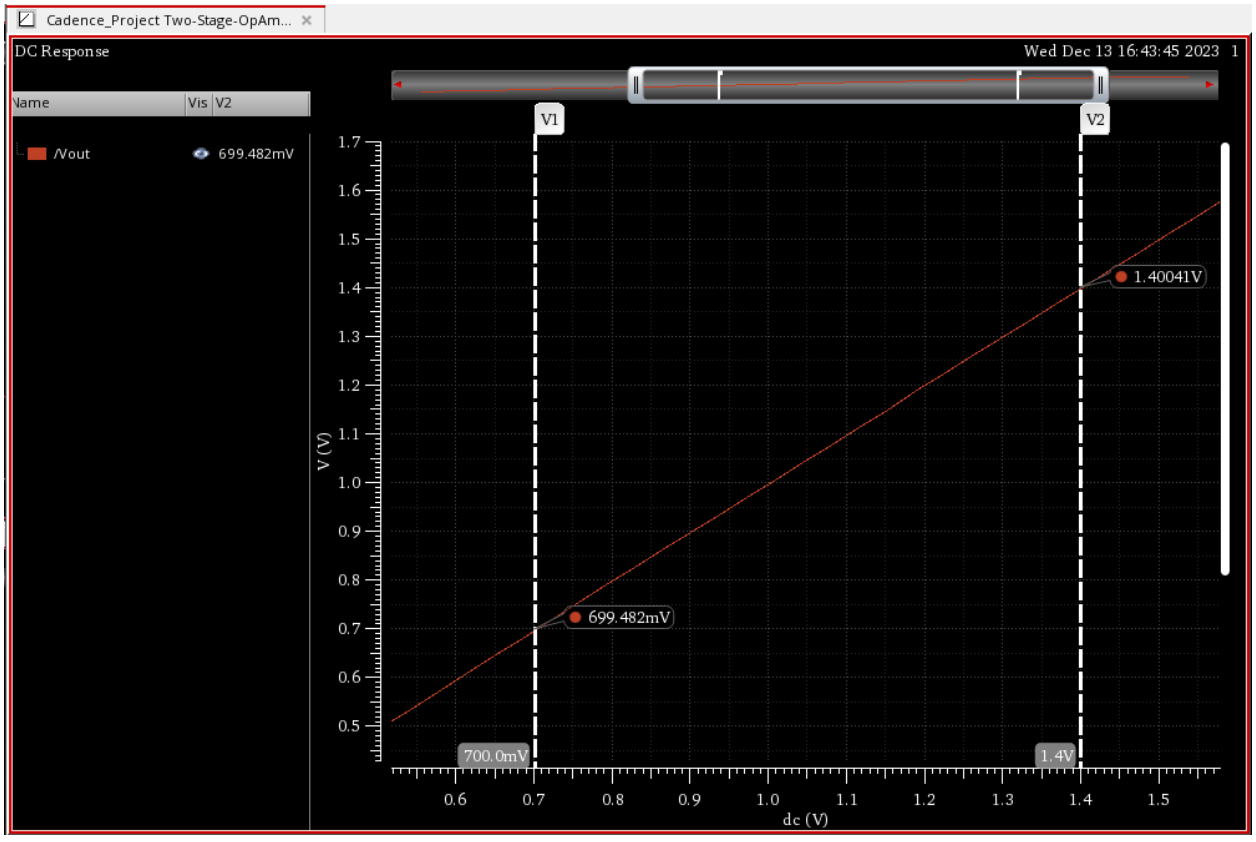
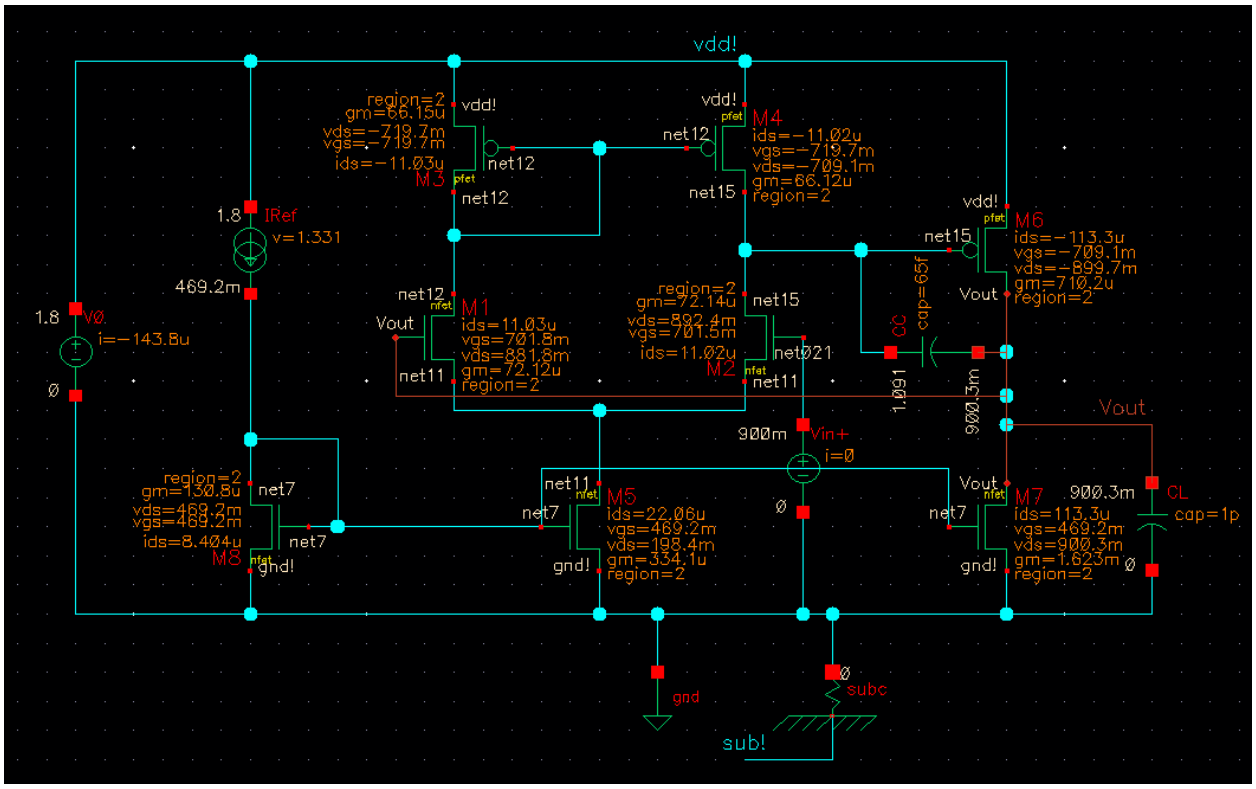
region=2
gm=66.15u
vgs=-718.7m
vds=-719.7m
ids=-11.03u
M3
pfet
net12
vdd!
M4
pfet
net12
ids=-11.02u
vgs=-719.7m
vds=-709.1m
gm=66.12u
region=2
net15
1.8
IRef
v=1.331
469.2m
vdd!
M6
pfet
net15
ids=-113.3u
vgs=-709.1m
vds=-899.7m
gm=710.2u
region=2
Vout
1.8
VØ
i=-143.8u
Ø
net12
M1
nfet
Vout
ids=11.03u
vgs=701.8m
vds=881.8m
gm=72.12u
region=2
net11
region=2
gm=72.14u
vds=892.4m
vgs=701.5m
ids=11.02u
net15
M2
nfet
net021
net11
CC
cap=65f
1.091
900.3m
Vout
900m
Vin+
i=Ø
region=2
gm=130.8u
vds=469.2m
vgs=469.2m
ids=8.404u
M8
nfet
net7
net7
gnd!
net11
M5
nfet
net7
gnd!
ids=22.06u
vgs=469.2m
vds=198.4m
gm=334.1u
region=2
Ø
Vout
M7
nfet
net7
gnd!
ids=113.3u
vgs=469.2m
vds=900.3m
gm=1.623m
region=2
900.3m
CL
cap=1p
Ø
gnd
Ø
subc
sub!


Cadence_Project Two-Stage-OpAm...
DC Response
Wed Dec 13 16:43:45 2023 1
Name
Vis
V2
/Vout
699.48mV
V1
V2
1.4004V
699.48mV
700.0mV
1.4V
V (V)
dc (V)


Cadence_Project Two-Stage-OpAm...
DC Response
Wed Dec 13 16:43:45 2023 1
Name
Vis
V2
/Vout
699.482mV
V1
V2
1.40041V
699.482mV
700.0mV
1.4V
V (V)
dc (V)

4. Power Dissipation

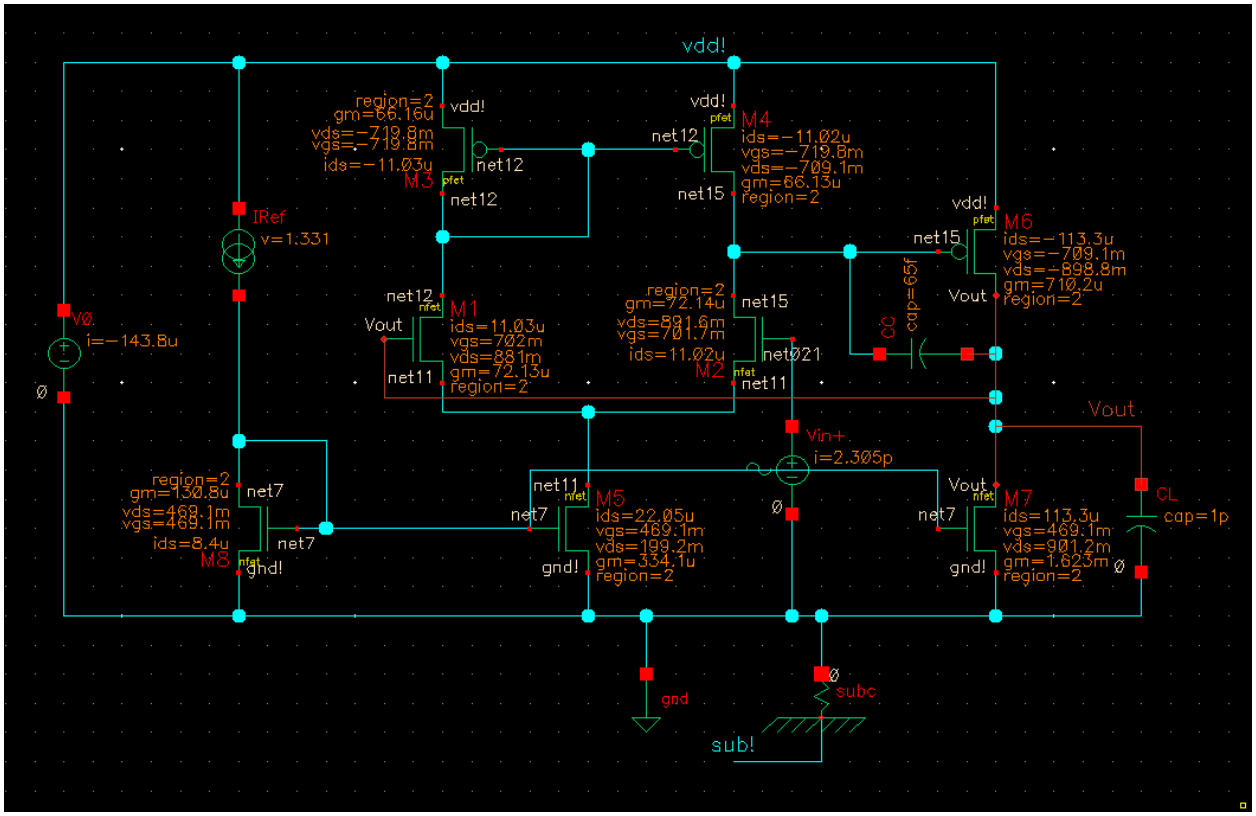


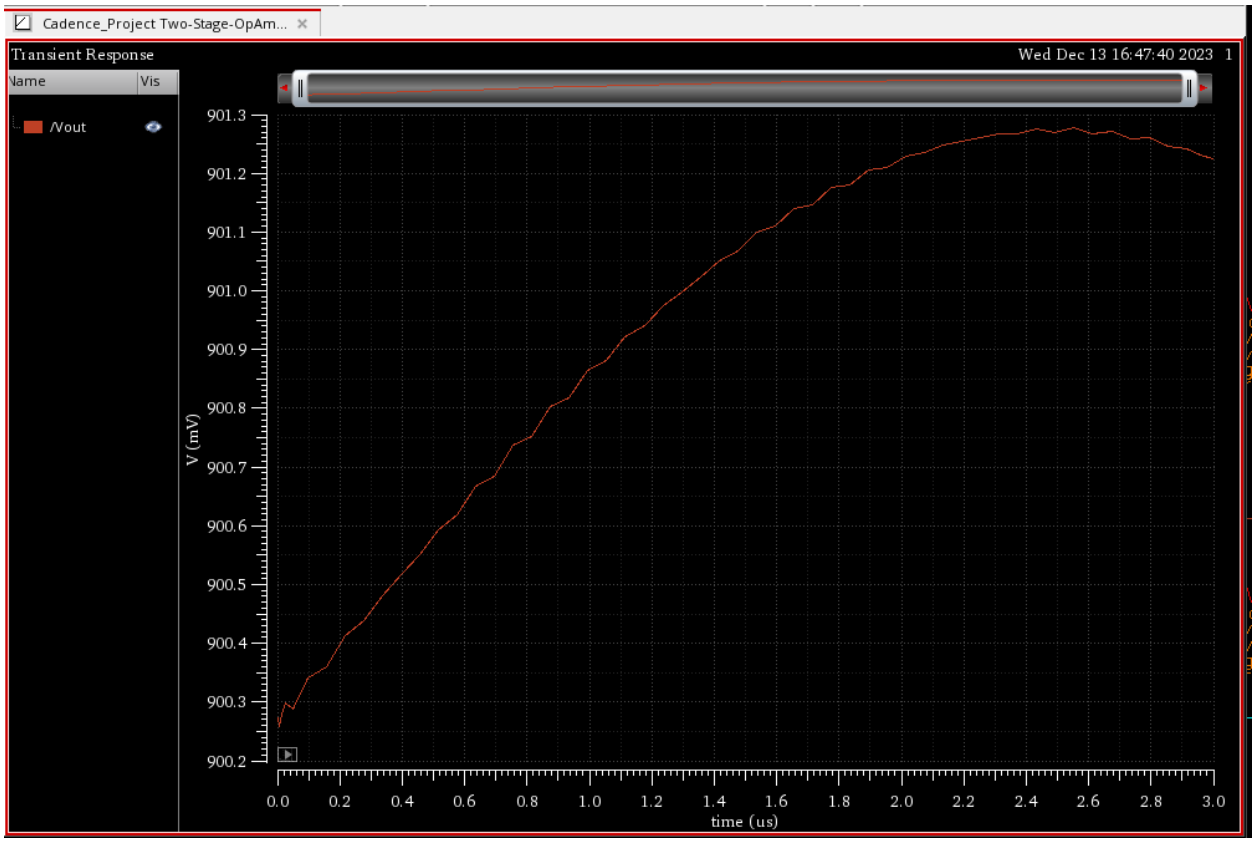
$P_{diss} = (1.8V * 143.8\mu A) = 258.84\mu W$

The power dissipation is 258.84 µW

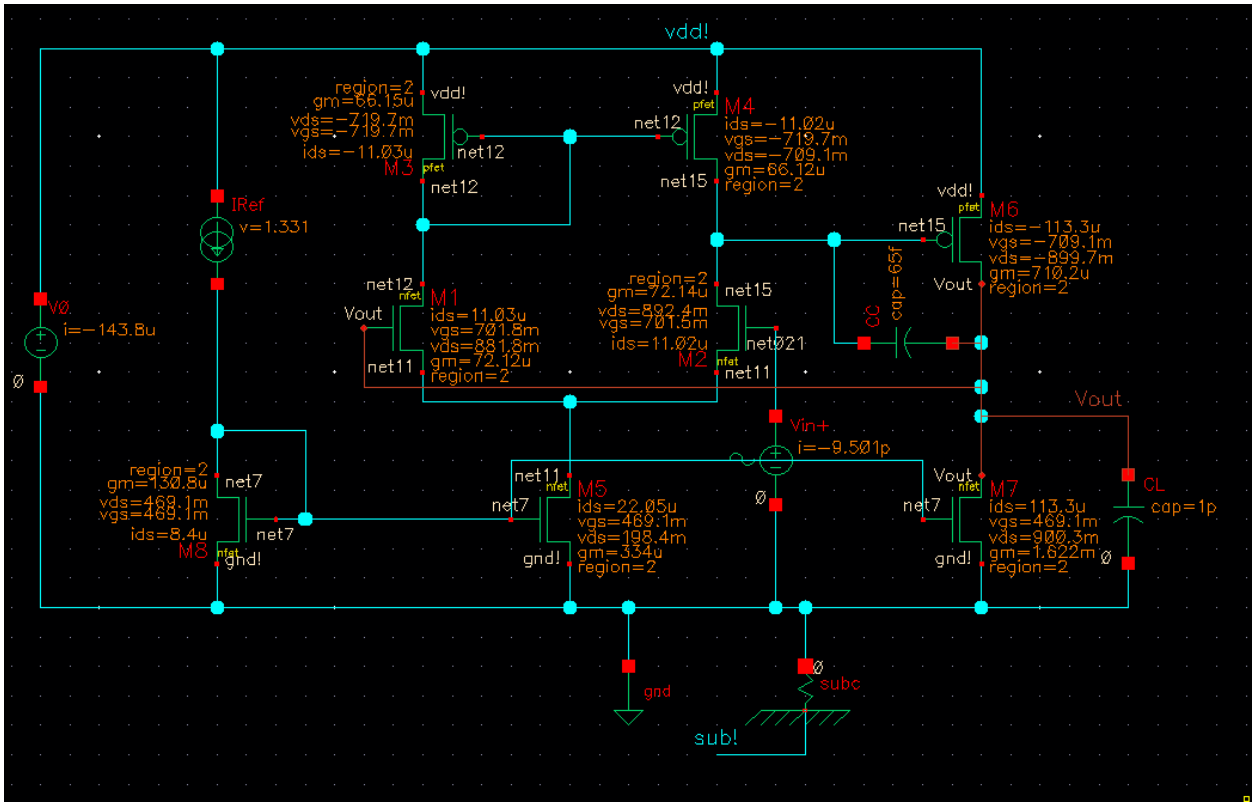
5. Transient Simulation

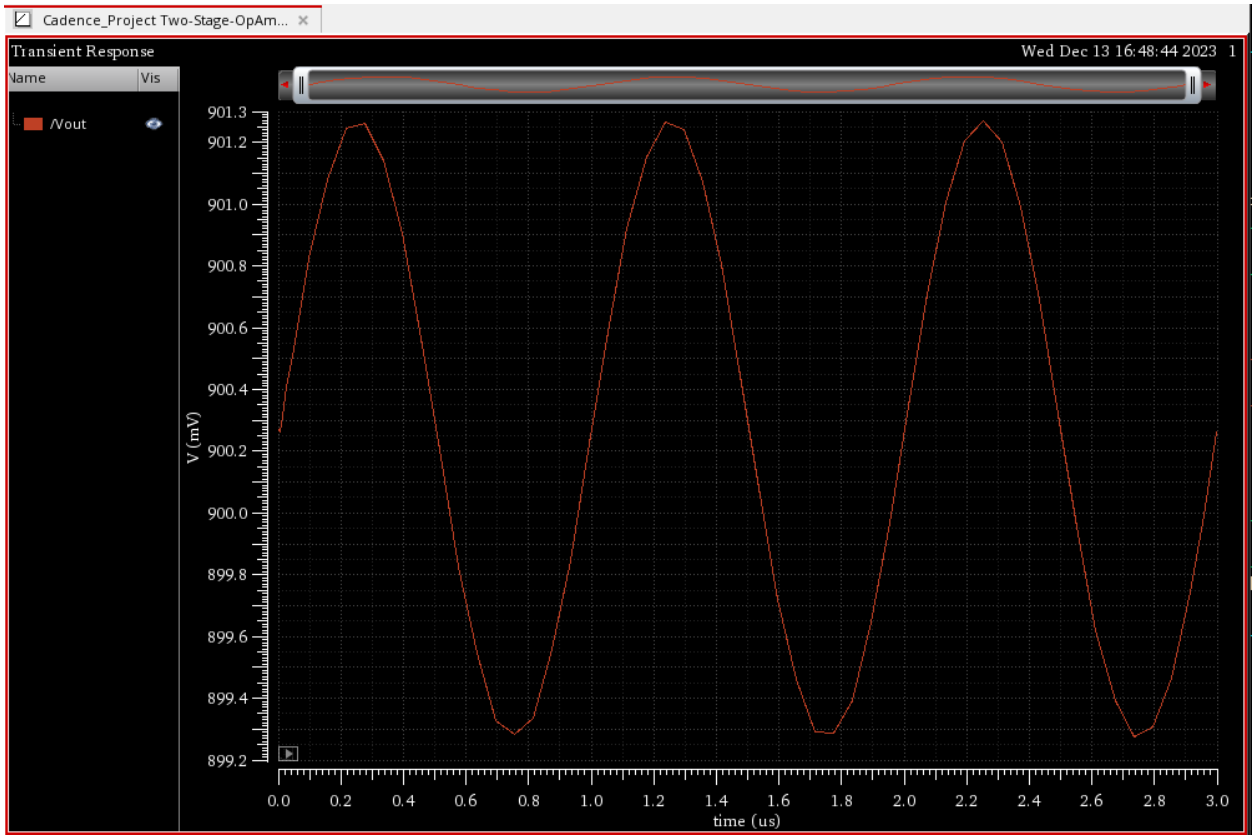
100KHz



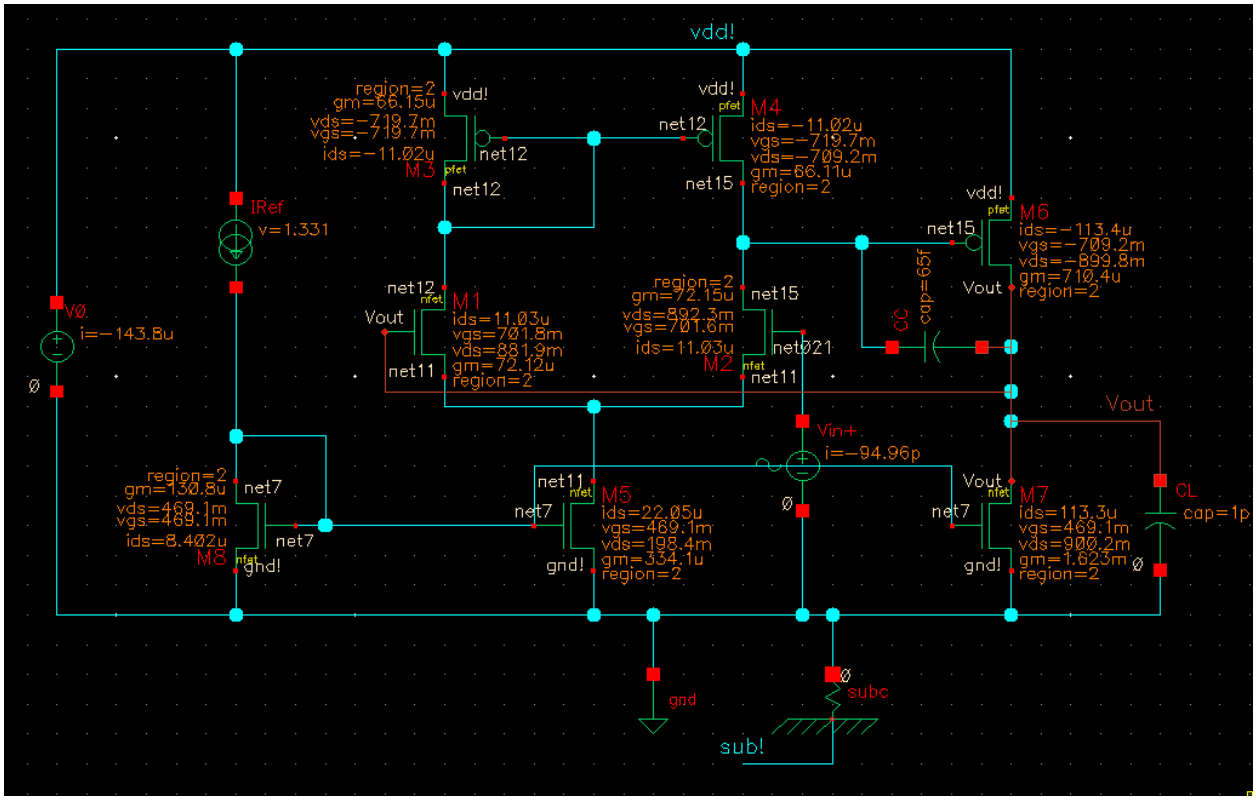


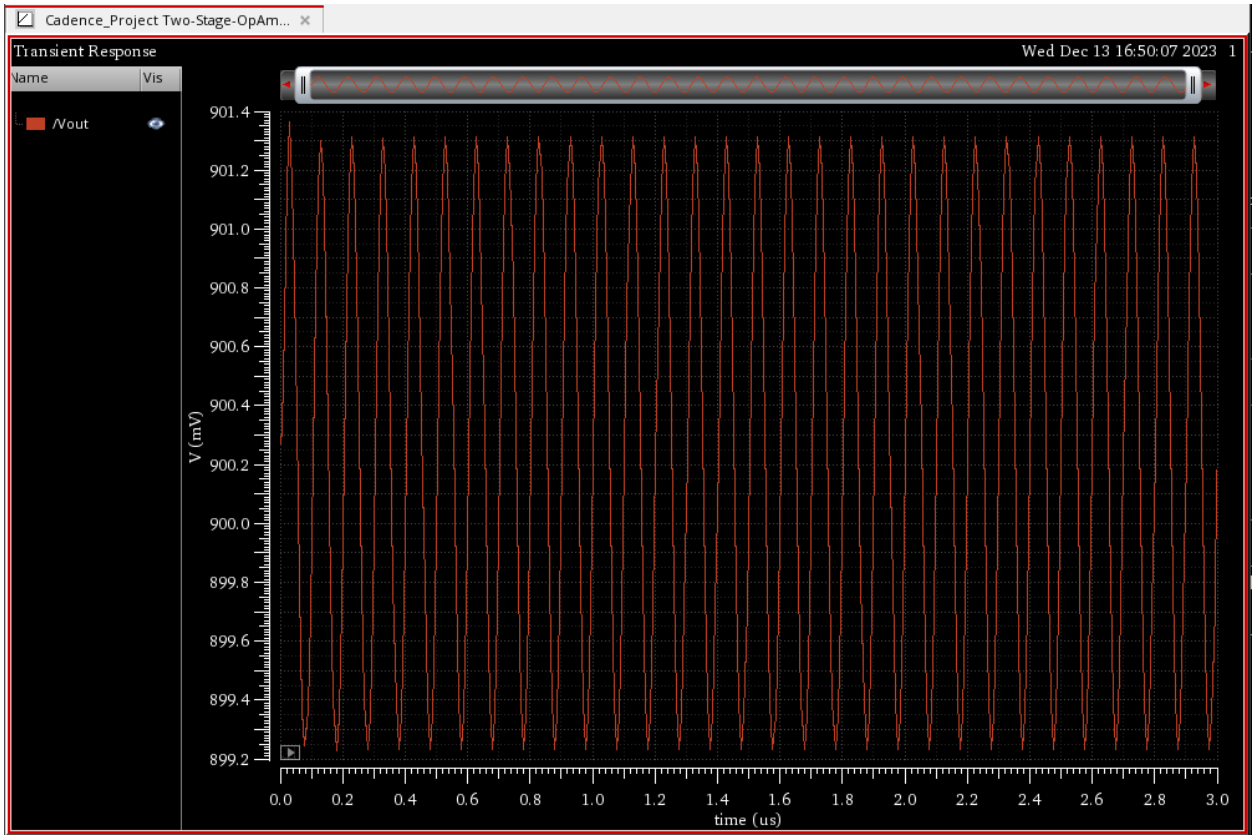
1 MHz (Next Page)



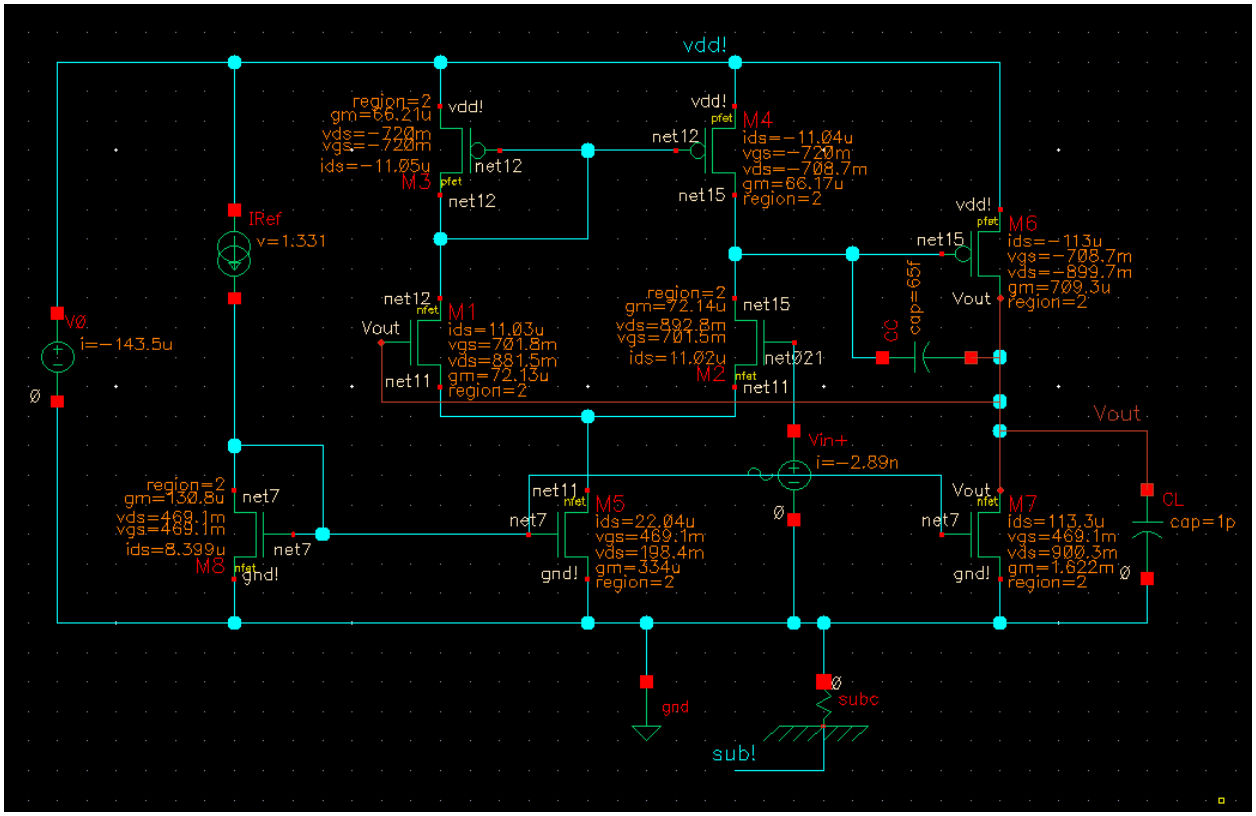


10 MHz (Next Page)





100MHz (Next Page)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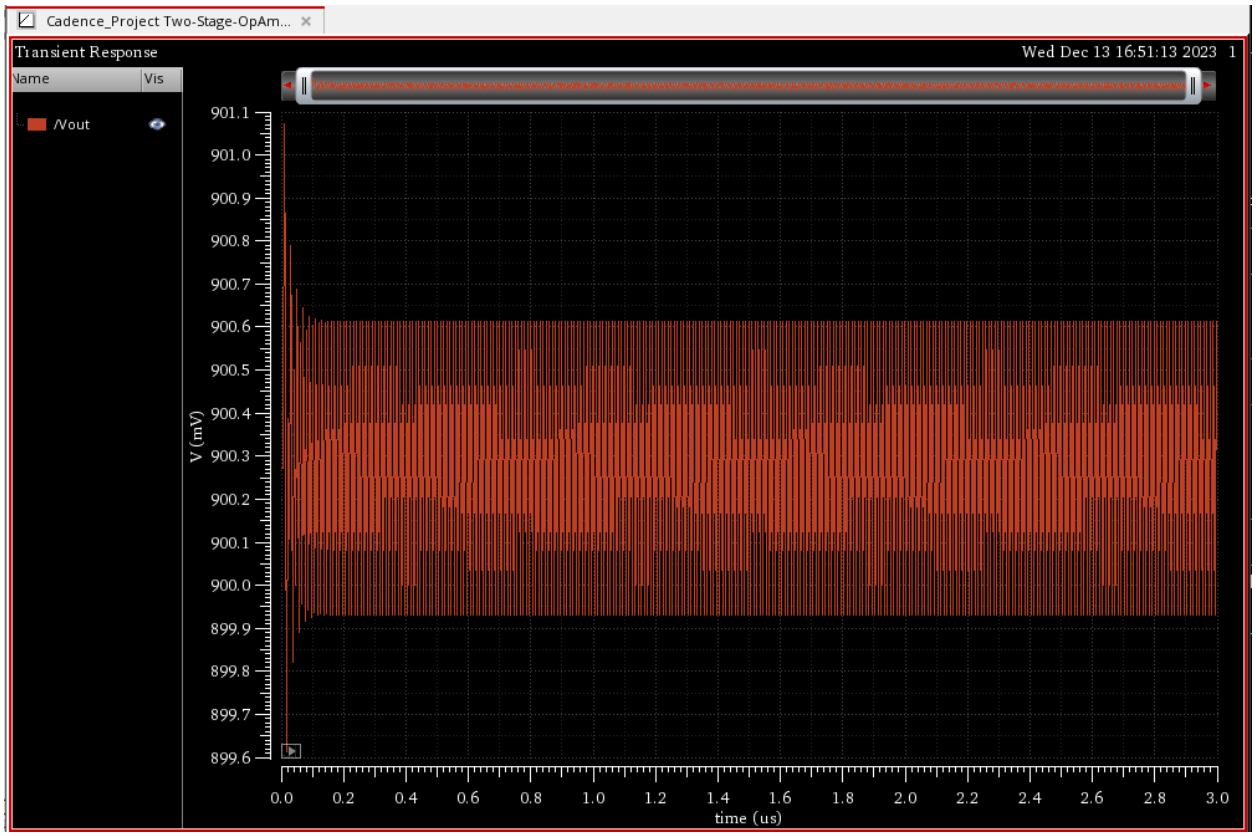
region=2
gm=66.21u
vds=-720m
vgs=-720m
ids=-11.05u
M3
net12
IRef
v=1.331
M4
ids=-11.04u
vgs=-720m
vds=-708.7m
gm=66.17u
region=2
net15
M6
ids=-113u
vgs=-708.7m
vds=-899.7m
gm=709.3u
region=2
Vout
cap=65f
CC
M1
ids=11.03u
vgs=701.8m
vds=881.5m
gm=72.13u
region=2
net11
region=2
gm=72.14u
vds=892.8m
vgs=701.5m
ids=11.02u
M2
net021
Vø
i=-143.5u
Vin+
i=-2.89n
region=2
gm=130.8u
vds=469.1m
vgs=469.1m
ids=8.399u
M8
net7
gnd!
M5
ids=22.04u
vgs=469.1m
vds=198.4m
gm=334u
region=2
M7
ids=113.3u
vgs=469.1m
vds=900.3m
gm=1.622m
region=2
CL
cap=1p
gnd
subc
sub!


Cadence_Project Two-Stage-OpAm...
Transient Response
Wed Dec 13 16:51:13 2023
Name
Vis
/Vout
V (mV)
time (us)
901.1
901.0
900.9
900.8
900.7
900.6
900.5
900.4
900.3
900.2
900.1
900.0
899.9
899.8
899.7
899.6
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0

In our transient simulation, our Vout (around 900 mV) is consistent across a wide range of frequencies, indicating that our system is stable and can provide a reliable output under various operating conditions. We have a smooth, and well controlled response without any excessive overshooting which indicates our design is theoretically stable.

6. A table summarizing the specifications

Specification	Value
Low Frequency Gain	60.05 dB
Gain Bandwidth	50.18 MHz
Input Common Mode Range (ICMR)	$0.69948 - 1.4$
Phase Margin	25°
Power Dissipation	$258.84\ \mu W$