



Course Name: Analog Electronics

Course Number and Section: 14:332:463

Experiment: Two Stage CMOS Op-Amp

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Description of your approach towards designing the two-stage op-amp, including equations and calculations of transistor's dimensions, DC current sources, capacitors, etc. (20 points)

Step 1.

We decided to choose $L = 1\mu\text{m}$

Step 2.

$$C_c > 0.22 * C_L \text{ where } C_L = 1\text{ pF}$$

$$C_c > 0.22 * 1\text{pF}$$

$$C_c > 0.22\text{ pF}$$

We can choose $C_c = 0.25\text{ pF}$

Step 3.

$$SR = \frac{I_{D5}}{C_c}$$

$$I_{D5} = SR * C_c \Rightarrow (100\text{ V}/\mu\text{s}) * (0.25\text{ pF}) = 25\mu\text{A}$$

$$I_{D5} = 22\mu\text{A}$$

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D5}}{2}$$

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 11\mu\text{A}$$

Step 4.

$$V_{IN,MAX} = [V_{DD} + V_{TH1}] - \left[\sqrt{\frac{I_{D5}}{\mu_P C_{ox} \left(\frac{W}{L}\right)_3}} + |V_{TH3}| \right]$$

Where $V_{TH1} = V_{THN}$, $V_{TH3} = V_{THP}$

$$1.4 = [1.8 + 0.345] - \left[\sqrt{\frac{22\mu A}{50\mu A * (\frac{W}{L})_3}} + 0.415 \right]$$

$$0.33 = \sqrt{\frac{22\mu A}{50\mu A * (\frac{W}{L})_3}}$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 4.35$$

$$gm_3 = gm_4 = \sqrt{2\mu_p c_{ox} \left(\frac{W}{L}\right)_3 I_{D3}}$$

$$gm_3 = gm_4 = \sqrt{2 * (50\mu A) * (4.35) * (11\mu A)} = 69.17369442\mu S$$

Step 5.

$$gm_1 = GB * C_c \Rightarrow 50MHz * 0.22pF * 2\pi$$

$$gm_1 = gm_2 = 69.11503838\mu S$$

$$gm_1 = \sqrt{2 * \mu_n c_{ox} * \left(\frac{W}{L}\right)_1 * I_{D1}}$$

$$69.11503838\mu S = \sqrt{2 * (250\mu A/V^2) * \frac{W}{L}_1 * (11\mu A)}$$

$$\frac{W}{L}_1 = 0.86852$$

So here we can estimate the $\frac{W}{L}_1 = \frac{W}{L}_2 \approx 1$

Step 6.

$$V_{IN,MIN} = V_{TH1} + \sqrt{\frac{I_{D5}}{\mu_n c_{ox} * \frac{W}{L}_1}} + \sqrt{\frac{2I_{D5}}{\mu_n c_{ox} * \frac{W}{L}_5}}$$

$$0.7 = 0.345 + \sqrt{\frac{22\mu A}{250\mu A * 0.987}} + \sqrt{\frac{2 * (22\mu A)}{250\mu A * \frac{W}{L}_5}}$$

$$\frac{W}{L}_5 = 130.74860$$

$$\text{Here we can estimate } \frac{W}{L}_5 \approx 131$$

Step 7.

using $gm_6 \geq 10gm_1$ decide a value for gm_6

$$gm_6 \geq 10 * 69.11503838\mu S$$

$$gm_6 \geq 691.1503838\mu S$$

Step 8.

$$V_{SG4} = V_{SG6}$$

$$\frac{gm_6}{gm_4} = \frac{\frac{W}{L}_6}{\frac{W}{L}_4}$$

$$\frac{691.1503838\mu S}{69.17369442\mu S} = \frac{\frac{W}{L}_6}{4.35}$$

$$\frac{W}{L}_6 = 43.46311405$$

$$gm_6 = \sqrt{2 * \mu_{P_{ox}} * \frac{W}{L}_6 * I_{D6}}$$

$$691.1503838\mu s = \sqrt{2 * 50\mu A * 43.46 * I_{D6}}$$

$$I_{D6} = 119.4\mu A$$

$$I_{D6} = I_{D7} = 119.4\mu A$$

Step 9.

$$\frac{I_{D7}}{I_{D5}} = \frac{\frac{W}{L}_7}{\frac{W}{L}_5}$$

$$\frac{119.4\mu A}{22\mu A} = \frac{\frac{W}{L}_7}{130.74860}$$

$$\frac{W}{L}_7 = 709.6083109$$

We also need to find $\frac{W}{L}_8$

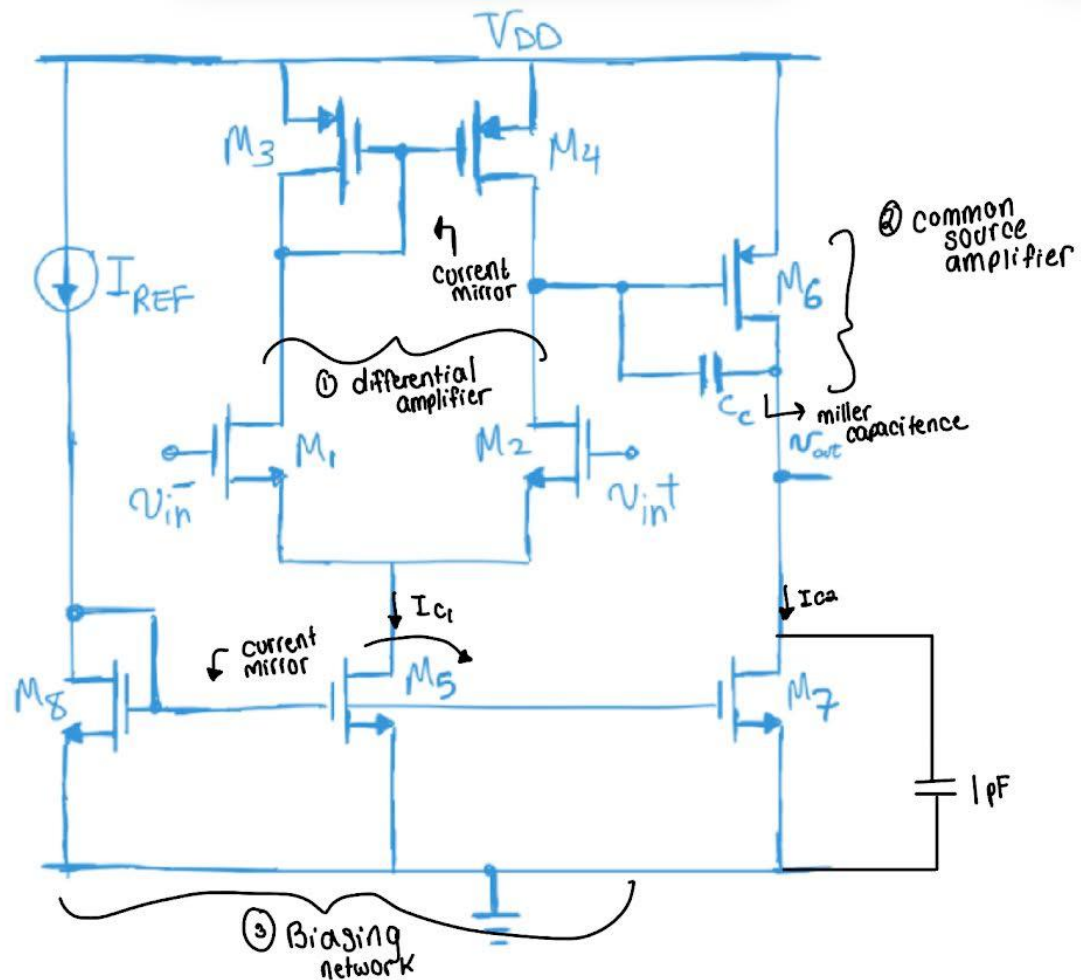
$$\frac{I_{D8}}{I_{D7}} = \frac{\frac{W}{L}_8}{\frac{W}{L}_7} \text{ where } I_{REF} = I_{D8} \text{ and we'll assume that } I_{REF} = 10\mu A$$

$$\frac{10\mu A}{119.4\mu A} = \frac{\frac{W}{L}_8}{709.6083}$$

$$\frac{W}{L}_8 = 59.43118182$$

Some FETs were in subthreshold or triode region, and so we had to make more adjustments to the $\frac{W}{L}$ ratios, dominant pole compensation capacitance, and the input bias current.

Transistor-level schematic of your op-amp. Identify the functionality of each part. For example, stage 1 of amplification, stage 2 of amplification, current mirrors, etc.



The above circuit is a two-stage CMOS Op-Amp.

1. The middle segment of the circuit (denoted as 1) functions as the input stage and comprises the differential amplifier, consisting of M_1 to M_5 . Within this configuration, a MOS differential pair operates with a current-mirror load. Additionally, a differential input exists between M_1 and M_2 , contributing to both voltage gain and high input resistance (due to no current going through the gate terminal). The drain terminal of M_4 is linked to a single-ended output, offering common-mode rejection properties.
2. The rightmost part of the circuit (labeled 2) is the output-stage. This consists of M_6 and M_7 . In this stage, there is a common source amplifier with a current source load. M_7 is the active load, supplying constant current. This stage provides voltage gain and high output resistance.
3. The bottom section of the circuit represents the biasing network. M_8 , M_5 , and M_7 are in a current mirror arrangement. The bias current of the input differential pair is provided by M_5 . The bias current of the second stage is provided by M_7 .

The capacitor helps make the circuit more stable in terms of poles and phase margins.

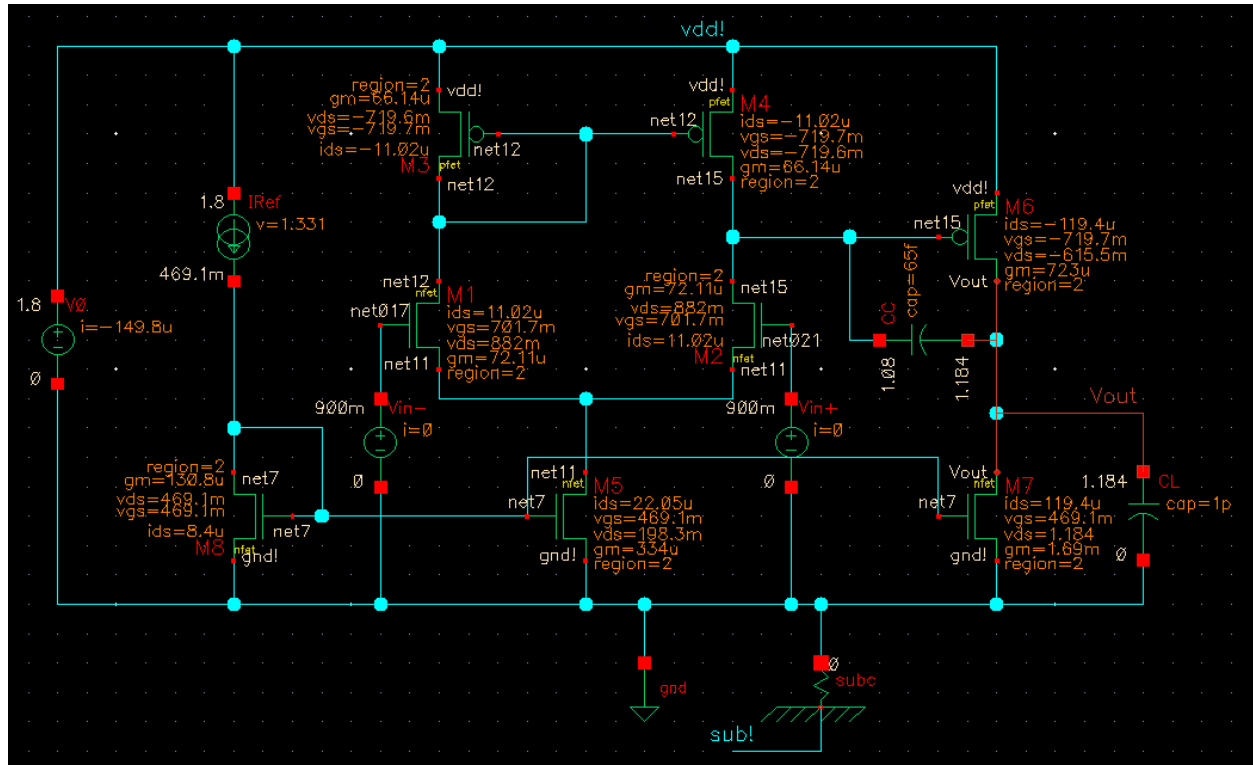
A table summarizing dimensions of the transistors (W/L) and value of resistors and capacitors used in your circuit.

MOSFET	Adjusted $\frac{W}{L}$ ratio
M1 = M2	1
M3 = M4	4.35
M5	15.2
M6	46
M7	59.7
M8	6

Simulation Results:

1. DC Analysis

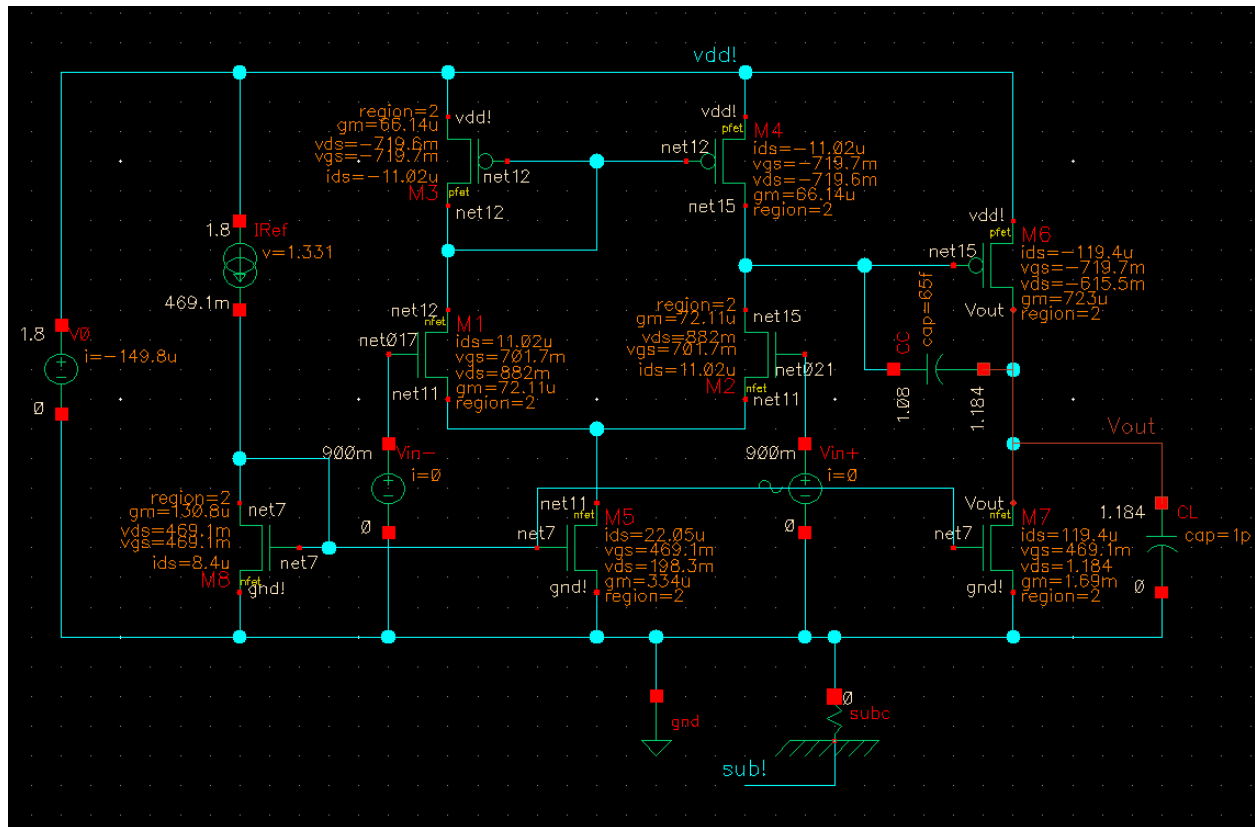
We produced this schematic using the adjusted $\frac{W}{L}$ ratios, where all the MOSFETs are in the saturation region (region 2) and for Vout we got 1.184V.

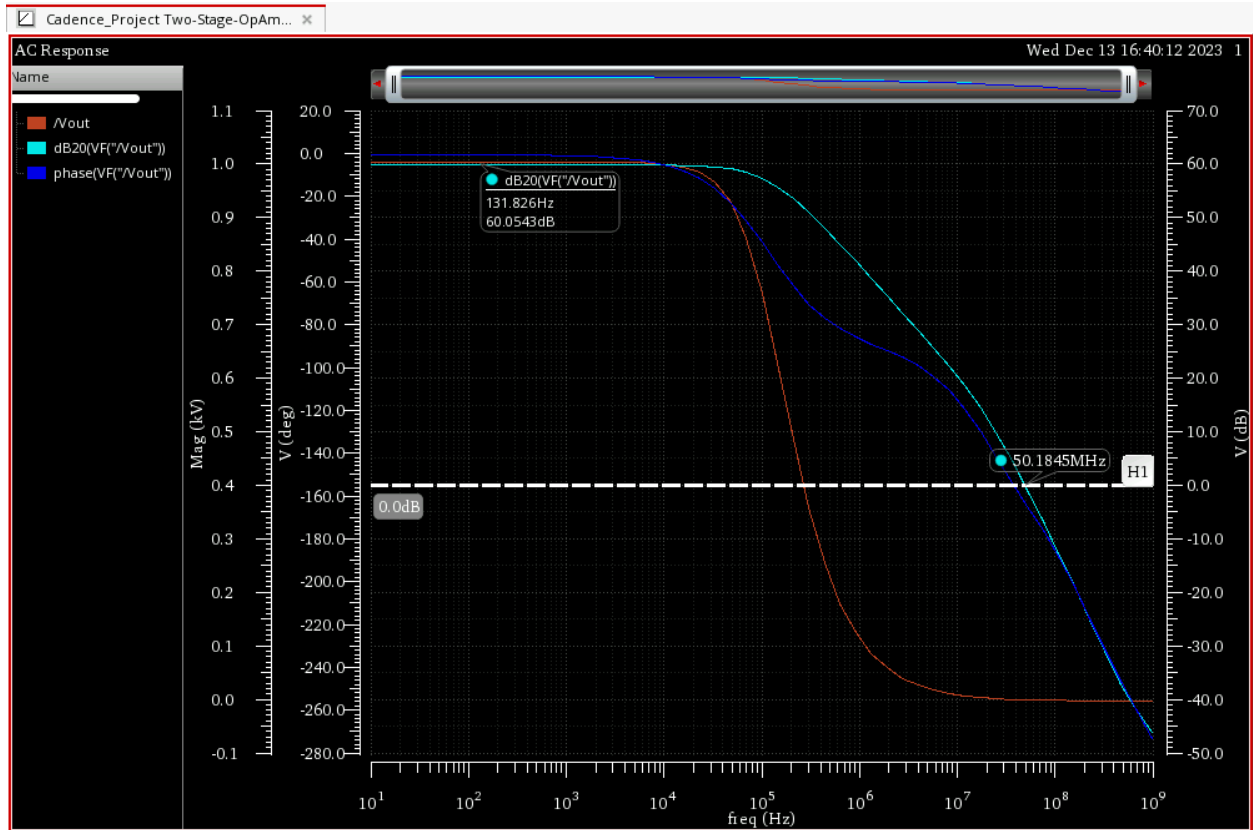


2. AC Analysis

For our schematic we had to make adjustments to our input bias current, dominant pole compensation capacitor, and the $\frac{W}{L}$ ratio of the output transistor (M6). We increased the $\frac{W}{L}$ ratio for the output transistor allowing us to shift our pole to a lower frequency on the bode plot allowing us to meet the required gain bandwidth, however doing so also made us decrease our input bias current. Reducing the compensation capacitance also helped us achieve 60dB for our low frequency voltage gain. Below is our schematic with all adjustments done, and our bode plot for the AC analysis where we show that we obtained a 60.05dB, 50.18MHz, and a 25° phase margin.

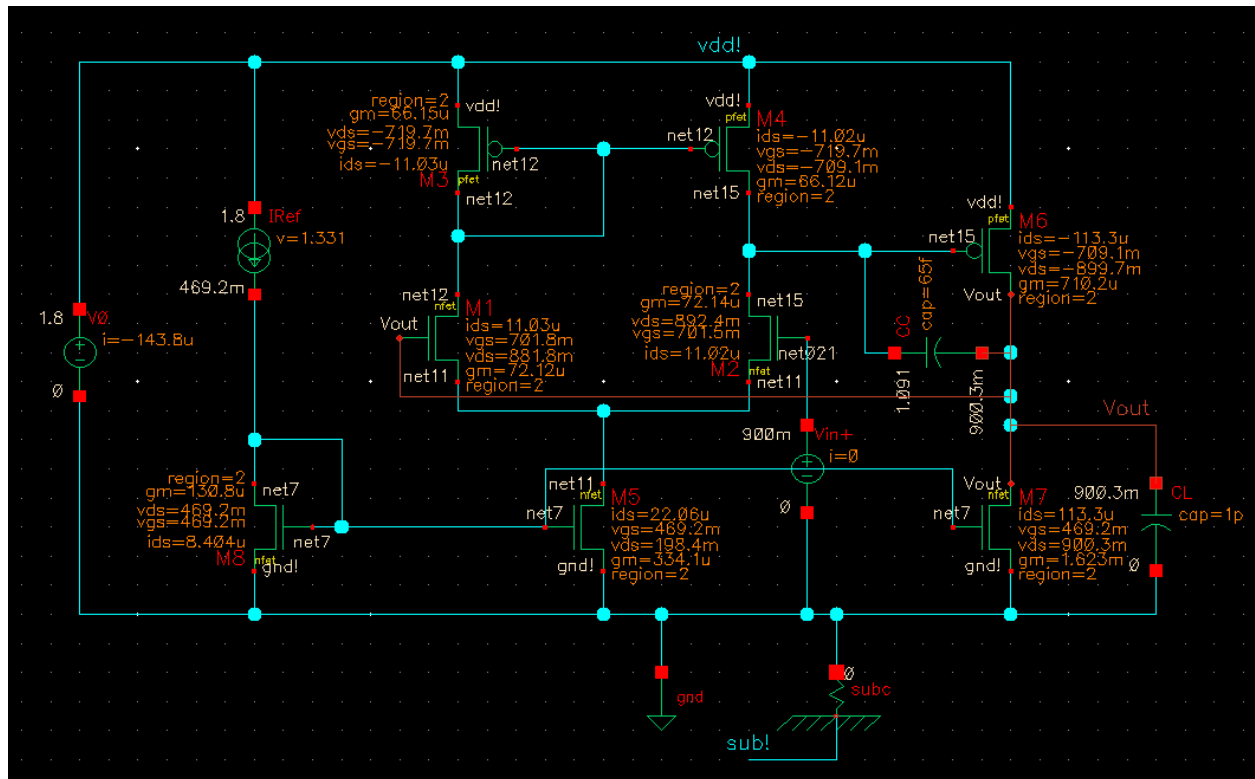
Additionally, in our simulations, we noticed that there was an intricate relationship between bandwidth, voltage gain, and phase margin. As we fine-tuned these parameters, it became evident that decreasing both the bandwidth and voltage gain increases the phase margin. For instance, in another design, we had the voltage gain, bandwidth, and phase margin at 57.35 dB, 42.05 MHz, and 50°, respectively. This highlights the inherent trade-offs in analog circuits to achieve the most effective solution for any application. Our optimized solution, 60.05dB, 50.18MHz, and a 25° phase margin, showed the most stability for this assignment.

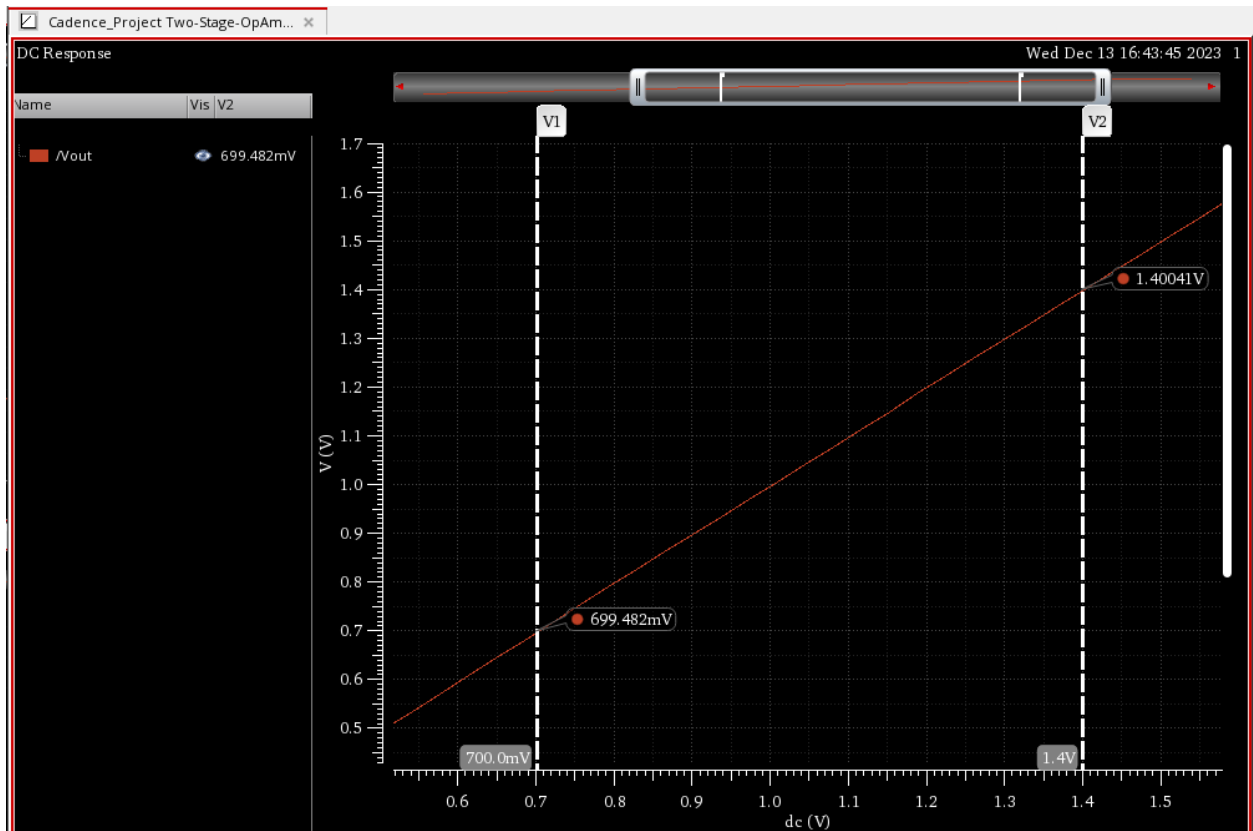
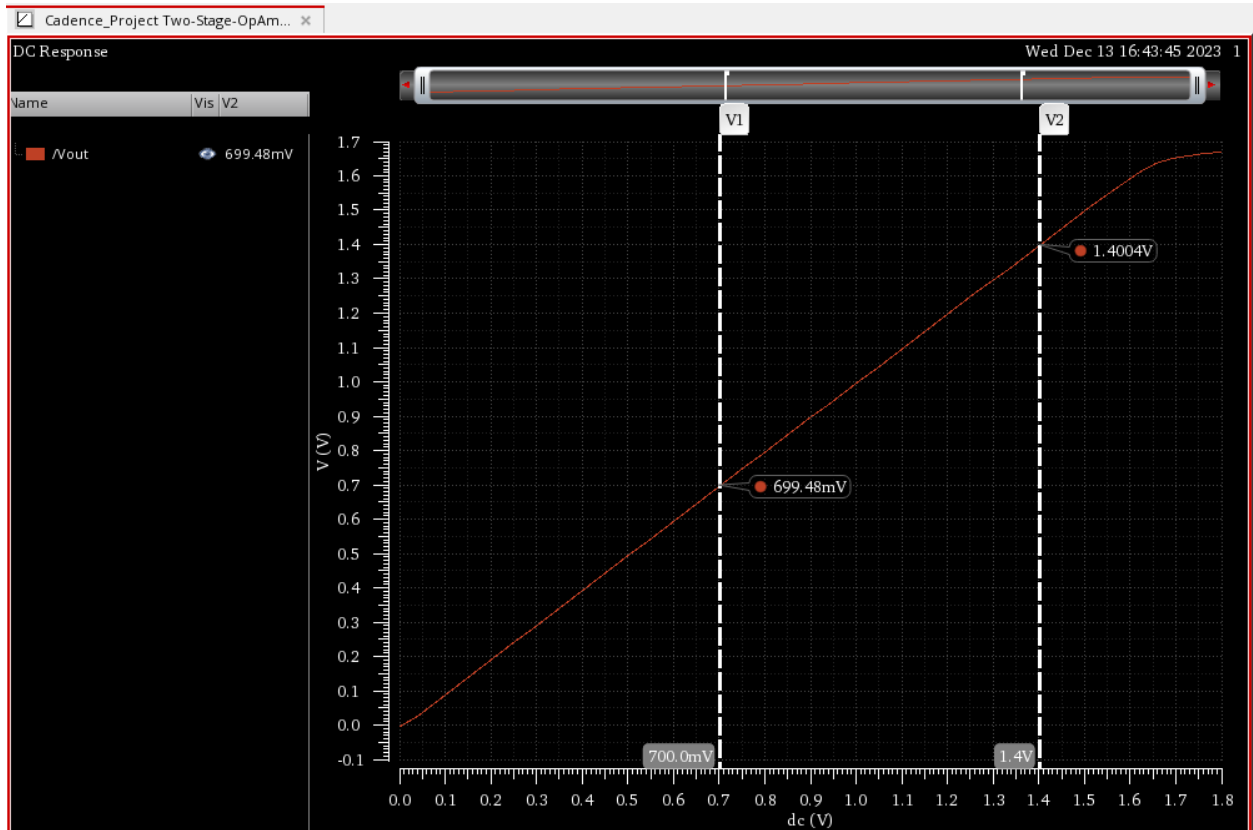




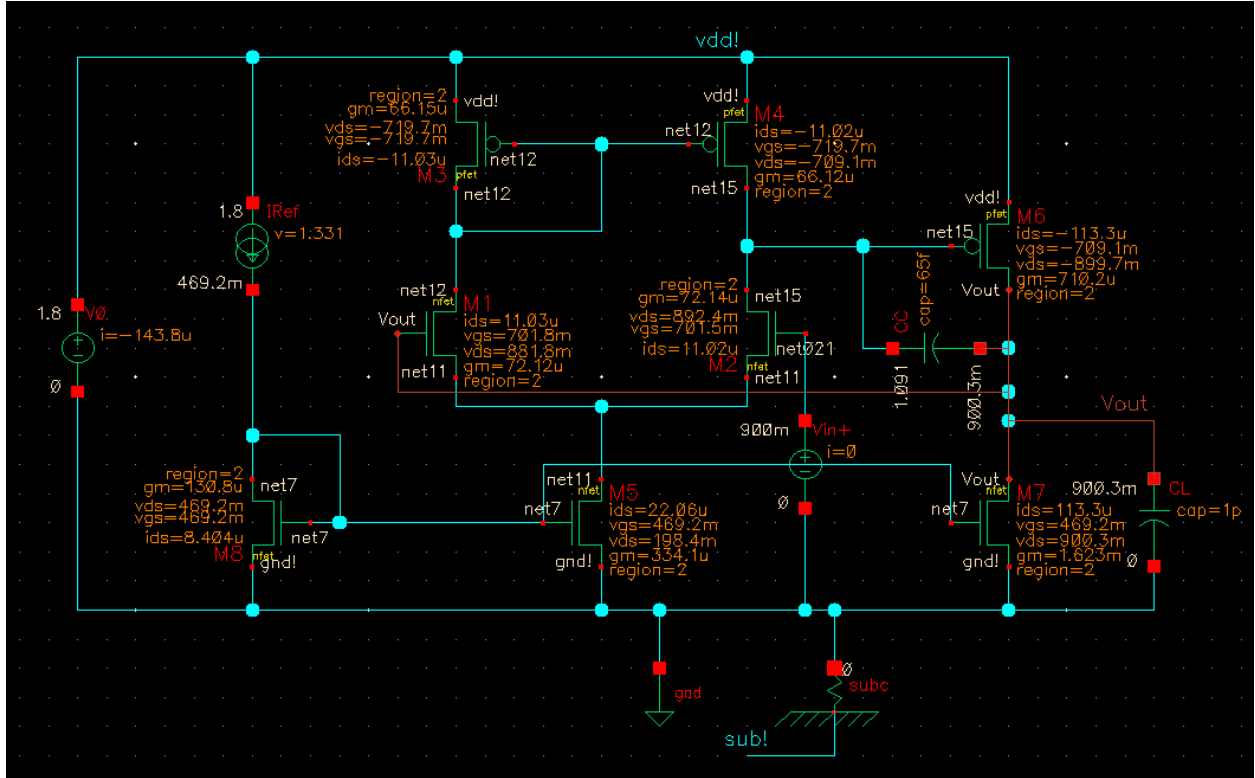
3. Measure Input Common Mode Range (ICMR)

Below we have our schematic that's been configured as a unity-gain buffer. Our closed loop gain is set to 1, and so the output voltage should be identical to the input voltage. From our V_{out} vs V_{in} plot, we can see that the slope is essentially equal to one. The ICMR range is 0.69948V to 1.4V meaning our numbers indeed meet the requirements.





4. Power Dissipation

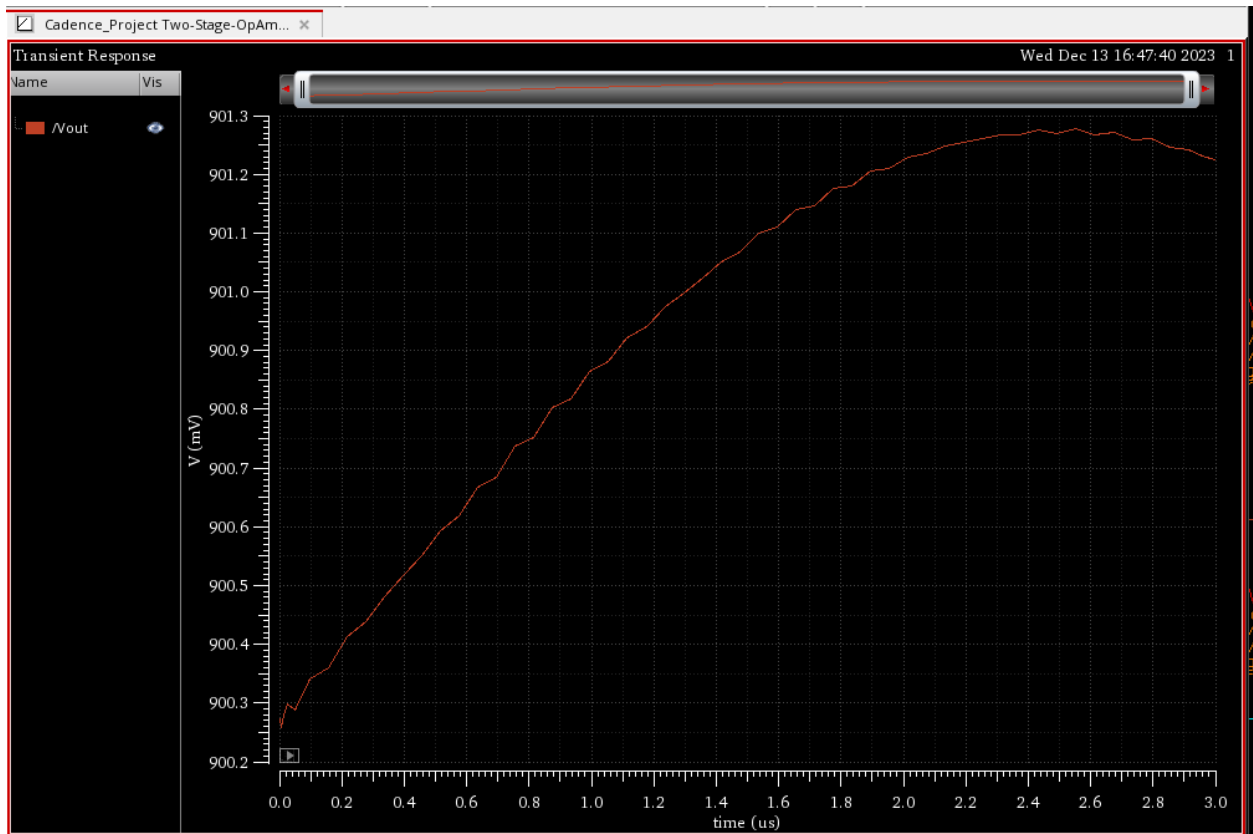
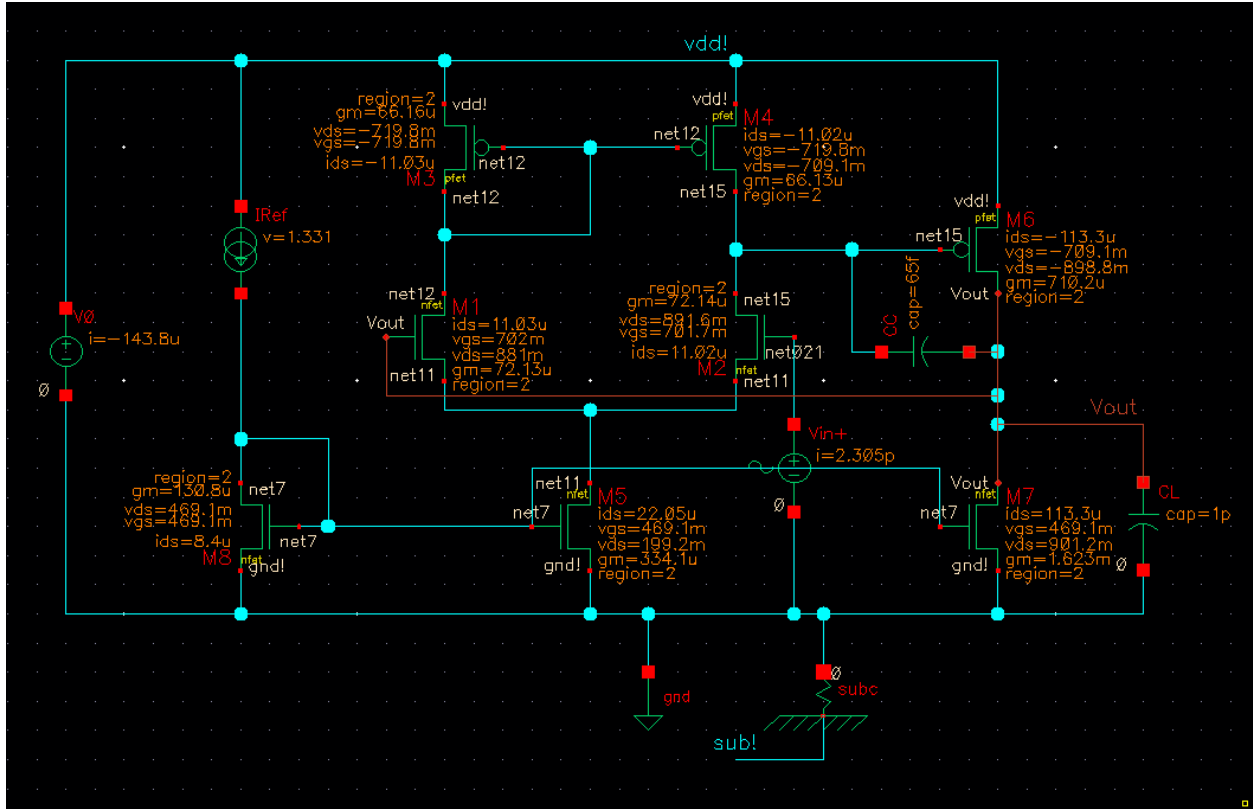


$$P_{diss} = (1.8V * 143.8\mu A) = 258.84\mu W$$

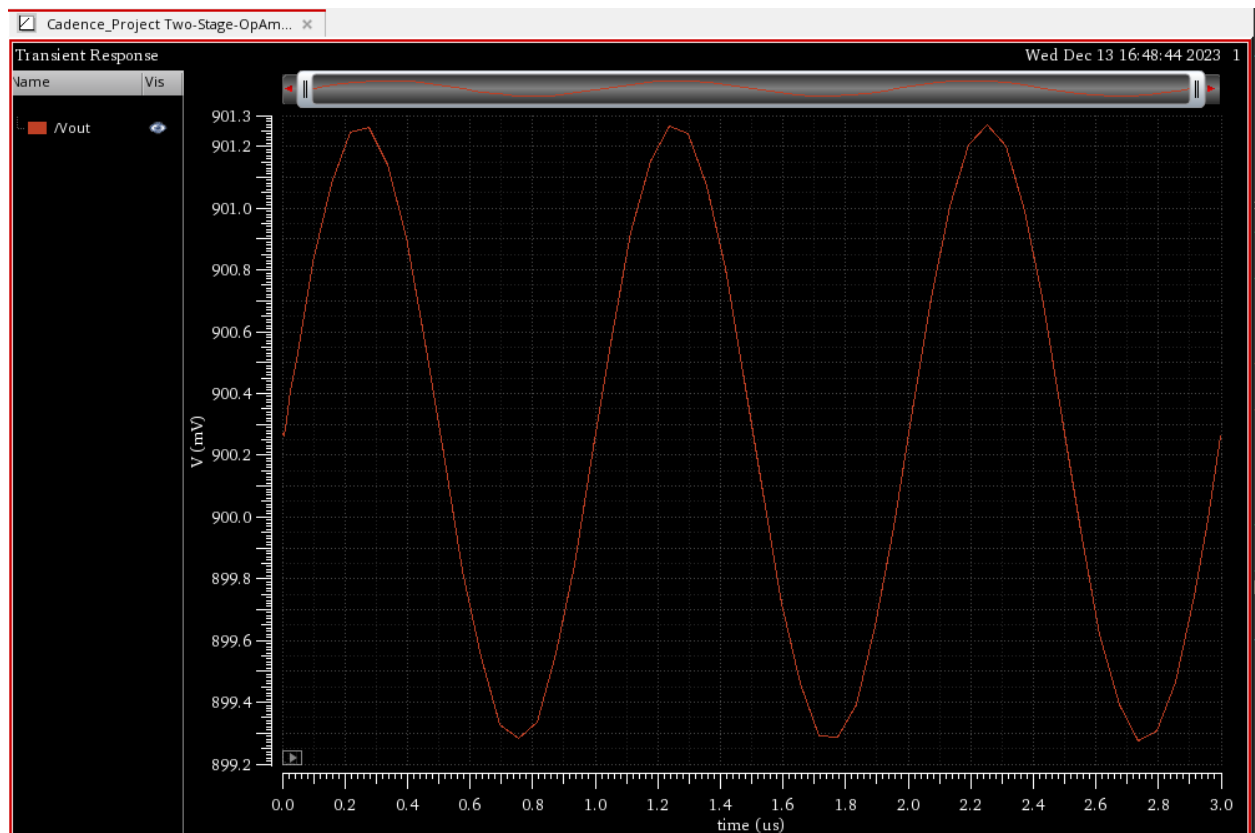
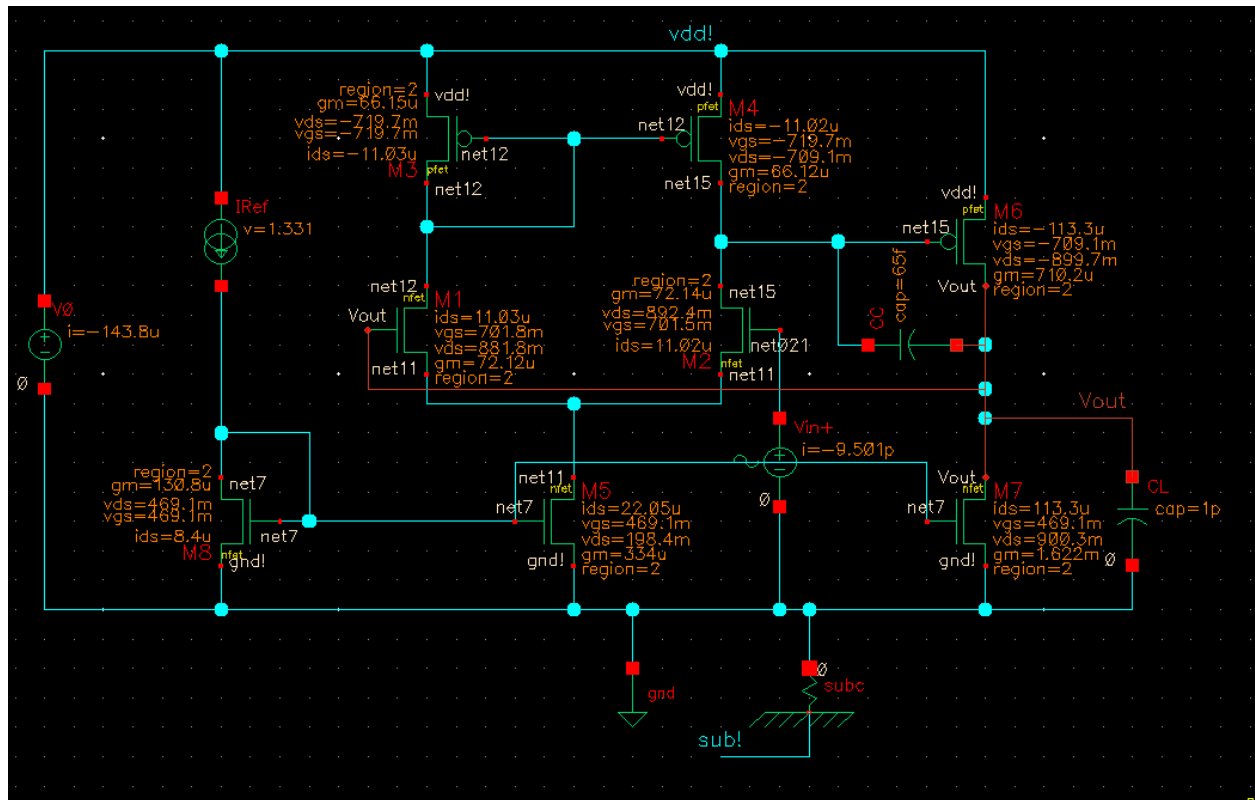
The power dissipation is 258.84 μ W

5. Transient Simulation

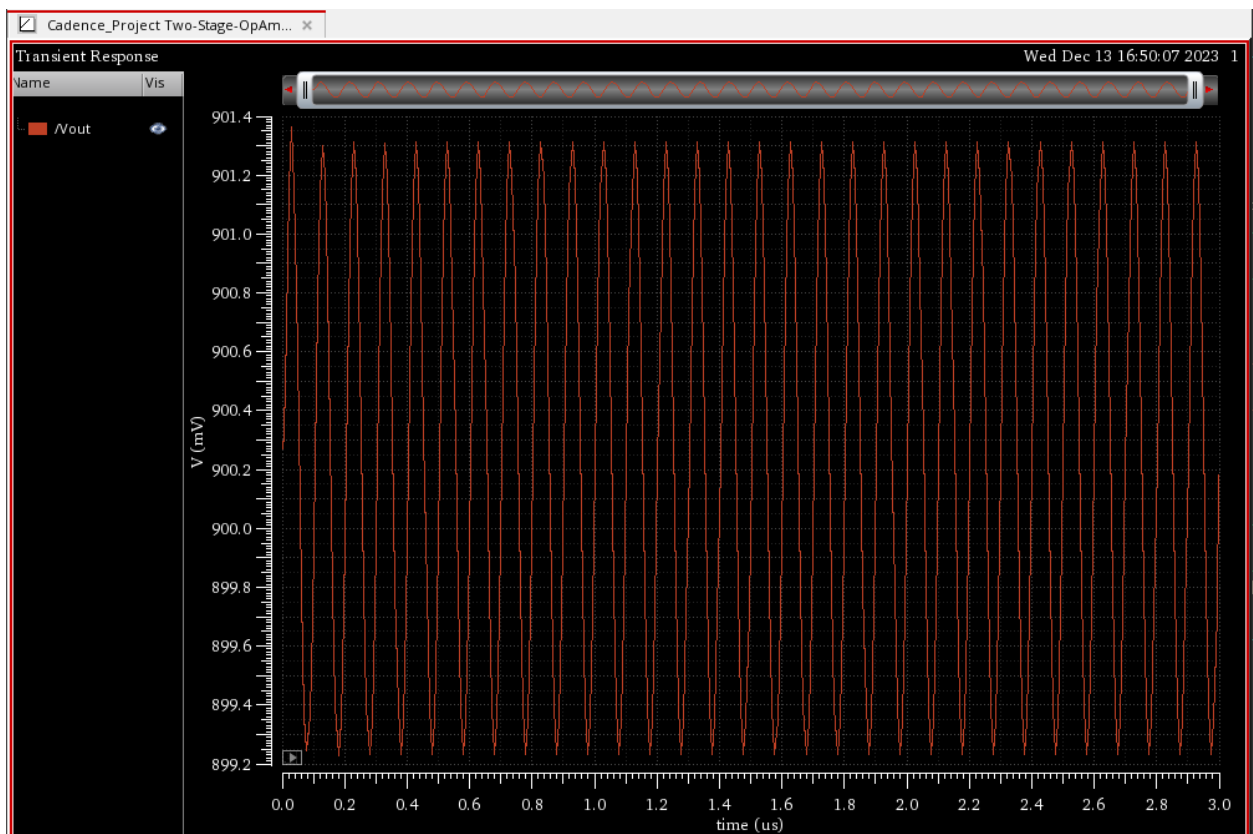
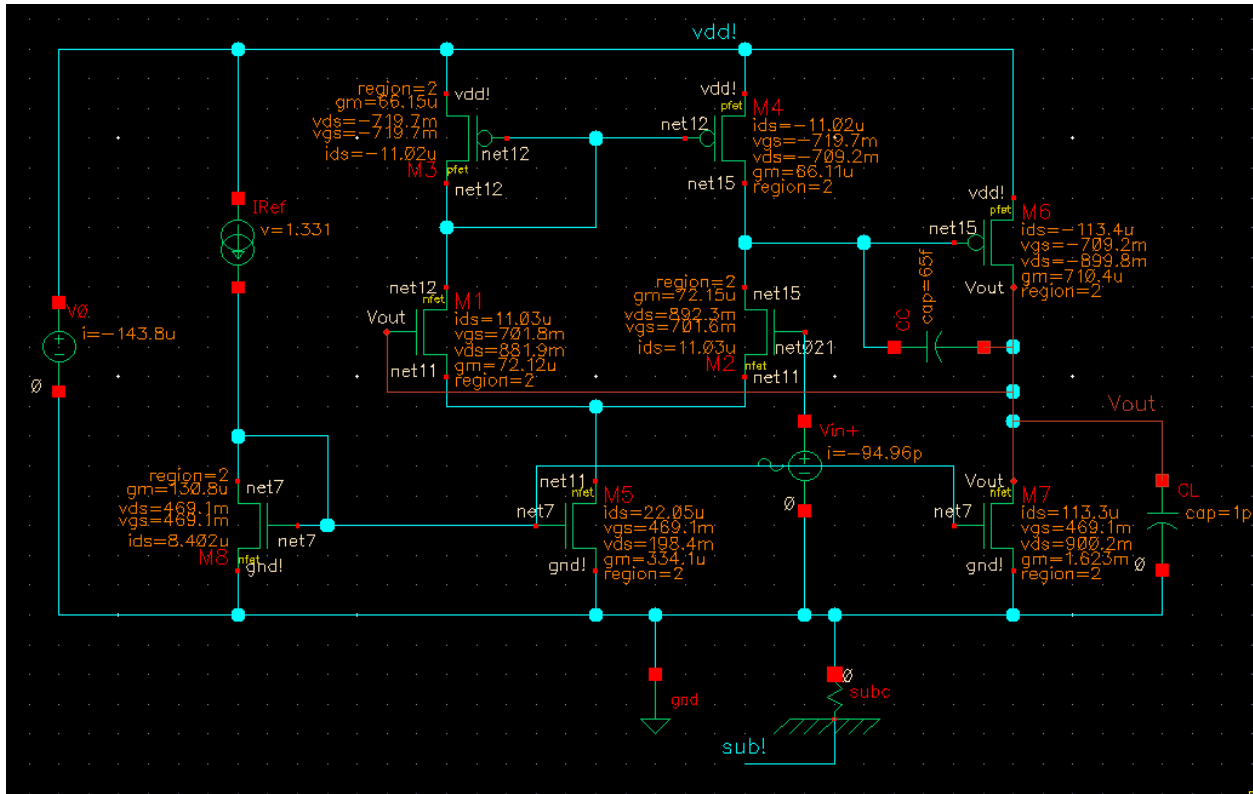
100KHz



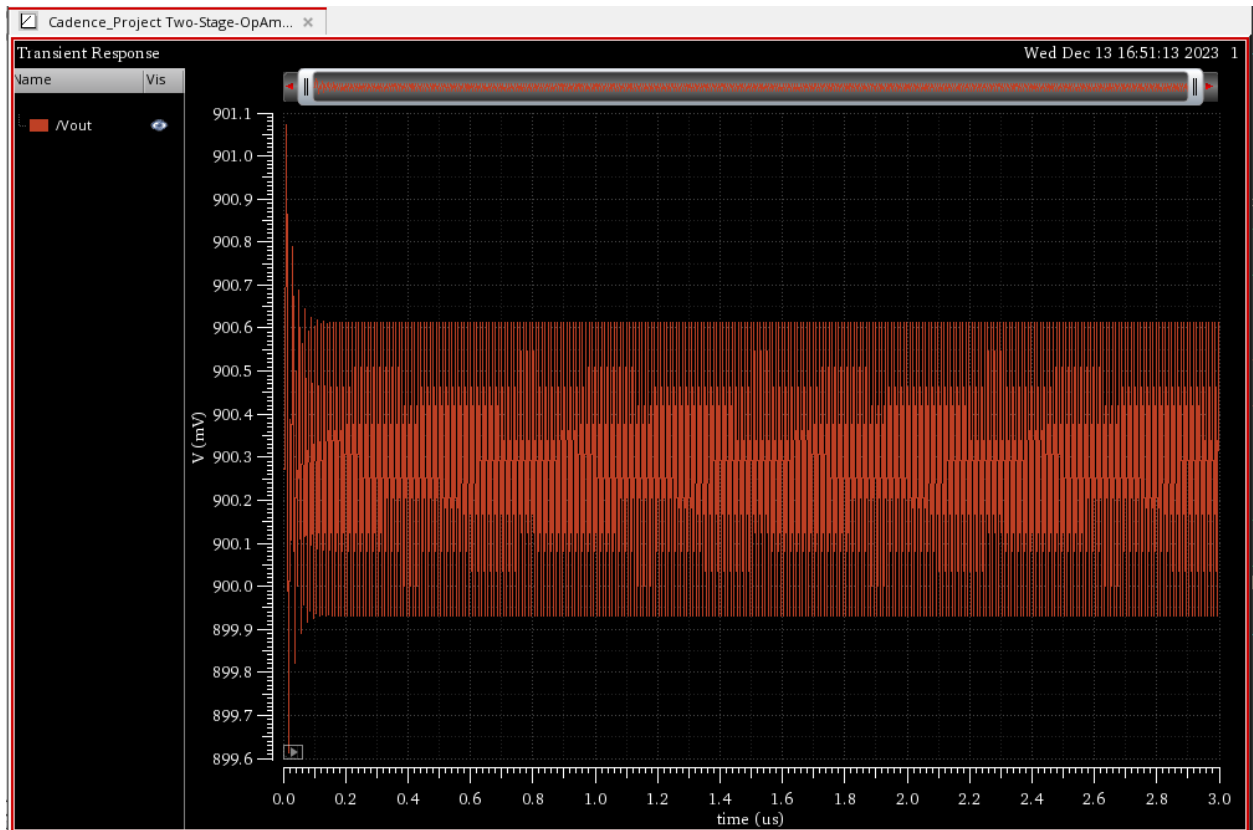
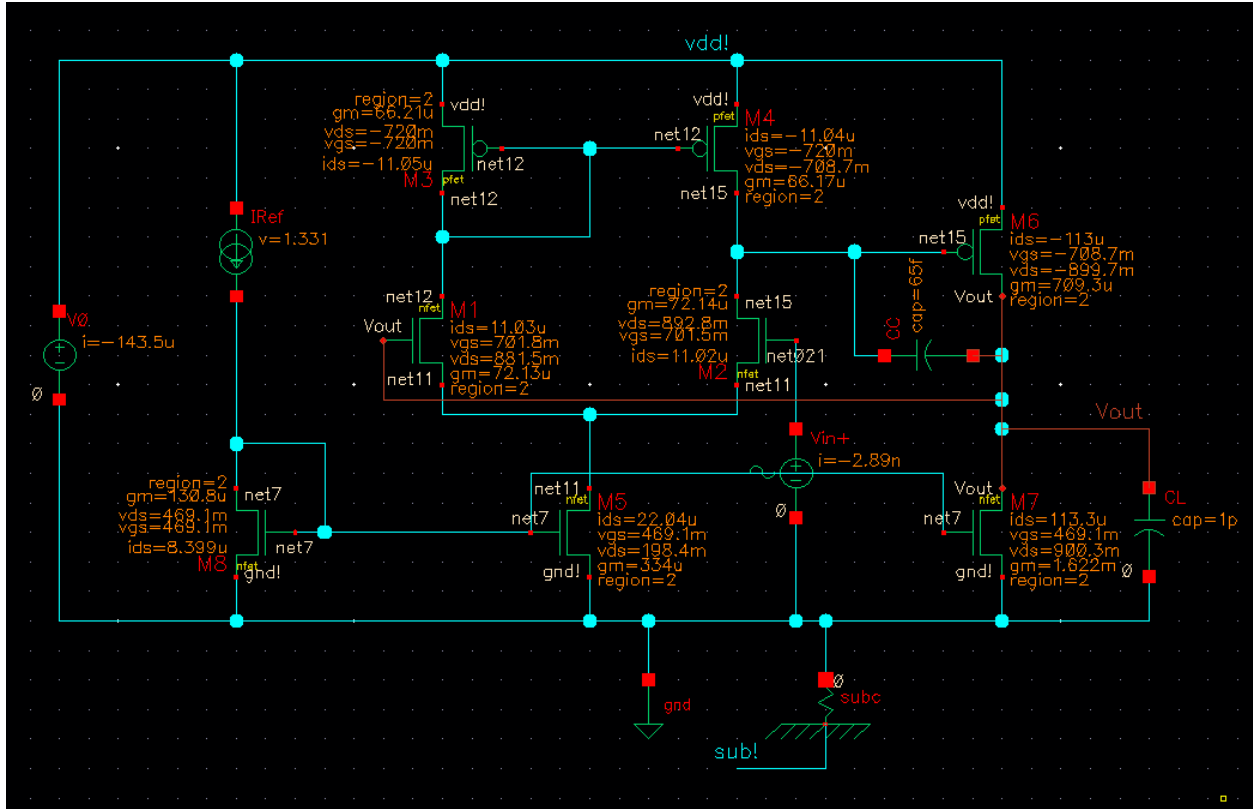
1 MHz (Next Page)



10 MHz (Next Page)



100MHz (Next Page)



In our transient simulation, our V_{out} (around 900 mV) is consistent across a wide range of frequencies, indicating that our system is stable and can provide a reliable output under various operating conditions. We have a smooth, and well controlled response without any excessive overshooting.

6. A table summarizing the specifications

Specification	Value
Low Frequency Gain	60.05 dB
Gain Bandwidth	50.18 MHz
Input Common Mode Range (ICMR)	0.69948 – 1.4
Phase Margin	25°
Power Dissipation	258.84 μW