TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
PULCHOWK CAMPUS

LAB REPORT

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Submitted To:
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Basic Gates: AND, OR, NOT Gates; Universal Gates: NAND, NOR Gates and XOR, XNOR Gates truth verifications.

1 Objectives

- To investigave differents gates.
- Veriy the truth table of the different gates.
- Construction and verification of three input AND gate using two input AND gate
- Construction and verification of four input OR gate using two input OR gates.
- To connenct interter gates in series in odd numbers and even numbers and observe thir property.

2 Theory

Logic gates are the basic building blocks of any digital system. Logic gate is an electronic circuit having one or more than one input and only one output. The relationship between the input and the ouput is based on a certain logic.
Logic gates perform some primary boolean operations and by combining various different logic gates, complex boolean functions can be implemented.

2.1 AND Gate

A gate that performs the logical AND operation is called AND Gate.It takes two or more inputs. The output of AND gate is high only when all the inputs are high. The logic is represented by dot(.) sign. For two inputs A and B, the output is written as $Y = A.B$.

Figure 1: AND Gate

A	B	$Y = A.B$
0	0	0
0	1	0
1	0	0
1	1	1

Table 1: Truth Table

2.2 OR Gate

A gate that performs the logical OR operation is called OR Gate. It takes two or more inputs. The output of OR gate is high when any one of the inputs is high. The logic is represented by plus(+) sign. For two inputs A and B, the output is written as $Y = A+B$.

Figure 2: OR Gate

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

Table 2: Truth Table

2.3 NOT Gate

A gate that performs the logical NOT operation is called NOT Gate. The output of NOT gate is high when the input is low and ouput is low when the input is high. It is a single input gate. The logic is represented by a complement symbol('). For a input A, the output is written as $Y = A'$

Figure 3: NOT Gate

A	$Y = A'$
0	1
1	0

Table 3: Truth Table

2.4 NAND Gate

A gate that performs the logical AND followed by NOT operation is called NAND Gate. It takes two or more inputs and gives one output. The output is high when any one of the input is low. It is one of the universal gates. For two inputs A and B, the output is written as $Y = (A.B)'$.

Figure 4: NAND Gate

A	B	$Y = (A.B)'$
0	0	1
0	1	1
1	0	1
1	1	0

Table 4: Truth Table

2.5 NOR Gate

A gate that perform the logical OR followed by NOT operation is called NOR Gate. It takes in two or more inputs and gives one output. The output is high only when none of the inputs are high. It is one of the universal gates. For two inputs A and B, the output is written as $Y = (A + B)'$

Figure 5: NOR Gate

A	B	$Y = (A + B)'$
0	0	1
0	1	0
1	0	0
1	1	0

Table 5: Truth Table

2.6 XOR Gate

Xor gate is a special type of gate. It performs the exclusive or operation of the input. It is also known as the even parity as the output is high only only when odd number of inputs are high. For two inputs A and B, the output is written as $Y = A \oplus B$.

Figure 6: XOR Gate

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Table 6: Truth Table

2.7 XNOR Gate

XNOR is a special type of gate. It perfroms the exclusive nor operation on the input. It is also knows as odd parity as the ouput is high only when even number of inputs are high. For two inputs A and B, the output is written as $Y = (A \oplus B)'$.

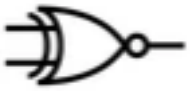

Figure 7: XNOR Gate

A	B	$Y = (A \oplus B)'$
0	0	1
0	1	0
1	0	0
1	1	1

Table 7: Truth Table

3 Lab

3.1 Materials Required

1. And Gate
2. Or Gate
3. Not Gate
4. Nand Gate
5. Nor Gate
6. Xor Gate
7. Xnor Gate
8. Logic probes
9. Logic State
10. Proteus

3.2 Observations

3.2.1 AND gate

A AND gate was connection to logic probe and logic states and its behaviour was observed. The circuit and truth table obtained are listen below.

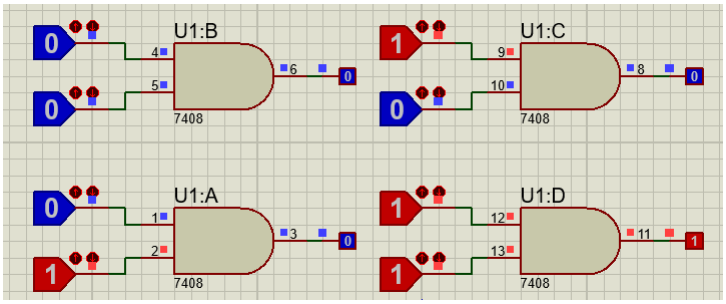

Figure 8: AND Gate

A	B	$Y = A.B$
0	0	0
0	1	0
1	0	0
1	1	1

Table 8: Truth Table

3.2.2 3 Input AND Gate

A 3 input AND gate can be constructed by using two and gates. In a 3 input AND gate, the output is high only when all 3 inputs are high.

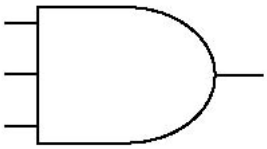

Figure 9: 3 Input AND Gate

A	B	C	$Y = A.B.C$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 9: Truth Table

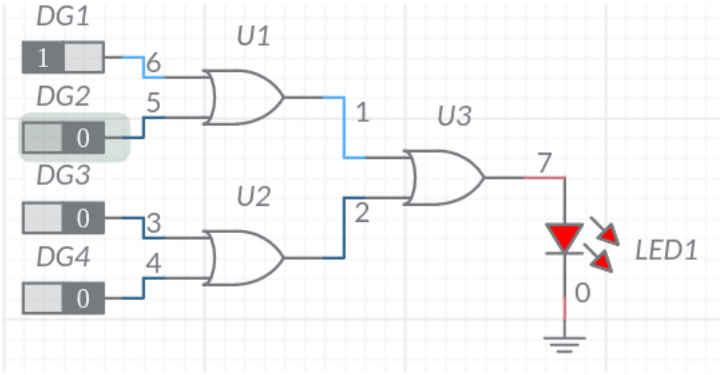

Figure 10: 4 Input OR

3.2.3 OR gate

A OR gate was connection to logic probe and logic states and its behaviour was observed. The circuit and truth table obtained are listen below.

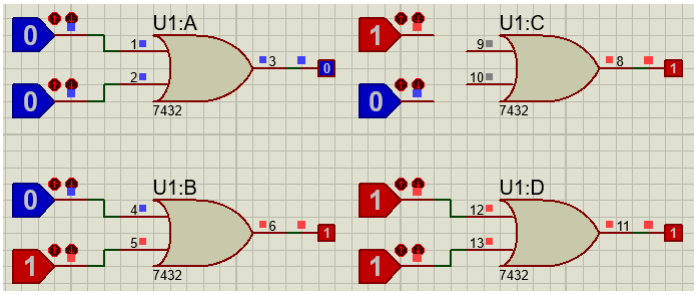

Figure 11: OR Gate

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

Table 10: Truth Table

3.2.4 4 Input OR Gate

A 4 input OR gate can be constructed using three 2 input OR Gates. The output of the gate is high when any one of the inputs is high.

Figure 12: 4 Input OR Gate

A	B	C	D	$Y = A + B + C + D$
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 11: Truth Table

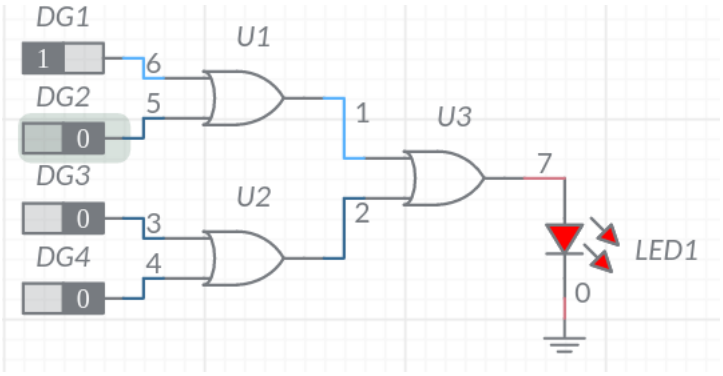

Figure 13: 4 Input OR

3.2.5 NOT gate

A NOT gate was connection to logic probe and logic states and its behaviour was observed. The circuit and truth table obtained are listen below.

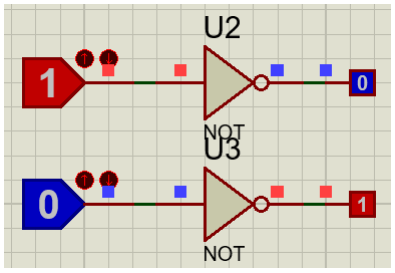

Figure 14: NOT Gate

A	$Y = A'$
0	1
1	0

Table 12: Truth Table

3.2.6 NAND gate

A NAND gate was connection to logic probe and logic states and its behaviour was observed. The circuit and truth table obtained are listen below.

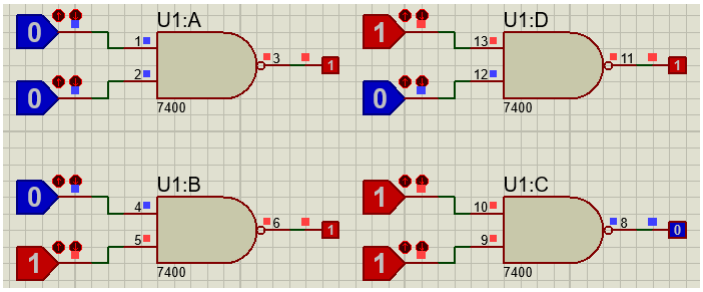

Figure 15: NAND Gate

A	B	$Y = (A.B)'$
0	0	1
0	1	0
1	0	0
1	1	0

Table 13: Truth Table

3.2.7 NOR gate

A NOR gate was connection to logic probe and logic states and its behaviour was observed. The circuit and truth table obtained are listen below.

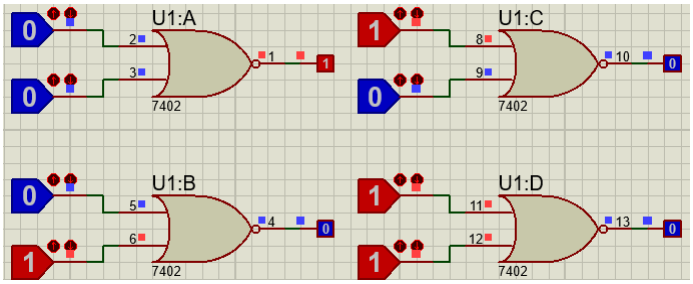

Figure 16: NOR Gate

A	B	$Y = (A + B)'$
0	0	1
0	1	1
1	0	1
1	1	0

Table 14: Truth Table

3.2.8 XOR gate

A XOR gate was connection to logic probe and logic states and its behaviour was observed. The circuit and truth table obtained are listen below.

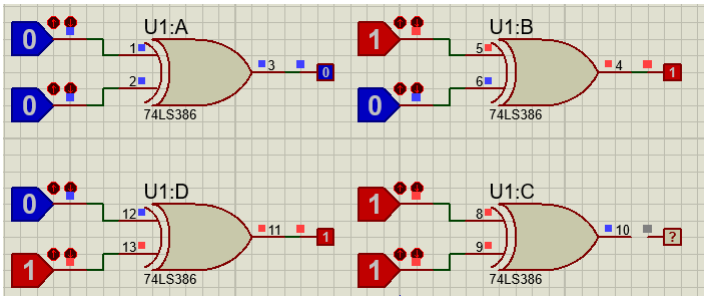

Figure 17: XOR Gate

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Table 15: Truth Table

3.2.9 XNOR gate

A XNOR gate was connection to logic probe and logic states and its behaviour was observed. The circuit and truth table obtained are listen below.

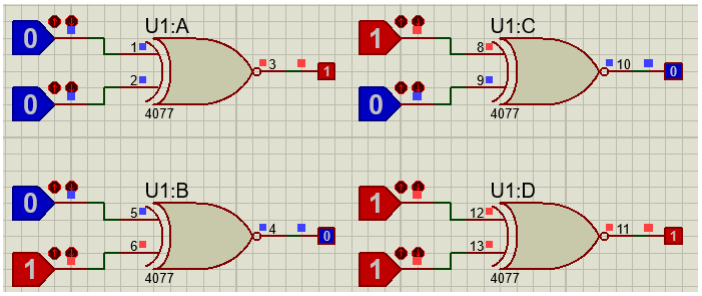

Figure 18: XNOR Gate

A	B	$Y = (A \oplus B)'$
0	0	1
0	1	0
1	0	0
1	1	1

Table 16: Truth Table

3.3 Realization of gates using Universal Gates

3.3.1 NAND gate

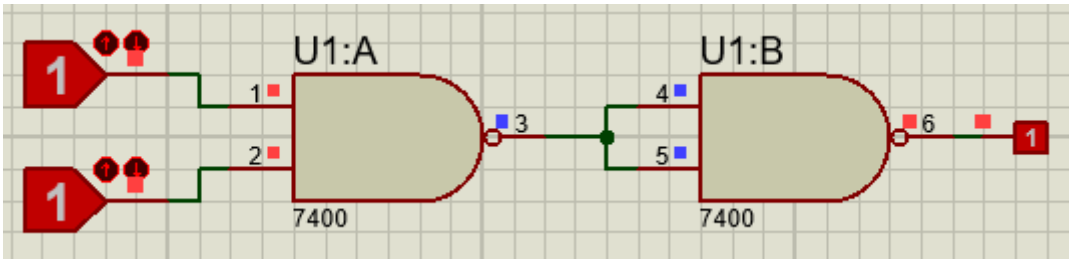

Figure 19: AND from NAND Gate

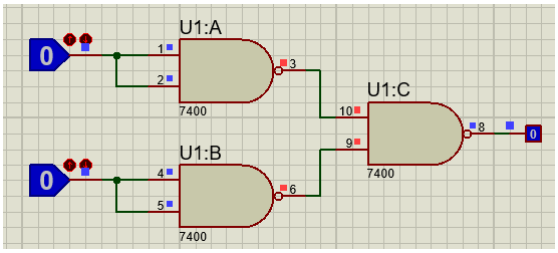

Figure 20: or from NAND Gate

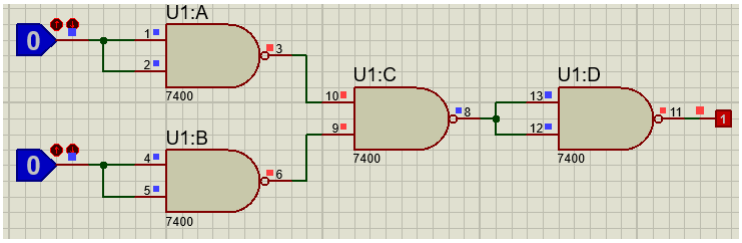

Figure 21: nor from NAND Gate

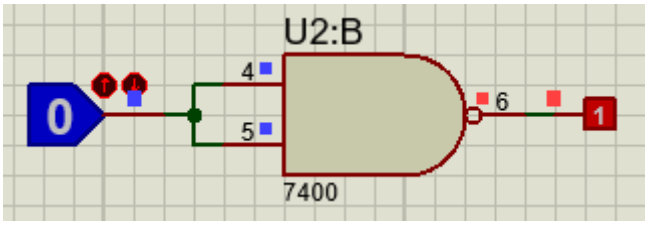

Figure 22: NOT from NAND Gate

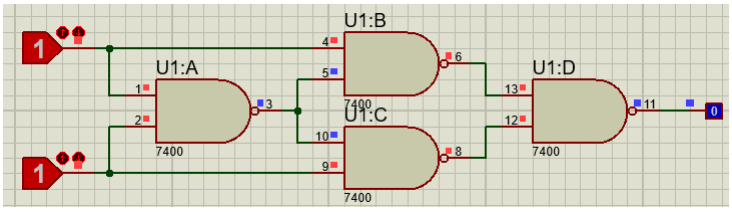

Figure 23: XOR from NAND Gate

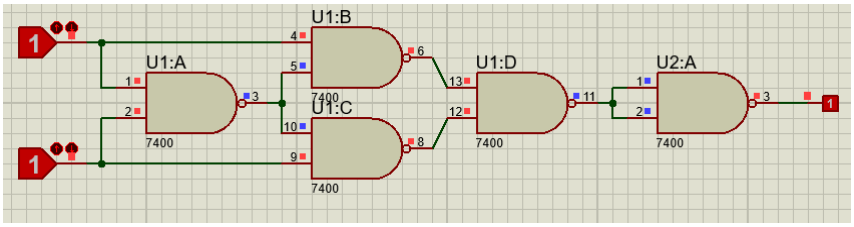

Figure 24: XNOR from NAND Gate

3.3.2 NOR gate

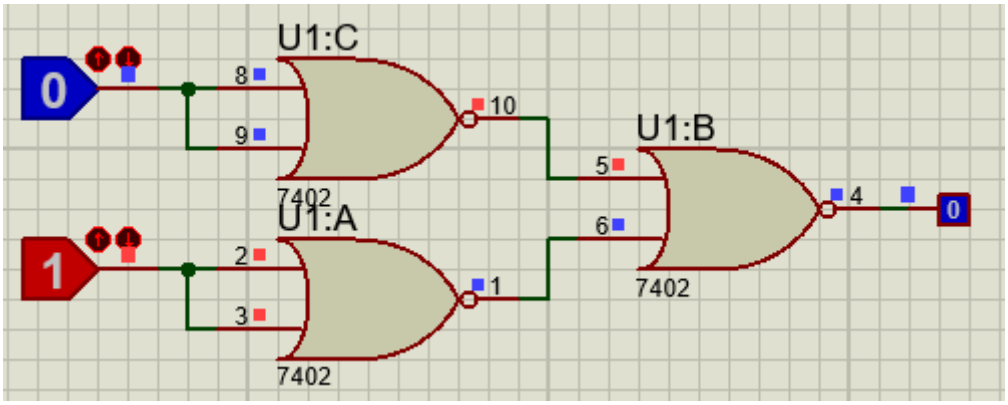

Figure 25: AND from NOR Gate

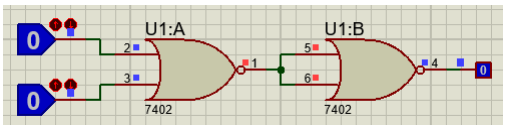

Figure 26: OR from NOR Gate

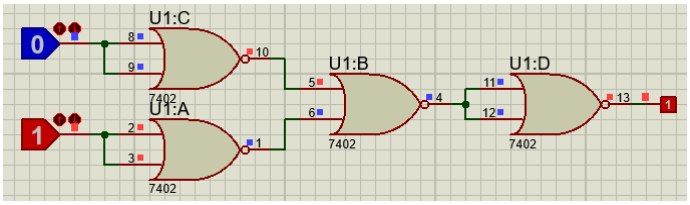

Figure 27: NAND from NOR Gate

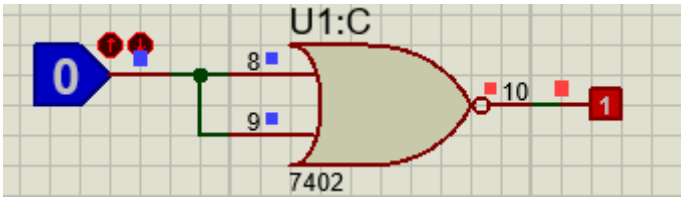

Figure 28: NOT from NOR Gate

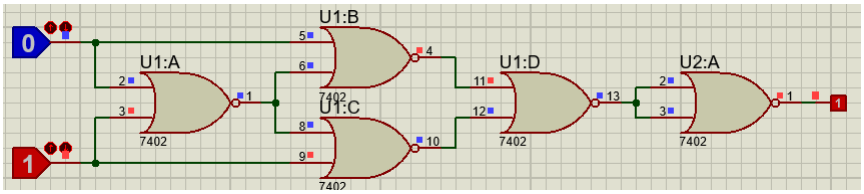

Figure 29: XOR from NOR Gate

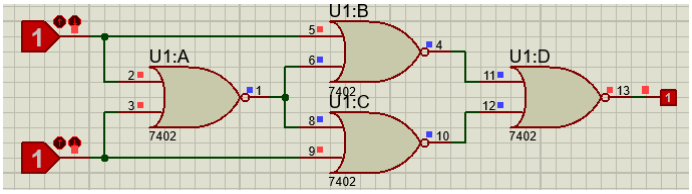

Figure 30: XNOR from NOR Gate

4 Discussion

The inputs and outputs of AND, OR, NOT, NOR, NAND, XOR and XNOR gates, their symbols and truth tables were studied. Then proteus was used to realize the gates and their respective truth tables were verified. The working of 3 input AND gate and 4 input OR gate was also studied. The theory behind the universal gates was also studied and they were used to make other gates.

5 Conclusion

Thus a concise understanding of various logic gates was obtained, my closely studying their behaviour, symbols, and their truth tables. And proteus was used for the verification of their truth tables. 3 input AND gate and 4 input OR gate was also studied. And the universal gates were used to construct other gates.