TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
PULCHOWK CAMPUS

LAB REPORT

Lab No:
Experiment Date: 2020-5-26
Submission Date: 2020-6-7

Submitted By:
Name: Suban Shrestha
Roll No: 076BCT082
Group: CD(D)

Submitted To:
Department of Electronics and Communications Enginnering

Verification of DeMorgan's Laws and Familiarization with NAND and NOR Gates

1 Objectives

1. To learn, understand and verify DeMorgan's Laws.
2. To get familiarized with NAND and NOR Gates, universal gates.
3. To construct various gates using universal gates.

2 Materials Required

1. Universal Gates(NAND and NOR gates).
2. Basic Logic Gates(AND, OR and NOT gates).
3. For computer simulation, a computer with simulation software.

3 Theory

3.1 DeMorgan's Law

DeMorgan's Theoreams are a set of laws developed from boolean expressions for AND, OR and NOT using two input variables, A and B. The two theorems allow the input variables to be negated and be converted from one boolean function to the opposite form. It can also be used to relate negative logic with positive logic.

3.1.1 DeMorgan's First Law

DeMorgan's First theorem proves that when two input variables are AND'ed and negated, the are equivalent to the OR of the complement of the individual variables. Thus the equivalent of the NAND function will be a negative-OR function.

$$(A.B)' = A' + B'$$

Inputs		Outputs				
A	B	$A.B$	A'	B'	$(A.B)'$	$A' + B'$
0	0	0	1	1	1	1
0	1	0	1	0	1	1
1	0	0	0	1	1	1
1	1	1	0	0	0	0

Table 1: Truth Table

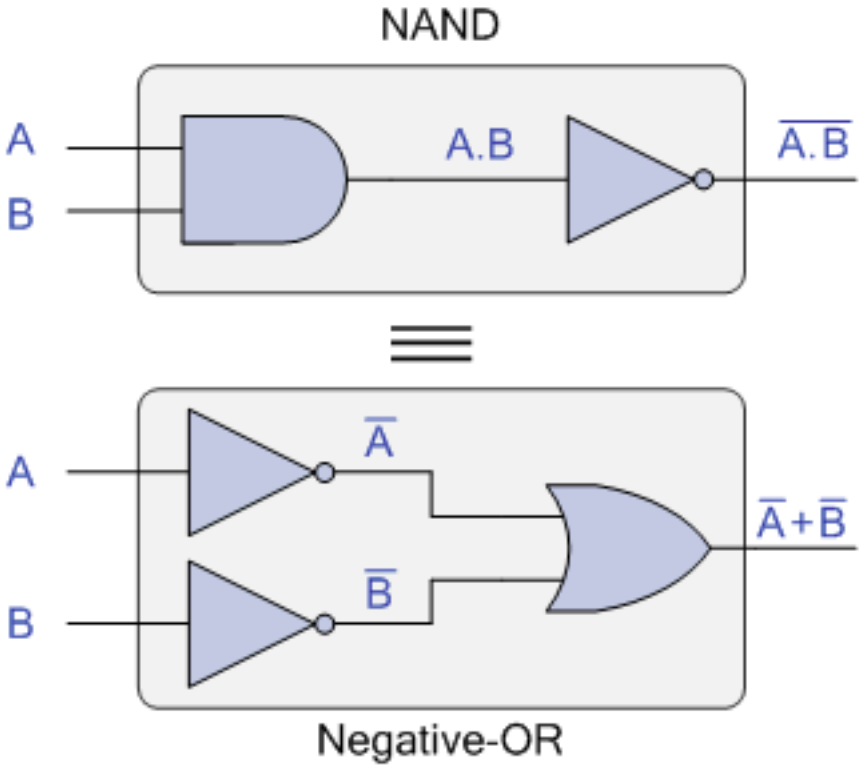


Figure 1: Implementation using Logic Gates

3.1.2 DeMorgan's Second Law

DeMorgan's Second theorem proves that when two input variables are OR'ed and negated, the equivalent to the AND of the complement of the individual variables. Thus the equivalent of the NOR function will be a negative-AND function.

$$(A + B)' = A'.B'$$

Inputs		Outputs				
A	B	$A + B$	A'	B'	$(A + B)'$	$A'.B'$
0	0	0	1	1	1	1
0	1	1	1	0	0	0
1	0	1	0	1	0	0
1	1	1	0	0	0	0

Table 2: Truth Table

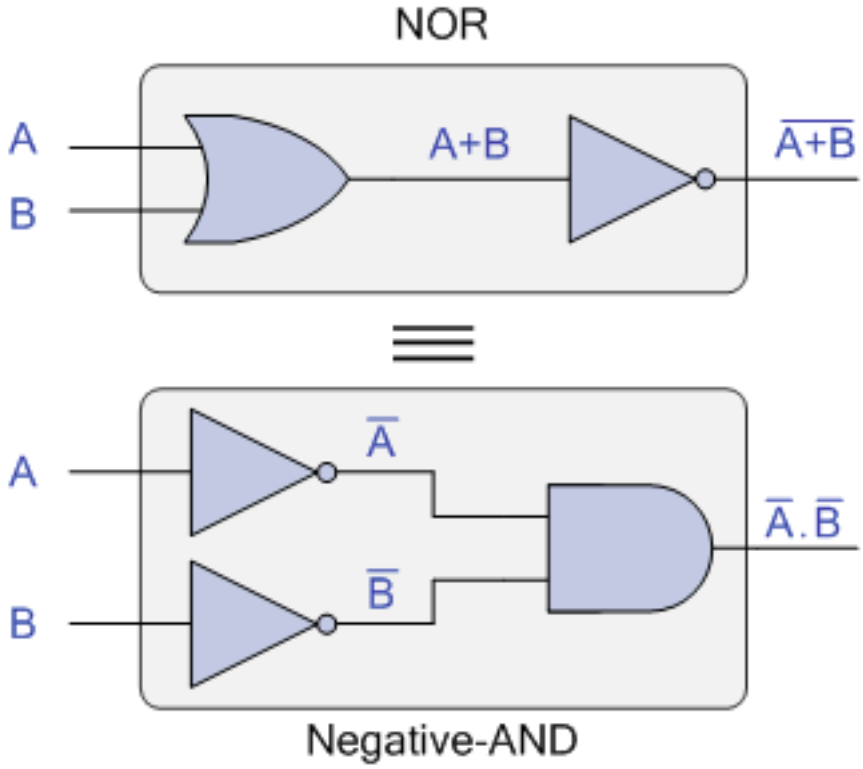


Figure 2: Implementation using Logic Gates

3.2 Universal Gates

The gates NAND and NOR are knows as universal gates. These gates can be used to create the logic of all ther other gates. Because of this, these are known as universal gates. Using only one type of gate is more efficient in building large scale devices and thus they are used.

4 Lab

4.1 DeMorgan's Laws

The circuits below were constructed for the verification of DeMorgan's laws. Various inputs were provided and the truth table was verified.

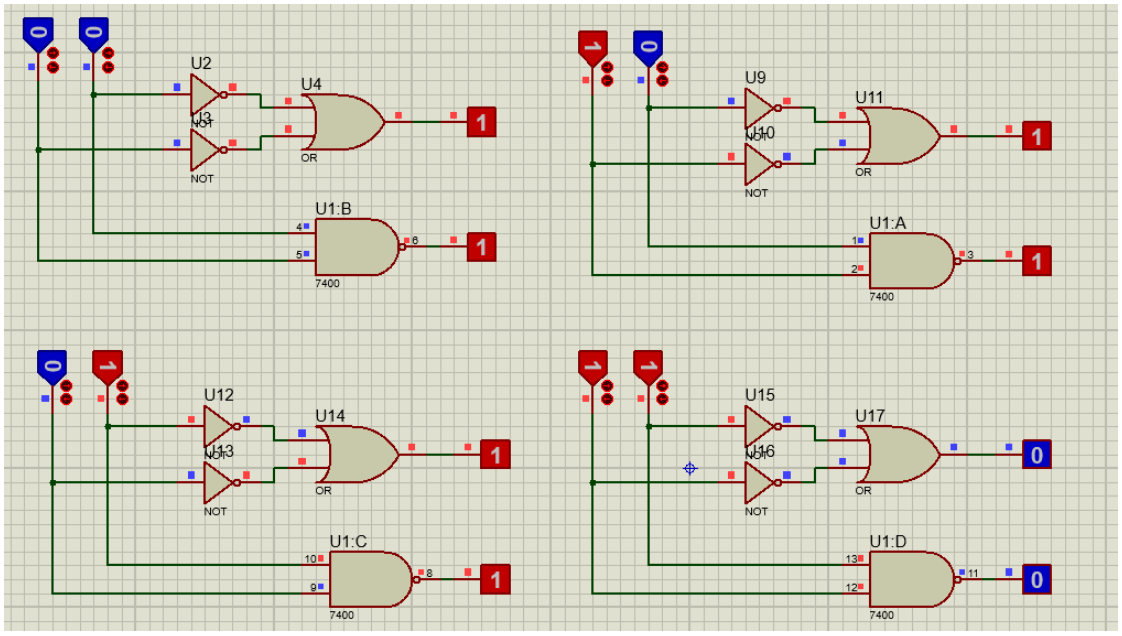


Figure 3: DeMorgan's First Law

A	B	$(A.B)'$	$A' + B'$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Table 3: Truth Table verification of DeMorgan's First Law

Thus DeMorgan's first law was verified

Simillarly Another circuit was constructed to verify DeMorgan's Second Law.

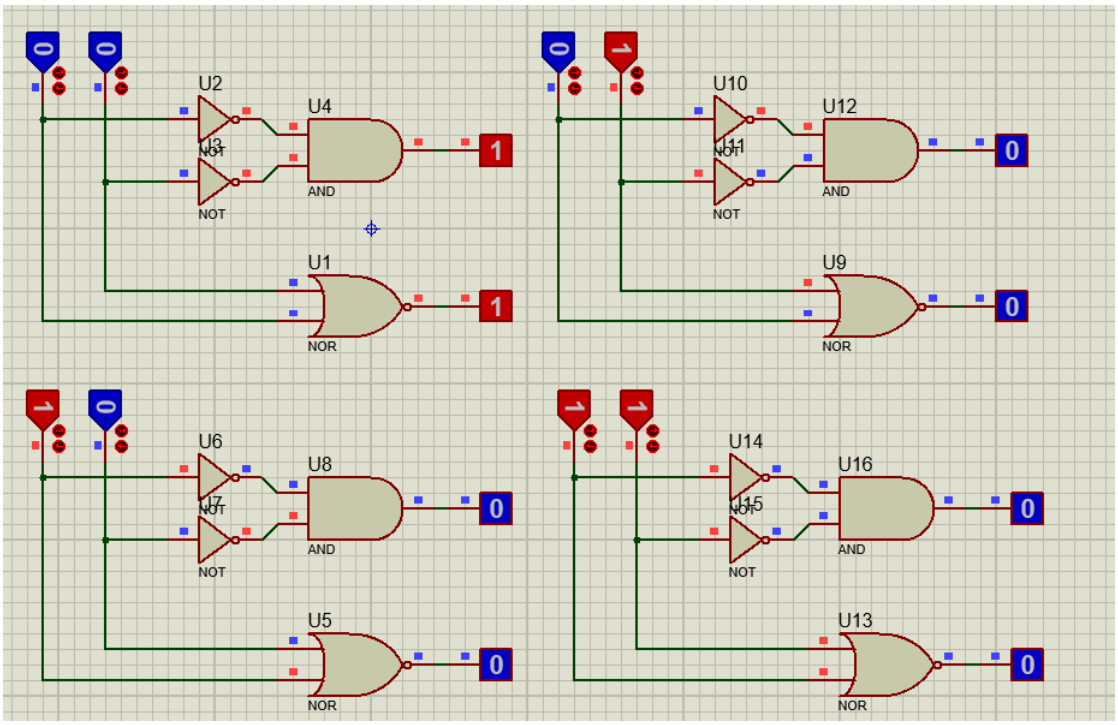


Figure 4: DeMorgan's Second Law

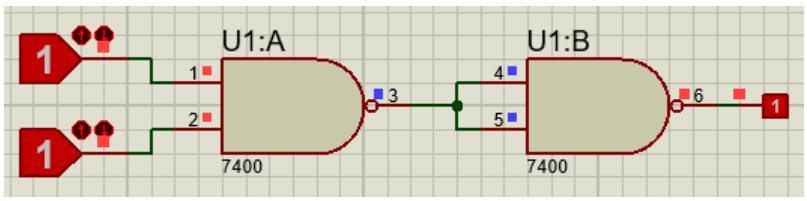
A	B	$(A+B)'$	$A'.B'$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Table 4: Truth Table verification of DeMorgan's Second Law

Thus DeMorgan's second law was verified.

4.2 Construction of Basic Gates from Universal Gates

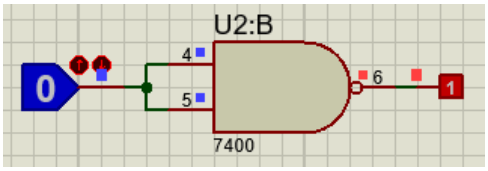
4.2.1 AND from NAND Gate



Boolean Logic

$$\begin{aligned} Y &= ((A.B)')' \\ &= A.B \end{aligned} \tag{1}$$

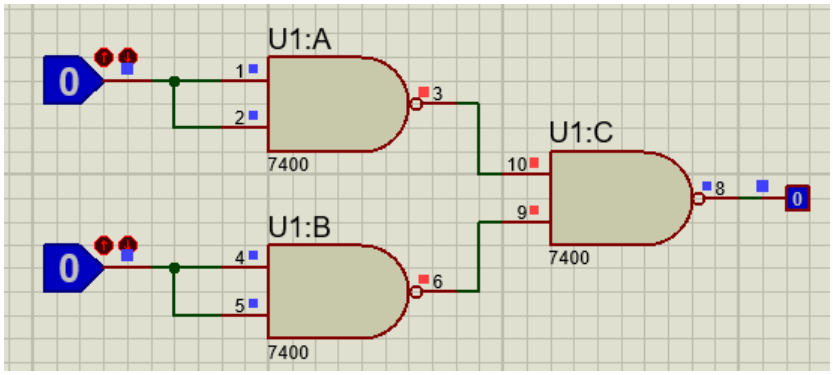
4.2.2 NOT from NAND Gate



Boolean Logic

$$\begin{aligned} Y &= (A.A)' \\ &= A' \end{aligned} \tag{2}$$

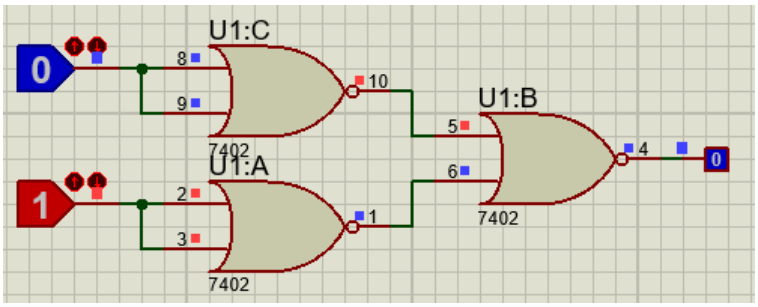
4.2.3 OR from NAND Gate



Boolean Logic

$$\begin{aligned} Y &= (A'.B')' \\ Y &= (A + B)'' \\ &= A + B \end{aligned} \tag{3}$$

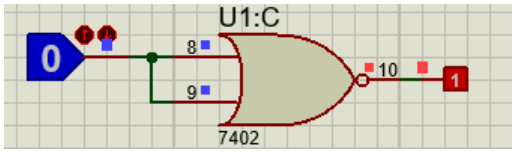
4.2.4 AND from NOR Gate



Boolean Logic

$$\begin{aligned} Y &= (A' + B')' \\ &= ((A.B)')' \\ &= A.B \end{aligned} \tag{4}$$

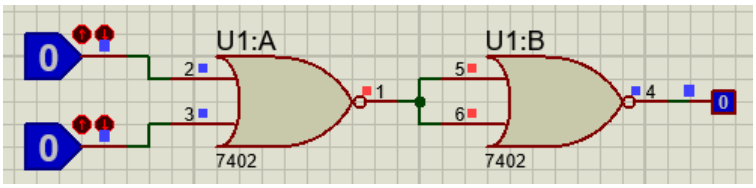
4.2.5 NOT from NOR Gate



Boolean Logic

$$\begin{aligned} Y &= (A + A)' \\ &= A' \end{aligned} \tag{5}$$

4.2.6 OR from NOR Gate

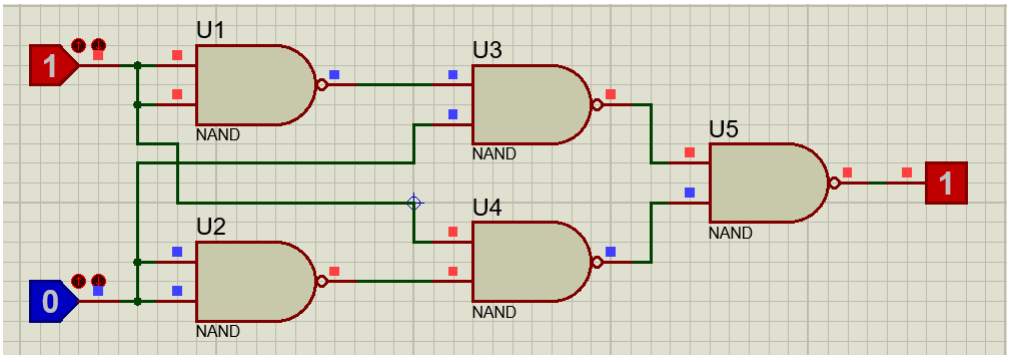


Boolean Logic

$$\begin{aligned} Y &= ((A + B)')' \\ &= (A + B)'' \\ &= A + B \end{aligned} \tag{6}$$

4.3 XOR and XNOR Gates

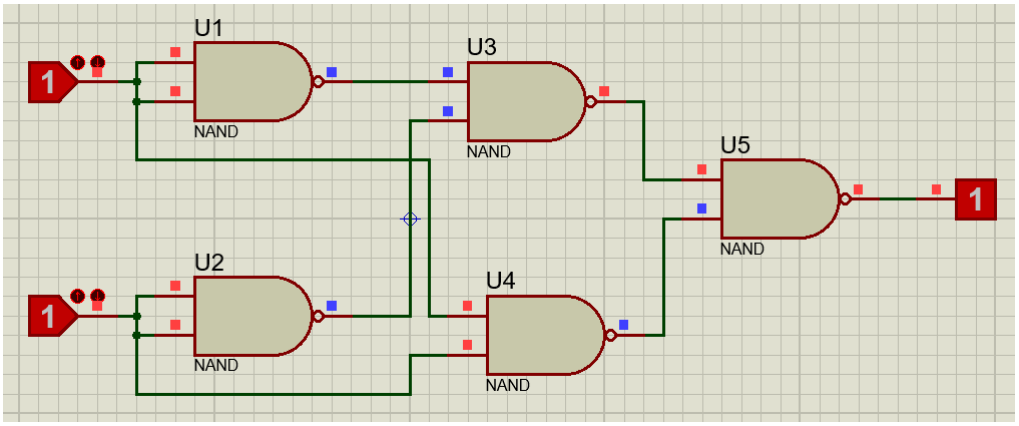
4.3.1 XOR from NAND Gate



Boolean Logic

$$\begin{aligned} Y &= AB' + A'B \\ &= (AB' + A'B)'' \\ &= ((AB')'.(A'B)')' \end{aligned} \tag{7}$$

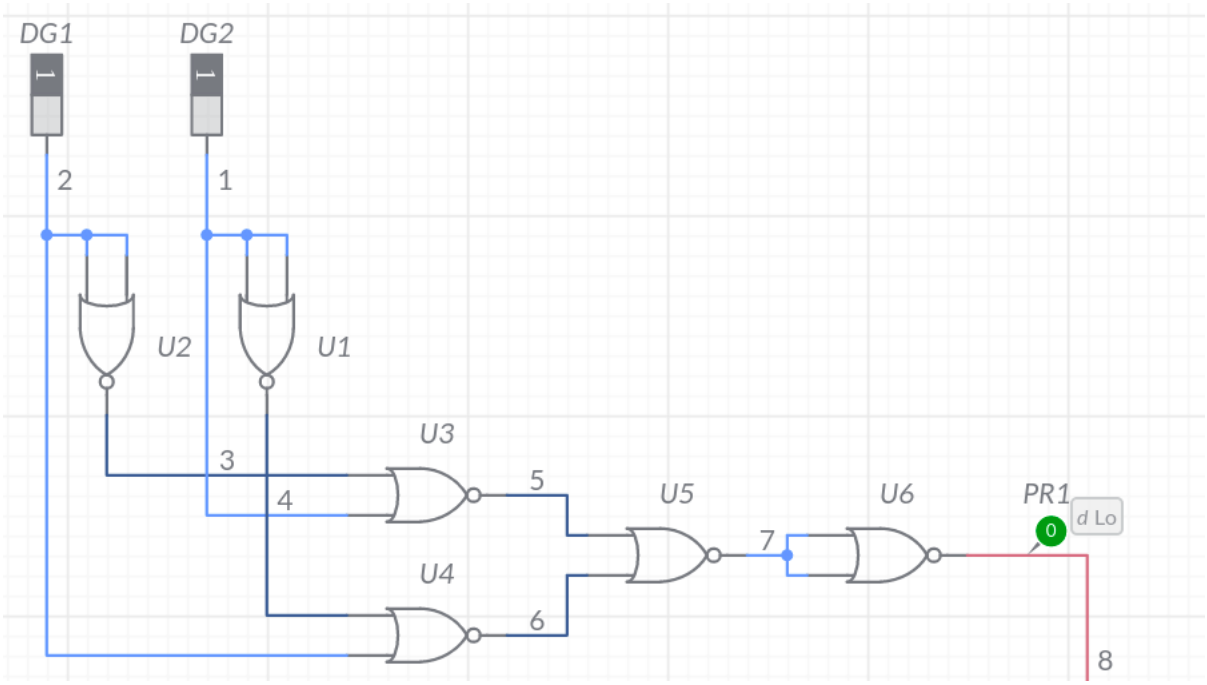
4.3.2 XNOR from NAND Gate



Boolean Logic

$$\begin{aligned} Y &= AB + A'B' \\ &= (AB + A'B')'' \\ &= ((AB)'.(A'B')')' \end{aligned} \tag{8}$$

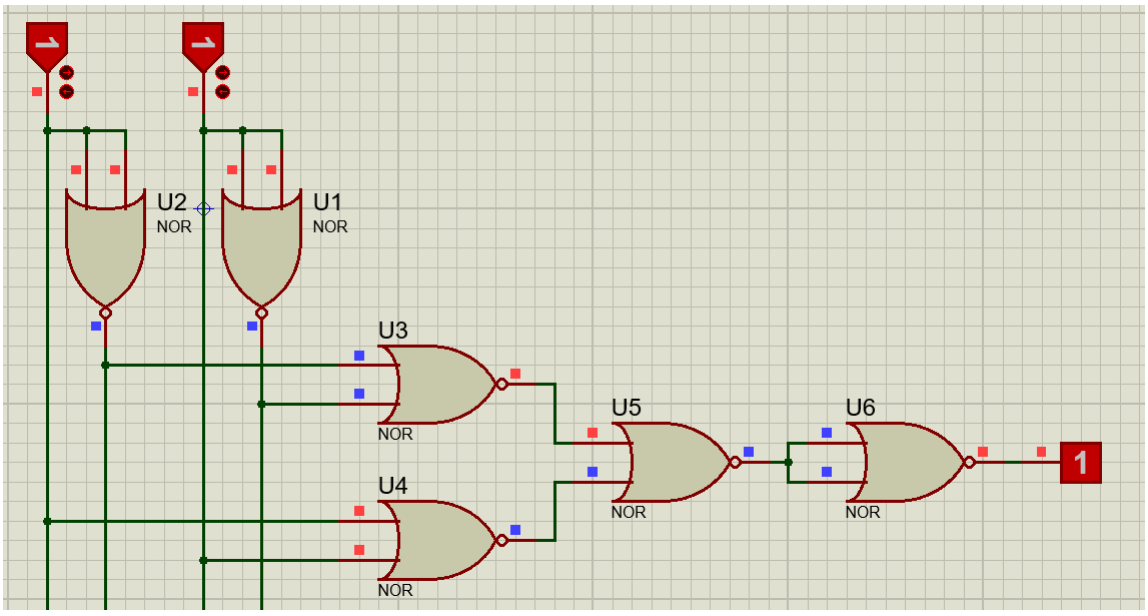
4.3.3 XOR from NOR Gate



Boolean Logic

$$\begin{aligned} Y &= (AB' + A'B) \\ &= (AB')'' + (A'B)'' \\ &= (A' + B)' + (A + B')' \\ &= ((A' + B)' + (A + B')')'' \end{aligned} \tag{9}$$

4.3.4 XNOR from NOR Gate



Boolean Logic

$$\begin{aligned} Y &= AB + A'B' \\ &= (AB)'' + (A'B')'' \\ &= (A' + B')' + (A + B)' \\ &= ((A' + B')' + (A + B)')'' \end{aligned} \tag{10}$$

5 Discussion

In this way, DeMorgan's laws were studied and verified using a truth table and circuit. A through understanding of the universal gates was also gained. The universal gates were then used to make other gates like AND, OR, NOT, XOR and XNOR, by the use of boolean algebra and DeMorgan's laws. The working of Negative OR and Negative AND gate was also gained. All of the simulation was done using a simulating software.

6 Conclusion

Thus, various circuits were constructed by the use of boolean algebra and DeMorgan's Laws, and were verified in the simulation. A through understanding of the Demorgan's laws and Universal Gates was obtained through the use of simulating software.