Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

# TOPICWISE : COMPUTER ORGANIZATION AND ARCHITECTURE-1 (GATE - 2019) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(17) | CORRECT(7) | INCORRECT(5) | SKIPPED(5)

## Q. 1

In a register / memory type CPU, the instruction lengths are typically variable. This presents a problem when a "PC" of the CPU is incremented during the fetch-execute cycle. Which of the following statement is true with regard to PC incrementing?

Solution Video | Have any Doubt ?

A
PC is incremented by the largest possible fixed value irrespective of the variability.

B
Increment value is known when the current instruction is decoded within the IR.

Your answer is **Correct**

**Solution :**
(b)
Increment value is known when the current instruction is decoded within the IR.

C
Increment value is known when the current instruction has completed execution.

D
The binary loader overcomes the problem by positioning instructions at word boundaries so that PC can be incremented by a constant amount.

QUESTION ANALYTICS

## Q. 2

Match **List-I (programming terms)** with **List-II (addressing modes)** and select the correct answer using the codes given below the lists:

| List-I | List-II |
|---|---|
| A. Constant | 1. Index addressing mode |
| B. Structure | 2. Immediate addressing mode |
| C. Global variable | 3. Register addressing mode |

**Codes:**

| | A | B | C |
|---|---|---|---|
| (a) | 1 | 3 | 2 |
| (b) | 2 | 1 | 3 |
| (c) | 3 | 2 | 1 |
| (d) | 2 | 3 | 1 |

Solution Video | Have any Doubt ?

A
a

B
b

Your answer is **Correct**

**Solution :**

Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

C
c

D
d

QUESTION ANALYTICS

**Q. 3**

A Program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given below:

| | Instruction Type | CPI | Instruction Mix |
|---|---|---|---|
| 1. | ALU | 1 | 60% |
| 2. | Load/Store with cache hit | 2 | 18% |
| 3. | Branch | 4 | 12% |
| 4. | Memory reference with cache miss | 8 | 10% |

If the clock frequency of the processor is 400 MHz. What is the avg CPI of the processor?

Solution Video | Have any Doubt ?

A
2.24

Your answer is **Correct**

**Solution :**
(a)

$$\text{Avg CPI} = \Sigma(IC_i \times CPI_i)$$
$$= (0.6 \times 1) + (0.18 \times 2) + (0.12 \times 4) + (0.1 \times 8)$$
$$= 2.24$$

B
3.24

C
2.5

D
2.4

QUESTION ANALYTICS

**Q. 4**

A computer system that used memory mapped IO configuration, has a 32-bit address space. Address with 1's in the three MSB refer to devices. What is the maximum amount of memory address and I/O port address that can be referenced in such a system respectively?

FAQ | Solution Video | Have any Doubt ?

A
$7 \times 2^{30}$ and $1 \times 2^{30}$

B
$1 \times 2^{30}$ and $7 \times 2^{30}$

C
$7 \times 2^{29}$ and $1 \times 2^{29}$

Your answer is **Correct**

Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

Similarly, since "111" are reserved hence rest of 7 combinations represent memory location to 110). So, the total memory address space will be $7 \times 2^{29}$.

D

$8 \times 2^{32}$ and $1 \times 2^{32}$

QUESTION ANALYTICS

## Q. 5

Consider the 2 GHz clock frequency processor used execute the following program segment.

| Instruction | Meaning | Size (in words) |
|---|---|---|
| $I_1$ : MOV r 0, (3000) | $r\,0 \leftarrow$ m[[3000]] | 2 |
| $I_2$ : MOV r 1, [2000] | $r\,1 \leftarrow$ m[2000] | 1 |
| $I_3$ : ADD r 0, r 1 | $r\,0 \leftarrow r\,0 + r\,1$ | 1 |
| $I_4$ : MUL r 0, r 1 | $rD \leftarrow r\,0 \times r\,1$ | 1 |
| $I_5$ : Mov (3000), r 0 | m[[3000]] $\leftarrow r\,0$ | 2 |
| $I_6$ : Halt | Machine halts | 1 |

Assume the 3 clock cycles required for Register to/from memory transfer, 1 clock cycle for ADD with both operands in register, 2 clock cycle MUL with both operands in register, 3 clock cycles per word for instruction fetch and decode. What is the total time required to complete the program execution (in ns)?

FAQ | Solution Video | Have any Doubt ?

A

12

Your answer is **Wrong**

B

15

C

18

Correct Option

**Solution :**
(c)

| Instruction | Size (in words) | Number of Clock Cycles |
|---|---|---|
| $I_1$ : MOV r 0, (3000) | 2 | $3 \times 2 + 3 = 9$ |
| $I_2$ : MOV r 1, [2000] | 1 | $3 \times 1 + 3 = 6$ |
| $I_3$ : ADD r 0, r 1 | 1 | $3 \times 1 + 1 = 4$ |
| $I_4$ : MUL r 0, r 1 | 1 | $3 \times 1 + 2 = 5$ |
| $I_5$ : Mov (3000), r 0 | 2 | $3 \times 2 + 3 = 9$ |
| $I_6$ : Halt | 1 | $3 \times 1 + 0 = 3$ |
| | | Total = 36 |

Total time = 36 cycles × 0.5 ns
= 18 ns

D

25

QUESTION ANALYTICS

## Q. 6

A system employs 10 stage instruction pipeline in which 5% instruction results in data dependency, 10% instruction results in control dependency, 2% instructions results in structural dependency. 10% instructions are exposed to data and control dependencies. If the penalty for structural dependency is 1 clock and the penalty for control dependency and data dependency are 3 clocks and 2 clocks respectively. The average instruction time is _____ [in cycles]

Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

1.92

Correct Option

**Solution :**
1.92

$$T_{avg} = (1 + \text{number of stalls/instruction}) \text{ cycle time}$$
$$T_{avg} = 1 + (5\% \times 2) + (10\% \times 3) + (2\% \times 1) + (10\% \times 5)$$
$$= 1 + 0.92$$
$$= 1.92 \text{ cycles}$$

Your Answer is .92

QUESTION ANALYTICS

**Q. 7**

The CPU supports the following instructions
LOAD $R_1, R_2$ (100) ; $R_2 \leftarrow [R_2 + 100]$
ADD $R_1, R_2$; $R_1 \leftarrow R_1 + R_2$
SUB $R_2, R_1$ ; $R_2 \leftarrow R_2 - R_1$
STORE $R_1$ (100), $R_2$ ; $[R_1+100] \leftarrow R_2$
4 stage pipeline is used to execute the above instructions i.e., Fetch, Decode, Execute and Write Back. Let all instructions consume 1 clock each for fetch, decode and write operations. Execution require 3 clocks for memory related operation and 1 clock is for other instructions. The minimum number of clocks needed with operand forwarding is _____.

FAQ | Solution Video | Have any Doubt ?

11

Correct Option

**Solution :**
11

| | $CC_1$ | $CC_2$ | $CC_3$ | $CC_4$ | $CC_5$ | $CC_6$ | $CC_7$ | $CC_8$ | $CC_9$ | $CC_{10}$ | $CC_{11}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_1$ | F | D | E | E | E | W | | | | | |
| $I_2$ | | F | D | /// | /// | E | W | | | | |
| $I_3$ | | | F | /// | /// | D | E | W | | | |
| $I_4$ | | | | /// | /// | F | D | E | E | E | W |

Minimum clock cycles = 11[CC = Clock cycle]

QUESTION ANALYTICS

**Q. 8**

Consider the byte addressable memory unit of a computer has 256 K words of 32 bit each. The computer has an instruction format with 4 fields:
1. An opcode field.
2. A mode field specify 1 of 7 addressing modes.
3. A register address field to specify 1 of 60 registers.
4. A memory address field.
If an instruction is 32 bits long then the number of different instructions possible are _____.

Solution Video | Have any Doubt ?

8

Correct Option

**Solution :**
8
Instruction format:

Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

QUESTION ANALYTICS

**Q. 9**

To execute an instruction by a 32-bit machine the following steps are carried out: Fetch, Decode,Execution, Memory access and Store, each of which takes 1 clock period. In a pipelined execution of a 5-step task, a new instruction is read and it takes 1 ns. If there are 100 instructions in sequence, then the speedup ratio of pipe line processing system over an equivalent non pipeline processing system is _____.

FAQ | Solution Video | Have any Doubt ?

4.8

Correct Option

**Solution :**
4.8

$$t_n = 5\text{ ns}$$
$$t_p = 1\text{ ns}$$
$$\text{K} = 5,\ n = 100$$
$$S = \frac{n.t_n}{(K+n-1)t_p}$$
$$S = \frac{100 \times 5\ ns}{(5+100-1)1\ ns}$$
$$S = \frac{500}{104}$$
$$S = 4.8$$

Your Answer is 20.8

QUESTION ANALYTICS

**Q. 10**

Suppose that a task makes extensive use of floating point operations with 40% of the time is consumed by floating point operations with a new hardware design. If the floating point module is speeded up by a factor of 4. What is the overall speedup?

FAQ | Solution Video | Have any Doubt ?

A
0.7

B
1.42

Correct Option

**Solution :**
(b)
By using Amdhal's law:

$$s = 4; f = 40\%$$
$$s_{\text{overall}} = \left[(1-f)+\frac{f}{s}\right]^{-1}$$

Here $f$ is most frequency used operation frequency and $s$ is speed up factor.

$$s_{\text{overall}} = \left[(1-0.4)+\frac{0.4}{4}\right]^{-1}$$
$$= [0.6 + 0.1]^{-1}$$
$$= 1.42$$

Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

D
2.5

Your answer is **Wrong**

QUESTION ANALYTICS

**Q. 11**

Consider the following statements.
S1: The RISC processor has CPI 1.
S2: In horizontal instruction control signals are in encoded form.
S3: In vertical instruction control signals are in encoded form.
S4: In terms of speed vertical instruction is slower than horizontal instruction.
Which of the above statements are true?

FAQ | Solution Video | Have any Doubt ?

A
Only S1, and S2

B
Only S2 and S3

C
Only S1, S3 and S4

Your answer is **Correct**

**Solution :**
(c)
S1 is true property of RISC architecture.
S2 is false, horizontal instruction control signals are in decoded form.
S3 is true, vertical instruction control signals are in encoded form.
S4 speed of vertical instruction is less than horizontal instruction.
[Encoded control signals need to be decoded first and then they are interpreted]

D
None of the above

QUESTION ANALYTICS

**Q. 12**

Consider a hypothetical CPU which supports 16 bit instruction, 64 registers and 1 KB memory space. If there exist 12 2-address instruction which uses register reference and 12 1-address memory reference instructions how many 0-address instructions are possible?

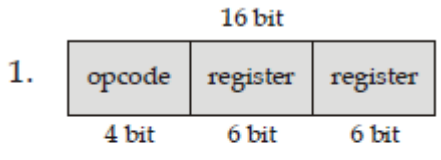
Solution Video | Have any Doubt ?

A
1024

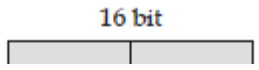
B
4096

Correct Option

**Solution :**
(b)




2. Number of 2-address instruction = $2^4 = 16$
3. Number of free opcodes = (16 – 12) = 4
4. Number of 1-address memory reference instruction



Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

6. Number of 0-address instruction opcodes = $4 \times 2^{\square} = 4096$

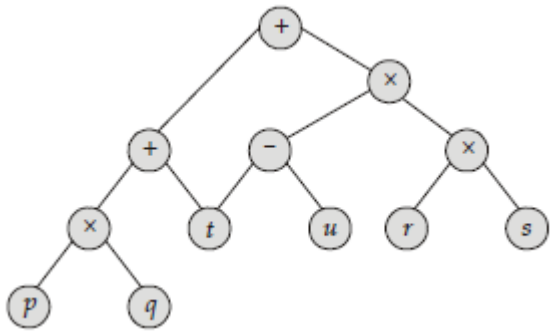
C
2048

D
8192

QUESTION ANALYTICS

**Q. 13**

Consider the evaluation of following expression tree on a machine in which memory can be accessed only through load and store instructions. The variable *p*, *q*, *r*, *s*, *t* and *u* are initially stored in memory. The binary operators used in the tree can be evaluated by the machine only when all operands are in register. The instruction produce result only in a register.




What is the minimum number of registers needed to evaluate the expression if, no intermediate results can be stored in memory?

FAQ | Solution Video | Have any Doubt ?

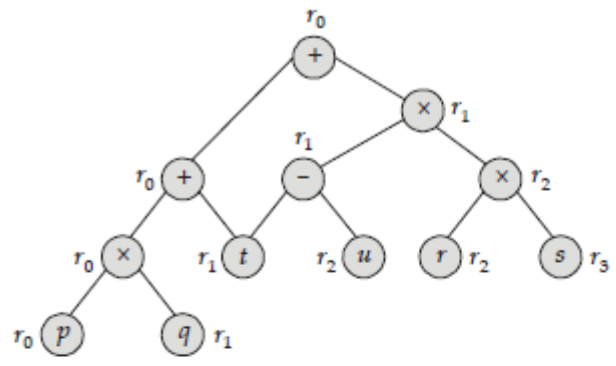
A
2

B
3

C
4

Correct Option

**Solution :**
(c)




Load $r_0$, $p$
Load $r_1$, $q$
MUL $r_0$, $r_1$ [store result in $r_0$]
Load $r_1$, $t$
Load $r_2$, $u$
ADD $r_0$, $r_1$ [store result in $r_0$]
SUB $r_1$, $r_2$ [store result in $r_1$]
Load $r_2$, $r$
Load $r_3$, $s$
MUL $r_2$, $r_3$ [store result in $r_2$]
MUL $r_1$, $r_2$ [store result in $r_1$]
ADD $r_0$, $r_1$ [store result in $r_0$]

So, 4 registers are required.

Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

QUESTION ANALYTICS

**Q. 14**

Assume that the control word is 32 bit wide. The micro-instruction format is divided into 3 fields. A micro operation field of 14 bits specifies the micro-operations to be performed. An address selection field specifies a condition based on flags and control memory address field. There are 16 flags. How many bits are in address selection field, address field and the size of control memory in words respectively?

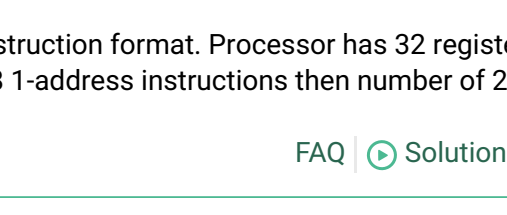
Solution Video | Have any Doubt ?

A
14 bits, 4 bits and 16384 C-Words

Your answer is **Correct**

**Solution :**
(a)

Control word structure:




Control memory size = $2^{14}$ control words
= 16384 control word

B
14 bits, 4 bits and 8192 C-Words

C
12 bits, 4 bits and 16384 C-Words

D
12 bits, 4 bits and 16384 C-Words

QUESTION ANALYTICS

**Q. 15**

Consider a processor uses 2 byte instruction format. Processor has 32 registers and support upto 2-address instruction. If processor support 128 1-address instructions then number of 2-address instructions are _____.

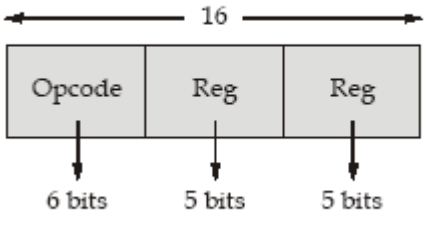
FAQ | Solution Video | Have any Doubt ?

60

Correct Option

**Solution :**
60

Instruction format:




So, total number of 2 address instructions = $2^6 = 64$
Given that number of 1-address instruction = 128
We know that maximum number of 1-address instruction

$$(2^6 - x) \times 2^5 = 128$$
$$[2^6 - x] = 2^{7-5}$$
$$[2^6 - x] = 2^2$$

Ashima Garg
Course: GATE
Computer Science Engineering(CS)

HOME
MY TEST
BOOKMARKS
MY PROFILE
REPORTS
BUY PACKAGE
ASK AN EXPERT
OFFER
EXCLUSIVE OFFER FOR OTS STUDENTS ONLY ON BOOK PACKAGES

QUESTION ANALYTICS

**Q. 16**

Consider a hypothetical control unit that supports 5 groups of mutually exclusive control signals. Also assume that group 1 & group 2 are using horizontal micro-programming whereas group-3, 4 and 5 are using vertical micro-programming. The total number of bits used for control words are _____.

| Groups | $G_1$ | $G_2$ | $G_3$ | $G_4$ | $G_5$ |
|---|---|---|---|---|---|
| Control signals | 43 | 29 | 76 | 130 | 100 |

Solution Video | Have any Doubt ?

94

Your answer is Correct94

**Solution :**
94

Group-1 and 2 are using horizontal micro-programming,
Hence, total bits are:

$$43 + 29 = 72$$

Group-3, 4 and 5 are using vertical micro-programming,
Hence, total bits are:

$$\lceil \log_2 76 \rceil + \lceil \log_2 130 \rceil + \lceil \log_2 100 \rceil = 7 + 8 + 7 = 22$$

$$\text{Total bits for control word} = 72 + 22 = 94 \text{ bits}$$

QUESTION ANALYTICS

**Q. 17**

The instruction pipeline of RISC processor has 200 instructions in which 100 are performing addition, 25 performing division and 75 are performing multiplications, where Excution state for addition take 1 clock cycle, multiplication take 3 clock cycles and division take 5 clock cycles. Assume pipeline has 5 stages IF, ID, EX, MA and WB and their is no data and control hazard. The number of clock cycles required for execution of sequence of instructions are _____.

FAQ | Solution Video | See your Answers

554

Correct Option

**Solution :**
554

Given, total number of instructions = 200

$$\text{Total number of processes, } n = 200 + (25 \times 2) + (75 \times 4)$$
$$= 550$$
$$\text{Total number of clock cycles} = (k + n - 1) \text{ cycles}$$
$$= (5 + 550 - 1) \text{ cycles}$$
$$= 554$$

Your Answer is 22.5

QUESTION ANALYTICS