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Computer Science Engineering(CS)

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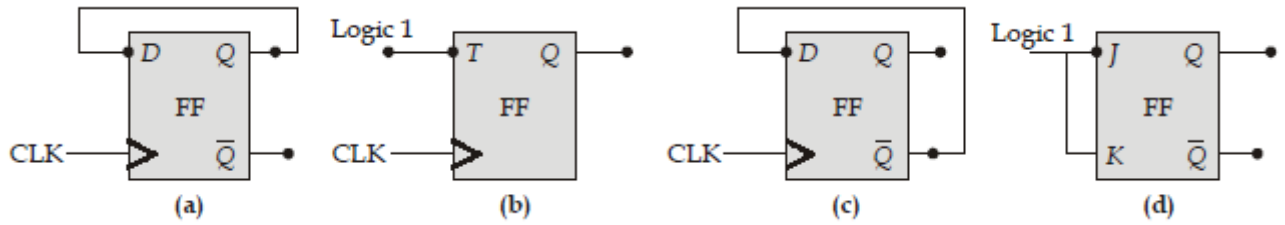
SINGLE SUBJECT : DIGITAL LOGIC (GATE - 2019) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(33) | CORRECT(23) | INCORRECT(7) | SKIPPED(3)

Q. 1

Which of the following FF (flip-flop) is acting as a complementing flip-flop?



Solution Video | Have any Doubt ?

A
Only (a) and (b)

B
Only (a), (b) and (d)

C
Only (b), (c) and (d)

Your answer is **Correct**

Solution :
(c)

Complementing FF - A flip-flop where output gets complemented when next clocks are ap

- A complementing FF can be obtained from JK-FF with the J and K inputs tied togeth from a JK FF.
- If the complemented output ($\overline{Q}$) is connected to the input of D-FF then it bec complementing FF.

D
All of the above

QUESTION ANALYTICS

Q. 2

Which of the following is not correct about the multiplexer circuit?

Solution Video | See your Answers

A
A MUX circuit can be used as a universal logic gate.

B
A MUX has 2n input lines an 1 output line.

Your answer is **Wrong**

C
A 16 × 1 MUX can be designed using 2 × 1 MUX.

D
None of the above

Correct Option

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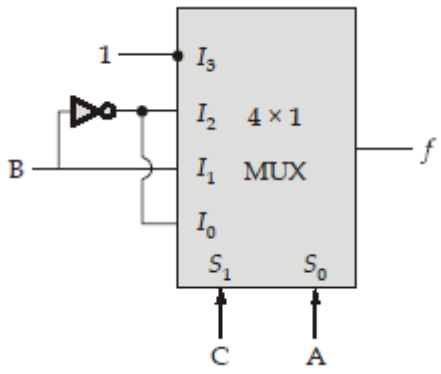
QUESTION ANALYTICS

Q. 3

Find the function f(A, B, C) realize by the given 4 × 1 MUX.



Solution Video | Have any Doubt ?

A

Σm (0, 1, 2, 4)

B

Σm (0, 1, 5, 6, 7)

Your answer is **Correct**

Solution :
(b)

C	A	
0	0	$\bar{B}$
0	1	B
1	0	$\bar{B}$
1	1	1

$$f(A, B, C) = \bar{A}\bar{B}\bar{C} + AB\bar{C} + \bar{A}\bar{B}C + AC$$

0 6 1 $A\bar{B}C$ (5) ABC (7)

$$= \sum m\ (0, 1, 5, 6, 7)$$

C

Σm (0, 1, 2, 4, 5)

D

Σm (2, 4, 5, 6, 7)

QUESTION ANALYTICS

Q. 4

Let $x_1 \oplus x_2 \oplus x_3 = 1$, where x_1, x_2, x_3 are boolean variables. Which one of the following always true?

Solution Video | Have any Doubt ?

A

$x_1 = x_2 \cdot x_3$

B

$x_1 x_2 \cdot x_3 = 0$

C

$x_1 + x_2 + x_3 \neq 1$

D

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Solution :
(d)

Given, $x_1 \oplus x_2 \oplus x_3 = 1$

x_1	x_2	x_3	$x_1 \oplus x_2 \oplus x_3$
0	0	0	0
0	0	1	①
0	1	0	①
0	1	1	0
1	0	0	①
1	0	1	0
1	1	0	0
1	1	1	①

$x_1 \oplus x_2 \oplus x_3 = 1$, whenever odd number of variables are 1.
Option (a) fails when $x_1 = 1, x_2 = 0, x_3 = 0$
Option (b) fails when $x_1 = x_2 = x_3 = 1$
Option (c) fails because odd number of variable are always 1.
Option (d) satisfies for every combination.
Hence option (d) is correct.

QUESTION ANALYTICS

Q. 5

Consider the following boolean expression for F.

$F(A, B, C, D) = \bar{C}D + \bar{A}\bar{C}\bar{D} + AB\bar{C}\bar{D}$

The minimal sum-of-products for the function F(A, B, C, D) is

Solution Video | Have any Doubt ?

A
$\bar{A} + \bar{B} + \bar{C} + \bar{D}$

B
$\bar{A}B + \bar{B}C + \bar{C}D$

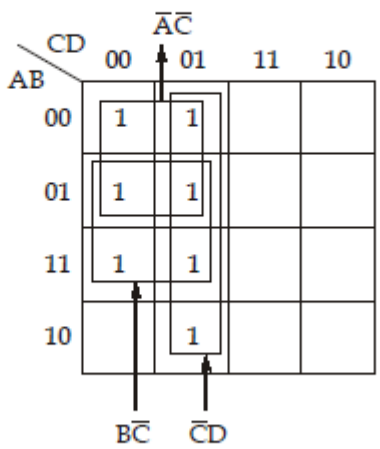
C
$\bar{A}\bar{C} + \bar{C}D + B\bar{C}$

Your answer is **Correct**

Solution :
(c)

$F = \bar{C}D + \bar{A}\bar{C}\bar{D} + AB\bar{C}\bar{D}$

$F = \bar{A}\bar{C} + \bar{C}D + B\bar{C}$



$F = \bar{A}\bar{C} + \bar{C}D + B\bar{C}$

D
$\bar{C}D + \bar{B} + \bar{D}$

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Q. 6

A 4 bit (Q_3 Q_2 Q_1 Q_0) binary down ripple counter is designed. The clock cycles are negative edge triggered and J-K-Flip-Flops (FF's) are used during the design process. Both the inputs J and K of FF's are connected to logic 1. What will be the input to clocks of next MSB FF's

Solution Video | Have any Doubt ?

A
Complemented output of previous LSB FF.

Your answer is **Correct**

Solution :
(a)
The count of four bit countdown counter starts from binary 15 and continuous to binary counts 14, 13, 12 ....., 0 and then back to 15. LSB bit is complemented with every count pulse. Any other bit in the sequence is complemented if its previous LSB bit goes from 1 to 0 because –ve edge triggered clocks are used. Hence complemented output of previous LSB Flip-Flip will be the input to the next MSB FF to make binary down counter.

B
Output of previous LSB FF.

C
Flip-Flops clock should always be 1.

D
None of the above

QUESTION ANALYTICS

Q. 7

Which of the following logic gate is used as equality and inequality checking respectively?

Solution Video | Have any Doubt ?

A
NAND and NOR

B
EX-NOR and EX-OR

Correct Option

Solution :
(b)
EX-NOR is equality checking gate.
EX-OR is inequality checking gate.

C
EX-NOR and OR

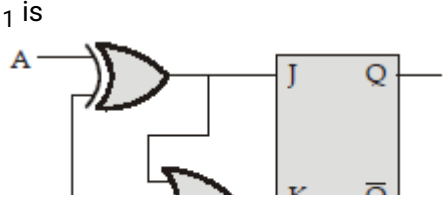
D
EX-OR and EX-NOR

Your answer is **Wrong**

QUESTION ANALYTICS

Q. 8

An AB flip-flop (FF) is constructed from a JK-FF as shown in the figure. The expression for the next state Q_{n+1} is



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A

$(A \oplus B)Q_n$

B

$\bar{A}(B \odot Q_n) + A\bar{B}$

C

$\bar{A}(B \oplus Q_n) + A\bar{B}\bar{Q}_n$

Your answer is **Correct**

Solution :
(c)

A	B	J	K	Q_{n+1}
0	0	0	0	Q_n
0	1	1	1	$\bar{Q}_n$
1	0	1	1	$\bar{Q}_n$
1	1	0	1	0

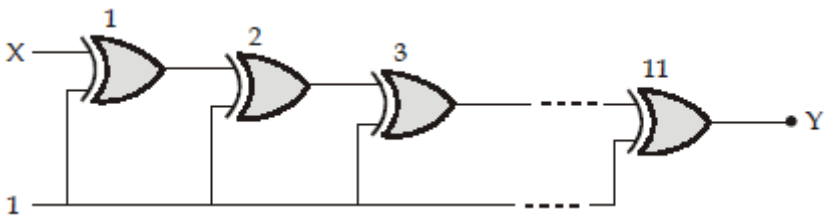
$$Q_{n+1} = \bar{A}\bar{B}Q_n + \bar{A}B\bar{Q}_n + A\bar{B}\bar{Q}_n + AB \cdot 0$$
$$= \bar{A}(B \oplus Q_n) + A\bar{B}\bar{Q}_n$$

D

$A\bar{B}Q_n + \bar{A}B$

QUESTION ANALYTICS

Q. 9



Assume in the above circuit 11 exclusive OR gate is connected in a similar fashion. What will be the output at *Y*?

Solution Video | Have any Doubt ?

A

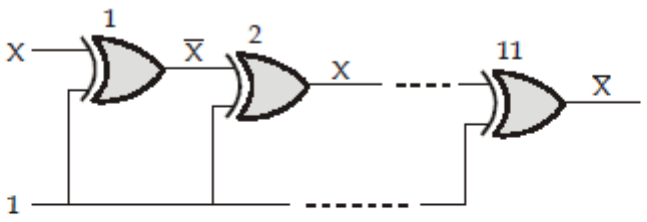
X

B

$\bar{X}$

Your answer is **Correct**

Solution :
(b)



After every two EX-OR with 1-input always 1 output the same other input (X) appear.

Hence after 10 EX-OR output will be X and last 11^{th} EX-OR output at Y will be $\bar{X}$.

C

0

D

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Q. 10

The representation of the value of a 16-bit unsigned integer X in hexadecimal number system is A72E. The representation of the value of X in octal number system is

Solution Video | Have any Doubt ?

A
12346

B
123456

Your answer is **Correct**

Solution :
(b)

Given hexadecimal value A72E in binary we can write:

1010 011 100 101 110
1 2 3 4 5 6

Now we can make the pair of 3 from left hand side to convert them int octal because oct
3 bits in each representation.
So answer will be $(123456)_8$ which is option (b).

C
125756

D
10634

QUESTION ANALYTICS

Q. 11

If $(504)_X$ in base-X is equal to $(2320)_4$. Then what will be the value of base-X (in decimal) _____?

Solution Video | Have any Doubt ?

6

Your answer is **Correct**6

Solution :
6

$$\text{Given,} \quad (504)_X = (2320)_4$$
$$(2320)_4 = 2 \times 4^3 + 3 \times 4^2 + 2 \times 4^1 + 0 \times 4^0$$
$$= 128 + 48 + 8$$
$$= (184)_{10}$$
$$\text{Now,} \quad (184)_{10} = (504)_X$$

$5x^2 + 4 = 184$
$5x^2 = 180$
$x^2 = 36$
$x = +6$
Hence base is 6.

QUESTION ANALYTICS

Q. 12

Consider a 4-bit ripple carry adder for computing sum of 2 different numbers X and Y. These numbers are represented in 2's complement form. If the decimal value of X is +7 the minimal decimal value of Y that leads to longest latency for the sum to stabilize is _____.

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Correct Option

Solution :
-7

Given,

$$X = +7 \Rightarrow 0111$$
$$Y = ?$$

For longest latency in the 4-bit ripple carry adder and also minimal.

It means to make longest latency carry should be propagated from LSB to MSB. To make t

$$X = \quad 0111 \quad (+7)$$
$$Y = +1001 \quad (-7)$$
$$\text{Carry out} \longrightarrow \textcircled{1}0001$$

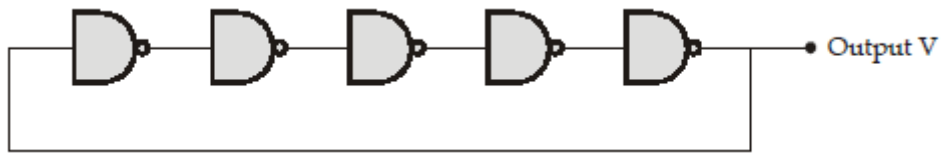
Hence the decimal value is (–7).

Your Answer is -1

QUESTION ANALYTICS

Q. 13

Each NAND gate has propagation delay of 100 nanoseconds (ns).



The frequency at output V (in MHz) is _____.

Solution Video | Have any Doubt ?

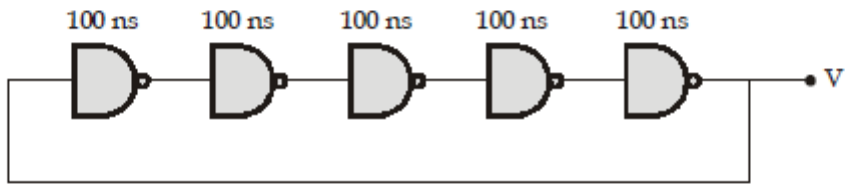
1

Correct Option

Solution :
1

Each NAND gate in the circuit is working as a NOT gate and number of NAND is odd. To a periodic signal with the odd number of gates, frequency (f) at V is

$$f = \frac{1}{2\times\text{Propagation delay}}$$



$$f = \frac{1}{2\times(100+100+100+100+100)\text{ns}}$$

$$= \frac{10^9}{10^3}\text{Hz} = 10^6\ \text{Hz} = 1\ \text{MHz}$$

Your Answer is 2

QUESTION ANALYTICS

Q. 14

A 16 × 1 MUX is implemented using 4 × 1 MUX. Assume at level 1 and level 2 of circuit X and Y number of MUX required respectively. Then value of (X – Y) is _____.

Solution Video | Have any Doubt ?

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Solution :
3

To implement 16 × 1 MUX using 4 × 1 MUX

A level 1:

$$\text{Number of } 4 \times 1 \text{ MUX required} = \frac{16}{4} = 4$$

Hence $X = 4$

A level 2:

$$\text{Number of } 4 \times 1 \text{ MUX required} = \frac{4}{4} = 1$$

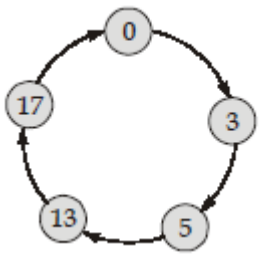
Hence $Y = 1$

$$X - Y = 4 - 1 = 3$$

QUESTION ANALYTICS

Q. 15

The sequence diagram of a counter is shown in the figure below:



If the state value shown in the diagram are decimal equivalents. The number of FF's required to implement the counter is _____.

Have any Doubt ?

5

Your answer is **Correct**5

Solution :
5

Here number of states = 5

But it is mentioned that decimal in the states.

So number of flip-flops required defined by the sequence not by the number of states.

Here maximum sequence number is 17.

$$2^n \geq 17 \; [n \text{ is number of FF}]$$

$$n \geq \lceil \log_2(17) \rceil$$

$$n = 5$$

QUESTION ANALYTICS

Q. 16

The maximum number of boolean functions in 3 boolean variables is _____.

Solution Video | Have any Doubt ?

256

Your answer is **Correct**256

Solution :
256

Total number of function on *n* variables are

$$= 2^{2^n}$$

$$\text{For 3 variable} = 2^{2^3} = 2^8$$

$$= 256$$

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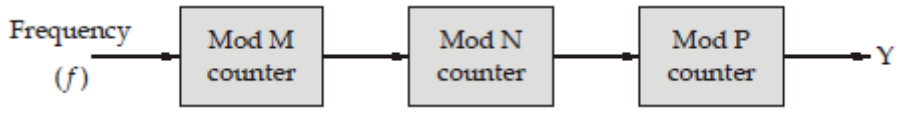
Q. 17

Consider the figure given below:



Assume frequency f is applied at M counter. All the counters M, N and P are cascaded one after another. The output is at Y after P counter. Which of the following option holds?

Solution Video | Have any Doubt ?

A
Mod M + N + P counter, f/(M + N + P) at Y.

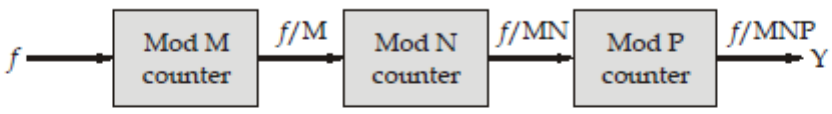
B
Mod M × N × P counter, (f/M + f/N + f/P) at Y.

C
Mod M × N × P counter, f/(MNP) at Y.

Your answer is **Correct**

Solution :
(c)

If Mod M, Mod N, Mod P counters are cascaded then it will act as a Mod M × N × P count



Frequency gets divided by number of states in counter, $\frac{f}{\text{Number of states}}$

After M counter, frequency becomes f/M input to N
After N counter, frequency becomes $f/M \times N$, input to P
After P counter, frequency becomes f/MNP
Hence at Y frequency will be f/MNP.

D
Count is not possible because cascaded.

QUESTION ANALYTICS

Q. 18

Consider the following statements:
(i) Number of unused states in Ring counter for N-bit is (2N – N).
(ii) Number of unused states in Johnson counter for N-bit is (2N – 2N).
(iii) Any count sequence can be designed with synchronous counter but not with asynchronous counter.
Which of the following statements are correct?

Solution Video | Have any Doubt ?

A
Only (i)

B
Only (ii)

C
Only (ii) and (iii)

D
All of the above

Correct Option

Solution :

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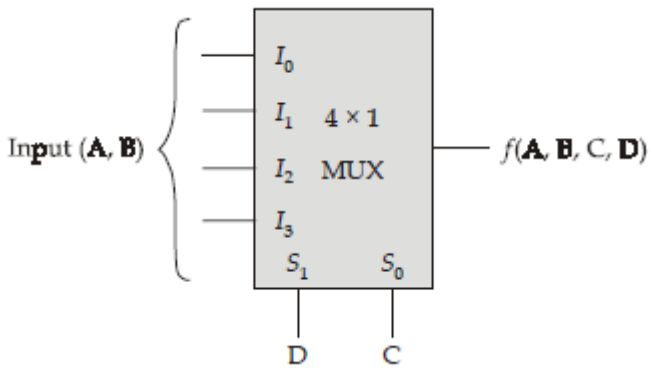
QUESTION ANALYTICS

Q. 19

A 4 × 1 MUX is used to realize a 4-variable function, f(A, B, C, D) = Σm (0, 3, 4, 8, 9, 15). The inputs to the MUX are from variables A and B, then the input to the MUX from I_0 to I_3 respectively are



Solution Video | Have any Doubt ?

A

$\overline{A}+\overline{B}, 0, A\overline{B}, A \odot B$

Your answer is **Correct**

Solution :
(a)
The input can be determined by constructing the table as below for function f(A, B, C, D).

Now,
$$I_0 = \overline{A}\,\overline{B} + \overline{A}B + A\overline{B}$$
$$= \overline{A}(B+\overline{B}) + A\overline{B}$$
$$= \overline{A} + A\overline{B}$$
$$= \overline{A} + \overline{B}$$
$$I_1 = 0$$
$$I_2 = A\overline{B}$$
$$I_3 = A\overline{B} + AB$$
$$= A \odot B$$

	$\overline{C}\overline{D}$ I_0	$C\overline{D}$ I_1	$\overline{C}D$ I_2	
$\overline{A}\,\overline{B}$	⓪	2	1	
$\overline{A}B$	④	6	5	
$A\overline{B}$	⑧	10	⑨	
AB	12	14	13	
	$\overline{A}+\overline{B}$	0	$A\overline{B}$	A

B

$\overline{A}, 0, \overline{A}B, A \oplus B$

C

$\overline{A}\,\overline{B}, 0, A\overline{B}, A \odot B$

D

$\overline{A}+\overline{B}, 1, A\overline{B}, A \oplus B$

QUESTION ANALYTICS

Q. 20

A 1-bit binary comparator is designed. The only one output is active high for any given input to the comparator out of the 3 outputs. The variable X is used to count minimum number of minterms for equality checking, Y for greater than and Z for less than comparison then X + Y + Z is

Solution Video | Have any Doubt ?

A

3

B

4

Your answer is **Correct**

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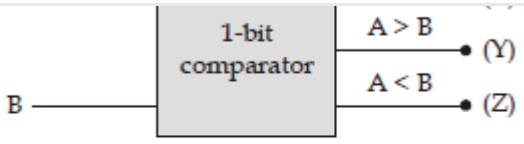


A	B	(A = B) X	A > B Y	A < B Z
0	0	(1)	0	0
0	1	0	0	(1)
1	0	0	(1)	0
1	1	(1)	0	0

$$X = \bar{A}\bar{B} + AB$$

Number of minterms = 2

$$Y = A\bar{B}$$

Number of minterms = 1

$$Z = \bar{A}B$$

Number of minterms = 1

Hence, $X + Y + Z = 2 + 1 + 1 = 4$

Total 4 minterms.

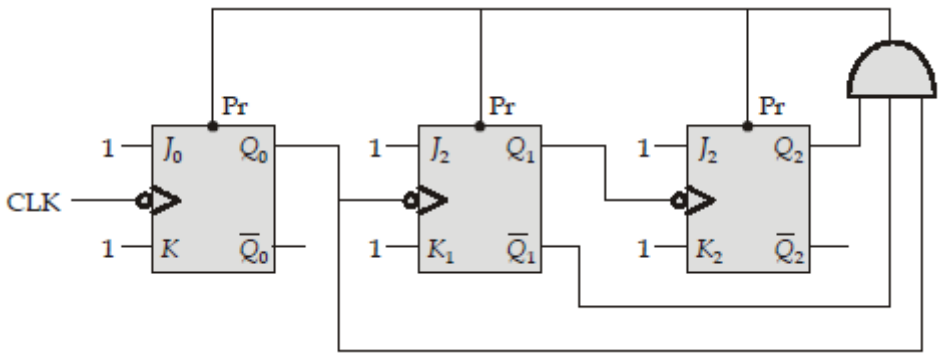
C
5

D
6

QUESTION ANALYTICS

Q. 21

Consider the below asynchronous sequential circuit. An active high preset button Pr is used in each J-K flip-flop. What will be the mod of the given circuit, initially all FF's are set.



Solution Video | Have any Doubt ?

A
4

B
5

Your answer is **Wrong**

C
6

Correct Option

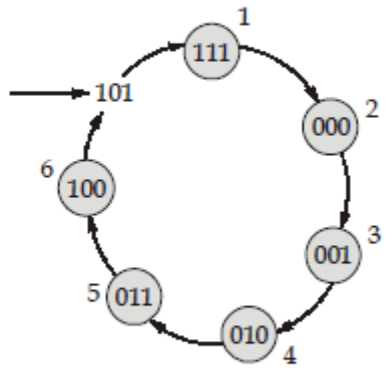
Solution :
(c)

Pr is high when, $Q_2\,\bar{Q}_1\,Q_0 = 101$

CLK	Q_2	Q_1	Q_0	$J_0=1$ $K_0=1$	$J_1=1$ $K_1=1$	$J_2=1$ $K_2=1$
	1	1	1	1 1	1 1	1 1
1	0	0	0	1 1	1 1	1 1
2	0	0	1	1 1	1 1	1 1

1	1	1	1	1	1	1	1	1	

After six clock pulses when $Q_2\bar{Q}_1Q_0 = 101$, suddenly state 101 disappears very fast and becomes 111 because of preset button becomes active.
State diagram is as follows:



Hence total 6 states will be counted.

D
7

QUESTION ANALYTICS

Q. 22

Which of the following is true?

Solution Video | Have any Doubt ?

A
Number of Prime Implicants (PI) is same as the number of terms obtained in minimized function of K-map.

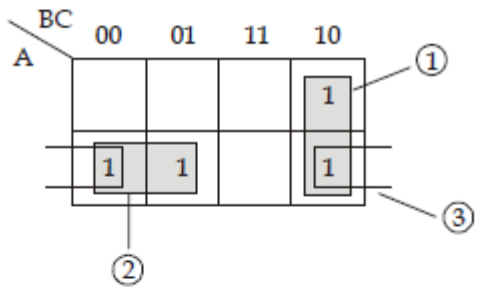
B
Minterms of K-map is always the subset of Prime Implicants (PI).

Correct Option

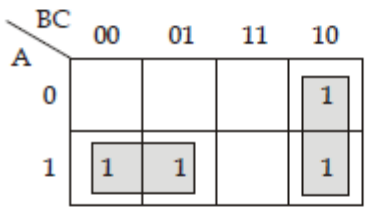
Solution :
(b)

A Prime Implicants is a product term obtained by combining the maximum possible num adjacent squares.

(a) It is not always true that number of PI is same as the number of terms in minimized fu of K-map.
For example, for same function number of PI differs with number of minterms as s below:



Number of prime implicants = 3
Prime implicants are ($A\bar{C}$, $B\bar{C}$, $A\bar{B}$)



Minimized function = $A\bar{B} + B\bar{C}$
Number of terms = 2

(b) Statement (b) is true. As we can see in above example minimized functions mintern present in Prime Implicants.

C
Both are true

D
None of the above

Your answer is **Wrong**

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Q. 23

Given the function F = X + Y'Z, when F is a function of 3 boolean variables X, Y and Z. Consider the following statements:

$S_1 : F = \sum (0, 1, 2, 3, 4)$
$S_2 : F = \sum (1, 4, 5, 6, 7)$
$S_3 : F = \Pi (0, 2, 3)$
$S_4 : F = \Pi (5, 6, 7)$

Which of the following is true?

Solution Video | Have any Doubt ?

A
S_1 - false, S_2 - true, S_3 - false, S_4 - true

B
S_1 - true, S_2 - false, S_3 - true, S_4 - false

C
S_1 - true, S_2 - false, S_3 - false, S_4 - true

D
S_1 - false, S_2 - true, S_3 - true, S_4 - false

Your answer is **Correct**

Solution :
(d)

X \ YZ	00	01	11	10
0	0	1	2	3
1	4 1	5 1	6 1	7 1

$F = \sum m (1, 4, 5, 6, 7) = \Pi_M (0, 2, 3)$

Hence statement S_2 and S_3 are true and S_1 and S_4 are false.

QUESTION ANALYTICS

Q. 24

Let A = 11111010 and B = 00001111 be two 8-bit 2's complement numbers. Their product in 2's complements is

Solution Video | Have any Doubt ?

A
01011010

B
10100110

Your answer is **Correct**

Solution :
(b)

$$A = 11111010 \text{ (MSB = 1, hence negative number)}$$
$$2\text{'s complement of A} = 00000110$$
$$\text{Magnitude of A} = (-6)_{10}$$
$$B = 00001111 \text{ (MSB = 0, hence positive number)}$$
$$\text{Magnitude of B} = (15)_{10}$$
$$A \times B = 15 \times (-6) = -90$$

So the value of A × B in 2's complement representation is [10100110]

$$+90 = 01011010$$
$$-90 = 10100110 \quad [2\text{'s complement}]$$

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D
11010101

QUESTION ANALYTICS

Q. 25

Consider a 5 bit ring counter with an initial value of 00001. The next counting sequence of this counter is

Solution Video | Have any Doubt ?

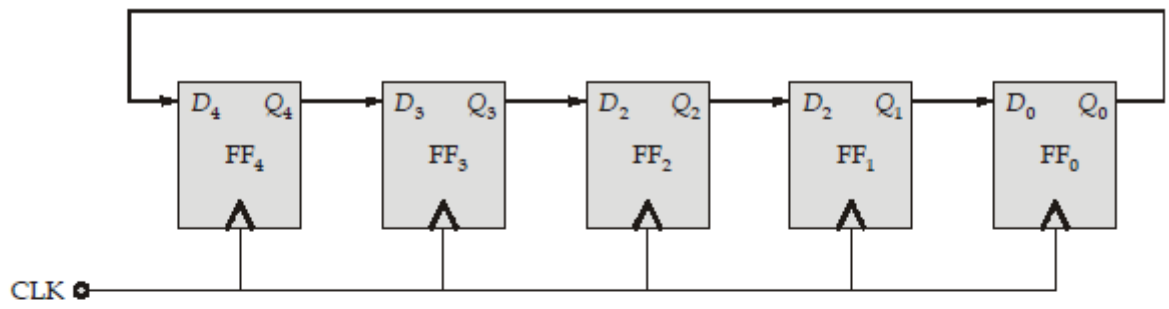
A
1, 2, 4, 8, 16, 1

Your answer is **Wrong**

B
1, 16, 8, 4, 2, 1

Correct Option

Solution :
(b)



The above circuit represents 5-bit ring counter.

CLK	$D_4 = Q_0$	Q_4	Q_3	Q_2	Q_1	Q_0	
		0	0	0	0	1	← Starting
1	1	1	0	0	0	0	
2	0	0	1	0	0	0	
3	0	0	0	1	0	0	
4	0	0	0	0	1	0	
5	0	0	0	0	0	1	

Hence the switching sequence is 1, 16, 8, 4, 2, 1.

C
1, 2, 3, 4, 5, 1

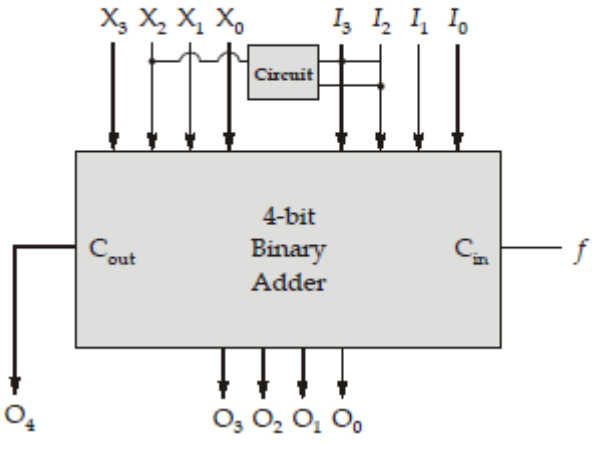
D
1, 4, 8, 16, 2, 1

QUESTION ANALYTICS

Q. 26

Consider the below circuit which has four bit binary number as input and a five bit binary number as output:

Input: $I_3\ I_2\ I_1\ I_0$
Output: $O_4\ O_3\ O_2\ O_1\ O_0$



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A
NAND, 2

B
AND, 4

Correct Option

Solution :
(b)
Logic gate AND is required whenever I_3I_2 becomes 1, then the value will exceed from 12 whic not allowed in base 12. Hence we need to add whenever input is $(1100)_2$. To make (1100) $(0000)_2$ we need to add (0100) to $(X_3X_2X_1X_0)$. X_2 will be 1 only when I_3 and I_2 is 1.
Hence AND gate is required and decimal value of (0100) is 4 will be added.

C
NAND, 4

D
AND, 12

QUESTION ANALYTICS

Q. 27

If $Y = ABC + \overline{\overline{BC} + \overline{A}C} + \overline{A}\overline{C}$ then dual of Y are

Solution Video | Have any Doubt ?

A
$(A+B+C)\cdot[\overline{B}\overline{C}+A]\cdot(A\overline{C})$

B
$(A+B+C)\cdot\left[\overline{(B+C)\cdot(C)}\right]\cdot(\overline{A}+\overline{C})$

C
$(A+B+C)\cdot(\overline{B}\overline{C}+A\overline{C})\cdot(\overline{A}+\overline{C})$

Your answer is **Correct**

Solution :
(c)

$$Y = ABC+\overline{\overline{BC}+\overline{A}C}+\overline{A}\overline{C}$$

$$\text{Dual of } Y \cdot Y_d = (A+B+C)\cdot\overline{(B+C)\cdot(\overline{A}+C)}\cdot(\overline{A}+\overline{C})$$

$$= (A+B+C)\cdot\left[\overline{(B+C)}+\overline{(\overline{A}+C)}\right]\cdot(\overline{A}+\overline{C})$$

$$= (A+B+C)(\overline{B}\overline{C}+A\overline{C})\cdot(\overline{A}+\overline{C})$$

Which is clearly option (c).

D
$(ABC)\cdot(\overline{B}\overline{C}+\overline{A}C)\cdot(\overline{A}+\overline{C})$

QUESTION ANALYTICS

Q. 28

Which of the following is not true?

Solution Video | Have any Doubt ?

B

The (r – 1)'s complement of a positive number N in base r is (r^n – N – 1).

C

The (r – 1)'s complement of a positive number N having n digits and m digits in integer and fraction respectively in base r is (r^n – r^{-m} – N).

D

The (r – 1)'s complement of a positive number N having n digit and m digits in integer and fraction part respectively in base r is (r^n – r^m – N).

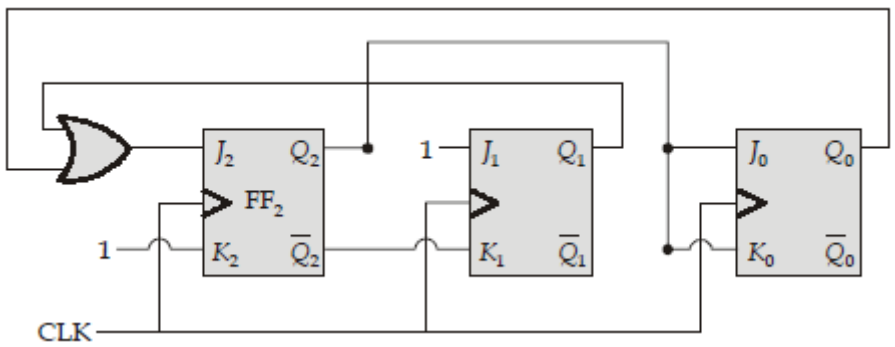
Your answer is **Correct**

Solution :
(d)

QUESTION ANALYTICS

Q. 29

Consider the below circuit:



The above circuit forms a counter of MOD _____.

Solution Video | Have any Doubt ?

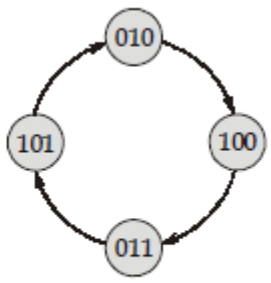
4

Your answer is **Correct**4

Solution :
4

CLK	Q_2	Q_1	Q_0	$J_2 = Q_1 + Q_0$	$K_2 = 1$	$J_1 = 1$	$K_1 = \overline{Q}_2$	$J_0 = Q_2$	$K_0 = Q_2$
	0	0	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1	0	0
2	1	0	0	0	1	1	0	1	1
3	0	1	1	1	1	1	1	0	0
4	1	0	1	1	1	1	0	1	1
	0	1	0						

Although we have started from $(Q_2Q_1Q_0) = (000)$ but we did not get $(Q_2Q_1Q_0) = (000)$ in clock cycles. Hence only 4 different states is repeating and (000) is unused state.



Hence the answer is 4.

QUESTION ANALYTICS

Q. 30

A 3 × 8 decoder has used to implement a full adder and only 2-input OR-gate is available to get the sum and

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6

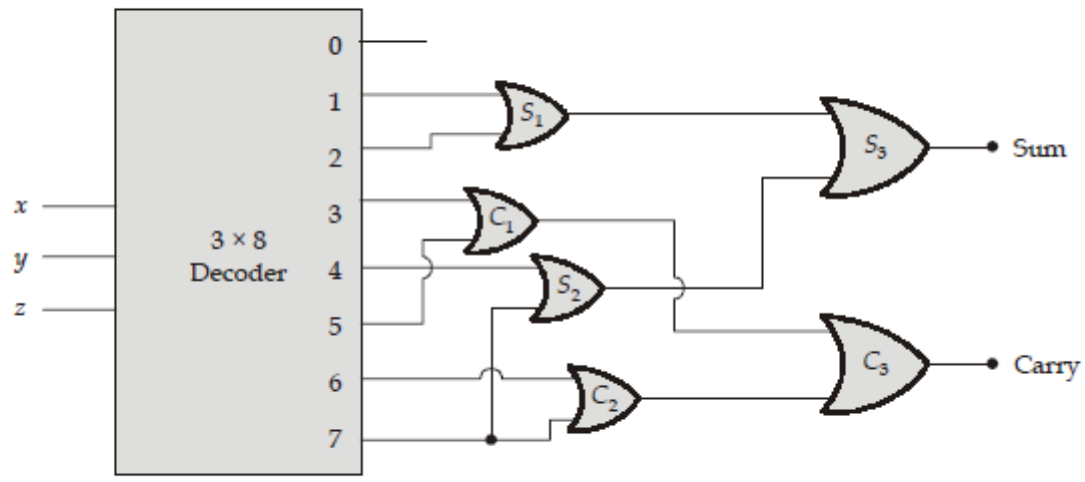
Correct Option

Solution :

6

To implement full adder using 3 × 8 decoder

$$\text{Sum}\ (x, y, z) = \Sigma(1, 2, 4, 7)$$
$$\text{Carry}\ (x, y, z) = \Sigma(3, 5, 6, 7)$$

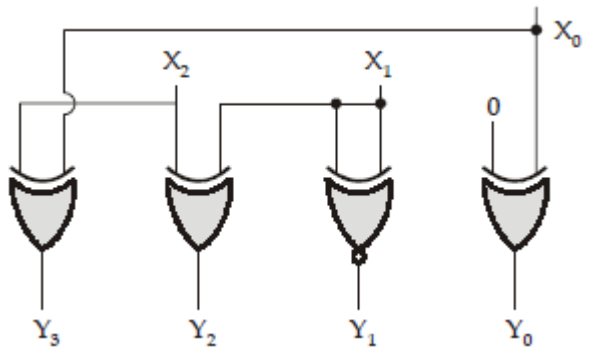


Hence 3 OR-gate is required for sum and 3-OR-gate is required for carry.
So, total 6 OR-gates is needed.

QUESTION ANALYTICS

Q. 31

Consider the circuit shown in the figure below:



If the three bit input to the circuit is $(X_2X_1X_0) = 111$ then the decimal equivalent of the corresponding output of the circuit $(Y_3Y_2Y_1Y_0)$ will be equal to _____.

Solution Video | Have any Doubt ?

3

Your answer is **Correct**3

Solution :

3

From the figure

$$Y_0 = X_0 \oplus 0$$
$$Y_1 = X_1 \odot X_1$$
$$Y_2 = X_1 \oplus X_2$$
$$Y_3 = X_0 \oplus X_2$$

Now for given input $(X_2X_1X_0) = 111$

$$Y_0 = 1$$
$$Y_1 = 1$$
$$Y_2 = 0$$
$$Y_3 = 0$$
$$= (0011)_2 = (3)_{10}$$

QUESTION ANALYTICS

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Solution Video | Have any Doubt ?

6

Your answer is Correct6

Solution :
6

To represent 19 bit of binary data the maximum value can be 2^{19}.

$$2^{19} = 10^n$$

n = Number of decimal digits required

$$n = \lceil \log_{10}(2^{19}) \rceil$$

$$n = \lceil \log_{10}(524288) \rceil$$

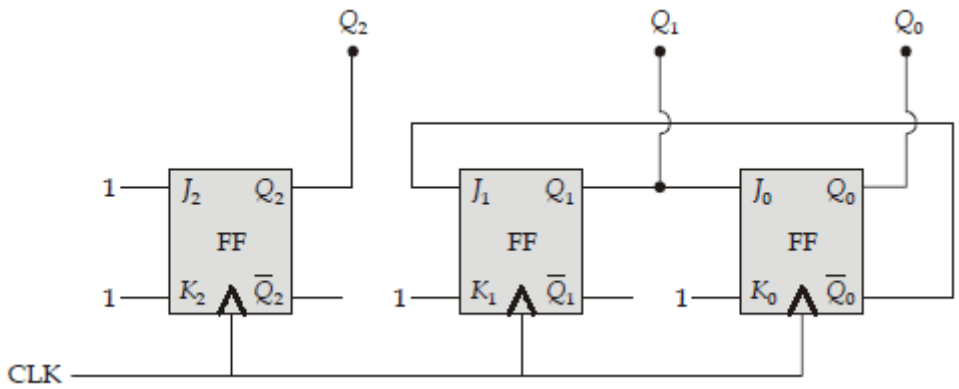
$$n = \lceil 5.719 \rceil$$

$$n = 6$$

QUESTION ANALYTICS

Q. 33

Consider the below sequential circuit using J-K flip-flops. Initially the output at $(Q_2Q_1Q_0) = (001)$.



The number of clock cycles required to get at $Q_2Q_1Q_0 = 000$ is _____.

Solution Video | Have any Doubt ?

4

Your answer is Correct4

Solution :
4

	Present state								
CLK	Q_2	Q_1	Q_0	$J_2=1$	$K_2=1$	$J_1=\overline{Q}_0$	$K_1=1$	$J_0=Q_1$	$K_0=1$
	0	0	1	1	1	0	1	0	1
1	1	0	0	1	1	1	1	0	1
2	0	1	0	1	1	1	1	1	1
3	1	0	1	1	1	0	1	0	1
4	0	0	0						

Hence total 4 clocks are required to get the desired state 000.

QUESTION ANALYTICS