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TOPICWISE : DIGITAL LOGIC-2 (GATE - 2019) - REPORTS

OVERALL ANALYSIS　　　COMPARISON REPORT　　　**SOLUTION REPORT**

ALL(17)　　　CORRECT(5)　　　INCORRECT(4)　　　SKIPPED(8)

Q. 1

The race around condition occurs in a level trigger J-K flip-flop when

▶ Solution Video　|　Have any Doubt ?　|　🔖

A
Both the inputs are 0

B
Both the inputs are 1

Your answer is **Correct**

Solution :
(b)
In J-K flip-flop

J	K	Output
1	0	Set
0	1	Reset
0	0	Hold
1	1	Race around

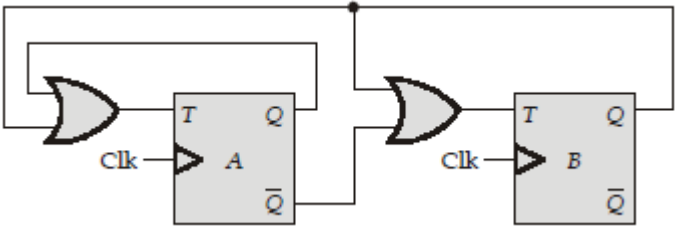**C**
J = 1 and K = 0

D
J = 0 and K = 1

QUESTION ANALYTICS

Q. 2

The circuit shown in figure below is:

FAQ　|　▶ Solution Video　|　Have any Doubt ?　|　🔖

A
a MOD-2 counter

B
a MOD-3 counter

Your answer is **Correct**

Solution :
(b)
The truth table for the circuit is obtained below:

Present state		FF input		Next state	
Q_A	Q_B	T_A $(Q_A + Q_B)$	T_B $(\bar{Q}_A + Q_B)$	Q_A^+	Q_B^+

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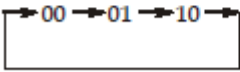
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So, the counter counts the sequence of 3 states as

00 → 01 → 10

Hence, the circuit is of a MOD-3 counter.

C

Generate sequence 00, 10, 01, 00 .....

D

Generate sequence 00, 10, 00, 10, 00 .....

QUESTION ANALYTICS

Q. 3

If Booth's Algorithm for multiplication is used then which of the following represents multiplier −29 in recorded form?

▶ Solution Video | Have any Doubt ? 🔖

A
$00 - 10 + 100 - 1$

B
$00 - 100 - 10 + 1$

C
$00 - 100 + 10 - 1$

Correct Option

Solution :
(c)
2's complement representation of −29 is 11100011.

1	0	−1
1	1	0
0	1	+1
0	0	0
0	0	0
1	0	−1
1	1	0
1	1	0

Recorded pair is : $00 - 100 + 10 - 1$.

D
$00 - 100 + 10 + 1$

QUESTION ANALYTICS

Q. 4

The representation of the value of 20 bit signed integer in 2's complement form is P = $(A72E5)_{16}$. Which of the following represents $16 \times P$ in 1's complement representation?

FAQ | ▶ Solution Video | See your Answers 🔖

A
$(72E4F)_{20}$

Correct Option

Solution :
(a)

$P = (A72E5)_{20}$
$= 1010\ 0111\ 0010\ 1110\ 0101$

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$$\frac{0111\ 0010\ 1110\ 0100\ 1111}{}^{-1}$$

$$= (72E4F)_{20}$$

B

$(72E50)_{20}$

C

$(72E4E)_{20}$

D

None of the above

Your answer is **Wrong**

QUESTION ANALYTICS

Q. 5

Amazon announce a new flip flop named Set-Reset-Toggle due to shortage elements to the electronics and computer industries. The device symbol and function table for this flip flop are shown below:

S	R	T	Function
X	X	1	Toggle
1	1	0	Set
0	0	0	Reset
0	0	0	Hold
1	1	0	Hold
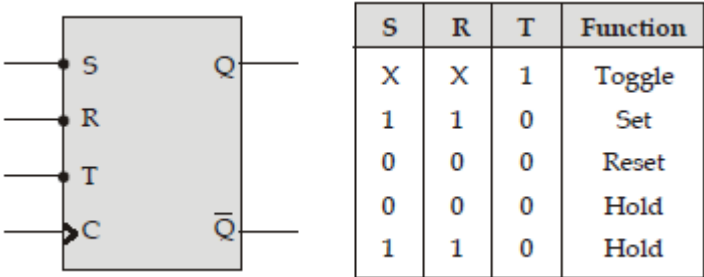
Which of the following is the characteristic equation?

FAQ | ⊙ Solution Video | Have any Doubt ?

A

$Q^{+} = TQ' + T'[Q(S \oplus R) + SR']$

B

$Q^{+} = (T \oplus Q) + S + R'Q$

C

$Q^{+} = T'Q + T[Q'(S + R) + SR']$

D

$Q^{+} = TQ' + T'[Q(S + R') + SR']$

Correct Option

Solution :
(d)

S	R	T	Q	Q⁺
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

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Q. 6

The minimum value of propagation delay in each Flip-Flop when a 10-bit ripple counter skip a count which is clocked at 10 MHz is _____ nsec.

▶ Solution Video | Have any Doubt ?

10

Correct Option

Solution :
10

We know that for a stage change to ripple through n stages i.e. $T_C = n \times t_{pd}$.

$$f_c = \frac{1}{T_C}$$

$$f_c = \frac{1}{n \times t_{pd}}$$

So,

$$t_{pd} = \frac{1}{n \times f_c}$$

$$t_{pd}(min) = \frac{1}{10 \times 10 \times 10^6 \, Hz}$$

$$= 0.01 \times 10^{-6} \, sec$$

$$= 10 \times 10^{-9} \, sec$$

$$= 10 \, nsec$$

Your Answer is 1000

Q. 7

Consider the counter circuit shown in the figure below:
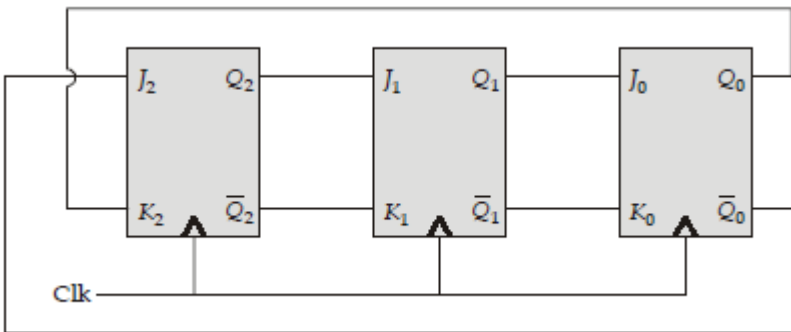
The present state ($Q_2 Q_1 Q_0$) of the counter before applying the clock pulse was (101). If the input clock frequency to the circuit is 100 kHz, then the output frequency of the circuit will be _____ kHz.

▶ Solution Video | Have any Doubt ?

50

Correct Option

Solution :
50

Clock	Q_2	Q_1	Q_0
0	1	0	1
1	0	1	0
2	1	0	1

Hence, the sequence repeats itself after 2 clock pulses. Thus it is a divide by two counter.

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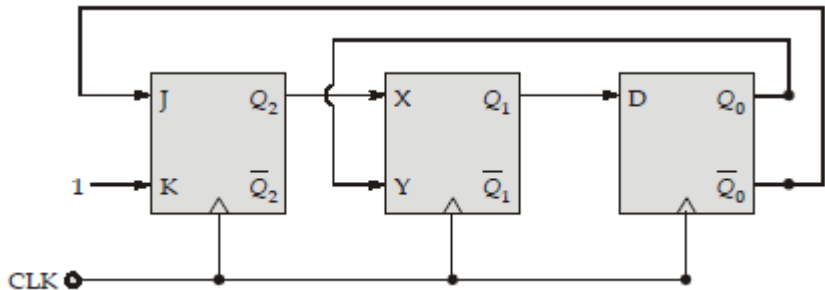Computer Science Engineering(CS)

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QUESTION ANALYTICS

Q. 8

A synchronous counter is designed using J-K FF, X-Y FF and D-FF as shown below. X-Y FF truth table is

X	Y	Q_{n+1}
0	0	1
0	1	$\overline{Q_n}$
1	0	0
1	1	Q_n

If the initial content of the counter is 001 at Q_2, Q_1, Q_0, after the number of clock pulses counter is back to the same state is _____.

▶ Solution Video | Have any Doubt ?

4

Correct Option

Solution :
4

CLK	Q_2	Q_1	Q_0	$J = \overline{Q_0}$	K = 1	$X = Q_2$	$Y = Q_0$	$D = Q_1$
				FF2		FF1		FF0
	0	0	1	0	1	0	1	0
1	0	1	0	1	1	0	0	1
2	1	1	1	0	1	1	1	1
3	0	1	1	0	1	0	1	1
4	0	0	1					

∴ Counter is back to the initial state after 4 clock pulses.

Your Answer is 3

QUESTION ANALYTICS

Q. 9

The difference between 201 and next larger double precision number is 2^P, if IEEE double precision format is used then the value of P is _____.

FAQ | ▶ Solution Video | Have any Doubt ?
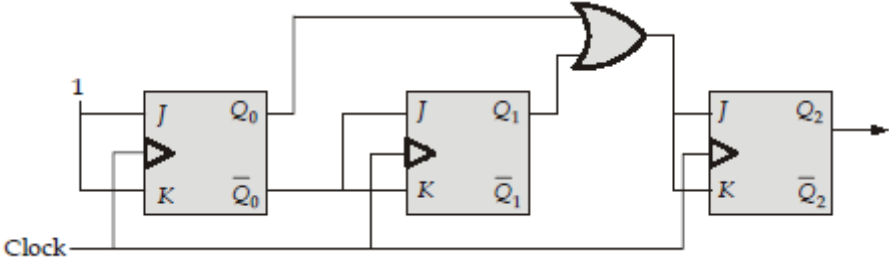
-45

Correct Option

Solution :
-45

Format of IEEE double Precision:

Sign	Exponant	Mantissa
1 bit	11 bits	52 bits

$$= 2^{-45}$$

Comparing with 2^P will gives P = –45.

QUESTION ANALYTICS

Q. 10

Consider the circuit given below with initial state $Q_2 Q_1 Q_0$ = 000.

Which one of the following is the correct state sequence of the circuit?

FAQ | ⊙ Solution Video | Have any Doubt ?

A

0, 6, 3, 4, 1, 7, 2, 5, 0

B

0, 3, 6, 1, 4, 7, 2, 5, 0

Your answer is **Correct**

Solution :
(b)

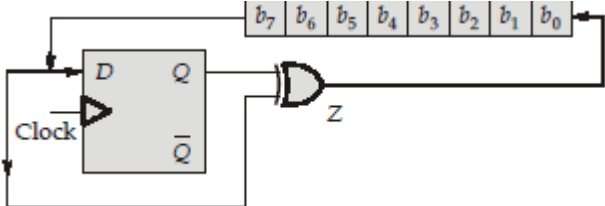| $J = K = 1$	$J = K = \overline{Q}_0$	$J = K = Q_0 + Q_1$	
Q_0	Q_1	Q_2	
0	0	0	= 0
1	1	0	= 3
0	1	1	= 6
1	0	0	= 1
0	0	1	= 4
1	1	1	= 7
0	1	0	= 2
1	0	1	= 5
0	0	0	= 0

So, sequence must be 0, 3, 6, 1, 4, 7, 2, 5, 0.

C

0, 3, 6, 4, 1, 7, 2, 5, 0

D

0, 6, 3, 1, 4, 7, 2, 5, 0

QUESTION ANALYTICS

Q. 11

Consider 8-bit left shift register and D flip-flop shown in figure below is synchronized with same clock. The D flip-flop is initially cleared.

Which of the following represents the behaviour of above circuit?

⊙ Solution Video | Have any Doubt ?

A

Binary to 2's complement converter

C

Binary to Excess−3 code converter

D

Binary to Gray code converter

Your answer is Correct

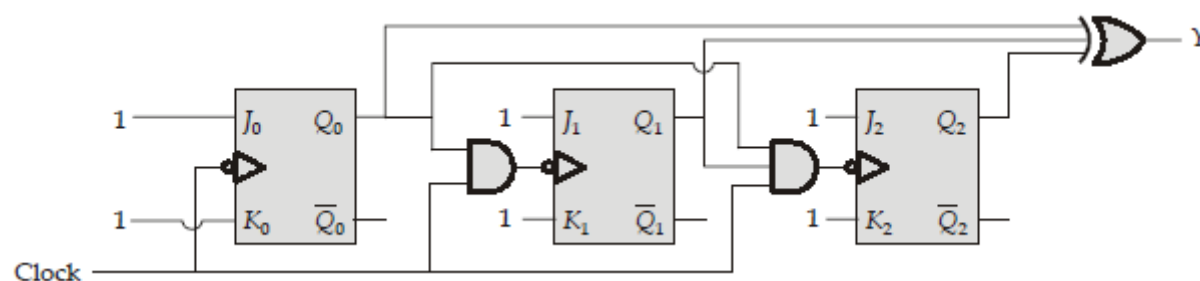**Solution :**

(d)

$$\text{Output of ExOR Gate} = b_i \oplus b_{i+1}$$

Initially $Q = 0$ assume

So,   After 1 clock, $Z = b_7 \oplus b_0$

            After 2 clock, $Z = b_7 \oplus b_6$

            After 3 clock, $Z = b_6 \oplus b_5$

            After 4 clock, $Z = b_5 \oplus b_4$

            After 5 clock, $Z = b_4 \oplus b_3$

            After 6 clock, $Z = b_3 \oplus b_2$

            After 7 clock, $Z = b_2 \oplus b_1$

            After 8 clock, $Z = b_1 \oplus b_0$

Which is same as Binary to gray code converter.

QUESTION ANALYTICS

Q. 12

Consider the circuit shown in the figure below:

The value of output $Q_0 Q_1 Q_2$ and the value of output Y after the 5th clock pulse is (Assume that initially all the flip-flop are in reset state)

FAQ | ▶ Solution Video | Have any Doubt ? 🔖

A

Output = 001 and $Y = 1$

B

Output = 101 and $Y = 0$

Correct Option

Solution :

(b)

The given circuit represents a 3-bit counter. So the count can be represented as

Clk	Q_2	Q_1	Q_0	
Initially	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	⇒ 5th clock pulse
6	1	1	0	
7	1	1	1	

∴

$$Y = Q_2 \oplus Q_1 \oplus Q_0$$
$$= 1 \oplus 0 \oplus 1 = 0$$

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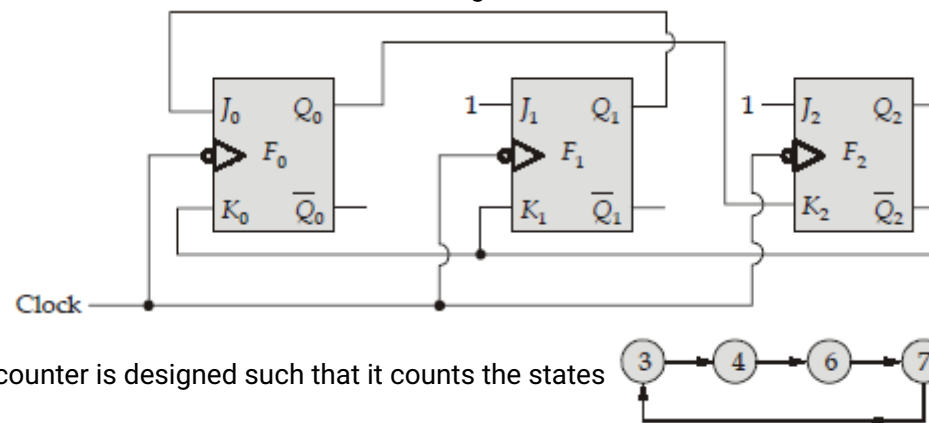

D

Output = 010 and $Y = 1$

QUESTION ANALYTICS

Q. 13

Consider the counter circuit shown in the figure below:

The counter is designed such that it counts the states $3 \rightarrow 4 \rightarrow 6 \rightarrow 7$, then which of the following statements about this counter is true?

FAQ | ▶ Solution Video | Have any Doubt ?

A

The counter enters into a lockout state if the counter starts from $(5)_{10}$

B

The counter enters into a lockout state if the counter starts from $(2)_{10}$

C

The counter enters into a lockout state if the counter starts from $(3)_{10}$

D

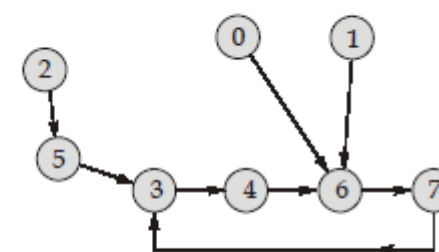The counter do not enters into a lockout state

Correct Option

Solution :
(d)
Test for Lockout

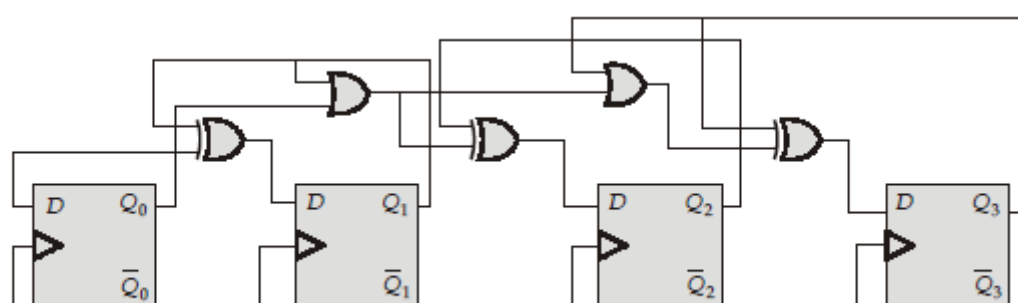| Present State			Present Input						Nest State		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2	Q_1	Q_0
0	0	0	1	0	1	1	0	1	1	1	0
0	0	1	1	1	1	1	0	1	1	1	0
0	1	0	1	0	1	1	1	1	1	0	1
1	0	1	1	1	1	0	0	0	0	1	1

Hence, the counter does not enter into lockout state.

QUESTION ANALYTICS

Q. 14

Consider Register R shown below:

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A

X

Correct Option

Solution :
(a)

After 1st clock tick:

$$x_0^+ = x_0$$
$$x_1^+ = x_0 \oplus x_1$$
$$x_2^+ = (x_0 + x_1) \oplus x_2$$
$$x_3^+ = (x_0 + x_1 + x_2) \oplus x_3$$

After 2nd clock tick:

$$(x_0^+)^+ = x_0^+ = x_0$$
$$(x_1^+)^+ = x_0^+ \oplus x_1^+ = x_0 \oplus x_0 \oplus x_1 = 0 \oplus x_1 = x_1$$
$$(x_2^+)^+ = (x_0^+ + x_1^+) \oplus x_2^+ = (x_0 + (x_0 \oplus x_1)) \oplus (x_0 + x_1) \oplus x_2$$
$$= x_0 \oplus x_0 \oplus x_1 \oplus x_0 \oplus x_0 x_1 \oplus x_0 \oplus x_1 \oplus x_0 x_1 \oplus x_2$$
$$= x_2$$
$$(x_3^+)^+ = (x_0^+ + x_1^+ + x_2^+) \oplus x_3^+$$
$$= x_3 \text{ only}$$

So, after 2 clock tick Register R contain X only.

B

X + 1

C

X + 2

D

X − 1

QUESTION ANALYTICS

Q. 15

Consider a binary counter is being pulsed by a 256 kHz clock signal. If the output frequency from the last flip-flop is 8 kHz, then the mod value of counter is _____.

▶ Solution Video | Have any Doubt ?

32

Correct Option

Solution :
32

We know that, for Mod-N counter $f_o = \dfrac{f_i}{N}$

$$f_o = \text{Output frequency} = 8 \text{ kHz}$$
$$f_i = \text{Input frequency} = 256 \text{ kHz}$$

$$\text{Mod N} = \dfrac{f_i}{f_0}$$

$$= \dfrac{256 \text{ kHz}}{8 \text{ kHz}} = 32$$

QUESTION ANALYTICS

1	1 0 0 0 0 1 0 1	1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Sign	Exponant	Mantissa

The value of the number in decimal form is _____.

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-116

Correct Option

Solution :
-116

$$\text{Exponent} = 1000\ 0101 = 133$$
$$\text{Biased exponent} = \text{Actual exponent} + \text{Bias}$$
$$\text{Actual exponent} = \text{Biased exponent} - \text{Bias}$$
$$= 133 - 127 = 6$$
$$\text{Mantissa} = 11010000000000000000000$$
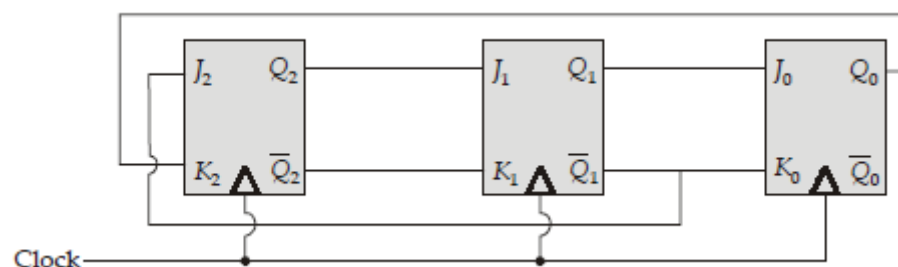$$\text{Number} = 1.1101 \times 2^6$$
$$= -1110100$$
$$= (-116)_{10}$$

Your Answer is 26

QUESTION ANALYTICS

Q. 17

Consider the circuit shown in the figure below:

Then the value of $(Q_2 Q_1 Q_0)$ after the first clock pulse is equal to _____. (Assume all the outputs to be '0' initially)

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100

Your answer is Correct 100

Solution :
100

At first cycle, the inputs of flip-flop are
$$J_2 K_2 = 1\ 0\ (\text{Set})$$
$$J_1 K_1 = 0\ 1\ (\text{Reset})$$
$$J_0 K_0 = 0\ 1\ (\text{Reset})$$
$$\therefore \qquad Q_2 = 1$$
$$Q_1 = 0$$
$$Q_0 = 0$$
$$\therefore \qquad \text{Output } (Q_2 Q_1 Q_0) = (100)_2$$

QUESTION ANALYTICS