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Computer Science Engineering(CS)

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TOPICWISE : COMPUTER ORGANIZATION AND ARCHITECTURE-2 (GATE - 2019) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(17) | CORRECT(5) | INCORRECT(7) | SKIPPED(5)

Q. 1

Which of the following is best characterize computers that use memory mapped I/O?

FAQ | Solution Video | Have any Doubt ?

A
The computer provides special instruction for manipulating I/O port.

B
I/O ports are placed at address on bus and as accessed just like other memory location.

Your answer is **Correct**

Solution :
(b)
Memory mapped I/O uses the same address bus to address both memory and I/O device
memory and registers of the I/O devices are mapped to address values.
So, when an address is accessed by the CPU, it can depict whether the address range belon
some I/O device or a memory location.

C
To perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation.

D
Ports are referenced only by memory mapped instruction of the computer and are located at hardwired memory location.

QUESTION ANALYTICS

Q. 2

Consider a direct mapped cache of size 64 KB with block size 32 bytes. The CPU generates 32 bit addresses, the size of tag memory is

Solution Video | Have any Doubt ?

A
2K × 16 byte

B
2K × 32 bit

C
1K × 32 bit

Your answer is **Correct**

Solution :
(c)

$$\text{Size of cache} = 64\ \text{KB} = 2^{16}\ \text{byte} = 16\ \text{bits}$$

$$\text{Number of cache line} = \frac{\text{Cache size}}{\text{Line size}}$$

$$= \frac{2^{16}}{2^{5}} = 2^{11}$$

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32

$$\text{Tag memory size} = \text{Number of cache lines} \times (\text{Number of tag bits in each line})$$
$$= 2^{11} \times 16$$
$$= 1K \times 32 \text{ bit}$$

D
1K × 16 byte

QUESTION ANALYTICS

Q. 3

Suppose after analyzing a new cache design, you discover that the cache has too many conflict misses and this needs to be resolved. You know that you must increase associativity in order to decrease the number of cache misses. What are the implications of increasing associativity?

Solution Video | Have any Doubt ?

A
Slower cache access time

Correct Option

Solution :
(a)
Increase in the associativity leads to increase in the number of tag comparisons. Hence it leads to increase in cache access time.

B
Increase index bits

C
Increase block size

D
All of these

Your answer is **Wrong**

QUESTION ANALYTICS

Q. 4

Consider a machine with a byte addressable main memory of 2^{24} bytes, block size is 32 bytes and 4-way set associative cache having 2^{15} cache blocks. What is the set and tag address of memory $(E4201F)_{16}$ in hexadecimal?

Solution Video | Have any Doubt ?

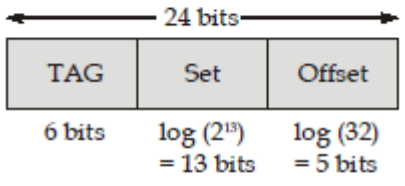
A
0100, 39

Your answer is **Correct**

Solution :
(a)

$$\text{Number of lines in cache} = 2^{15}$$

$$\text{Number of sets} = \frac{2^{15}}{2^2} = 2^{13}$$



$$\text{Tag size} = 24 - (13 + 5) = 6 \text{ bits}$$

So, $(E4201F)_{16} = 111001\ 000010\ 000000\ 011111$

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B
0010, 1F

C
0100, 27

D
0110, 37

QUESTION ANALYTICS

Q. 5

Consider a direct mapped cache with 16 blocks with block size of 16 bytes. Initially the cache is empty. The following sequence of access of memory blocks:
Ox80000, Ox80008, Ox80010, Ox80018, Ox30010
is repeated 10 times. Which of the following represents number of compulsory and conflict misses?

FAQ | Solution Video | Have any Doubt ?

A
Compulsory = 2 and conflict = 18

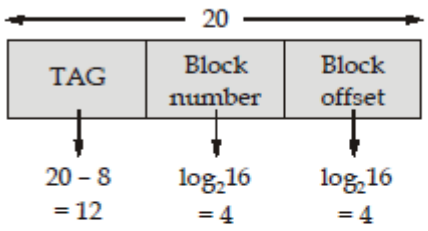
B
Compulsory = 3 and conflict = 18

Correct Option

Solution :
(b)

Main memory address size = 5 × 4 = 20 bits

Direct mapped cache:



1st pass:

1. Ox800 0 0 = Compulsory misses
2. Ox800 0 8 = Hit
3. Ox800 1 0 = Compulsory misses
4. Ox800 1 8 = Hit
5. Ox300 1 0 = Compulsory misses

2nd pass:

1. Ox800 0 0 = Hit
2. Ox800 0 8 = Hit
3. Ox800 1 0 = Conflict misses
4. Ox800 1 8 = Hit
5. Ox300 1 0 = Conflict misses

So for 10 passes:

Compulsory misses = 3
Conflict misses = 2 × 9 = 18

C
Compulsory = 3 and conflict = 16

D
None of these

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Q. 6

Consider a Direct cache with 32 blocks and each block of size 32 bytes. The byte address 1216 of main memory will mapped to line number _____ of cache.

Solution Video | Have any Doubt ?

6

Correct Option

Solution :
6

We know that,

$$\text{Block number in main memory} = \frac{\text{Byte address}}{\text{Bytes per block}}$$

$$= \left\lfloor \frac{1216}{32} \right\rfloor = \lfloor 38 \rfloor = 38$$

Now, block number 38 will mapped to line number 38 mod 32 = 6

Your Answer is 16

QUESTION ANALYTICS

Q. 7

Consider a memory access to main memory takes 100 nsec and memory access to cache on cache hit takes 10 nsec. If 75% of processor's memory requests results in cache hit, then the average memory access time is _____ nsec.

FAQ | Solution Video | See your Answers

35

Correct Option

Solution :
35

$$\begin{aligned} T_{avg} &= H_C T_C + (1 - H_C)(T_M + T_C) \\ &= 0.75\ (10) + (1 - 0.75)(100 + 10) \\ &= 7.5 + 0.25\ (110) \\ &= 7.5 + 27.5 \\ &= 35\ \text{nsec} \end{aligned}$$

Your Answer is 32.5

QUESTION ANALYTICS

Q. 8

Consider a DRAM that must be given a refresh cycle 64 times per msec. Each refresh operation require 100 nsec and a memory cycle require 200 nsec. The percentage of the memory's total operating time must be given to refresh is _____. (Upto 2 decimal places)

Solution Video | Have any Doubt ?

0.64

Correct Option

Solution :

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$$= \frac{200 \times 10^{-9} \times 64}{10^{-3}}$$

$$= 12.8 \times 10^{-3} \text{ refreshments}$$

Total refreshment time in 200 nsec

$$= 12.8 \times 10^{-3} \times 100 \text{ nsec}$$

$$= 1.28 \text{ nsec}$$

So, percentage of memory's operating time must be

$$= \left[\frac{1.28}{200}\right] \times 100$$

$$= 0.64\%$$

QUESTION ANALYTICS

Q. 9

Consider a two level memory organization L_1 (cache) has an accessing time of 10 nsec and main memory has accessing time 100 nsec. Assume the hit ratio read operation is 0.75 and 40% references are for write operation. The average access time for system (in nsec) if it uses write through technique _____.

FAQ | Solution Video | Have any Doubt ?

59.5

Your answer is **Correct** 59.5

Solution :
59.5

$$T_{average\ (Read)} = \text{Hit\%} \times (\text{Cache Time}) + (1 - \text{Hit\%}) \times (\text{Cache} + \text{Main Memory})$$
$$= (0.75)\ (10) + (1 - 0.75)\ (10 + 100)$$
$$= 7.5 + (0.25)\ (110)$$
$$= 7.5 + 25$$
$$= 32.5 \text{ nsec}$$
$$T_{average\ (Write)} = \text{Main Memory Time}$$
$$= 100 \text{ nsec}$$
$$T_{average} = \text{Frequency}_{(Read)} \times (T_{average\ (Read)}) + \text{Frequency}_{(Write)} \times (T_{average\ (Write)})$$
$$= 0.60\ (32.5) + 0.40\ (100)$$
$$= 19.5 + 40$$
$$= 59.5 \text{ nsec}$$

QUESTION ANALYTICS

Q. 10

Consider a computer system has a main memory consisting of 1 M 16 bit words. It also has a 4 K-word cache organized in the block set associative manner, with 4 blocks per set and 64 words per block. What is the number of bits in each of the TAG, SET and word field of main memory address format?
(Consider byte adderessable memory)

Solution Video | Have any Doubt ?

A
11, 4, 6 bits

Your answer is **Wrong**

B
10, 5, 6 bits

C
10, 4, 7 bits

Correct Option

Solution :
(c)
Memory format:

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$$\begin{aligned}
\text{Word offset} &= 1 \text{ block} \\
&= 64 \text{ words} \\
&= 64 \times 16 \text{ bits} \\
&= 64 \times 2\text{B} \\
&= 128 \text{ B} \\
&= \log_2 128 \\
&= 7 \text{ bits} \\
\text{SET offset} &= \frac{2^{12}}{2^6 \times 2^2} \\
&= \frac{2^{12}}{2^8} = 2^4 = 16 \\
&= \log_2 16 \\
&= 4 \text{ bits} \\
\text{TAG} &= 21 - (7 + 4) \\
&= 31 - 11 \\
&= 10 \text{ bits}
\end{aligned}$$

D
11, 4, 7 bits

QUESTION ANALYTICS

Q. 11

Consider the following statements:
S_1 : Doubling the line size halves the number of tags in the cache.
S_2 : Doubling the associativity doubles the number of tags in the cache.
S_3 : Doubling the line size usually reduce compulsory misses.
Which of the above statements is always true?

Solution Video | Have any Doubt ?

A
Only S_1 and S_2

Your answer is **Wrong**

B
Only S_2 and S_3

Correct Option

Solution :
(b)

(i) It is not true, because doubling line size do not effect the number of tag bits in cache halves the number of lines i.e.

$$\begin{aligned}
\text{Main memory size} &= 2^{30} \text{ B} \\
\text{Cache memory size} &= 2^{20} \text{ B} \\
\text{Initially size of line} &= 256 \text{ B}
\end{aligned}$$

10	12 bits	8 bits
Tag bits	Lines	Line offset

After doubling line size = 512 B

10	11 bits	9 bits
Tag bits	Lines	Line offset

So false.

(ii) Consider

$$\begin{aligned}
\text{Main memory size} &= 2^{30} \text{ B} \\
\text{Cache memory size} &= 2^{20} \text{ B} \\
\text{Initially size of line} &= 256 \text{ B} \\
\text{Initially associativity} &= 4 \text{ way}
\end{aligned}$$

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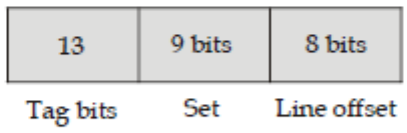
After doubling associativity i.e. 8 way



So true.

(iii) Doubling line size decrease the compulsory misses. Since during miss more items are into memory in comparison to without doubling line size. Chance of miss are less.

So true.

C

Only S_1 and S_3

D

All of the statements

QUESTION ANALYTICS

Q. 12

In a direct cache controller each main memory address can be viewed as consisting of three fields. The least significant 'w' bits identify a unique word/byte within a block. The cache logic interprets the remaining 's' bits as a tag of ($s - r$) bits (most significant portion) and a line field of 'r' bits. What is the size of main memory and cache memory respectively.

Solution Video | Have any Doubt ?

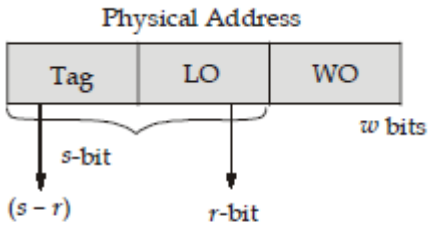
A

$2^{(s+w)}$ Bytes/words and $2^{(r+w)}$ Bytes/words

Your answer is **Correct**

Solution :

(a)



$\therefore$ Main memory size $= 2^{(s+w)}$ Bytes

Cache memory size $= 2^{(r+w)}$ Bytes

B

$2^{(s-r)}$ Bytes/words and 2^{rw} Bytes/words

C

2^{sw} Bytes/words and $2^{(s-r)}$ Bytes/words

D

2^{s} Bytes/words and $2^{(r-w)}$ Bytes/words

QUESTION ANALYTICS

Q. 13

Consider a typical disk that rotates at 3600 rotations per minute (RPM) and has a transfer rate of 100×10^6 bytes/sec. If the average seek time of the disk is twice the average rotational delay, then which of the following represents the average time (approx.) to read or write a 1024 byte sector of the disk?

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Solution :
(a)

3600 rotations → 1 minute
1 rotation → ?

$$\text{Rotational latency} = \frac{1}{3600} \times 1 \text{ minute}$$

$$= \frac{60 \text{ sec}}{3600} = 16.6 \text{ msec}$$

$$\text{(i)Average rotational latency} = \frac{1}{2} \times 16.6 \text{ msec} = 8.3 \text{ msec}$$

$$\text{(ii)} \quad \text{Average seek time} = 2 \times \text{Average rotational delay}$$
$$= 16.6 \text{ msec}$$
$$\text{Transfer rate} = 100 \times 10^6 \text{ bytes/sec}$$
$$\text{Sector size} = 1024 \text{ byte}$$

1024 byte → ?

$$\text{(iii)} \quad \text{Transfer time} = \frac{1024}{100 \times 10^6} \times 1 \text{ sec}$$
$$= 0.01024 \text{ msec}$$
$$\therefore \quad \text{Average time} = \text{Average seek time} + \text{Average rotational delay} + \text{Transfer t}$$
$$= 16.6 + 8.3 + 0.01024$$
$$= 24.91 \text{ msec}$$

B
26.62 msec

C
30.60 msec

D
None of these

Your answer is **Wrong**

QUESTION ANALYTICS

Q. 14

Consider 1 MBPS IO device interfaced to 64 bit CPU in a programmed-IO mode. Data transmission between the CPU and IO is in word-wise. Interrupt overhead is 2 μsec. What is the performance gain when the device is operating under Interrupt-IO over programmed-IO mode?

Solution Video | Have any Doubt ?

A
4

Correct Option

Solution :
(a)

Prog. IO : CPU time depends on IO speed.
i.e., 1 MB ..... 1 sec
8 B(1 word) ..... ?

$$ET_{\text{Prog IO}} = \frac{8B}{1 \text{ MB}} \text{sec} = 8 \, \mu \text{sec}$$

INT-IO : CPU time depends on interface latency.

$$ET_{\text{INT-IO}} = 2 \, \mu\text{sec}$$

$$S = \frac{ET_{\text{Prog-IO}}}{ET_{\text{INT-IO}}} = \frac{8}{2} = 4$$

B
2

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D
8

QUESTION ANALYTICS

Q. 15

Consider a two level cache system. For 100 memory references 20 misses in the first level cache and 10 misses in second level cache. Miss penalty from second level cache to main memory is 40 cycles. If the average memory access time is 7.6 cycles then the hit time of second level cache is _____ cycles. (Assume hit time of second level cache is two times of first level cache)

FAQ | Solution Video | Have any Doubt ?

5.142

Correct Option

Solution :
5.142

$$T_{avg} = \text{Hit time}_{L1} + \text{Miss rate}_{L1} \times (\text{Hit time}_{L2} + (\text{Miss rate}_{L2} \times \text{Miss penalty}_{L2}))$$

$$7.6 \text{ cycles} = x + \frac{20}{100} \times \left(2x + \left(\frac{10}{20} \times 40\right)\right)$$

$$7.6 = x + 0.2\,(2x + 20)$$
$$7.6 = 1.4x + 4$$
$$1.4x = 7.6 - 4$$
$$1.4x = 3.6$$
$$x = \frac{3.6}{1.4}$$
$$x = 2.571$$
$$\text{Hit time}_{L2} = 2x$$
$$= 2 \times 2.571$$
$$= 5.142 \text{ cycles}$$

Your Answer is 6.8

QUESTION ANALYTICS

Q. 16

Consider a system employing interrupt driven I/O for a particular device that transfer data at an average of 8 KB/sec on a continuous basis. Consider interrupt processing takes about 100 µsec i.e. time to jump to ISR, execute it and return to main program. The fraction of processor time consumed by this I/O device if interrupts occur for every byte is _____. (Upto 2 decimal places)

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0.8 (0.80 - 0.82)

Correct Option

Solution :
0.8 (0.80 - 0.82)

$$\text{Data transfer} = 8 \text{ KB/sec}$$
$$1 \text{ sec} = 8 \text{ KB}$$
$$? \text{ sec} = 1 \text{ B}$$
$$= \frac{1}{8K} \text{sec}$$
$$= 0.125 \text{ msec} = 125 \text{ µsec}$$
$$\text{Interrupt processing time} = 100 \text{ µsec}$$

So percentage of processor time consumed by I/O device

$$= \frac{100 \text{ µsec}}{} = 0.8$$

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QUESTION ANALYTICS

Q. 17

Consider a direct cache of size 64 bytes, with block size 16 bytes and main memory is divided into blocks of 16 bytes each i.e. block 0 has address 0 to 15 so on. Consider the following program that access memory in given sequence:

1. Access address 63 through 70
2. Loop (i) 15 through 32,
   (ii) 80 through 95
   Jump to Loop

If cache is organized as direct cache and loop is accessed 10 times, then the hit ratio is _____.
(Assume line 0 contain address 0, 4, 8 etc. and line 1 contain address 1, 5, 7 etc. and so on.) [Upto 2 decimal places]

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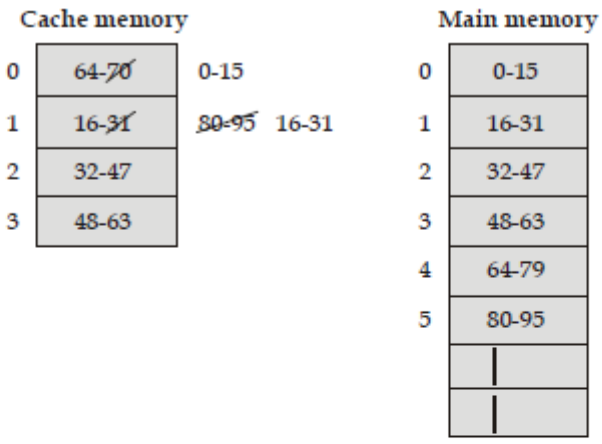
0.93 (0.93 - 0.94)

Correct Option

Solution :
0.93 (0.93 - 0.94)



Step 1: Access 63 through 70:

1. 63 address - 1 miss (16 bytes 48-63)
2. 64 address - 1 miss (16 bytes 64-79)
3. 65-70 address - 6 hits (already in memory)

First loop:

Step 2:

(i) Access 15 through 32:

1. 15 address = 1 miss (16 bytes 0-15)
2. 16 address = 1 miss (16 bytes 16-31)
3. 17-31 address = 15 hits (already in memory)
4. 32 address = 1 miss (16 bytes 32-47)

(ii) Access 80 through 95:

1. 80 address = 1 miss (16 bytes 80-95)
2. 81-95 address = 15 hit (already in memory)

Second loop:

(i) Access 15 through 32:

1. 15 address = 1 hit (already in memory)
2. 16 address = 1 miss (not in memory, 16 byte, 16-31)
3. 17-31 address = 15 hit (already in memory)
4. 32 address = 1 hit (already in memory)

(ii) Access 80 through 95:

1. 80 address = 1 miss (16 bytes 80-95)
2. 81-95 address = 15 hit (already in memory)

Repeat same for 9 times:

$$\text{Hit} = 6 + 30 + 32(9) = 36 + 288 = 324$$

$$\text{So, hit ratio} = \frac{324}{348} = 0.931$$

QUESTION ANALYTICS