CIRCUIT DIAGRAM

CONTROLLED ARRAY MULTIPLIER

GROUP-3

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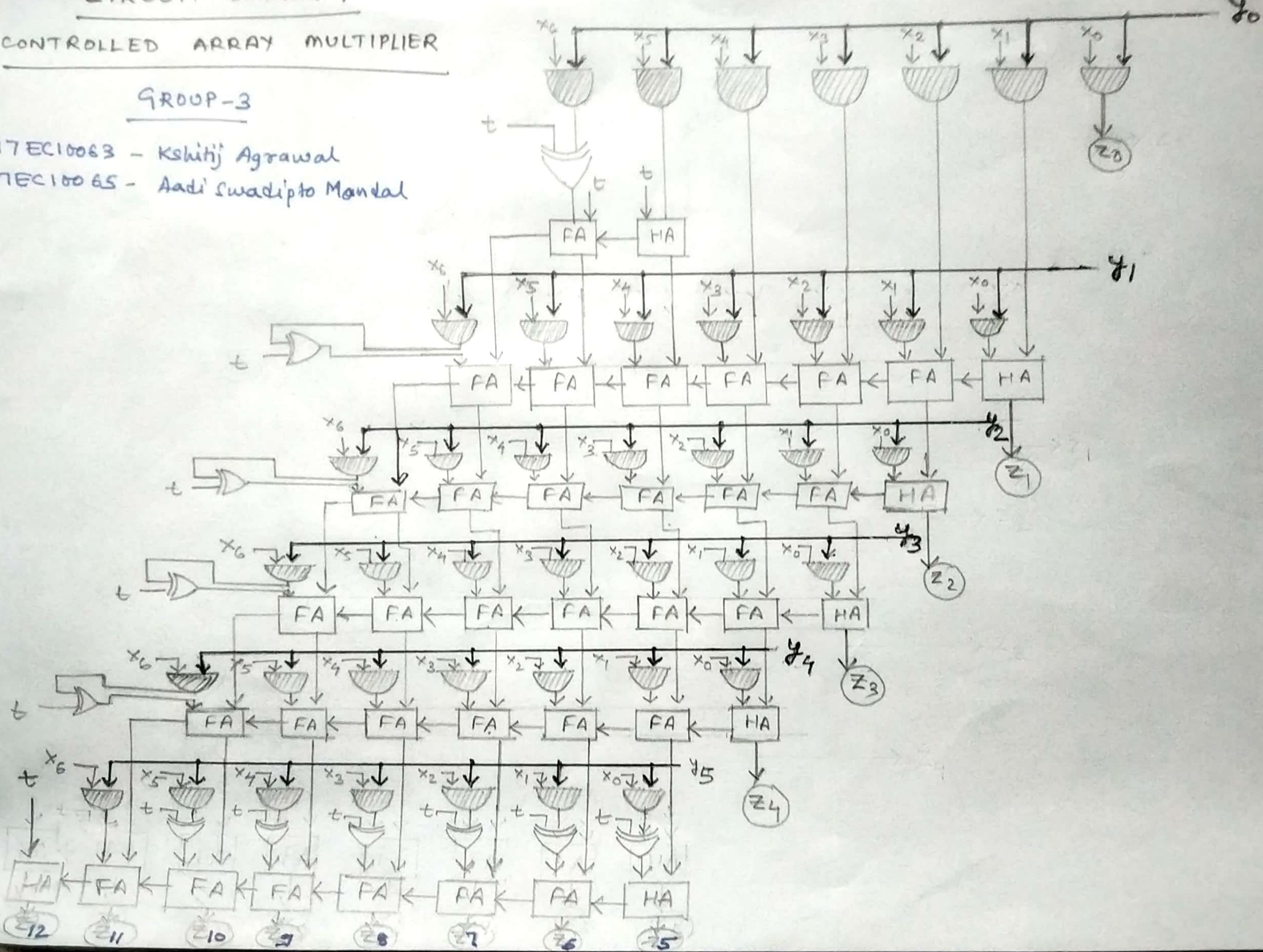


Answer these questions

① $m \times n$ multiplication with control i/p t

$\boxed{p_i^j = x_i \,\&\, y_j}$ where $x \leftarrow$ multiplicand (m-bits)
$y \leftarrow$ multiplier (n-bits)

General multiplication result looks as -

$$
\begin{array}{rlllllll}
 & \overbrace{p_{m-1}^{0} \cdots p_{m-1}^{0}}^{n} & p_{m-1}^{0} & p_{m-1}^{0} & p_{m-2}^{0} & \cdots & p_2^{0} & p_1^{0} \; p_0^{0} \\
+ & \overbrace{p_{m-1}^{1} \cdots p_{m-1}^{1}}^{n-1} & p_{m-1}^{1} & p_{m-2}^{1} & \cdots & & p_1^{1} & p_0^{1} \\
 & \vdots & & & & & & \\
+ & p_{m-1}^{n-2} \cdots p_{m-1}^{n-2} & p_{m-1}^{n-2} & \cdots & p_1^{n-2} & p_0^{n-2} & & \\
- & p_{m-1}^{n-1} & p_{m-1}^{n-1} & p_{m-2}^{n-1} & \cdots & p_0^{n-1} & &
\end{array}
\Bigg\} \; n\text{-layers}
$$

N.B. As both signed & unsigned multiplication are performed condionally the mult. structure will resemble signed multiplier [Baugh-wooley] with control i/p selecting the multiplier

If $(m \geq n)$ $(m-n+1)$ least significant bits of last layer overlap with the most significant bits of first layer.

case 1 $(m = n)$

clearly each of the $(n-1)$ layers (except the first) will require 1 HA & $(m-1)$ FA [can be 2 HA also if only unsigned multiplication is considered but the introduction of control input forces us to consider the general case]. Also the $(m+n)^{th}$ bit needs to be added to the control input, leading to one more HA.

No. of layers ↓ In each layer ↓

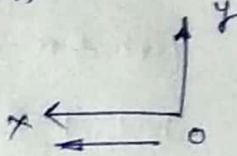
$$
\therefore \text{Total} \quad \boxed{\begin{aligned} FA &= (n-1)(m-1) \\ HA &= (n-1)+1 = n \end{aligned}}
$$

case 2 $(m > n)$

Some extra FA & HA are needed in this case to include the extra ones added to consider the compliments at each stage overall addition / subtraction of ones looks like

These ones get consumed in the full adders at resp. bits

$$\left\{\begin{array}{l} +1 \ \overline{\quad m-1 \quad} \\ +1 \ \overline{\quad m \quad} \\ \quad \vdots \\ +1 \ \overline{\quad m+n-2 \quad} \end{array}\right\} n\text{- Layers}$$



Extra ones

$$\left\{\begin{array}{l} - \quad \underbrace{1\,1\,1 \cdots 1_a}_{n\text{-ones}} \\ + \qquad\qquad\qquad 1_b \end{array}\right.$$

1_b (complementing the last layer)

As per the convention on the right side

1_b lies on index $(n-1)$ & 1_a lies on index $(m-1)$

$\because m > n \quad pos(1_a) > pos(1_b)$

$\therefore$ The overall addition looks as

$$\begin{array}{lr} - & 1\,1\,1\,1 \cdots 1_a \\ + & 1_b \end{array}$$

or

$$\underset{m+n-1}{1}\,0\,0\,0 \cdots 0_a \quad 1_a\,1_b$$

$1_{(m+n-1)}$ can be accounted for using a Half Adder as in prev. case. 1_b also similarly as it is the first bit in the sequence. Now, position ~~b (m~~ $(b+1)$ to a require additional full adders $= m - \cancel{1} - n + \cancel{1} = (m-n)$

$\therefore$ Total $\boxed{\begin{array}{l} FA = (m-1)(n-1) + \underbrace{(m-n)}_{(1_b \text{ to } 1_a)} \\ HA = (n-1) + 1 + \underbrace{1}_{(\text{Due to } 1_b)} \\ \quad\ = n+1 \end{array}}$

<u>case 3</u> $(m < n)$

This is exactly similar to case 2 just with no overlapping bits betn the first & last layer. The result remains the same

$$\boxed{\begin{array}{l} FA = (m-1)(n-1) + (n-m) \\ HA = (n-1) + 2 = n+1 \end{array}}$$

(ii) (a) Baugh Wooley Multiplier

$\tau_{pd} = (m+n-3)\tau_{FA} + 2\tau_{HA}$ { 2 HA in critical path, rest all FA }

(b) Braun's Array Multiplier

$\tau_{pd} = (m+n-4)\tau_{FA} + 2\tau_{HA}$ { critical path as mentioned in slides }

(c) Signed Magnitude Multiplier

$\tau_{pd} = (m+n-1-1+n-2)\tau_{FA} + \tau_{HA}$

$\tau_{pd} = (2n+m-4)\tau_{FA} + \tau_{HA}$

{ 1 HA in layer 1
$(m+n-1)-1$ FA in layer 1
Rest all $(n-2)$ FA in each further layers }

τ_{pd} ← Propagation delay

τ_{FA} ← Prop. delay of FA

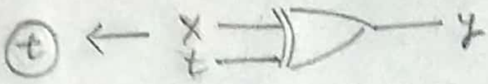
τ_{HA} ← Prop. delay of HA

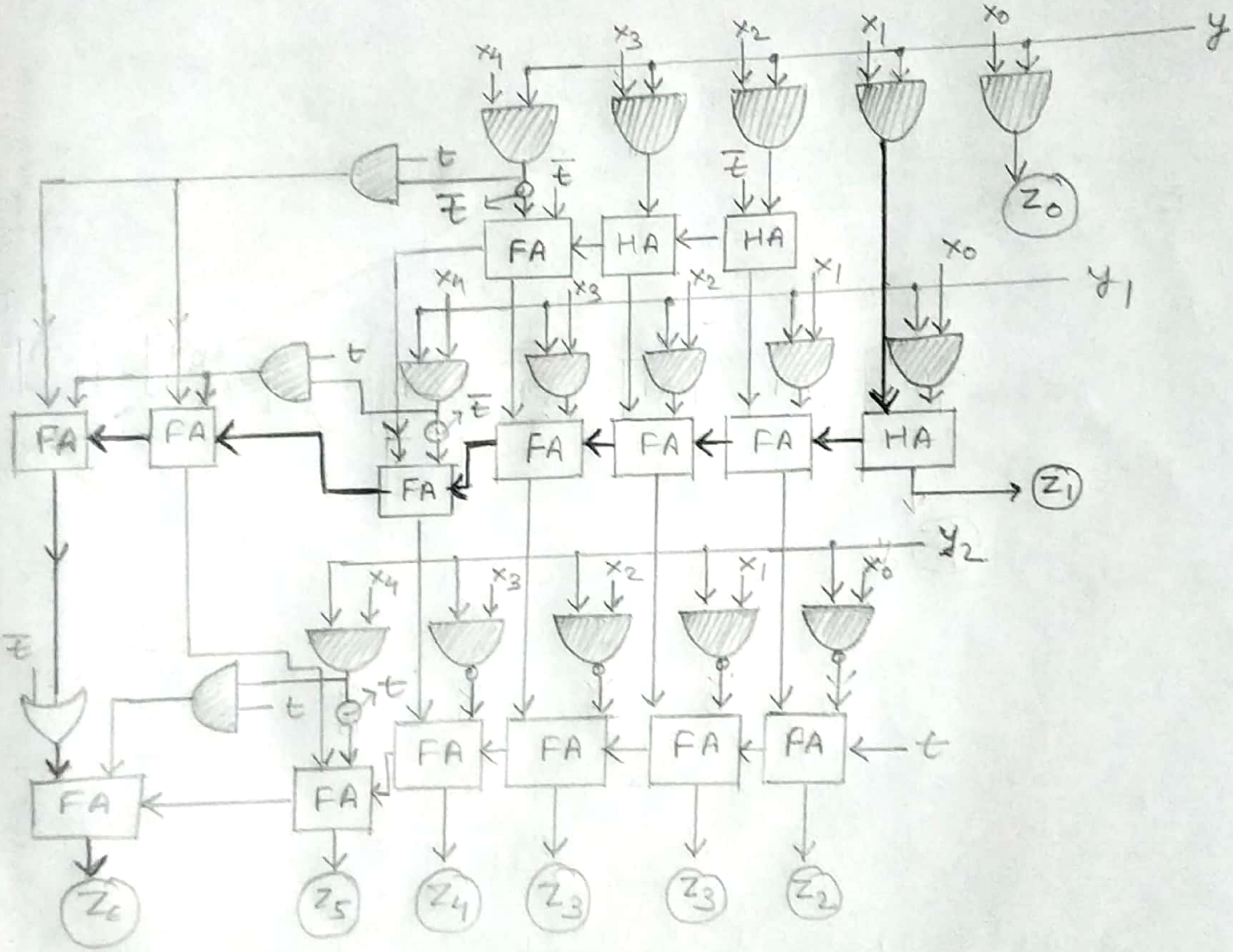
N.B. All these prop. delays are calculated considering critical path to be comprising max. carry propagation

(2) $X \leftarrow$ 5 bits (multiplicand) $t = 1 \leftarrow$ Sign-Magnitude Mul.

$Y \leftarrow$ 3 bits (multiplier) $t = 0 \leftarrow$ 2's complement Mul.

LEGEND





critical path includes the path from the start to the product bit which is generated last. In either case of $t=0$ or 1, Z_6 is the last bit produced ((considering carry prop. time as the main delay factor)

∴ The critical path will be same for both $t=0$ & 1

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