ECE 551
HW2 Extra Credit Opportunity

- Due Weds Feb 23rd Along With HW2

(but in a separate drop box)

- A lot of extra work for 10pts extra credit, but useful to see if you are coding synthesizeable verilog and to get you a jump start on synthesis.

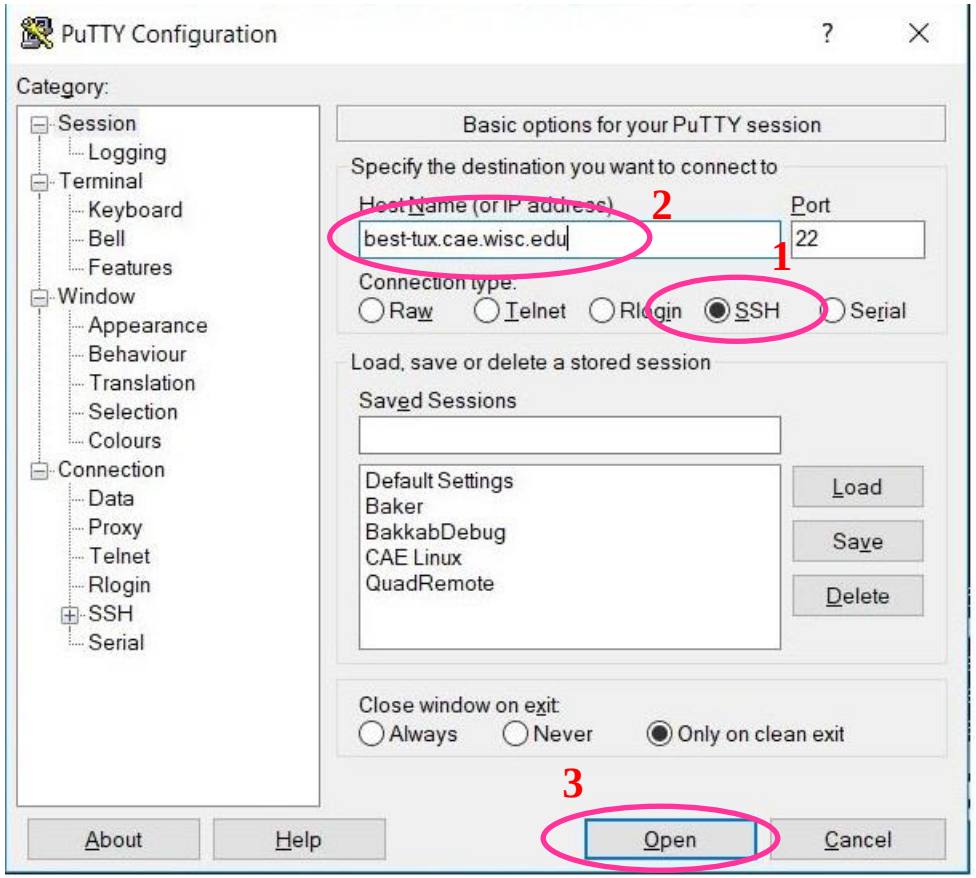
Basic Synthesis

- Around week8 in the semester we will learn synthesis proper (with proper constraints).
- For now this document will show you the basics of synthesis so you can at least read your system verilog into the tool *(dc_shell from Synopsys)* and check if it indeed synthesizes.
- **dc_shell** only works on Linux, so you must be logging into linux to perform this. We will use command line based synthesis so a GUI X-11 forwarding environment is not required *(can get by with simple xterm like Putty).*

Basic Synthesis (continued)

- Using PuTTy (installed on CAE machines) login to a Linux machine (easy as 1,2,3)

- Once logged in to Linux do an **ls**. You should see you have an **ece551** directory already (at least you should if you created on in your **I:drive** area.) Everything on your **I:drive** exists on Linux…magic!



Basic Synthesis (continued)

- Synthesis tools need to target a cell library. A cell library is a library of NANDs, NORs, ANDs, ORs and flops used to implement your digital design.

- Our cell library is a 32nm library provided by Synopsys. We must first copy a hidden file to our home linux directory that lets **dc_shell** know the location of the cell library we are targeting.

- From your linux prompt copy the file **.synopsys_dc.setup** from user ejhoffman to your home directory. ~ references your home directory in linux no matter what directory you are currently in. **NOTE:** this is a hidden file *(it begins with a* **.** *)*

```
linux_prompt> cp ~ejhoffman/.synopsys_dc.setup  ~
```

Basic Synthesis (continued)

- Since your I:drive is mapped to your linux home and vice versa file transfer is not necessary. As long as you have your verilog files in a logical spot on your I:drive they should show up in the corresponding directory under your linux home.

- If you did your work on your own machine you will have to transfer files to linux. This can be done with an ftp tool like **psftp**, or better yet with **MobaXterm**. There is a video under the tutorials section of your Canvas page called "FTPing files". Take a look at that if needed.

- Once you have your verilog files to by synthesize gathered in a logical directory on linux you would next kick off **dc_shell**.

```
linux_prompt> dc_shell
```

Basic Synthesis (continued)

- **Step 1:** Reading in verilog

```
dc_shell> read_file –format sverilog shifter.sv
```

- Did this step work? … or did it complain about something in your verilog? You may have to fix up your code if it did not like something.

- **Step 2:** Actually kicking off the synthesis

```
dc_shell> compile
```

- Since we are doing a completely unconstrained synthesis this step should not take long. It will spit a bunch of info to the **dc_shell** terminal as it goes. Take a look and see if you can figure out what it is telling you.

Basic Synthesis (continued)

- Was the compile successful? If so you are ready to output the results.

- **Step 3:** Output structural gate level netlist.

```
dc_shell> write –format verilog shifter –output
shifter.vg
```

- The output of synthesis is a gate level verilog netlist. **NOTE** the **.vg** extension (verilog gates). Take a look at this file it writes out. It is simply a listing of all the required gates and their interconnetions needed to implement your design using the SAED32 (Synopsys 32nm) cell library.

- Careful to not do something stupid and –output to shifter.sv and thus overwrite your source verilog.

Basic Synthesis (continued)

- Finally, I want to see the area of your design.
- **Step 4:** Generate area report

```
dc_shell> report_area > shifter_area.txt
```

- This will output a report of the number of gates and their corresponding area in square microns. Any report echoed to the terminal screen of dc_shell can also be directed to a file by using **>**
- Turn in **shifter.vg**, **shifter_area.vg** to the **separate** dropbox for extra credit.
- Then do it all again for **desiredDrive.sv** and submit **desiredDrive.vg** and **desiredDrive_area.txt**