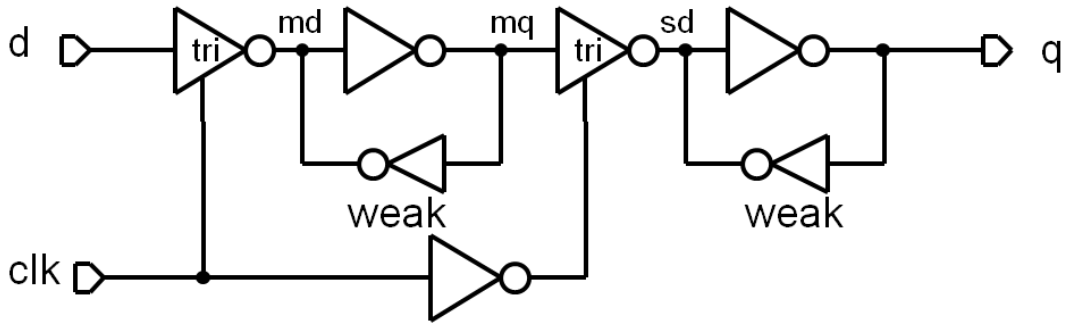
# ECE 551
# Exercise03

## This is the last problem of HW1

**Submit whatever you have for both the DUT and the testbench to the dropbox by end of class time.**




a) Code this circuit structurally in Verilog (in Modelsim environment)(attach the Verilog code for this module)(**Note:** tri-state gates might need a 1 time unit delay modeled for proper simulation, an inverting tri-state is verilog primitive **notif1**).

b) b) Create a testbench, instantiate and simulate this circuit. Attach a print out of the waveforms, and the Verilog of the test bench

c) c) Add an active **low asynchronous** reset input to this circuit. Please print this drawing and write over the top of it showing how you would add a reset. Take a picture and submit the picture. Code this new circuit in Verilog and update your test bench to test the new input. Again attach Verilog and waveforms

d) Was the cost of adding the asynch reset high, medium, or low? Think in terms of number of transistors.