Exercise 6 (Shifter/Rotator (HW2 Prob1)):

- Using Dataflow/RTL Verilog, implement a shifter capable of performing both arithmetic and logical right shifts on a 16-bit input (**src[15:0]**). The shift/rotate amount can be anywhere from 0 to 15-bits, and is specified by a 4-bit input (**amt[3:0]**). The result goes to a signal called **res[15:0]**. You are **not** allowed to use the >> or >>> operator. Write a testbench to verify its operation. This testbench does not need to be self checking, stimulus generation only (Please ensure reasonably comprehensive coverage with stimulus. i.e. cover multiple 16-bit quantities for both arithmetic and logical and for multiple shift amounts).

Signal Name:	Dir:	Description:
src[15:0]	in	Input vector to be left shifted
ars	in	If asserted then operation is arithmetic
amt[3:0]	in	Specifies the amount of the shift 0 to 15 bits
res[15:0]	out	Result of the shift

Submit as much as you completed to the dropbox. You have to finish this as part of HW2

Exercise 6 (Hints on building a shifter):

This topology is referred to as a logarithmic shifter.

This is showing a left shift, it should be trivial to convert this to right instead. It is a bit trickier to think of how to make it perform arithmetic or logical, but think about another set of muxes at each level that do something a bit different with the MSB(s).