ELEN 115L Lab 7: MOSFET Characteristics

Nicky Castillo and Christian Garcia
Thursday 2:15-5:00pm
5/27/21

Objective

In Part 1 of this lab we will examine the i-v curves for MOSFETs. From these i-v curves we will be able to learn about the three different modes that these devices can be in; cutoff, saturation, and liner. We also will see how different voltages affect this device. In Part 2 of the lab we will see how MOSFETs will create CMOS Logic Gates. We will use different combinations of PMOS and NMOS MOSFETS in order to create NOT, NAND, and NOR gates. We will see how these circuits behave in similar ways to their logic gate counterparts. We will see how they produce the same truth tables to the NOT, NAND, and NOR logic equivalents.

Part 1: MOS i-v Characteristics

The first step is to create a simple circuit with a voltage source connecting the gate to the source and another source connecting the drain to the source, as shown in Figure 1 below.

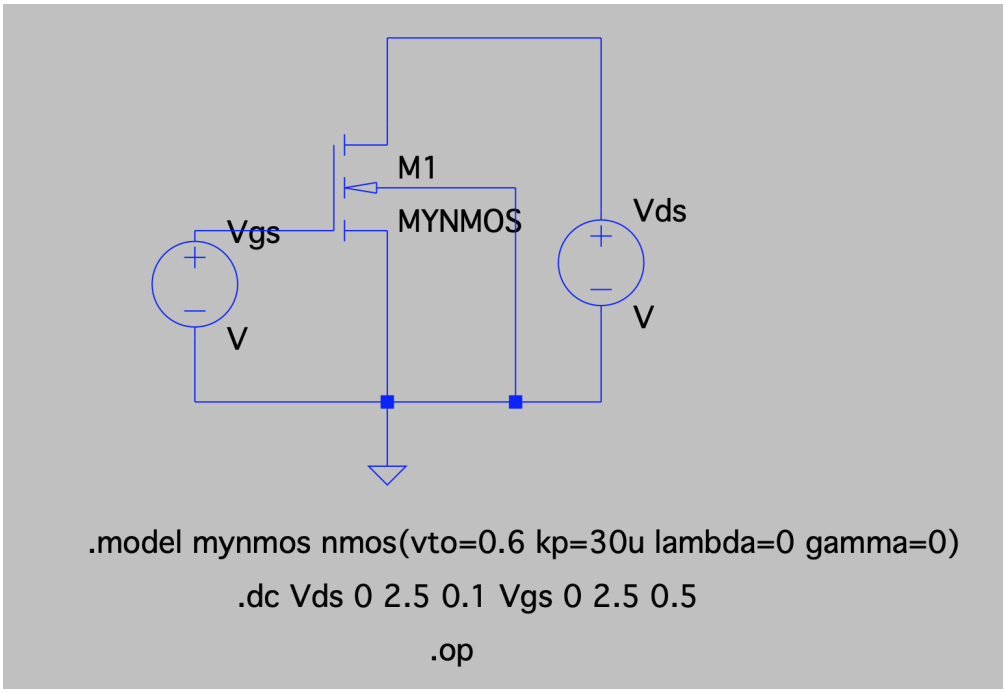


Figure 1: Circuit used to test NMOS

Next, define the MOSFET with the values shown in Figure 1 for V_T, K_P, lambda, and gamma. Also, use a nested sweep for V_{GS} and V_{DS}, ranging them from 0V to 2.5V in steps of 0.5V. Finally, run the simulation and examine the results, noting where the cutoff, linear, and saturation modes are on the plot.

After running through the lab procedure, our team achieved the resultant plot in Figure 2. Note that the different modes of operation are annotated on the plot.

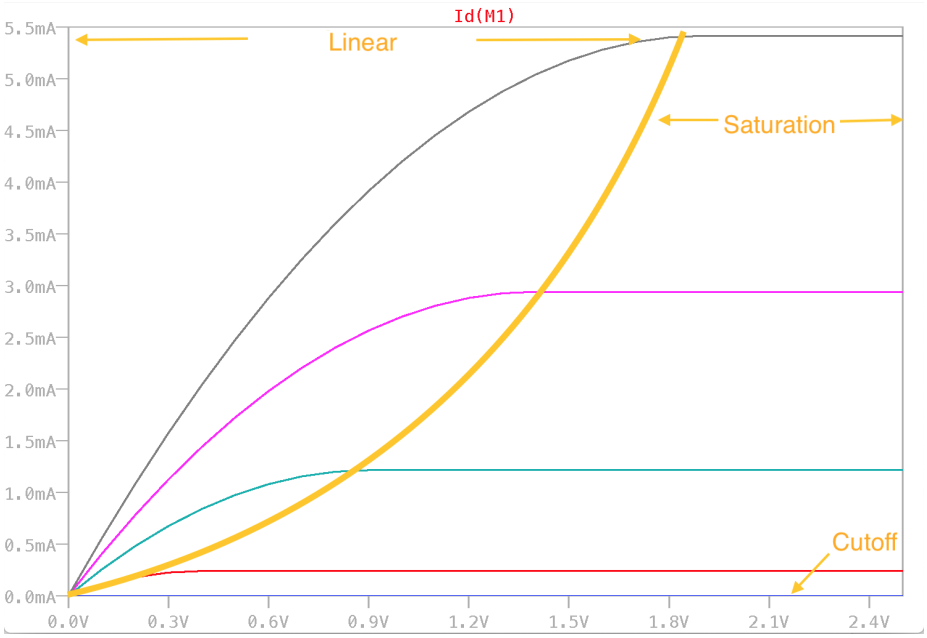


Figure 2: Plot of I_D versus V_{DS} with modes of operation annotated

Part 2: CMOS Logic Gates

A. NOT Gate

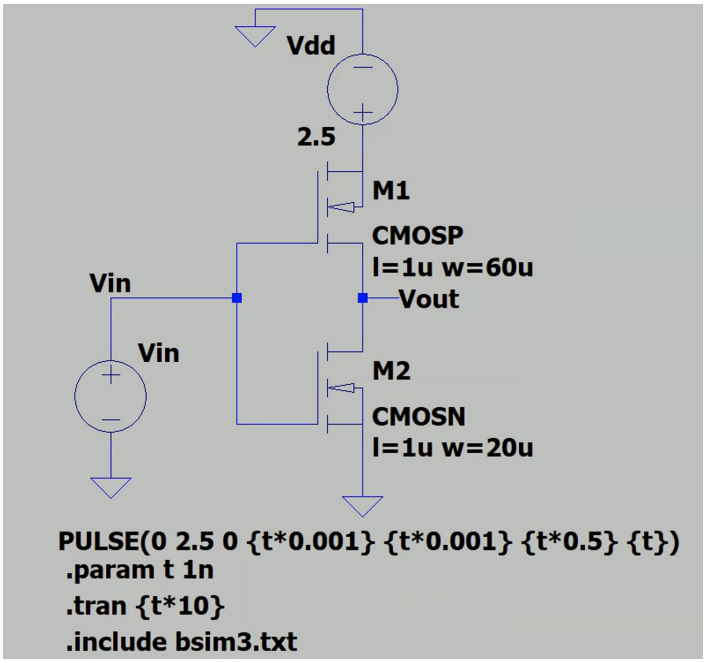
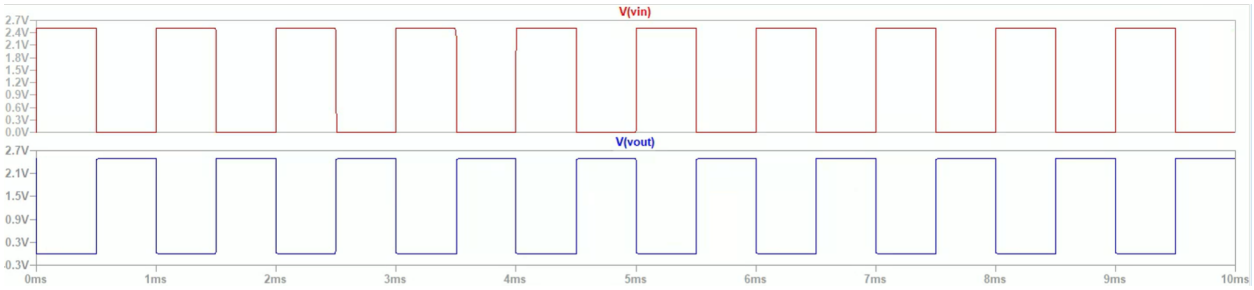
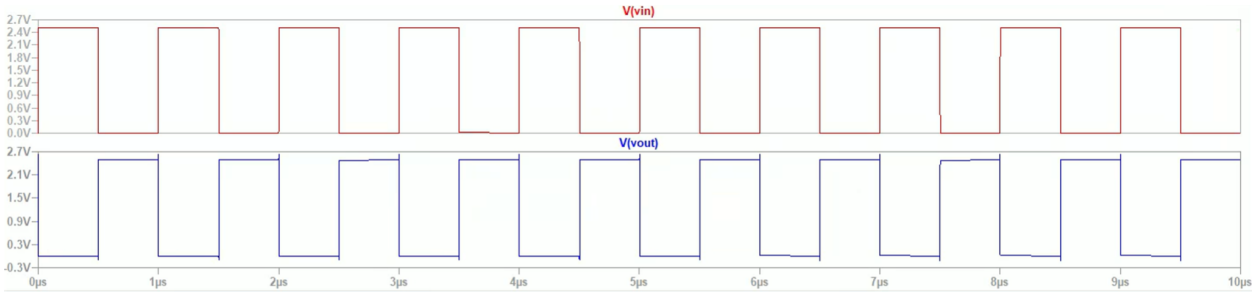


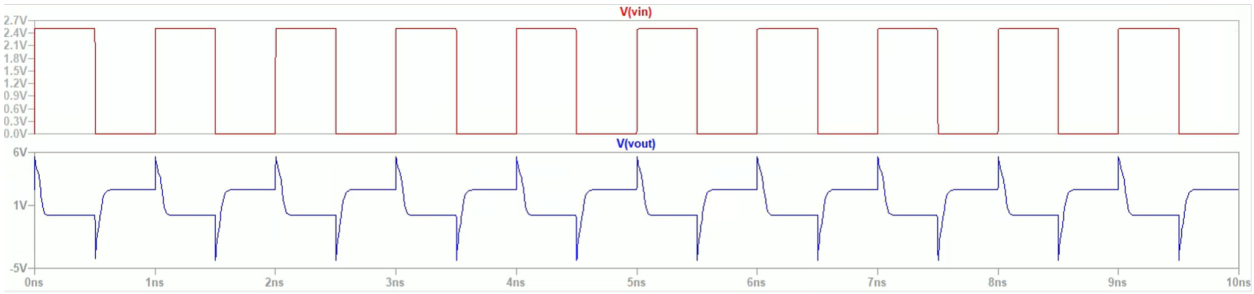
Figure 3: Image of a logic inverter (NOT gate)



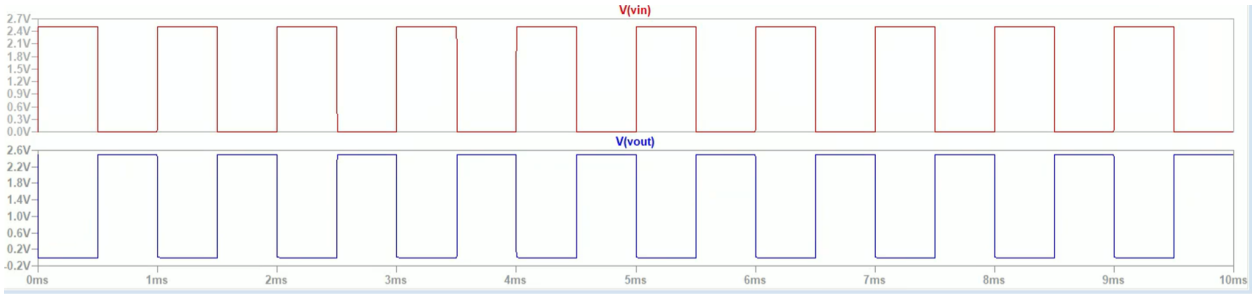
Graph 1: NOT Gate at Time 1ms with Length 1um



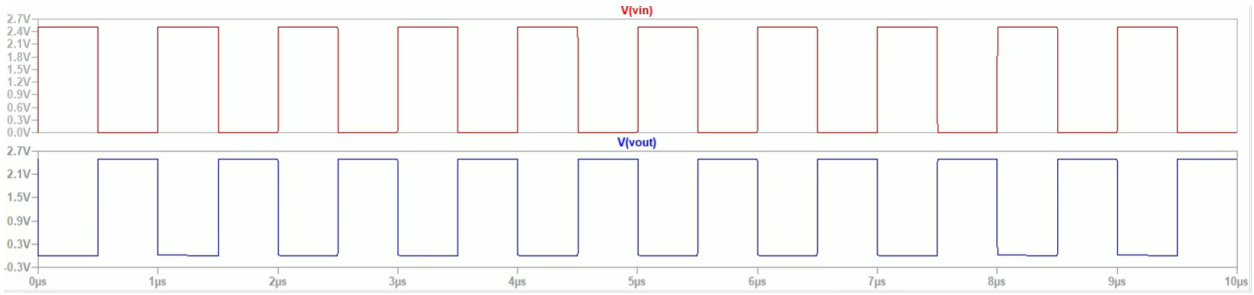
Graph 2: NOT Gate at Time 1us with Length 1um



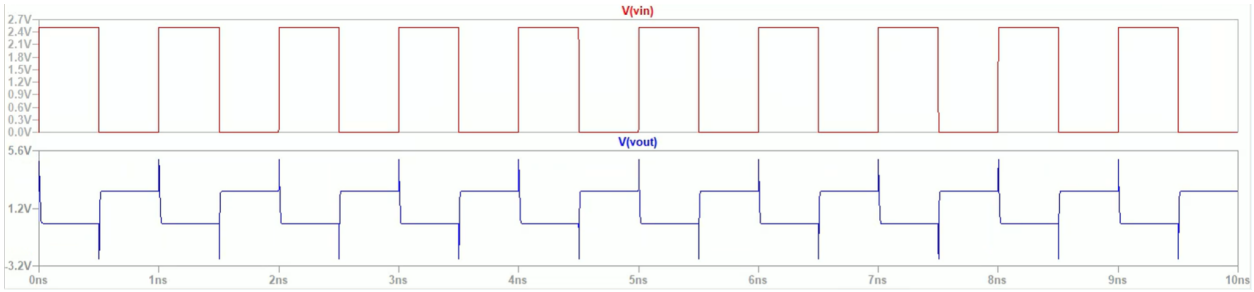
Graph 3: NOT Gate at Time 1ns with Length 1um



Graph 4: NOT Gate at Time 1ms with Length 0.25um



Graph 5: NOT Gate at Time 1us with Length 0.25um



Graph 4: NOT Gate at Time 1us with Length 0.25um

Figure 4: Resulting plots for Part 2

Table 1: Truth table of NOT gate

Vin	Vout
1	0
0	1

This MOSFET circuit is inverting our input. So when the input is increasing the output is decreasing and vice versa, when the input is decreasing the output is increasing. At the input's maximum the output is at its minimum and when the input is at its minimum the output is at its maximum.

We can see that as we change our speed from 1ms to 1us to 1ns the end of our output becomes gradually more distorted with the value being a lot larger than the original 2.5V. This is because it has a difficult time switching at high speeds. The graph is expected to be the opposite of our input but as we can see from the bottom graph of our output where it is switching at 1ns it has a hard time handling the high speeds.

When we changed the length from 1us to 0.25us we saw how it did slightly better at handling high speeds but still wasn't great. From this we observed that the smaller the size of the device the better it was at handling high speeds.

B. NAND Gate

Create the NAND gate as shown in Figure 5, using a V_{DD} of 2.5V.

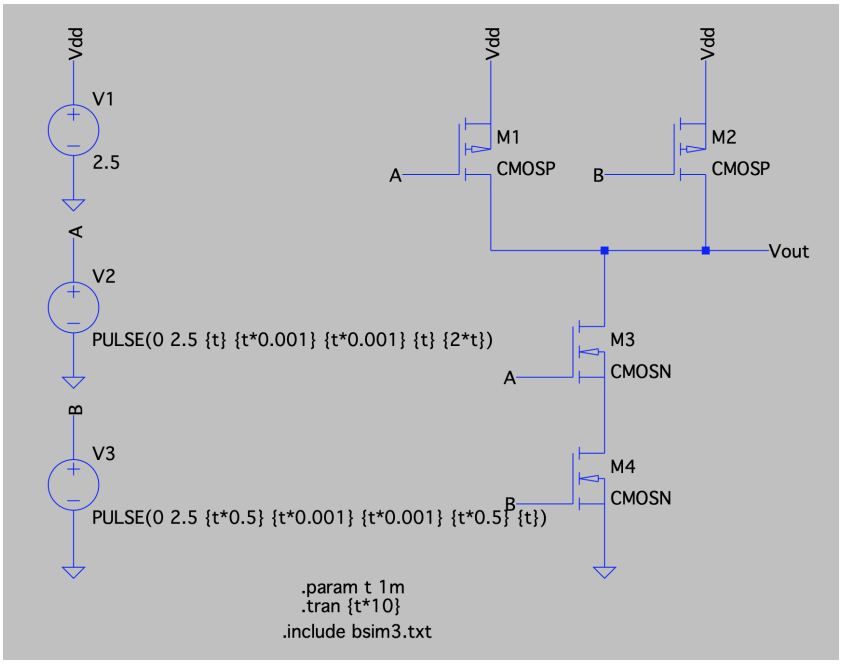


Figure 5: NAND MOSFET logic gate circuit

Make the voltage sources pulses sources switching from 0V to 2.5V, and make them run through an ascending binary order. Run a transient analysis and observe the resulting plot of both the input voltages and the output voltage. Create a truth table of the results and discuss the operation of the gate.

Our team found the following plot of A, B, and V_{OUT} with respect to time shown in Figure 6.

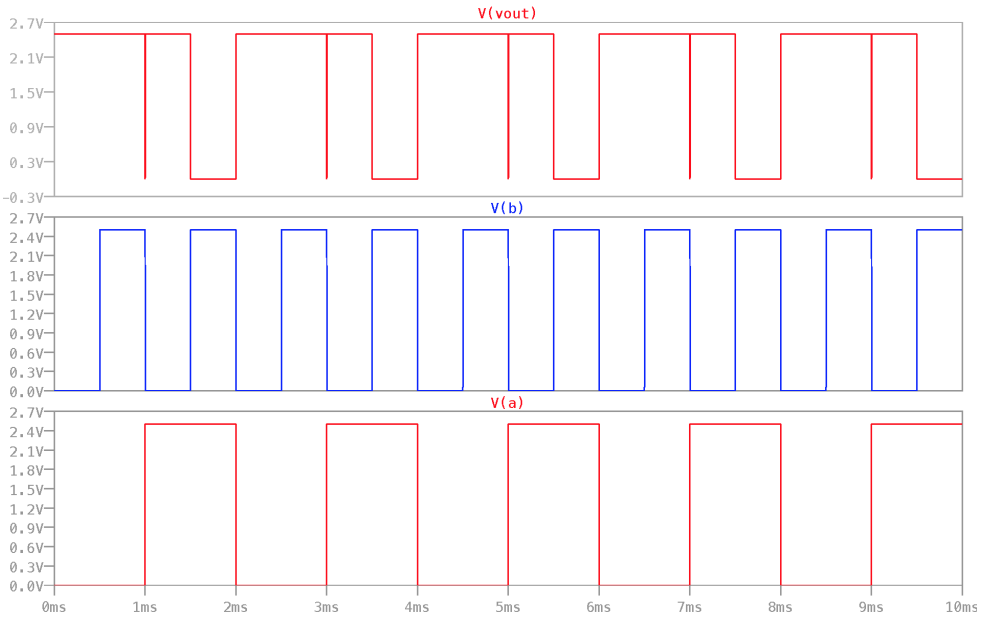


Figure 6: Plot of inputs A and B and the output voltage with respect to time for NAND gate

The plot from Figure 6 was then translated into a truth table. Table 2 is the truth table of the NAND gate.

Table 2: Truth table of NAND Gate

A	B	Vout
0	0	1
1	0	1
0	1	1
1	1	0

C. NOR Gate

Create the NOR gate as shown in Figure 7, using a V_{DD} of 1.8V.

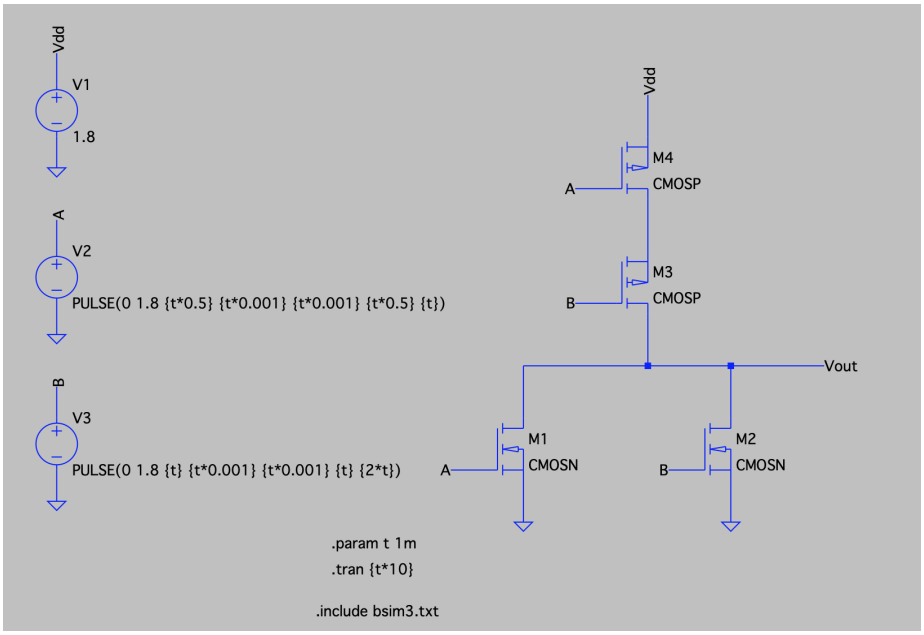


Figure 7: NOR MOSFET logic gate circuit

Make the voltage sources pulses sources switching from 0V to 1.8V, and make them run through an ascending binary order. Run a transient analysis and observe the resulting plot of both the input voltages and the output voltage. Create a truth table of the results and discuss the operation of the gate.

Our team found the following plot of A, B, and V_{OUT} with respect to time shown in Figure 8.

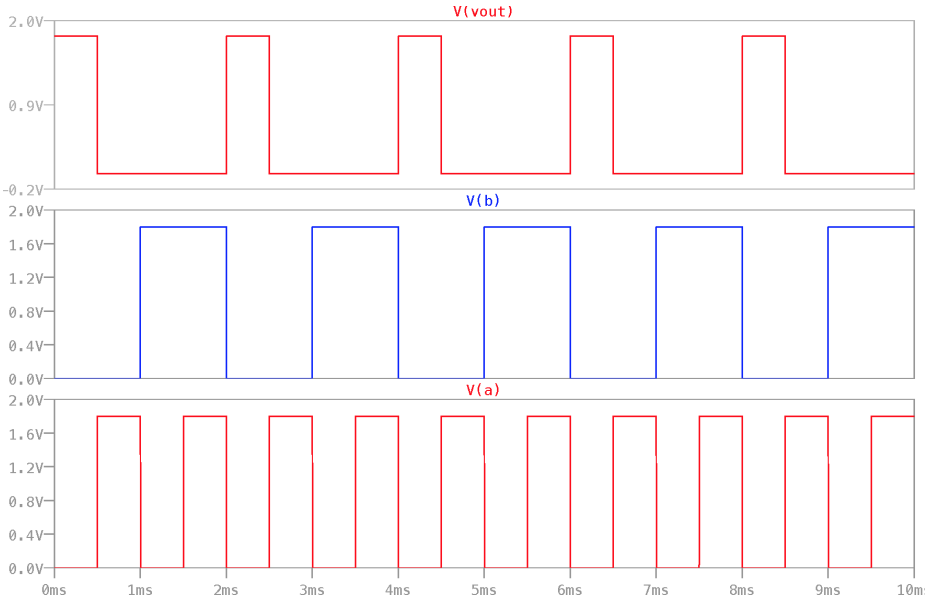


Figure 8: Plot of inputs A and B and the output voltage with respect to time for NOR gate

The plot from Figure 8 was then translated into a truth table. Table 3 is the truth table of the NOR gate.

Table 3: Truth table of NOR Gate

A	B	Vout
0	0	1
1	0	1
0	1	1
1	1	0

Conclusion

In this lab we examined the different characteristics of MOSFETs. We saw how it behaved in the cutoff, saturation, and linear regions. From there we created NOT, NAND, and NOR gates. We saw how they gave us the same outputs as their logical equivalents, we then put this data in a truth table. With the NOT gate we saw how the device struggled to handle high switching speeds. Although it was able to handle higher switching speeds with a smaller length, which

helped us create the relationship between length and switching speed. For the NAND and the NOR gate we saw how both the PMOS and NMOS gates affected the output.