Lab 5

Register maps:

10.2.3 SYSCFG external interrupt configuration register 1 (SYSCFG_EXTICR1)

Address offset: 0x08 Reset value: 0x0000 0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
/	15	14	13	12	11	10	9	8	7	6	5	4	_ 3	2	1	0
	Res	EXTI3[2:0] Res		Res	EXTI2[2:0]			Res	EXTI1[2:0]			Res	EXTI0[2:0]			
		rw	rw	rw		rw	rw	rw		rw	rw	rw		nw	rw	rw
1										/						

Bits 31:15 Reserved, must be kept at reset value.

Bits 14:12 EXTI3[2:0]: EXTI 3 configuration bits

These bits are written by software to select the source input for the EXTI3 external interrupt.

000: PA[3] pin 001: PB[3] pin

010: PC[3] pin

011: PD[3] pin

100: PE[3] pin 101: PF[3] pin

110: PG[3] pin 111: Reserved

Bit 11 Reserved, must be kept at reset value.

Problem 1:

Main:

INCLUDE core cm4 constants.s ; Load Constant Definitions

INCLUDE stm32l476xx constants.s

INCLUDE jstick.h

INCLUDE leds.h

AREA main, CODE, READONLY

EXPORT main

ENTRY

mainPROC

r0,=RCC_AHB2ENR_GPIOBEN ldr

bl portclock en

r0,=RCC AHB2ENR GPIOEEN ldr

bl portclock en

```
ldr
                         r0,=GPIOB BASE
                         r1,=GPIO MODER MODER2 0
            ldr
            bl
                         port bit pushpull
            ldr
                         r0,=GPIOE BASE
            ldr
                         r1,=GPIO_MODER_MODER8_0
            bl
                         port_bit_pushpull
            bl
                         porta_init
                         exti3 init
            bl
            bl
                          exti0 init
endlessb
                   endless
            ENDP
EXTI3 IRQHandler PROC
            EXPORT
                         EXTI3 IRQHandler
            push
                   \{lr\}
            bl
                         red tog
                          \{lr\}
            pop
            ldr
                         r2,=(EXTI BASE+EXTI PR1)
                         r1,#EXTI PR1 PIF3
            mov
            str
                         r1,[r2]
            dsb
            bx
                         lr
            ENDP
EXTI0 IRQHandler PROC
            EXPORT
                         EXTI0 IRQHandler
            push
                   \{lr\}
            bl
                          green_tog
            pop
                   \{lr\}
            ldr
                   r2,=(EXTI_BASE+EXTI_PR1)
                         r1,#EXTI_PR1_PIF0
            mov
                   r1, [r2]
            str
            dsb
                         lr
            bx
            ENDP
```

ALIGN

AREA myData, DATA, READWRITE

ALIGN

END

Jstick.s

exti0_init	PROC	
	EXPORT	exti0_init
	ldr	r2,=(RCC_BASE+RCC_APB2ENR)
	ldr	r1,[r2]
	orr	r1,#RCC_APB2ENR_SYSCFGEN
	str	r1,[r2]
	ldr	r2,=(SYSCFG_BASE+SYSCFG_EXTICR0)
	ldr	r1,[r2]
	bic	r1,#0x00000007
	str	r1,[r2]
	ldr	r2,=(EXTI_BASE+EXTI_RTSR1)
	ldr	r1,[r2]
	orr	r1,#EXTI_RTSR1_RT0
	str	r1,[r2]
	ldr	r2,=(EXTI_BASE+EXTI_FTSR1)
	ldr	r1,[r2]
	bic	r1,#EXTI_FTSR1_FT0
	str	r1,[r2]
	ldr	r2,=(EXTI BASE+EXTI IMR1)

```
r1,[r2]
      ldr
                  r1,#EXTI_IMR1_IM0
      orr
                  r1,[r2]
      str
                  r2,=(NVIC BASE+NVIC ISER0)
      ldr
                  r1,=(1<<6)
      ldr
                  r1,[r2]
      str
                  lr
      bx
      ENDP
      ALIGN
      END
      IMPORT porta init
      IMPORT
                  read_jstick
                  exti3 init
      IMPORT
                  exti0 init
      IMPORT
      END
INCLUDE core cm4 constants.s
INCLUDE stm32l476xx constants.s
INCLUDE jstick.h
INCLUDE leds.h
            AREA main, CODE, READONLY
                        __main
            EXPORT
            ENTRY
```

mainPROC

Jstick.h

Problem 2:

Main:

ldr bl ldr bl	r0,=RCC_AHB2ENR_GPIOBEN portclock_en r0,=RCC_AHB2ENR_GPIOEEN portclock_en
ldr	r0,=GPIOB_BASE
ldr	r1,=GPIO_MODER_MODER2_0
bl	port bit pushpull

```
ldr
                          r0,=GPIOE BASE
             ldr
                          r1,=GPIO_MODER_MODER8_0
             bl
                          port bit pushpull
             bl
                          porta init
             bl
                          exti3_init
                          exti5_init
             bl
endlessb
                   endless
             ENDP
EXTI3 IRQHandler PROC
             EXPORT
                          EXTI3 IRQHandler
             push
                   \{lr\}
             bl
                          red_tog
                          \{lr\}
             pop
             ldr
                          r2,=(EXTI BASE+EXTI PR1)
                          r1,#EXTI_PR1_PIF3
             mov
             str
                          r1,[r2]
             dsb
                          lr
             bx
             ENDP
EXTI9 5 IRQHandler PROC
             EXPORT
                          EXTI9 5 IRQHandler
                          r3,=(EXTI_BASE+EXTI_PR1)
             ldr
             ldr
                          r4, [r3]
                          r4, #EXTI PR1 PIF5
             tst
                   return
             beq
             push
                   \{lr\}
             bl
                          green tog
                   \{lr\}
             pop
             ldr
                   r2,=(EXTI_BASE+EXTI_PR1)
                          r1,#EXTI_PR1_PIF5
             mov
                   r1, [r2]
             str
             dsb
return bx
                   lr
             ENDP
```

ALIGN

AREA myData, DATA, READWRITE

ALIGN

END

Jstick.s:

exti5_init	PROC	
	EXPORT	exti5_init
	ldr	r2,=(RCC_BASE+RCC_APB2ENR)
	ldr	r1,[r2]
	orr	r1,#RCC_APB2ENR_SYSCFGEN
	str	r1,[r2]
	ldr	r2,=(SYSCFG_BASE+SYSCFG_EXTICR0)
	ldr	r1,[r2]
	bic	r1,#0x00000070
	str	r1,[r2]
	ldr	r2,=(EXTI_BASE+EXTI_RTSR1)
	ldr	r1,[r2]
	orr	r1,#EXTI_RTSR1_RT5
	str	r1,[r2]
	ldr	r2,=(EXTI_BASE+EXTI_FTSR1)
	ldr	r1,[r2]
	bic	r1,#EXTI_FTSR1_FT5
	str	r1,[r2]
	ldr	r2,=(EXTI_BASE+EXTI_IMR1)

ldr r1,[r2]

orr r1,#EXTI_IMR1_IM5

str r1,[r2]

ldr r2,=(NVIC_BASE+NVIC_ISER0)

ldr r1,=(1<<23)

str r1,[r2] bx lr

ENDP

Jstick.h:

IMPORT porta_init

IMPORT read_jstick IMPORT exti3_init IMPORT exti5_init

END

Problem 3:

tim2 init PROC ;initialize Timer 2 for this program and setup its interrupt

EXPORT tim2 init

ldr r2,=(RCC BASE+RCC APB1ENR1) ;enable timer 2

clock

ldr r1,[r2]

orr r1,#RCC APB1ENR1 TIM2EN

r1,[r2]

ldr r2,=(TIM2_BASE+TIM_PSC) ;Setup the prescaler.

Assuming a 4MHz clock, this gives 1ms timer ticks

ldr r1,=39 str r1,[r2]

ldr r2,=(TIM2 BASE+TIM ARR) ;Setup the reload.

Assuming a 1ms tick, this gives 1s overflows

ldr r1,=49 str r1,[r2] ldr r2,=(TIM2_BASE+TIM_CR1) ;enable the counter in

control register 1

ldr r1,[r2]

orr r1,#TIM_CR1_CEN

str r1,[r2]

ldr r2,=(TIM2_BASE+TIM_DIER) ;enable the timer

update interrupt

ldr r1,[r2]

orr r1,#TIM_DIER_UIE

str r1,[r2]

ldr r2,=(NVIC_BASE+NVIC_ISER0) ;enable the TIM2 interrupt in

NVIC_ISER0

1dr r1,=(1<<28)

 $\begin{array}{ccc} str & & r1,[r2] \\ bx & & lr \end{array}$

ENDP ALIGN

END

