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ELEN 120 Lab

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## Lab 2: Conditional Execution and Loops

### Problem 1:

1. This code subtracts the value 1 from the value in R6 and puts this new value into R6. It also sets any necessary condition flags.
2. The statements are executed 10 times.
3. The statements are executed 4 times.
4. The result is 0xFFFFFFFF.
5. The result is 0xFFFFFFFF.

### Problem 2:

```

10
11
12         AREA      main, CODE, READONLY
13         EXPORT    __main
14         ENTRY
15
16         __main    PROC
17
18         ;*****
19         LDR        r0, =Array
20         MOV        r1, #0xC
21         MOV        r5, #1
22 loop      ADD        r0, r0, #4
23         LDR        r3, [r0]
24         ADD        r3, r3, #5
25         STR        r3, [r0]
26         ADD        r5, r5, #1
27         CMP        r5, #7
28         BLT        loop
29
30 endless   B         endless
31         ;*****
32
33         ENDP
34
35         ALIGN
36
37         ;*****
38 Array DCD      23, 45, 18, -1, 27, 22, 36, 2, -73, -15, 63, -19
39         ;*****
40
41         END
42
43

```

[illegible][illegible]

### Problem 3:

The screenshot displays the Keil uVision IDE's Disassembly window. On the left, the Register window shows the state of Core registers (R0-R15, xPSR) and System/Internal registers. The main window shows the disassembly of the startup\_cm4.s file, specifically the \_main function. The assembly code includes instructions like CMP, BLT, B, DCW, and LDR, along with comments and labels like loop, endless, and END.

[illegible]

## Problem 4:

Registers

Register	Value
<b>Core</b>	
R0	0x000001C9
R1	0x00001120
R2	0x000001E4
R3	0x000001E8
R4	0x000001EC
R5	0x00003247
R6	0x00005431
R7	0x00001120
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x10001500
R14 (LR)	0xFFFFFFFF
R15 (PC)	0x000001E2
xPSR	0x21000000
<b>Banked</b>	
<b>System</b>	
<b>Internal</b>	
Mode	Thread
Privilege	Privileged
Stack	MSP
States	102
Sec	0.00000850

Disassembly

0x000001DE	BF28	IT	CS
0x000001E0	4639	MOVCS	r1, r7
0x000001E2	E7FE	B	0x000001E2
0x000001E4	3247	DCW	0x3247
0x000001E6	0000	DCW	0x0000
0x000001E8	5431	DCW	0x5431
0x000001EA	0000	DCW	0x0000

startup\_cm4.s

mainproto.s

13	EXPORT	__main
14	ENTRY	
15		
16	__main	PROC
17		
18	; *****	
19	LDR	r2, =num1
20	LDR	r3, =num2
21	LDR	r4, =num3
22	LDR	r5, [r2]
23	LDR	r6, [r3]
24	LDR	r7, [r4]
25	CMP	r5, r6
26	MOVLO	r1, r5
27	MOVHS	r1, r6
28	CMP	r1, r7
29	MOVHS	r1, r7
30		
31	endless	B endless
32	; *****	
33		
34		
35	ENDP	
36		
37	ALIGN	
38		
39	; *****	
40	num1	DCD 0x03247
41	num2	DCD 0x05431
42	num3	DCD 0x01120
43	; *****	
44		
45	END	
46		

### Problem 5:

```

12          AREA      main, CODE, READONLY
13          EXPORT   __main
14          ENTRY    __main
15
16  __main  PROC
17
18  ; *****
19          ldr        r0,=numElements
20          ldr        r1,=sequence
21          MOV        r2, #1
22          ldr        r0, [r0]
23  loop    ldr        r3, [r1]
24          ldr        r4, [r1, #4]!
25          add        r5, r3, r4
26          str        r5, [r1, #4]
27          sub        r0, r0, #1
28          cmp        r0, #0
29          bne        loop
30
31  endless  B          endless
32  ; *****
33
34          ENDP
35
36          ALIGN
37
38  ; *****
39
40  numElements  DCD      10
41  sequence     DCD      0,1,0,0,0,0,0,0,0,0
42  ; *****
43
44          END
45

```

[illegible]