Laboratory 8: Buck Converter Open Loop Characteristics

ELEN: 164L

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Fall Quarter

Performed and analyzed by Christian Garcia and Jake Taylor

Materials Supplied by Santa Clara University

Part 2: Open-Loop Characteristics

100mOhm:

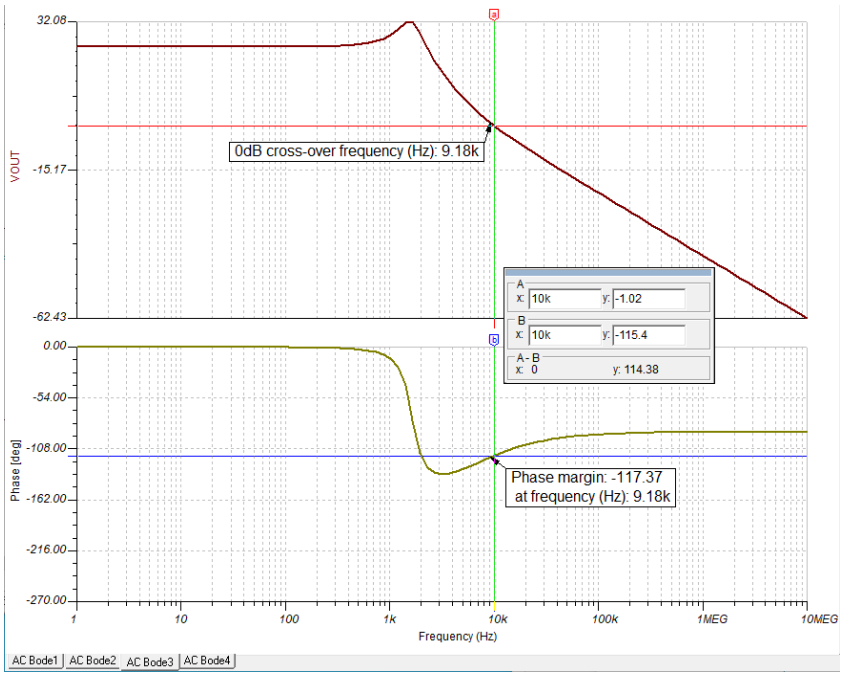

Figure 1: Magnitude and Phase with 100mOhm ESR

Cutoff Frequency: -1.02dB at 10kHz

Crossover Frequency: 9.18kHz

Magnitude: 0dB

Phase: -117.37°

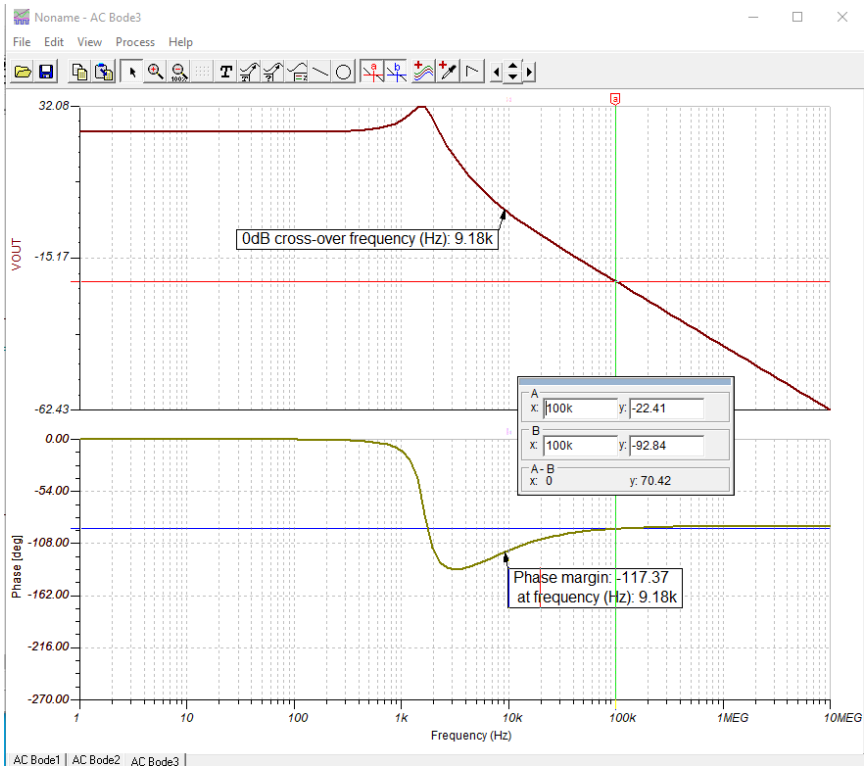

Figure 2:Magnitude and Phase at Switching Frequency

Gain at 100kHz: -22.41dB

Phase Margin: -117.37°

From the phase margin, we can see that this system is overdamped. We know that overdamped systems are slightly unstable so it may be unstable.

10mOhm:

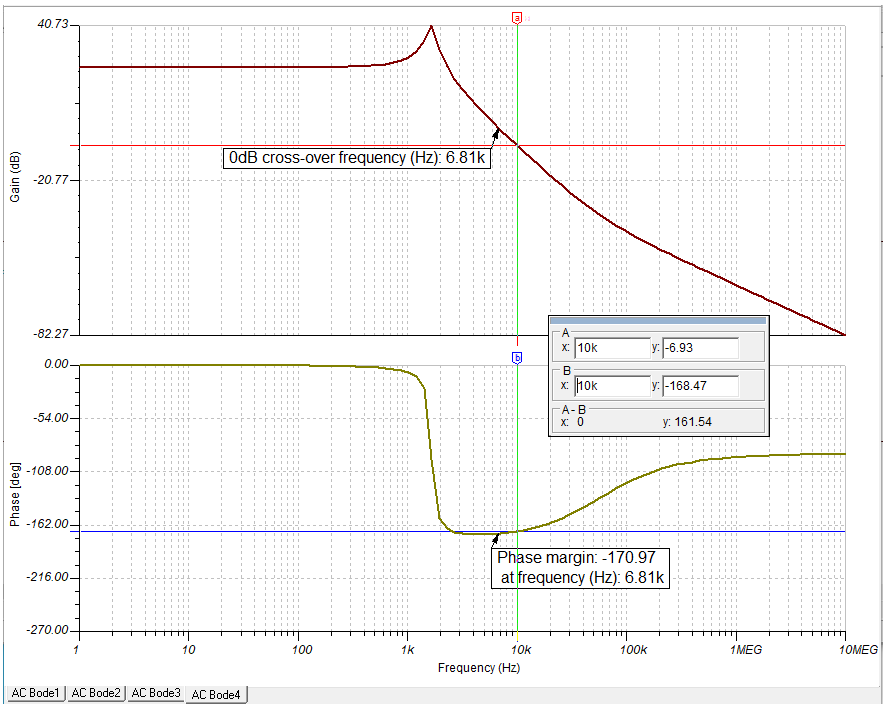

Figure 3: Magnitude and Phase with 100mOhm ESR

Cutoff Frequency: -1.02dB at 10kHz

Crossover Frequency: 9.18kHz

Magnitude: 0dB

Phase: -117.37°

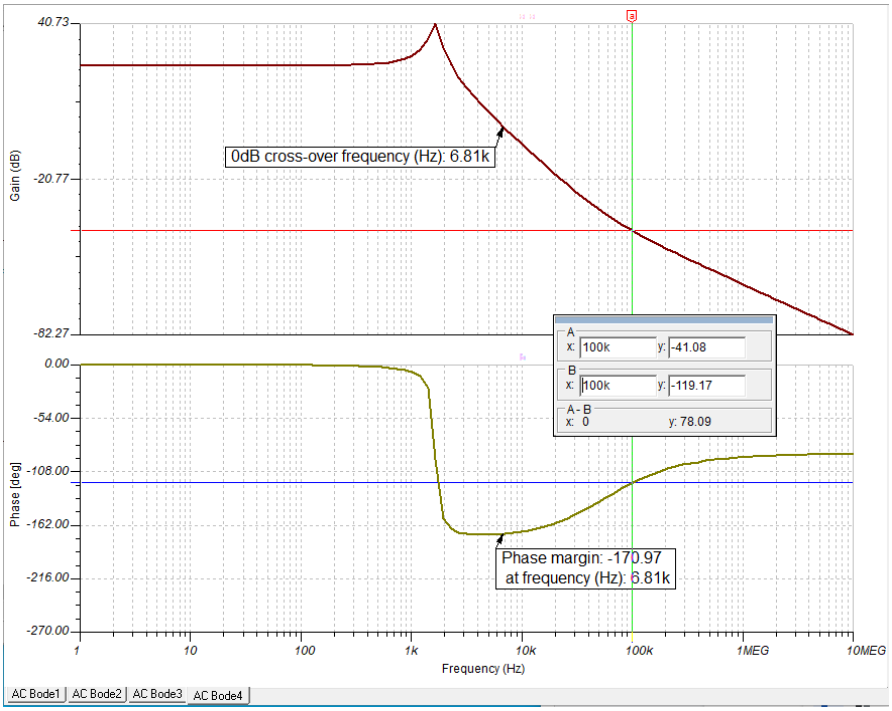

Figure 4:Magnitude and Phase at Switching Frequency

Gain at 100kHz: -41.08dB

Phase Margin: -170.97°

From the phase margin we can see that this system is underdamped. Since this system is underdamped we know that it is a stable system.

Part 3: Transient Response

Output Ripple Voltage and ILoad Waveform

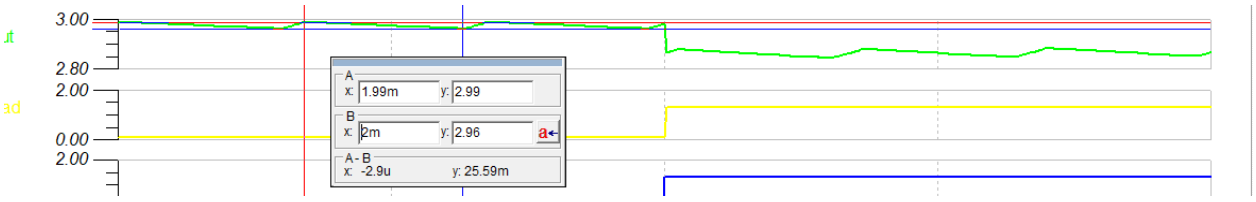

Figure 5: ILoad and Vout waveform for 100mOhm ESR with Graph labels

Figure 6: ILoad and Vout waveform for 100mOhm ESR

Figure 7:ILoad and Vout waveform for 100mOhm ESR Expanded View

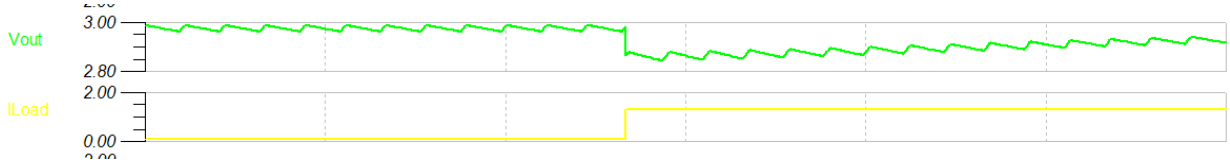

Figure 8: ILoad and Vout waveform for 100mOhm ESR Slightly zoomed in view

Switching ESR

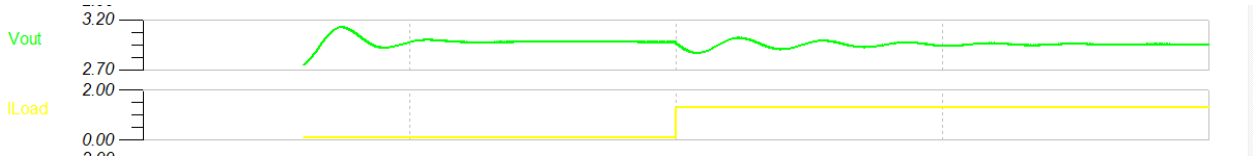

Figure 9: ILoad and Vout waveform for 10mOhm ESR zoomed in view

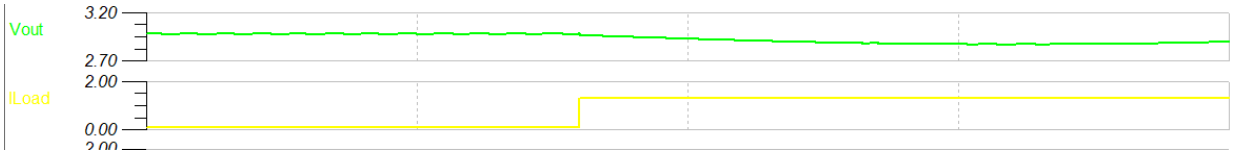

Figure 10: ILoad and Vout waveform for 10mOhm ESR very zoomed in view

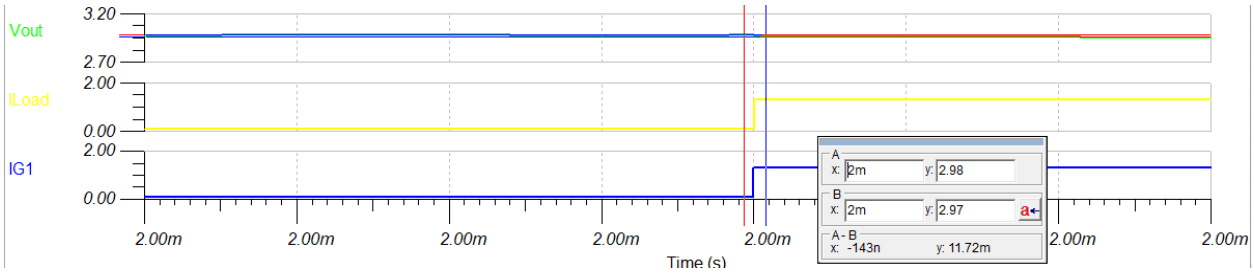

Figure 11: ILoad and Vout waveform for 10mOhm ESR very zoomed in view with graph labels for ripple

Observations:

1. The bode plot is shaped like a normal curve. From the graph we can clearly see the presence of a double pole at around 1kHz. Then we can slightly see a zero at around 10kHz.
2. The DC gain is at around 26dB. The Gain for this converter is high because we need it to amplify voltage. It is a boost converter, and it's function is to take an input voltage and output a higher Vout. In order to do that this circuit will need to have a relatively large DC gain.
3. The gain begins to drop off at a little bit greater than 1kHz. The formula for this point is f=1/2pi*sqrt(LC). The slope here is -40dB/dec because of the introduction of a double pole. The reason for the introduction of this pole is so that our graph can hit the crossover frequency before the switching frequency so that we can get the maximum amount of negative gain. Since it is a double pole we know that the angle here is -90°.
4. The next change occurs at 9.18kHz. This is because of the introduction of a zero in our circuit. The formula for this point is f=1/2pi*ESR*C. Yes this is intentional so that we are able to control the phase of the graph. It helps so that our crossover frequency remains under 10% of the switching frequency.
5. At the Switching frequency the gain is -41.08 dB for a 100mOhm impedance and it is -22.01 dB for a 10mOhm impedance.

6. The Gain crosses the 0dB point for the 100mOhm at a phase angle of -117.37 degrees the phase margin for the system is also at -117.31. The Gain crosses the 0dB point for the 10mOhm at a phase angle of -117.31. However the phase margin is -170.97 degrees
7. When the ESR is increased our gain increases. Our phase plot then experiences a smaller drop and one that drops more slowly. This will make our system more and more overdamped which also makes our system gradually less stable.
8. When the ESR is decreased our gain is Increased. The phase margin is also a lot larger and we see the drop happen a lot quicker. This means that the system will become more and more underdamped which in turn also makes the system more and more stable. Further when the ESR is decreased the output voltage ripple also decreases.
9. We see that the greater the ESR the less stable our system is. This makes sense because when we perform an analysis on an ideal circuit we take measurements with no ESR.
10. ESR should be a design factor since in any real system there will always be losses and nonidealities Although since ESR can not be controlled other factors shall have to be taken into account when designing a circuit i.e. lining up capacitors in parallel in order to reduce the ESR of the system.