Laboratory 7: Buck Converter Non-Idealities

ELEN: 164L

November 3rd, 2021

Fall Quarter

Performed and analyzed by Christian Garcia and Jake Taylor

Materials Supplied by Santa Clara University

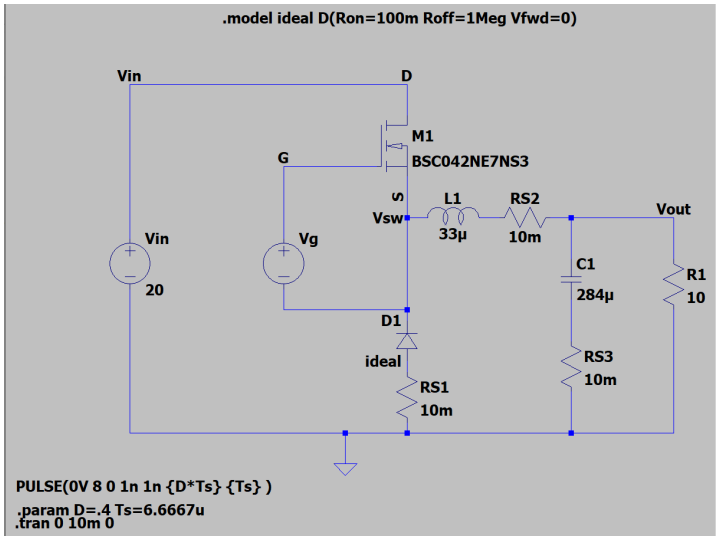


Figure 1: Buck Converter Schematic with a non-ideal switch

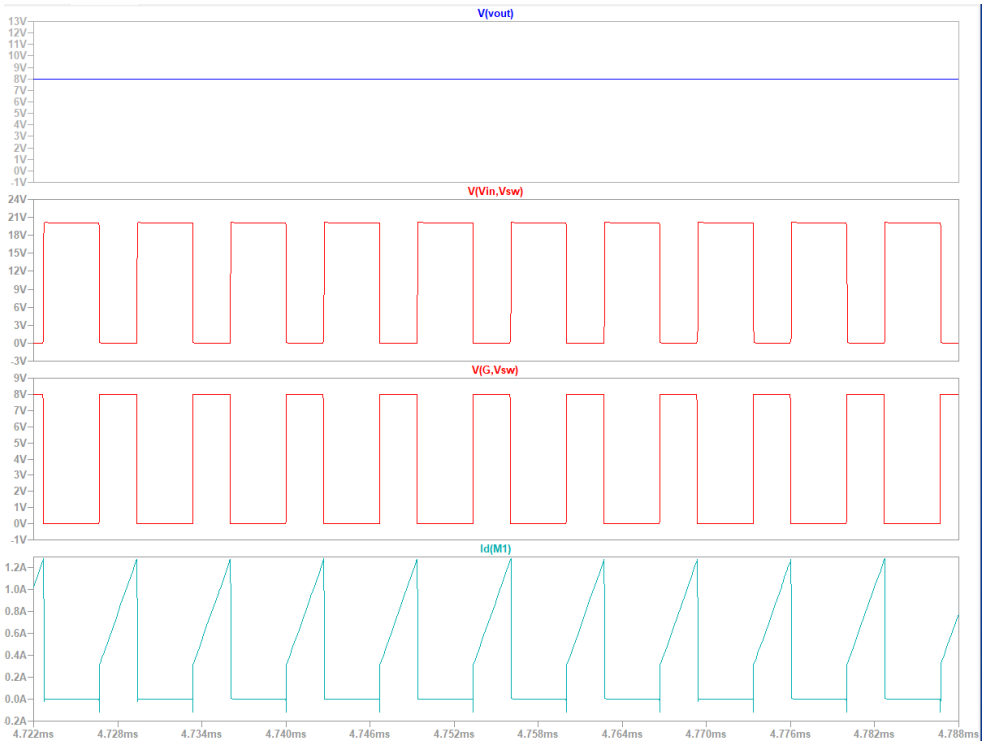


Figure 2: Simulation 1 Switching characteristics waveform outputs from buck converter

The MOSFET Rise time = 31.775nano seconds

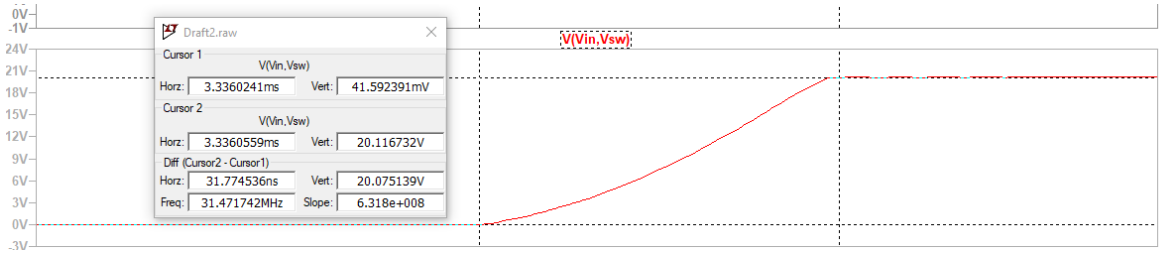


Figure 3: Mosfet Voltage waveform zoomed in

Mosfet Delay Time = 4.915nano seconds

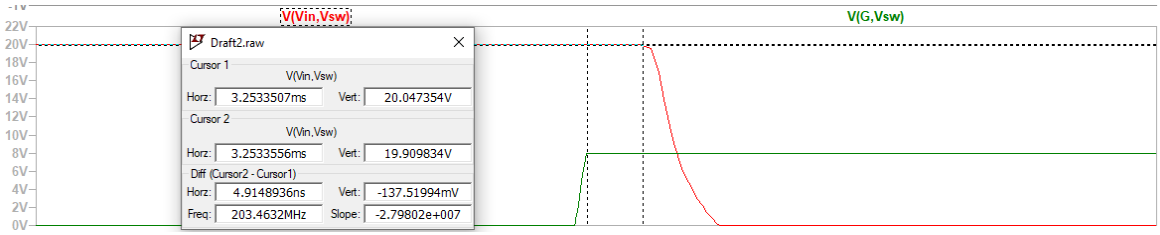


Figure 4: Mosfet Voltage waveform zoomed in plus Vgs section

Mosfet Fall Time = 6.277nano seconds

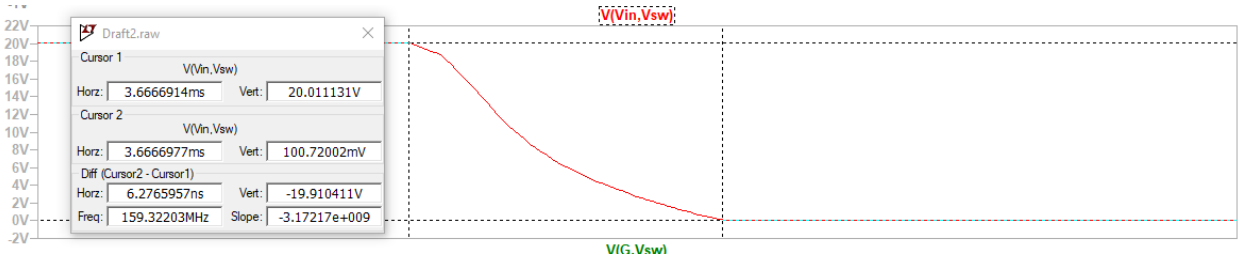


Figure 5: Mosfet Voltage waveform zoomed in plus Vgs section cursor values

❖ What is the peak gate voltage?

Peak Gate Voltage = 27.997

❖ Why is the negative terminal of Vg connected to the MOSFET source rather than the circuit ground?

The negative terminal of Vg is connected to the MOSFET because if it were connected to the circuit ground it means that the MOSFET would always be turned on and we want it to be able to turn on and off.

❖ If the negative terminal of Vg were connected to the circuit ground, how would you change the PULSE statement so that the circuit still functions?

We would make the PULSE statement begin at a value greater than 0V.

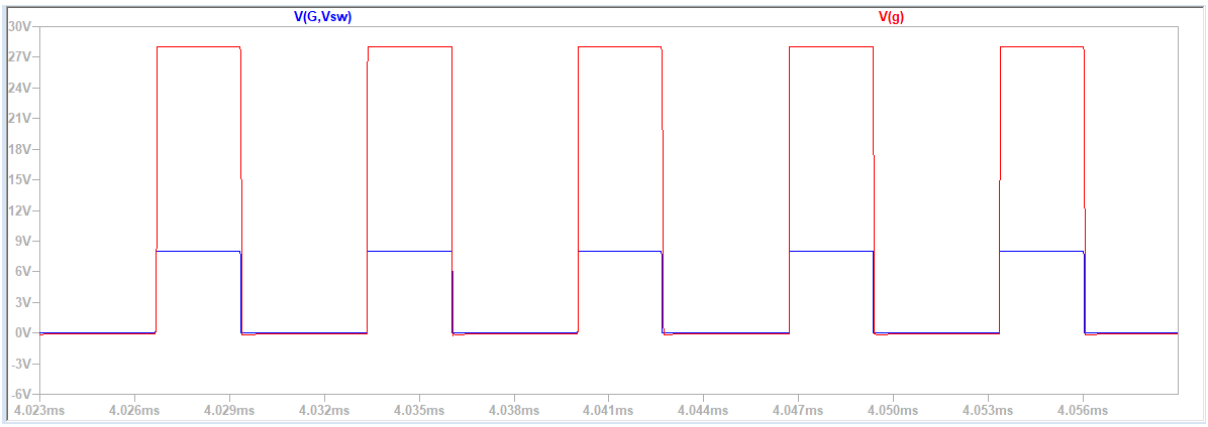


Figure 6: MOSFET gate-source voltage waveform overlaid with the absolute MOSFET gate voltage

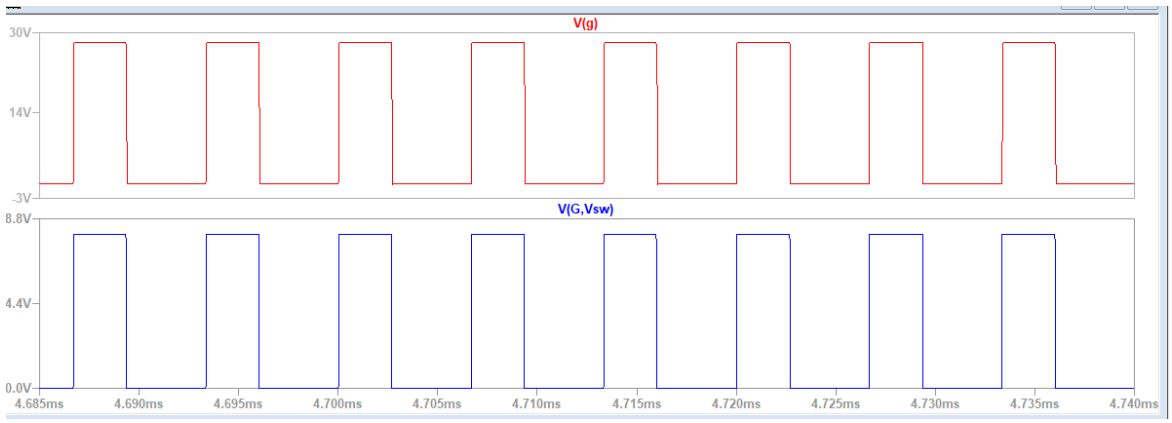


Figure 7: MOSFET gate-source voltage waveform separate from the absolute MOSFET gate voltage

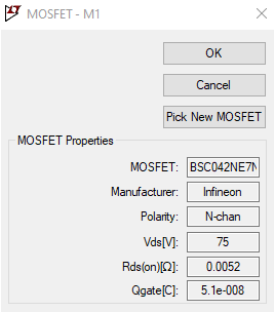
3. Power Loss Measurements

Assignment:

❖ What portion is conduction loss and what is the switching loss (circle it on the waveform for each)?

Conduction loss is on the falling edge of the voltage graphs while switching loss is on the rising edge of the voltage graphs.

❖ Note the RDSON for the MOSFET.



Rdson= 0.052 ohms

❖ Plot the power of the various components.

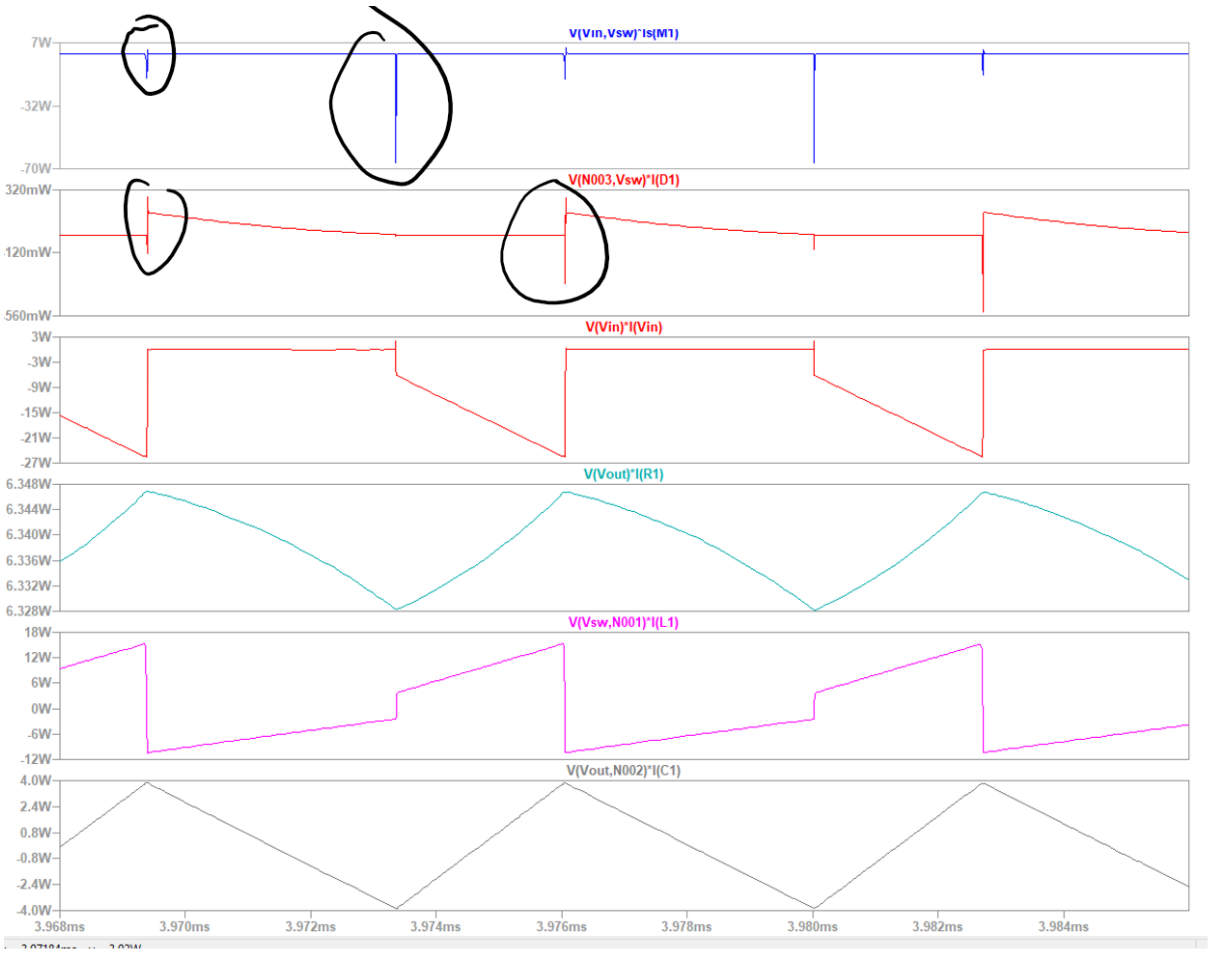
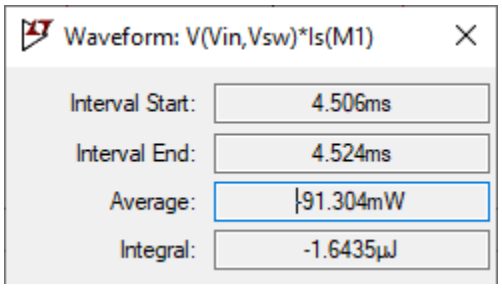
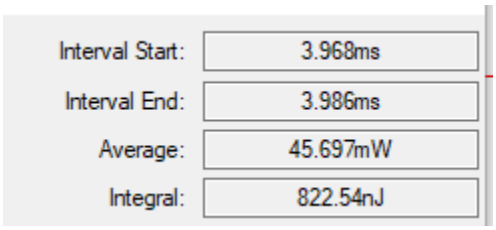


Figure 8: Power Output Waveforms

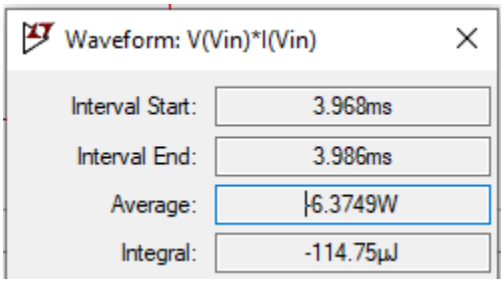
Power in the mosfet



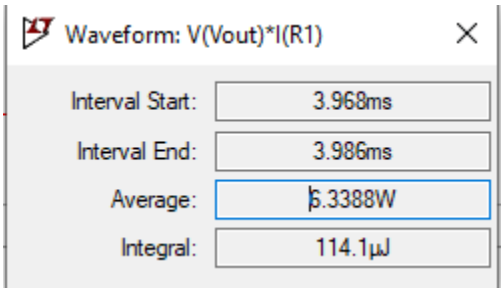
Power in the Diode



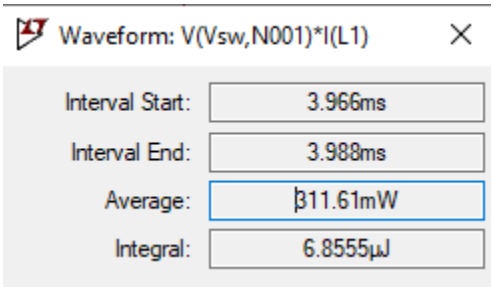
Power in the Input



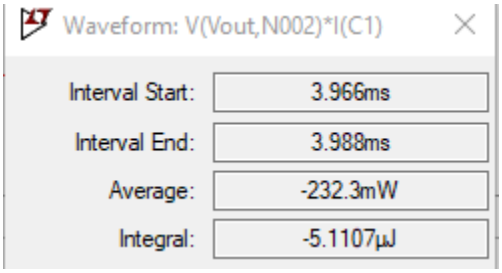
Power in the Output



Power in the Inductor



Power in the Capacitor



❖ Check power dissipated in all the components (ideal or not) to account for all the power losses in the system. Clearly state where power loss terms come from.

❖ Make sure to calculate the power from all the sources.

❖ Pin=Pout + ? + ? + ……..

Figure 9: MOSFET Voltage, Current, and Power Waveforms

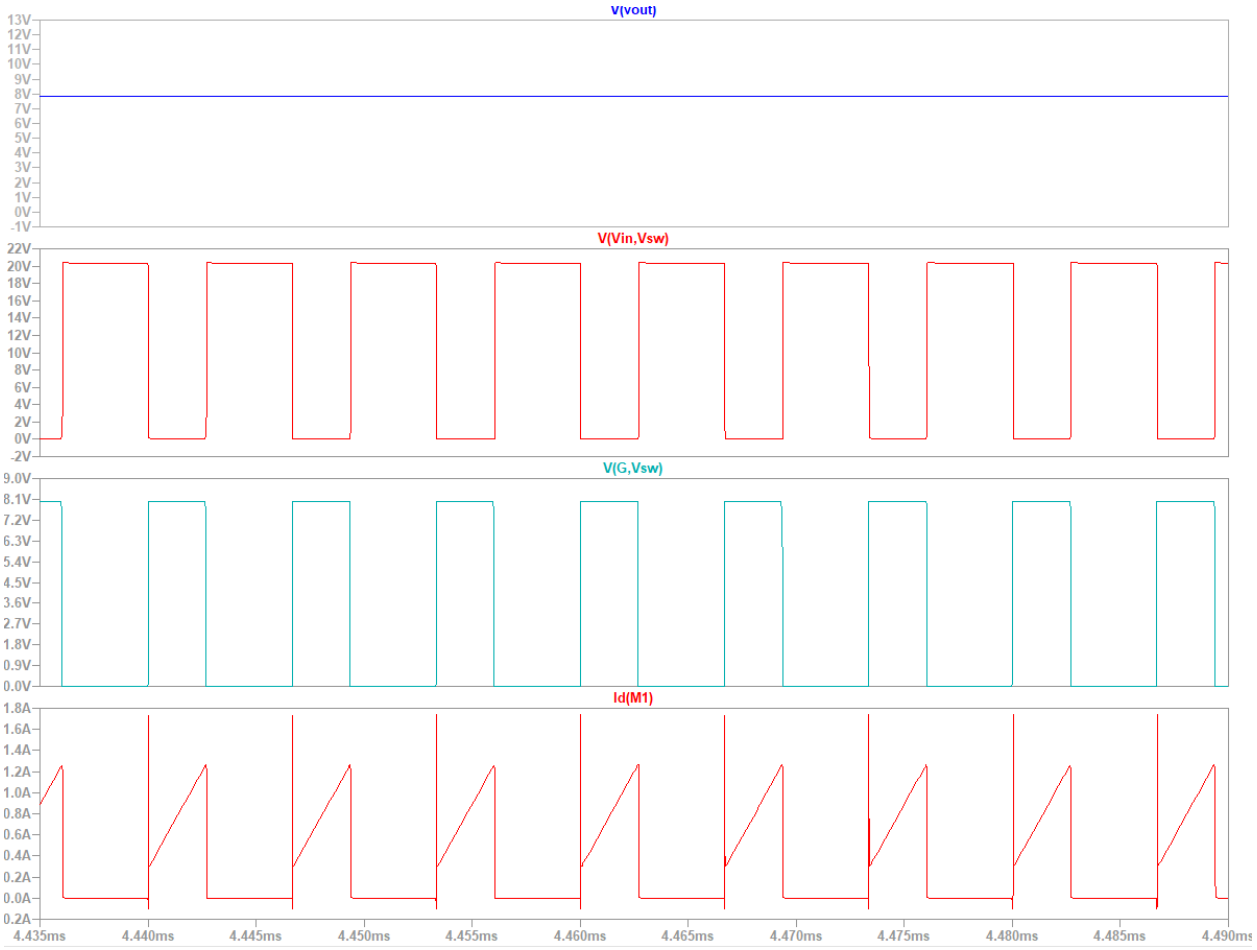


Figure 10: Voltage and Current waveforms for the DIODE,MOSFET, Gate source voltage, and output

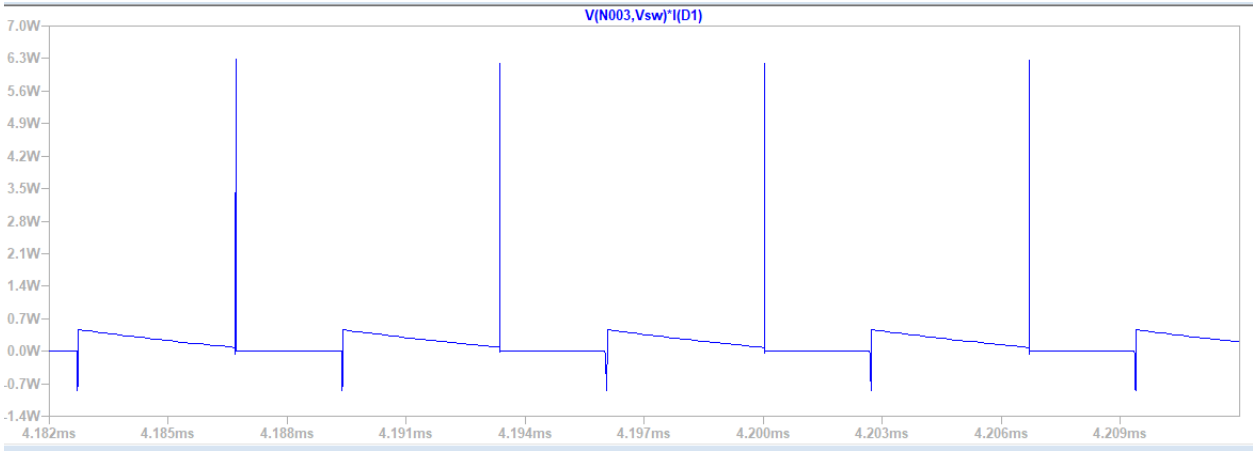
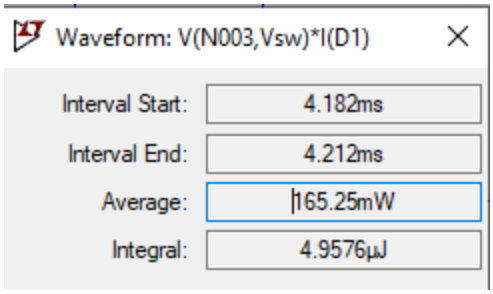


Figure 11: NON ideal diode power waveform



The main differences between item 1 and 4 is the current graph. We see the difference on the rising edge where we see the non-idealities effect. With the major peak on the graph.

Report Questions:

1. Do you see a change in output voltage compared to when your system was all ideal elements? Explain why or why not.
    a. The ideal diode vs non ideal diode affects the power losses and operation of the overall schematic itself. It does not affect the Voltage output. So no, there is no change in output voltage because the diode's main effect is controlling when the MOSFET turns on and off, not changing the output voltage.
2. How would increasing the switching frequency impact the performance of these converters? Consider results from Lab 5 and Lab 6 when you answer this question.
    a. With a greater switching frequency the switch would turn from on and off more times which increases the losses of the system. This is indicated from our results in the previous labs.